SN74LVC1G135B-Q1 Automotive 1-Channel, 2-Input 1.1V to 5.5V NAND Gate with Schmitt-Trigger Inputs and Open-Drain Outputs

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Operating range from 1.1V to 5.5V
- Over-voltage tolerant inputs support up to 5.5V independent of V_{CC}
- Open-drain outputs support 5.5V independent of V_{CC}
- Supports partial-power-down with back drive protection (I_{off})
- High open-drain output drive strength:
  - 32mA at 5V
  - 24mA at 3.3V
  - 8mA at 2.5V
  - 4mA at 1.8V
- Maximum propagation delay of 4.8ns
- Latch-up performance exceeds 100mA per JESD78 and AEC-Q100-004

2 Applications

- Combine power good signals
- Combine enable signals

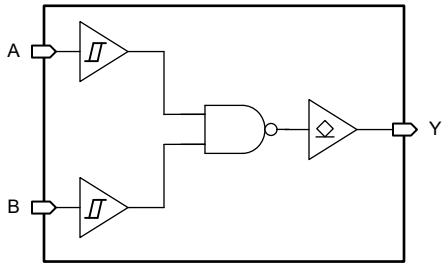
3 Description

The SN74LVC1G135B-Q1 device is a single 2-input positive NAND gate with an open-drain output. This device performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \bar{A} + \bar{B}$ in positive logic. The device functions as an independent gate with Schmitt-trigger inputs, so the device has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals to provide hysteresis (ΔV_T) which makes the device tolerant to slow or noisy input signals.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LVC1G135B-Q1	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DCK (SC70, 5)	2mm × 2.1mm	2mm × 1.25mm
	DTX (X2SON, 5)	1.1mm × 0.85mm	1.1mm × 0.85mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram

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4 Pin Configuration and Functions

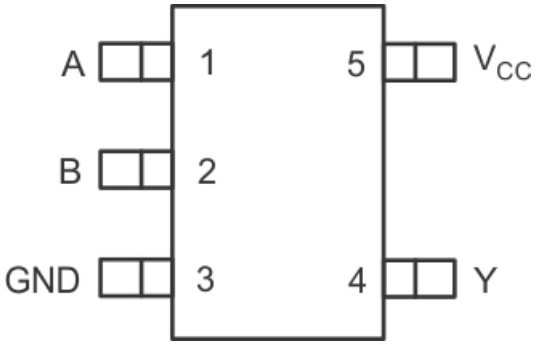


Figure 4-1. DCK , DBV Package 5-Pin SC70 , SOT-23 Top View

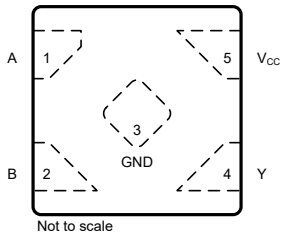


Figure 4-2. DTX Package 5-PIN X2SON Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
GND	3	G	Ground
V_{CC}	5	P	Power supply
Y	4	O	Output Y

(1) I= input, O = output, P = Positive supply, G = Ground

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range(2)		-0.5	6.5	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
V_O	Output voltage range - High-Impedance(2)		-0.5	6.5	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.1	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
V_O	Output voltage	High Impedance	0	5.5	V
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DCK (SOT-SC70, 5)	5	371	297.5	258.6	195.6	256.2	-	°C/W
DTX (XSON, 5)	5	393.6	103.2	331.8	69.8	331.9	179.9	°C/W
DBV (SOT-23, 5)	5	357.1	263.7	264.4	195.6	262.2	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{T+}	Positive-going input threshold voltage	1.1V	0.67		0.72	V
		1.3V	0.79		0.85	
		1.65V	0.98		1.09	
		1.95V	1.13		1.26	
		2.3V	1.31		1.46	
		2.7V	1.51		1.68	
		3V	1.66		1.82	
		3.6V	1.95		2.1	
		4.5V	2.39		2.56	
		5.5V	2.91		3.08	
V_{T-}	Negative-going input threshold voltage	1.1V	0.37		0.46	V
		1.3V	0.44		0.51	
		1.65V	0.56		0.61	
		1.95V	0.66		0.71	
		2.3V	0.78		0.84	
		2.7V	0.92		0.99	
		3V	1.03		1.11	
		3.6V	1.26		1.34	
		4.5V	1.58		1.69	
		5.5V	1.95		2.08	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	1.1V	0.24		0.33	V
		1.3V	0.31		0.39	
		1.65V	0.38		0.51	
		1.95V	0.43		0.59	
		2.3V	0.47		0.67	
		2.7V	0.52		0.75	
		3V	0.56		0.78	
		3.6V	0.63		0.83	
		4.5V	0.74		0.92	
		5.5V	0.88		1.04	
V_{OL}	I_{OL}= 100µA	1.1V to 5.5V			0.15	V
	I_{OL}= 4mA	1.65V			0.45	
	I_{OL}= 8mA	2.3V			0.3	
	I_{OL}= 12mA	2.7V			0.4	
	I_{OL}= 16mA	3V			0.4	
	I_{OL}= 24mA	3V			0.55	
	I_{OL}= 32mA	4.5V			0.55	
I_I	$V_I = V_{CC}$ or GND	V_{CC} = 0V to 5.5V			±5	µA
I_{OFF}	V_I or $V_O = V_{CC}$	V_{CC} = 0V			±10	µA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5V			±15	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	V_{CC} = 1.1V to 5.5V			10	µA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	3V to 5.5V			500	µA

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5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
C_I	V_I = V_{CC} or GND	3.3V		3.5		pF
C_O	V_O = V_{CC} or GND	3.3V		6.3		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	A or B	Y	C_L = 15pF	1.2V ± 0.1V			66.7	ns
				1.5V ± 0.12V			12.4	
				1.8V ± 0.15V			8.4	
				2.5V ± 0.2V			5.1	
				3.3V ± 0.3V			3.9	
				5.0V ± 0.5V			3.3	
			C_L = 30pF	1.8V ± 0.15V			9.4	
				2.5V ± 0.2V			5.7	
			C_L = 50pF	3.3V ± 0.3V			4.8	
				5.0V ± 0.5V			3.8	
C_{pd}			f = 10MHz	1.8V		4		pF
				2.5V		5		
				3.3V		5		
				5V		6		

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6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

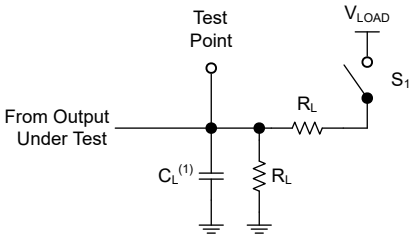
The outputs are measured individually with one input transition per measurement.

Table 6-1. Open-Drain Outputs

TEST	S1
t_{PLZ}, t_{PZL}	CLOSED

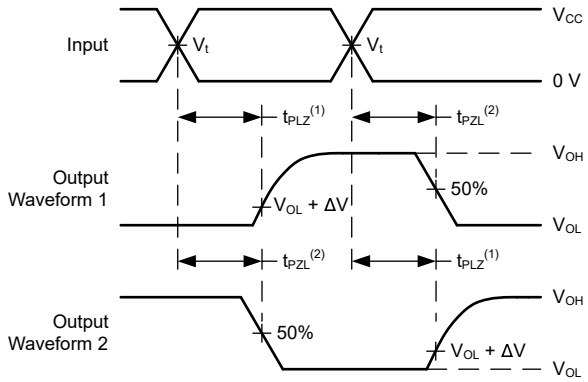
Table 6-2. 3-State or Open-Drain Outputs

V_{CC}	V_t	R_L	C_L	ΔV	V_{LOAD}
1.8V ± 0.15V	V_{CC}/2	1kΩ	15pF/30pF	0.15V	2×V_{CC}
2.5V ± 0.2V	V_{CC}/2	500Ω	15pF/30pF	0.15V	2×V_{CC}
3.3V ± 0.3V	1.5V	500Ω	15pF/50pF	0.3V	6V
5.0V ± 0.5V	1.5V	500Ω	15pF/50pF	0.3V	6V



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Open-Drain Outputs



(1) t_{PLZ} is the same as t_{dis}.
(2) t_{PZL} is the same as t_{en}.

Figure 6-2. Voltage Waveforms Propagation Delays

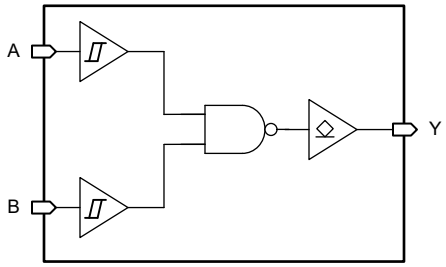
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7 Detailed Description

7.1 Overview

The SN74LVC1G135B-Q1 device is a single 2-input positive NAND gate with an open-drain output. This device performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \bar{A} + \bar{B}$ in positive logic. The device functions as an independent gate with Schmitt-trigger inputs, so the device has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals to provide hysteresis (ΔV_T) which makes the device tolerant to slow or noisy input signals.

7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Open-Drain CMOS Outputs

Open-drain outputs are included in SN74LVC1G135B-Q1. Open-drain outputs can only drive the output low. When in the high logical state, outputs are in a high-impedance state, meaning outputs neither source nor sink current (with the exception of minor leakage current as defined in the *Electrical Characteristics* table). In the high-impedance state, the output voltage is not controlled by SN74LVC1G135B-Q1 and is dependent on external factors.

Because of the high-impedance state, an external pull-up resistor is required to define a logic high. Without a pull-up resistor, the output will float and have an undefined logic level. The resistor value depends on factors like parasitic capacitance and power consumption; typically, a 10kΩ resistor is suitable.

The drive capability of SN74LVC1G135B-Q1 can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, outputs can drive higher currents than SN74LVC1G135B-Q1 is designed to handle continuously. Limit the device output power to avoid damage due to overcurrent. Follow the electrical and thermal limits defined in the *Absolute Maximum Ratings* at all times. See the *Recommended Operating Conditions* table for the maximum output voltage that can be externally connected to SN74LVC1G135B-Q1.

Leave unused open-drain CMOS outputs disconnected.

7.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, properly terminating unused inputs is still recommended. Driving the inputs with slow transitioning signals increases dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

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7.3.3 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.4 Clamp Diode Structure

Figure 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

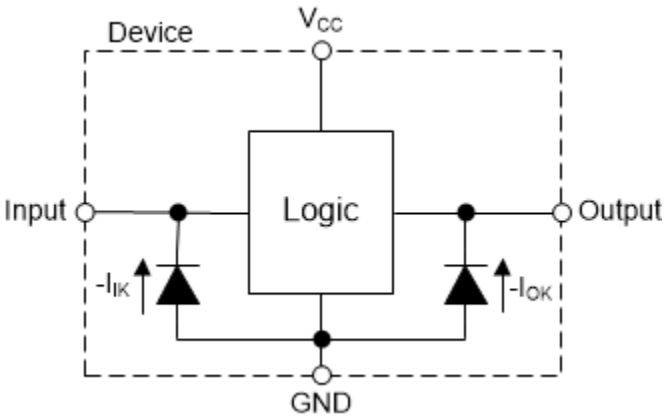


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.5 Over-Voltage Tolerant Inputs

The SN74LVC1G135B-Q1 includes over-voltage tolerant inputs. The input pins support high-state input voltages larger than the supply voltage by utilizing an input protection circuit that does not include a standard positive clamp diode. See *Recommended Operating Conditions* for the recommended input voltage.

CAUTION

Do not exceed the maximum input voltage range provided in *Absolute Maximum Ratings*. Exceeding the maximum input voltage range rating can cause immediate and permanent damage to the device.

7.4 Device Functional Modes

The Function Table lists the functional modes of SN74LVC1G135B-Q1.

Table 7-1. Function Table

INPUTS(1)		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, a two-input NAND gate with open-drain outputs is used to drive an LED. The SN74LVC1G135B-Q1 is used to turn on an indicator LED. The LED lights up when the power good signals are HIGH, indicating that the power supplies have reached the desired voltage.

8.2 Typical Application

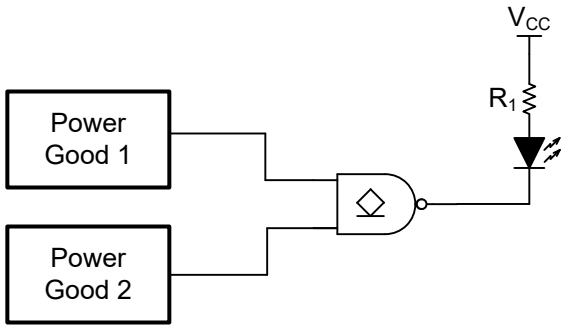


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC1G135B-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC1G135B-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, TI recommends adding a series resistor between the output and capacitor to prevent excessive current.

The SN74LVC1G135B-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

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CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC1G135B-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC1G135B-Q1 has no input signal transition rate requirements because the device has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the Electrical Characteristics . This hysteresis value provides the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the Typical Characteristics .

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SN74LVC1G135B-Q1 to the receiving device.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

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8.2.3 Application Curves

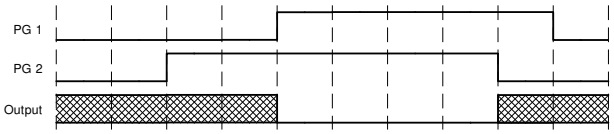


Figure 8-2. Typical Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Verify that each V_{CC} terminal has a good bypass capacitor to prevent power disturbance. For the SN74LVC1G135B-Q1, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

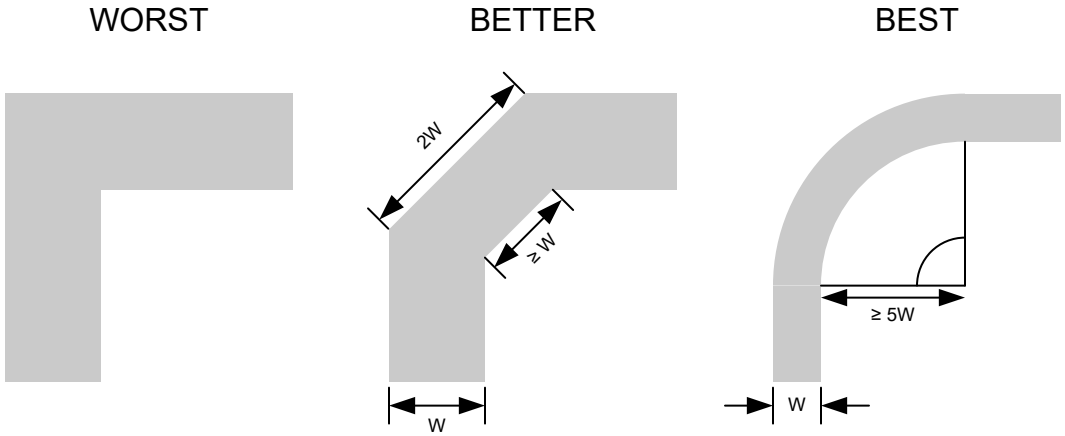


Figure 8-3. Example Trace Corners for Improved Signal Integrity

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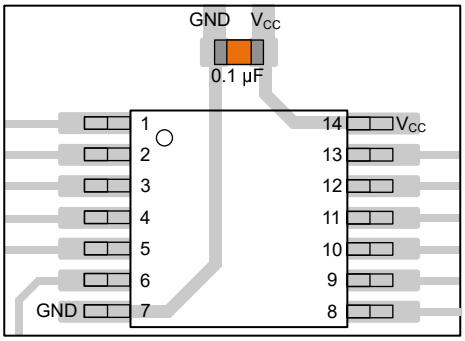


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

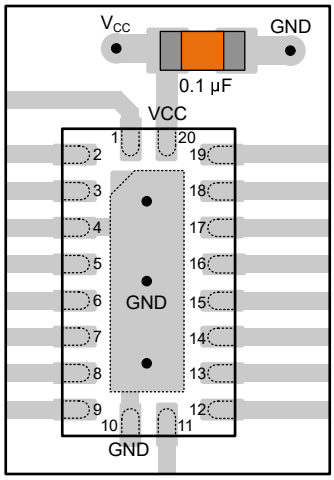


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

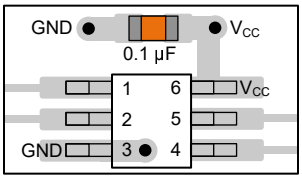


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

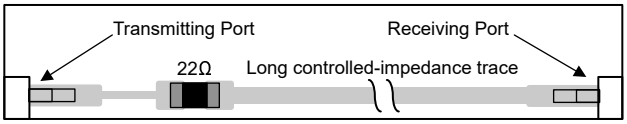


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2026	*	Initial Release

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CLVC1G135BDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3WBF
CLVC1G135BDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	25G
CLVC1G135BDTXRQ1	Active	Production	X2SON (DTX) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G135B-Q1 :

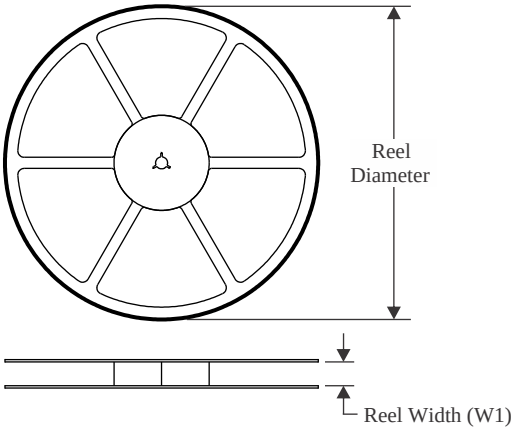
- Catalog : SN74LVC1G135B

NOTE: Qualified Version Definitions:

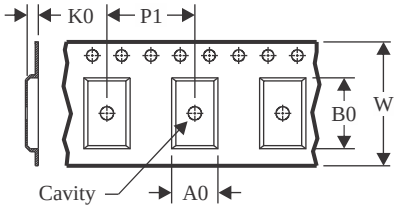
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

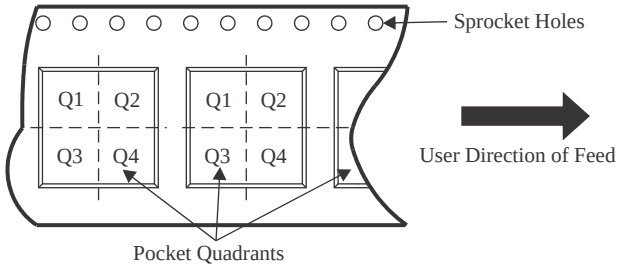


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

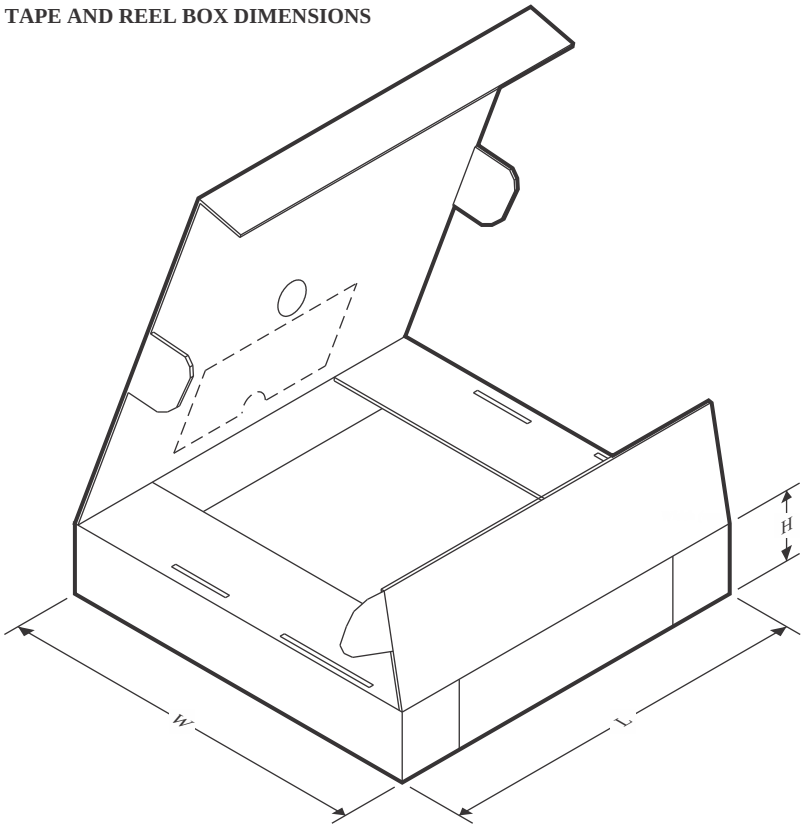
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC1G135BDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
CLVC1G135BDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
CLVC1G135BDTXRQ1	X2SON	DTX	5	3000	180.0	8.4	1.0	1.25	0.48	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

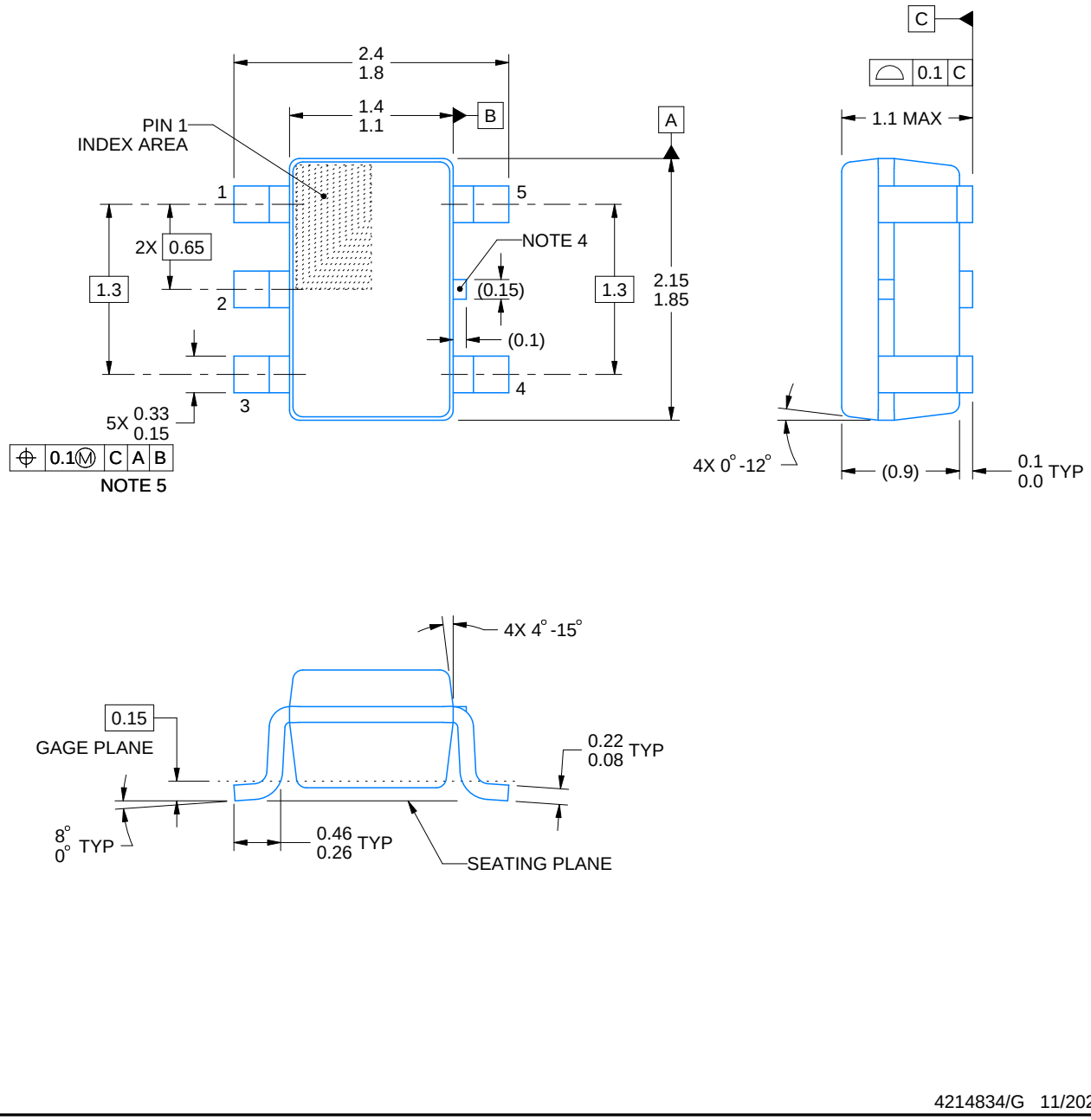
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC1G135BDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
CLVC1G135BDCKRQ1	SC70	DCK	5	3000	210.0	185.0	35.0
CLVC1G135BDTXRQ1	X2SON	DTX	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

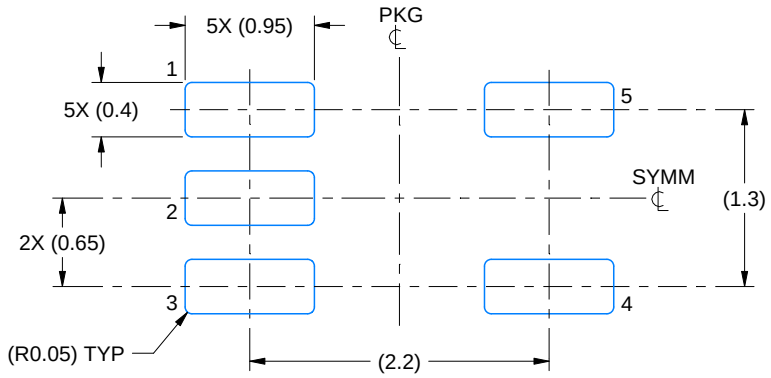
SMALL OUTLINE TRANSISTOR



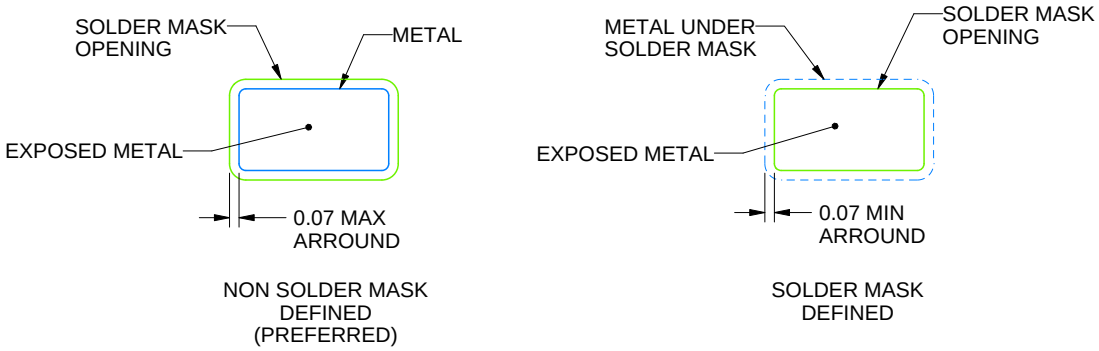
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

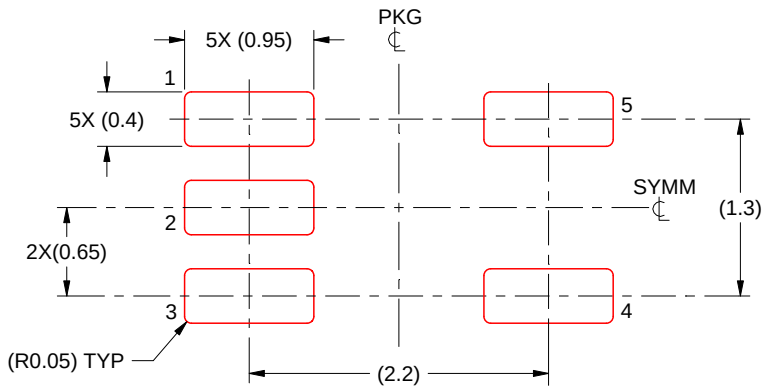


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

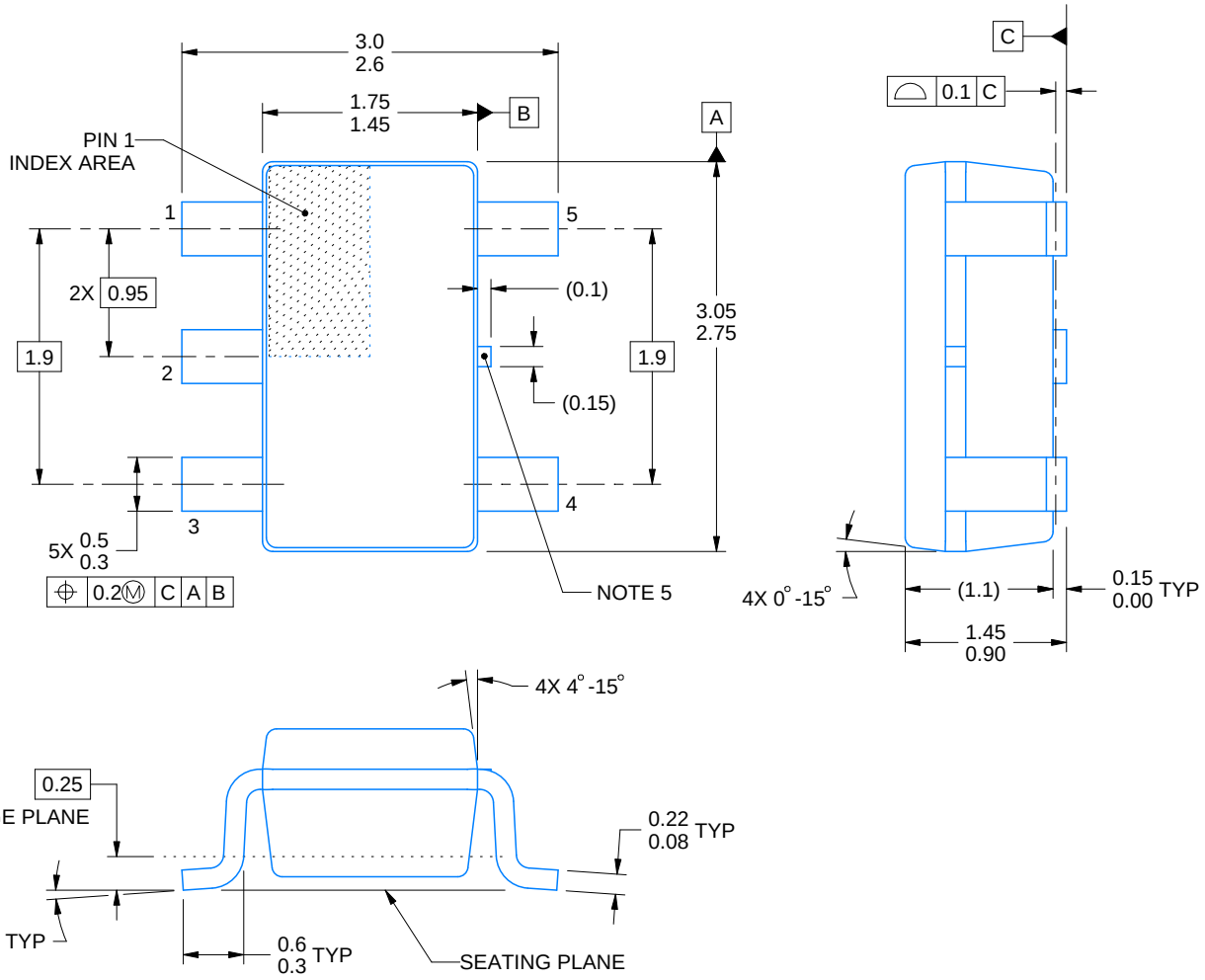
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

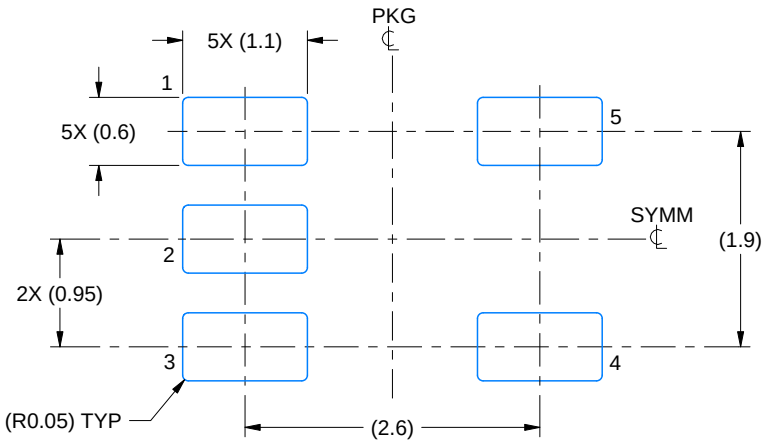
SMALL OUTLINE TRANSISTOR



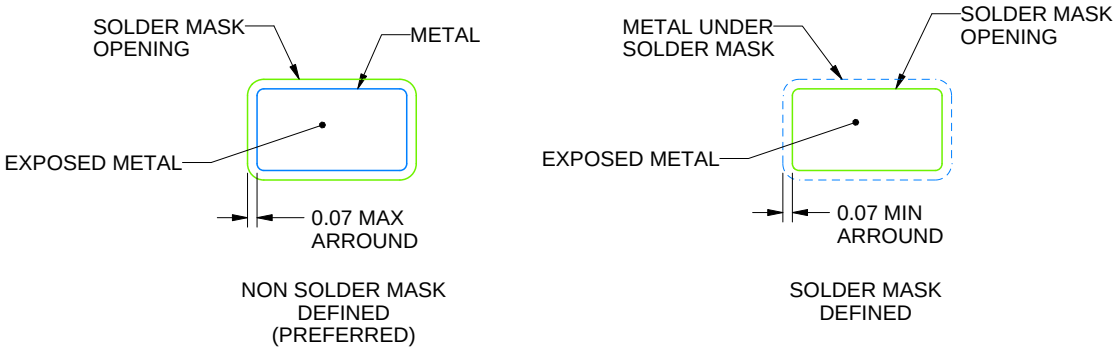
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

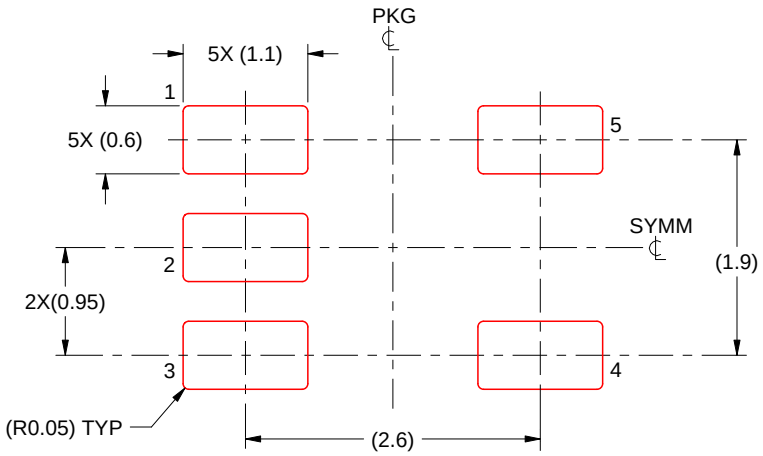


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

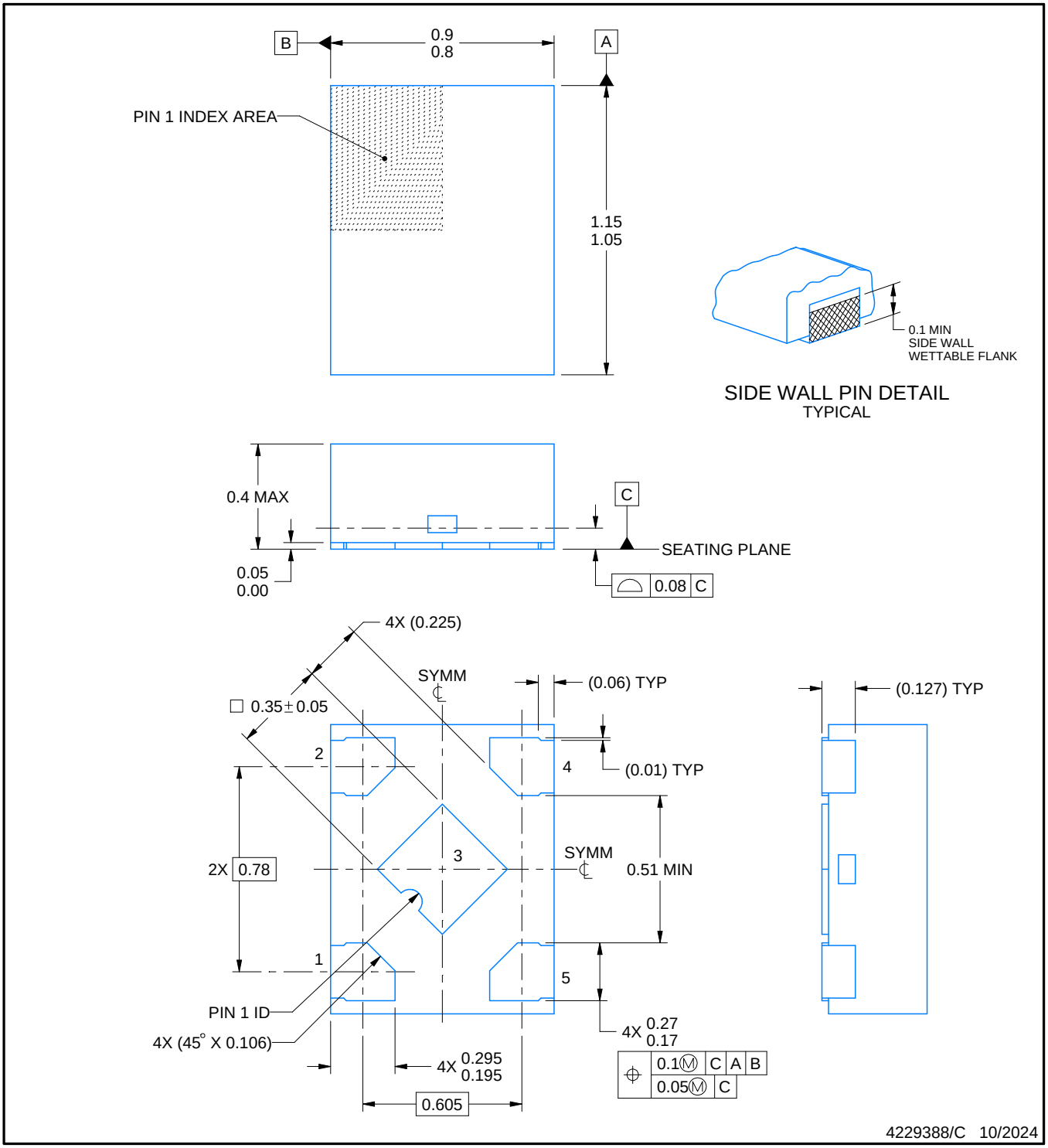
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DTX0005A

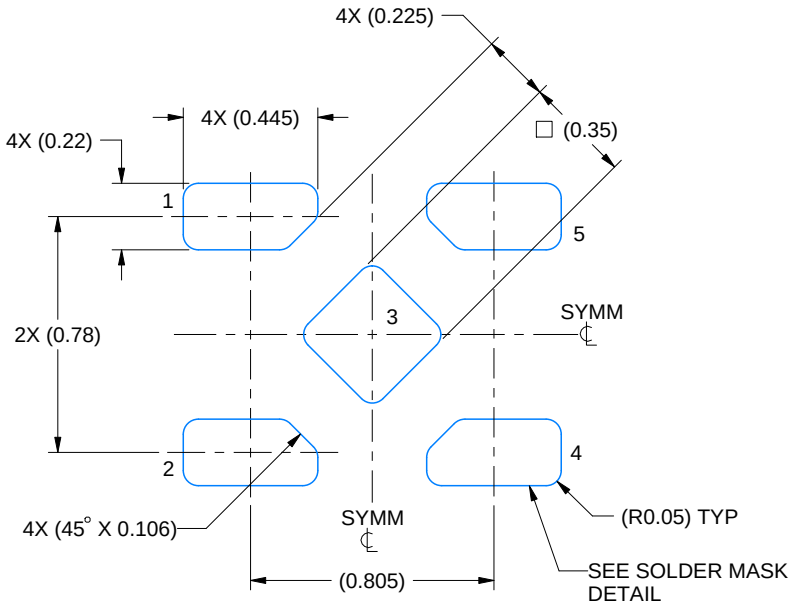
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

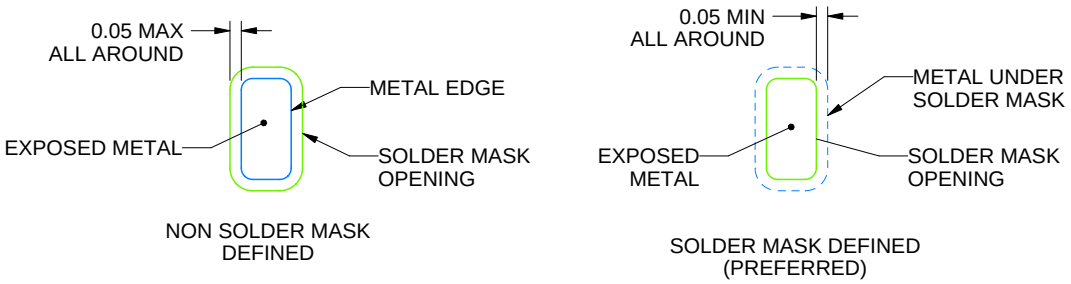


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

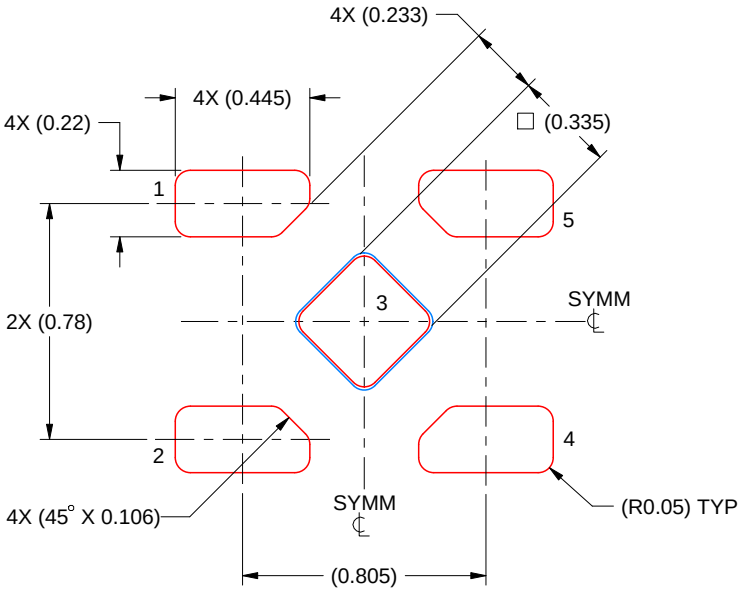


SOLDER MASK DETAILS

4229388/C 10/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

PRINTED SOLDER PASTE COVERAGE BY AREA UNDER PACKAGE
PAD 5: 92%

4229388/C 10/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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