SN74LVC1G06 Single Inverter Buffer or Driver With Open-Drain Output

1 Features

- ESD protection exceeds JESD 22
  - 2000V human body model (A114-A)
  - 200V machine model (A115-A)
  - 1000V charged-device model (C101)
- Available in the Texas Instruments NanoFree™ package
- Supports 5V V_{CC} operation
- Input and open-drain output accept voltages up to 5.5V
- Maximum t_{pd} of 4.5ns at 3.3V at 125°C
- Low power consumption, 10µA maximum I_{CC}
- ±24mA output drive at 3.3V for open-drain devices
- I_{off} supports partial-power-down mode and back-drive protection
- Latch-up performance exceeds 100mA per JESD 78, class II
- Can be used for up or down translation
- Schmitt trigger action on all ports

2 Applications

- AV receivers
- Blu-ray players and home theaters
- DVD recorders and players
- Desktop or notebook PCs
- Digital radio or internet radio players
- Digital video cameras (DVC)
- Embedded PCs
- GPS: personal navigation devices
- Mobile internet devices
- Network projector front-ends
- Portable media players
- Pro audio mixers
- Smoke detectors
- Solid state drive (SSD): enterprise
- High-definition (HDTV)
- Tablets: enterprise
- Audio docks: portable
- DLP front projection systems
- DVR and DVS
- Digital picture frame (DPF)
- Digital still cameras

3 Description

This single inverter buffer and driver is designed for 1.65V to 5.5V V_{CC} operation.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

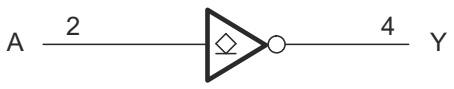
The output of the SN74LVC1G06 device is open-drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32mA.

This device is fully specified for partial-power-down applications using I_{off}.The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)(3)
SN74LVC1G06	DBV (SOT-23, 5)	2.90mm × 2.80mm	2.90mm × 1.60mm
	DCK (SC70, 5)	2.00mm × 2.10mm	2.00mm × 1.25mm
	DRL (SOT-5X3, 5)	1.60mm × 1.60mm	1.60mm × 1.20mm
	DRY (USON, 6)	1.45mm × 1.00mm	1.45mm × 1.00mm
	DSF (X2SON, 6)	1.00mm × 1.00mm	1.00mm × 1.00mm
	YZP (DSBGA, 5)	1.75mm × 1.25mm	1.40mm × 0.90mm
	YZV (DSBGA, 4)	1.25mm × 1.25mm	0.90mm × 0.90mm
	DPW (X2SON, 5)	0.80mm × 0.80mm	0.80mm × 0.80mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

Table of Contents

4 Pin Configuration and Functions

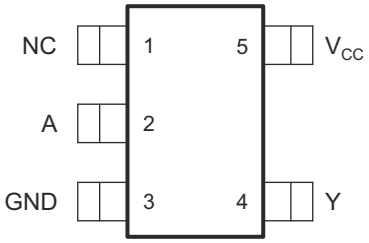


Figure 4-1. DBV Package 5-Pin SOT-23 Top View

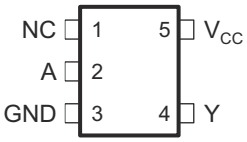


Figure 4-2. DRL Package 5-Pin SOT-5X3 Top View

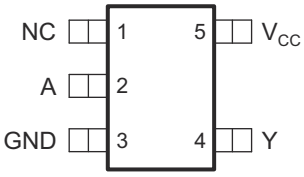


Figure 4-3. DCK Package 5-Pin SC70 Top View

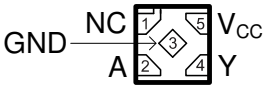


Figure 4-4. DPW Package 5-Pin X2SON Top View

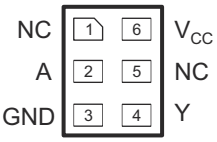


Figure 4-5. DRY Package 6-Pin SON Top View

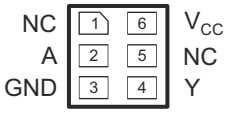


Figure 4-6. DSF Package 6-Pin SON Top View

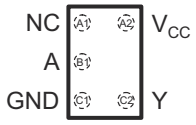


Figure 4-7. YZP Package 5-Pin DSBGA Top View

Figure 4-8. YZV Package 4-Pin DSBGA Top View

Table 4-1. Pin Functions [2]

PIN					I/O	DESCRIPTION
NAME	DBV, DCK, DRL, DPW	DRY, DSF	YZP	YZV		
A	2	2	B1	A1	I	Input
DNU	—	—	A1	—	—	Do not use
GND	3	3	C1	B1	—	Ground
NC[1]	1	1 5	—	—	—	Not connected
V_{CC}	5	6	A2	A2	—	Power pin
Y	4	4	C2	B2	O	Output

(1) NC – No internal connection
(2) See mechanical drawings for dimensions.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2) (3)		–0.5	6.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_j	Junction temperature		–65	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	
		Machine Model (MM), per A115-A	200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65V to 1.95V	0.65 × V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3V to 3.6V	2		
		V_{CC} = 4.5V to 5.5V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65V to 1.95V		0.35 × V_{CC}	V
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3V to 3.6V		0.8	
		V_{CC} = 4.5V to 5.5V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	5.5	V
I_{OL}	Low-level output current	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3V		16	
				24	
		V_{CC} = 4.5V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
		V_{CC} = 3.3V ± 0.3V		10	
		V_{CC} = 5V ± 0.5V		5	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to establish proper device operation. See *Implications of Slow or Floating CMOS Inputs* application report.

5.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G06							UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT-5X3)	DRY (SON)	DPW (X2SON)	YZV (DSBGA)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	5 PINS	5 PINS	4 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	357.1	371.0	296.2	369.6	511	168.2	144.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	263.7	297.5	137.3	257.6	241.9	2.1	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	264.4	258.6	145.3	230.8	374.2	55.9	39.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	195.6	195.6	14.7	77.2	45	1.1	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	262.2	256.2	145.9	231	373.3	56.3	39.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	168	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OL}	High-level output voltage	I_{OL} = 100µA		1.65V to 5.5V			0.1	V
		I_{OL} = 4mA		1.65V			0.45	
		I_{OL} = 8mA		2.3V			0.3	
		I_{OL} = 16mA		3V			0.4	
		I_{OL} = 24mA					0.55	
		I_{OL} = 32mA		4.5V			0.55	
I_I	Inflection-point current	V_I = 5.5V or GND	A input	0 to 5.5V			±1	µA
I_{off}	Off-state current	V_I or V_O = 5.5V		0			±10	µA
I_{CC}		V_I = 5.5V or GND, I_O = 0		1.65V to 5.5V			10	µA
ΔI_{CC}		One input at V_{CC} – 0.6V, other inputs at V_{CC} or GND		3V to 5.5V			500	µA
C_I	Input capacitance	V_I = V_{CC} or GND		3.3V		4		pF
C_O	Off-state capacitance	V_O = V_{CC} or GND		3.3V		5		pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

5.6 Switching Characteristics: –40°C to +85°C

over recommended operating free-air temperature range, T_A = –40°C to +85°C (unless otherwise noted) (see Figure 6-1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	Propagation delay	A	Y	1.8V ± 0.15V	2.2	6.5	ns
				2.5V ± 0.2V	1.1	4	
				3.3V ± 0.3V	1.2	4	
				5V ± 0.5V	1	3	

5.7 Switching Characteristics: –40°C to +125°C

over recommended operating free-air temperature range, T_A = –40°C to +125°C (unless otherwise noted) (see Figure 6-1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	Propagation delay	A	Y	1.8V ± 0.15V	2.2	7	ns
				2.5V ± 0.2V	1.1	4.5	
				3.3V ± 0.3V	1.2	4.5	
				5V ± 0.5V	1	3.5	

5.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10MHz	1.8V	3	pF
			2.5V	3	
			3.3V	4	
			5V	6	

5.9 Typical Characteristics

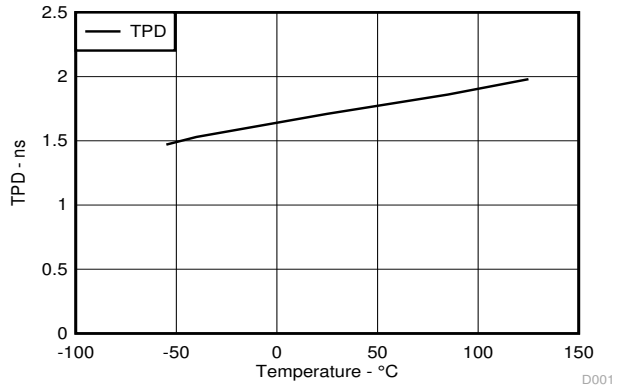


Figure 5-1. TPD Across Temperature at 3.3V V_{CC}

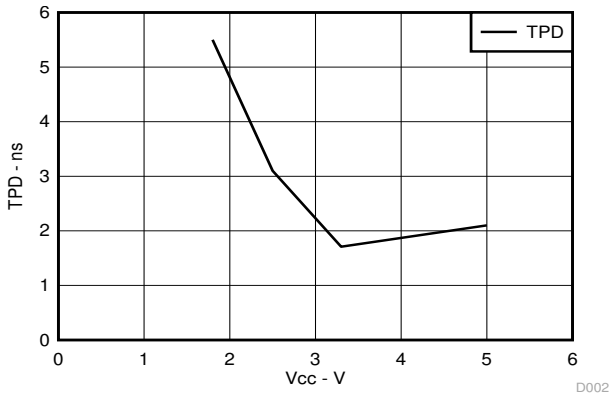
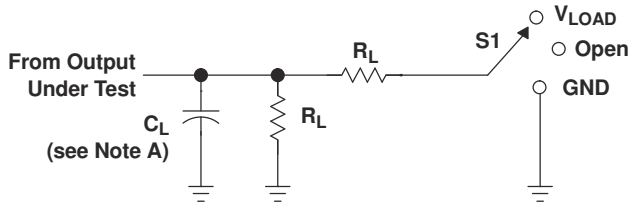


Figure 5-2. TPD Across V_{CC} at 25°C

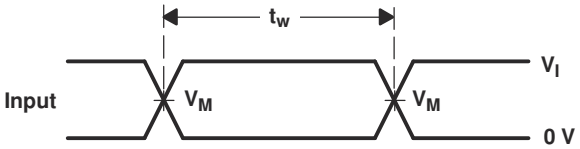
Parameter Measurement Information



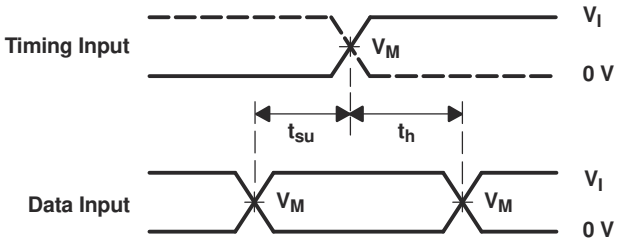
LOAD CIRCUIT

TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

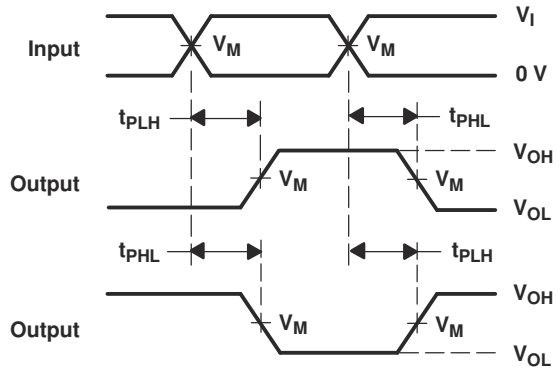
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



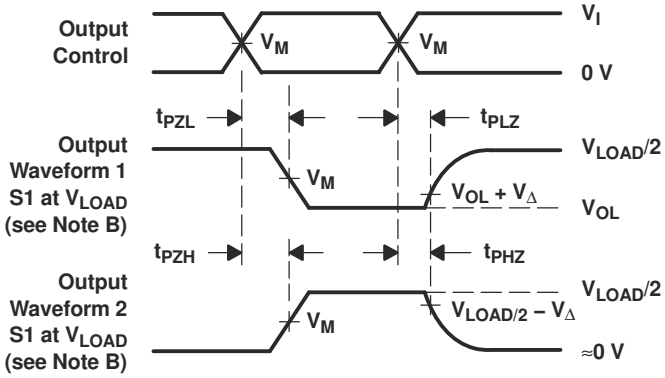
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
F. t_{PZL} is measured at V_M.
G. t_{PLZ} is measured at V_{OL} + V_Δ.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms (Open Drain)

6 Detailed Description

6.1 Overview

The SN74LVC1G06 device contains one open-drain inverter with a maximum sink current of 32mA. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

6.2 Functional Block Diagram

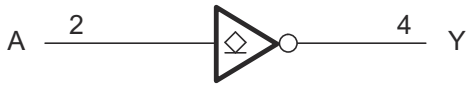


Figure 6-1. Logic Diagram (Positive Logic)

6.3 Feature Description

6.3.1 CMOS Open-Drain Outputs

The open-drain output allows the device to sink current to GND but not to source current from V_{CC}. When the output is not actively pulling the line low, it will go into a high impedance state (tri-state). This allows the device to be used for a wide variety of applications, including up-translation and down-translation, as the output voltage can be determined by an external pullup.

Consider the drive capability of this device creates fast edges into light loads so routing and load conditions prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

6.3.2 Standard CMOS Inputs

The impendence for standard CMOS inputs is high. Typically, a CMOS input is modeled as a resistor in parallel with the input capacitance as shown in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal before the standard CMOS input.

6.3.3 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in Figure 6-2.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and the output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

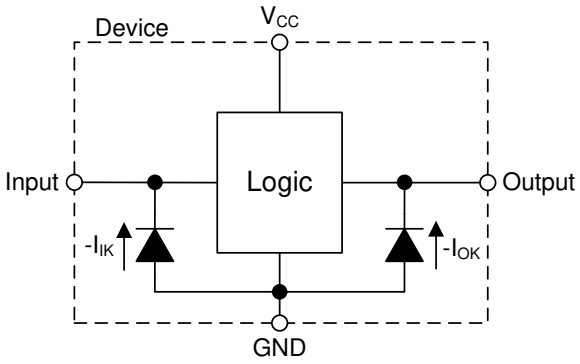


Figure 6-2. Electrical Placement of Clamping Diodes for Each Input and Output

6.3.4 Partial Power Down (I_{off})

Each input and output enter a high impedance state when the supply voltage is 0V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

6.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage as long as the input signals remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

6.4 Device Functional Modes

Table 6-1 lists the functional modes of the SN74LVC1G06.

Table 6-1. Function Table

INPUT A	OUTPUT Y
L	Hi-Z
H	L

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The SN74LVC1G06 is a high-drive CMOS device that can be used to implement a high output drive buffer, such as an LED application. It can sink 32mA of current at 4.5V making it appropriate for high-drive applications. It is good for high-speed applications up to 100MHz. The inputs are 5.5V tolerant allowing it to translate up or down to V_{CC}. Below shows a simple LED driver application for a single channel of the device.

7.2 Typical Application

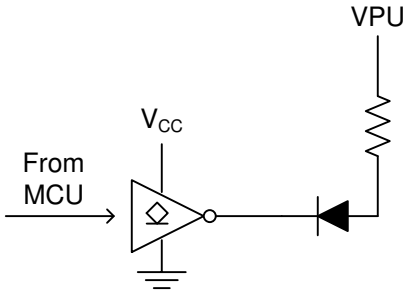


Figure 7-1. Typical Application Diagram

7.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

7.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommended Output Conditions
   - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
   - Outputs should not be pulled above 5.5V.

7.2.3 Application Curve

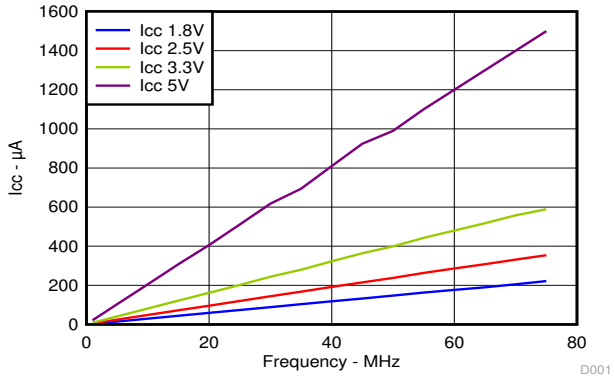


Figure 7-2. I_{CC} vs Frequency

7.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

The V_{CC} pin must have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended, and it is acceptable to parallel multiple bypass caps to reject different frequencies of noise. 0.1µF and 1µF capacitors are commonly used in parallel. For the best results, install the bypass capacitor as close to the power pin as possible.

7.4 Layout

7.4.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 7-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

An example layout is given in Figure 7-4 for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this data sheet. A via of diameter 0.1mm (3.973mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout.

7.4.2 Layout Example

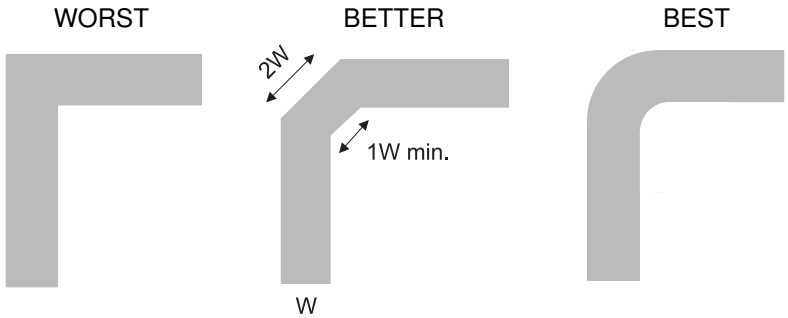


Figure 7-3. Trace Example

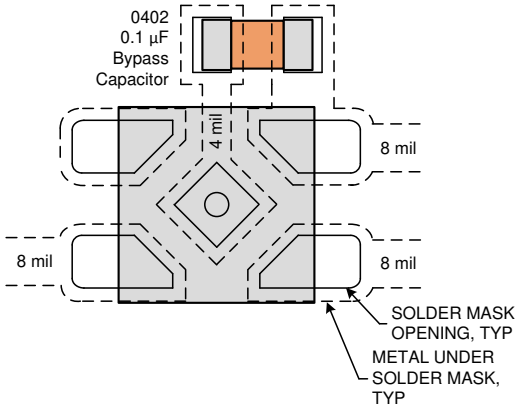


Figure 7-4. Example Layout With DPW (X2SON-5) Package

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

NanoFree™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision AA (June 2025) to Revision AB (October 2025)	Page
• Changed Junction-to-ambient thermal resistance value for DCK package from: 276.1°C/W to: 371.10C/W	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 178.9°C/W to: 297.5°C/W	5
• Changed Junction-to-board thermal resistance value for DCK package from: 70.9°C/W to: 258.2°C/W	5
• Changed Junction-to-top characterization value for DCK package from: 47°C/W to: 195.6°C/W	5
• Changed Junction-to-board characterization value for DCK package from: 69.3°C/W to: 256.2°C/W	5

Changes from Revision Z (November 2017) to Revision AA (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed *Device Information* table to *Package Information*	1
• Changed Junction-to-ambient thermal resistance value for DBV package from: 231.5°C/W to: 357.1°C/W	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 139.4°C/W to: 263.7°C/W	5
• Changed Junction-to-board thermal resistance value for DBV package from: 71.1°C/W to: 264.4°C/W	5
• Changed Junction-to-top characterization value for DBV package from: 45.2°C/W to: 195.6°C/W	5
• Changed Junction-to-board characterization value for DBV package from: 70.7°C/W to: 262.2°C/W	5

Changes from Revision Y (February 2017) to Revision Z (November 2017)	Page
• Changed values in the Thermal Information table to align with JEDEC standards	5
• Updated Feature Description to include more detailed information about specific device features.	9

- Added DPW layout example 12

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G06DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C065, C06F, C06J, C06R, C06T) (C06H, C06P, C06S)
SN74LVC1G06DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C065, C06F, C06J, C06R, C06T) (C06H, C06P, C06S)
SN74LVC1G06DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C065, C06F, C06J, C06R, C06T) (C06H, C06P, C06S)
SN74LVC1G06DBVRE4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F
SN74LVC1G06DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F
SN74LVC1G06DBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F
SN74LVC1G06DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C065, C06F, C06J, C06R) (C06H, C06P, C06S)
SN74LVC1G06DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C065, C06F, C06J, C06R) (C06H, C06P, C06S)
SN74LVC1G06DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F
SN74LVC1G06DBVTG4.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C06F
SN74LVC1G06DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTJ, CTK, CTR, CTT) (CTH, CTS)
SN74LVC1G06DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTJ, CTK, CTR, CTT) (CTH, CTS)
SN74LVC1G06DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTJ, CTK, CTR, CTT) (CTH, CTS)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G06DCKRE4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKRE4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT5
SN74LVC1G06DCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT5
SN74LVC1G06DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTJ, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTJ, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKTE4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKTE4.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKTG4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DCKTG4.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5, CTF, CTK, CTR) (CTH, CTS)
SN74LVC1G06DPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CO
SN74LVC1G06DPWR.B	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CO
SN74LVC1G06DRLR	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CT7, CTR)
SN74LVC1G06DRLR.B	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CT7, CTR)
SN74LVC1G06DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DRYRG4	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DRYRG4.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CT

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G06DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DSFRG4	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06DSFRG4.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT
SN74LVC1G06YZPR	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CTN
SN74LVC1G06YZPR.B	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CTN
SN74LVC1G06YZVR	Active	Production	DSBGA (YZV) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CT N
SN74LVC1G06YZVR.B	Active	Production	DSBGA (YZV) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CT N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVC1G06 :

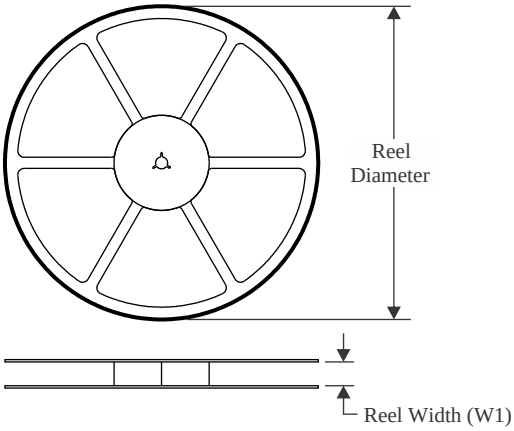
- Automotive : SN74LVC1G06-Q1
- Enhanced Product : SN74LVC1G06-EP

NOTE: Qualified Version Definitions:

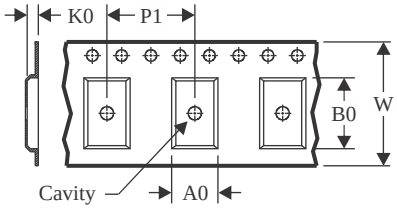
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

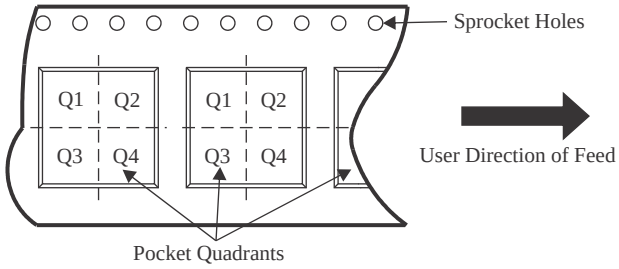


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

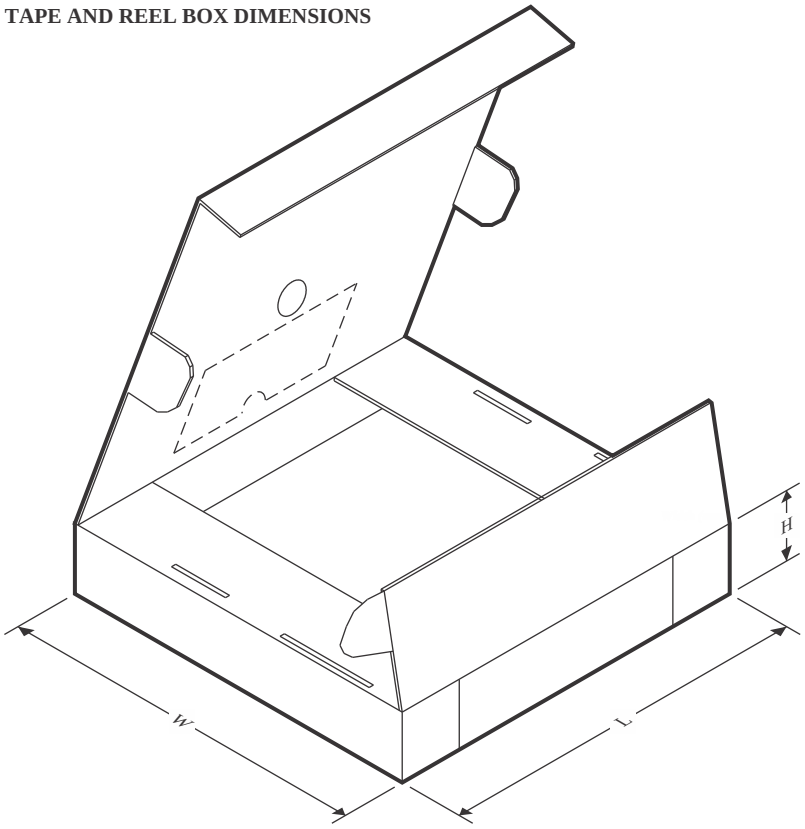


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G06DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G06DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G06DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G06DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G06DCKRE4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G06DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G06DCKTE4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKTE4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G06DCKTE4	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G06DCKTG4	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G06DCKTG4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G06DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G06DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G06DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G06DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G06DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G06DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G06DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G06YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G06YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G06DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G06DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G06DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G06DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G06DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G06DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G06DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
SN74LVC1G06DCKRE4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G06DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKTE4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKTE4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DCKTE4	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G06DCKTG4	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G06DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0

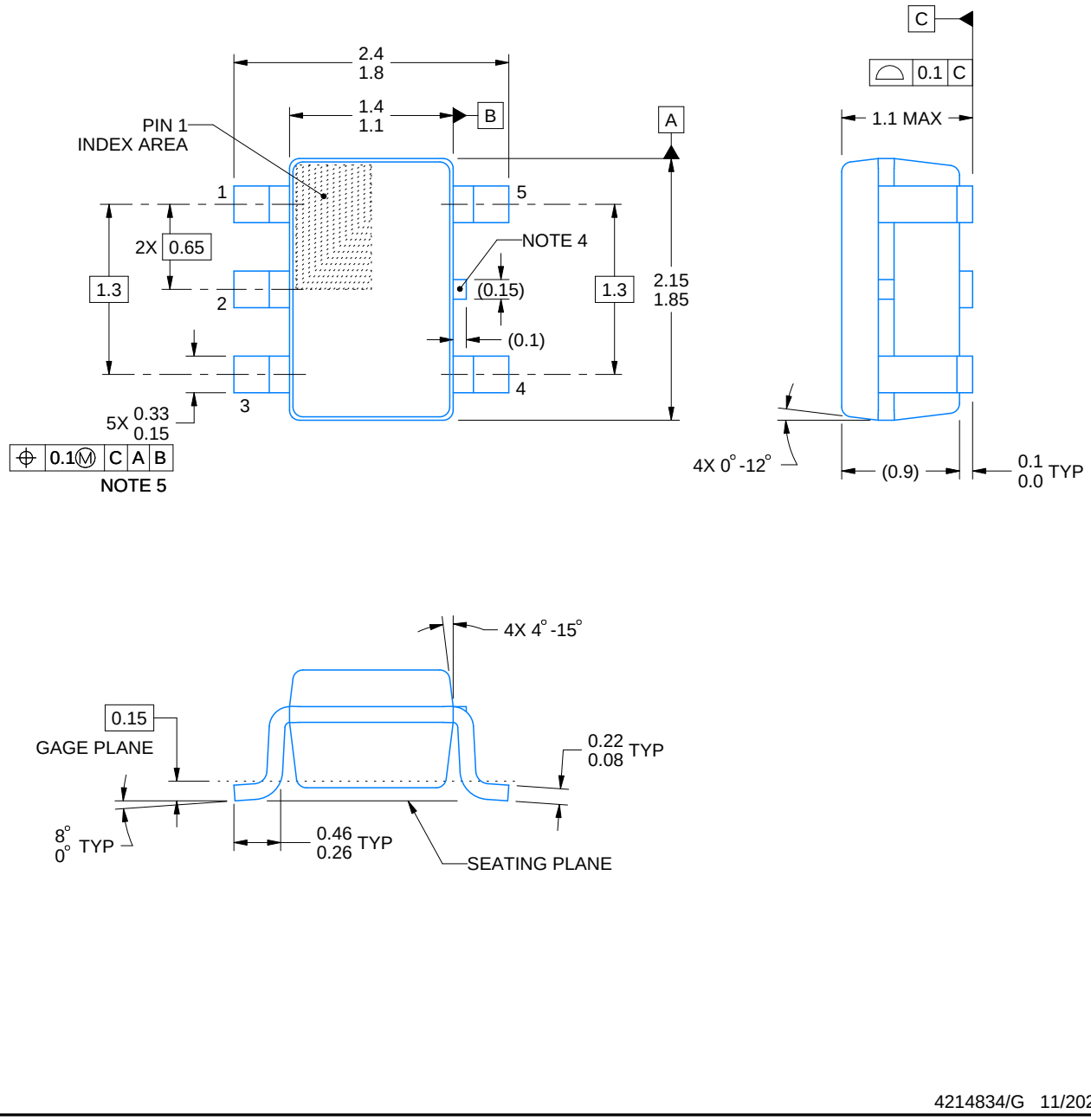
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G06DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G06DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G06DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G06DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G06DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G06DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G06DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G06YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G06YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

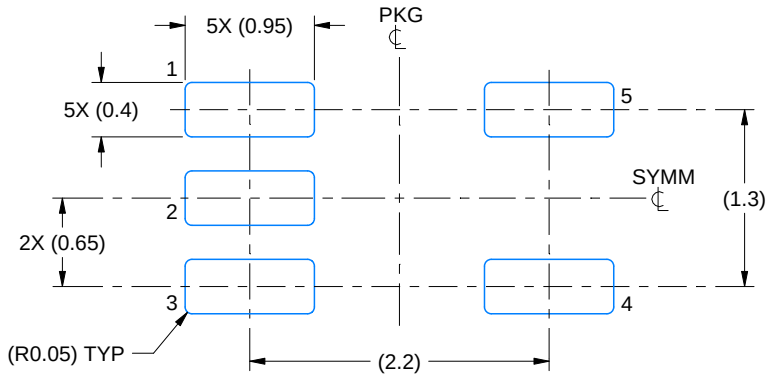
SMALL OUTLINE TRANSISTOR



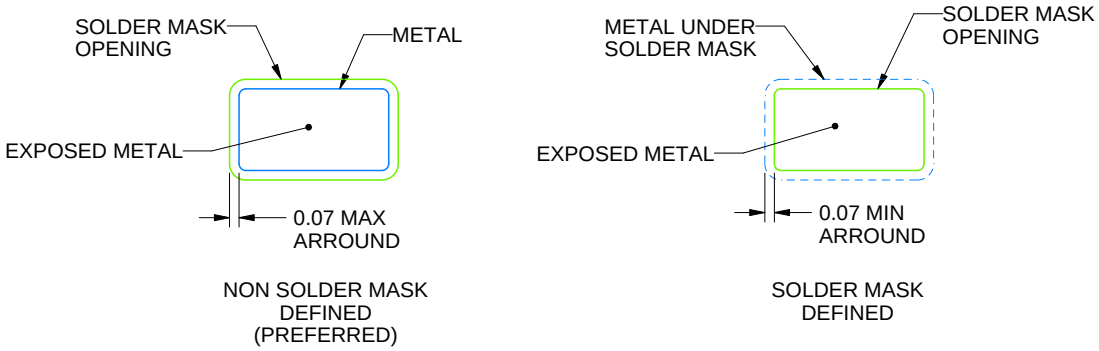
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

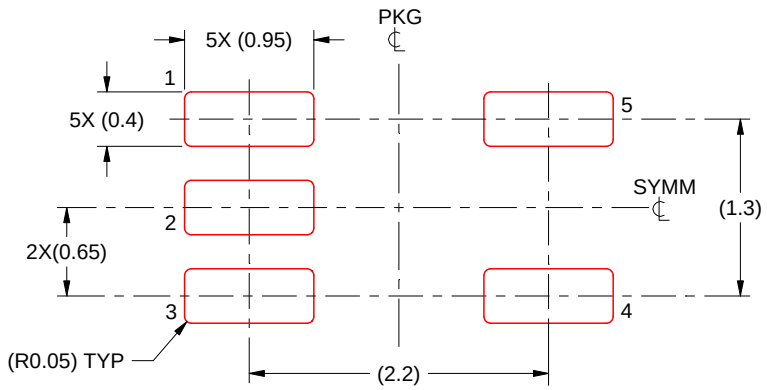


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

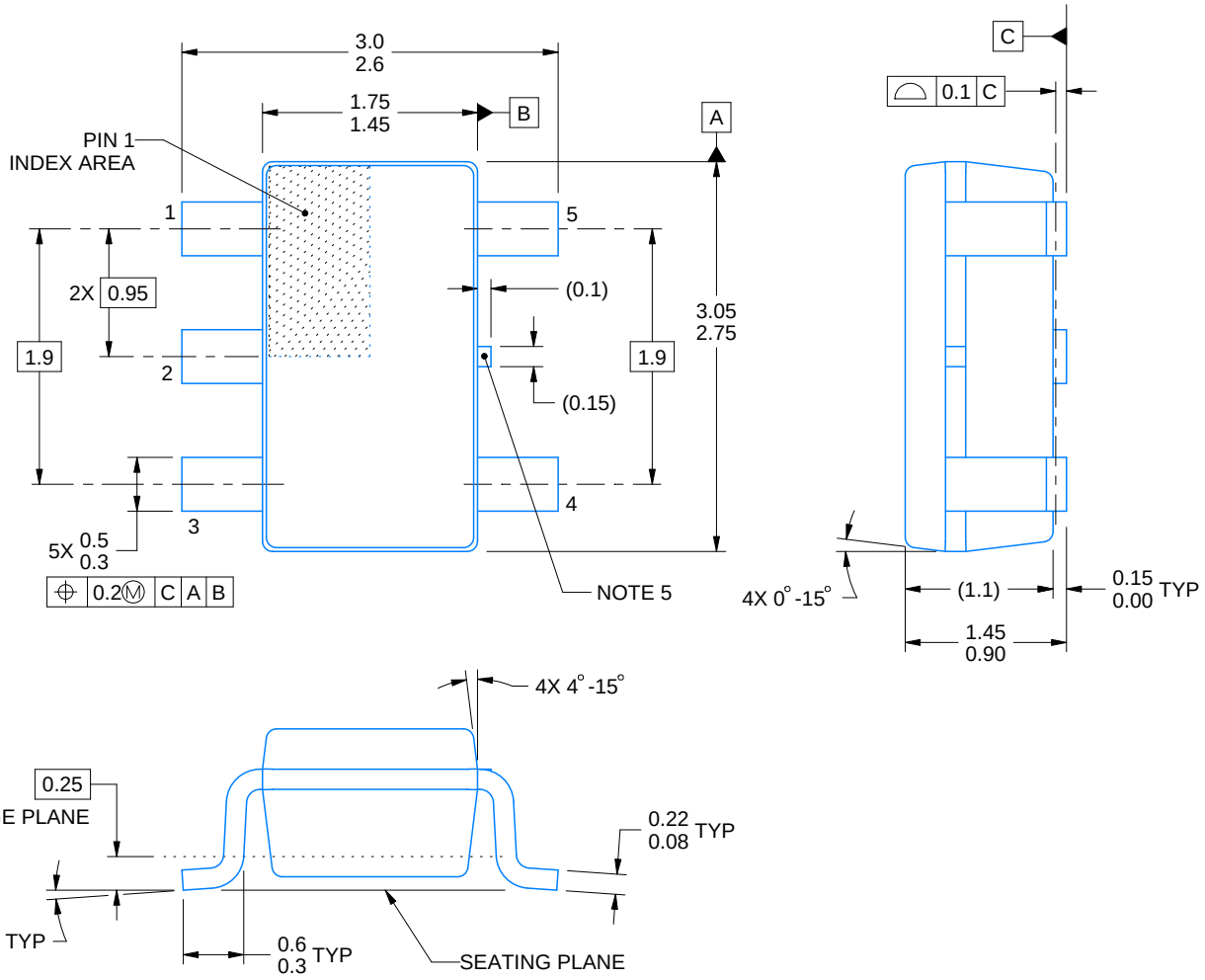
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

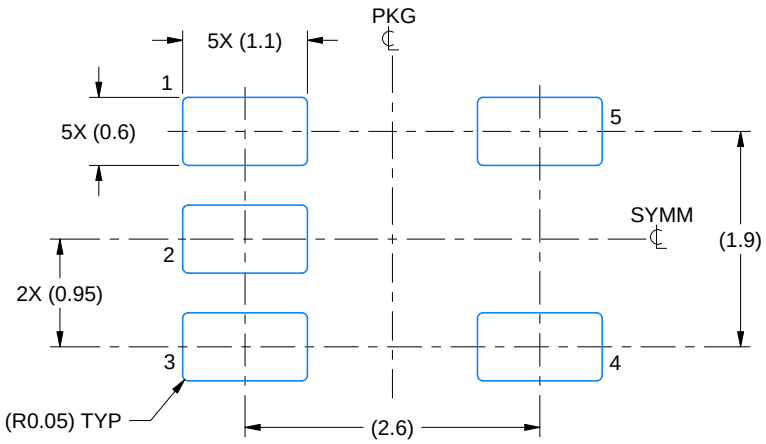
SMALL OUTLINE TRANSISTOR



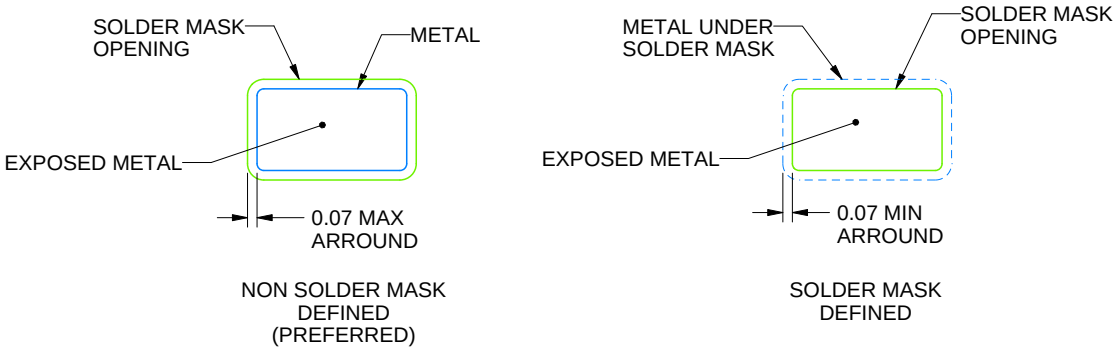
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

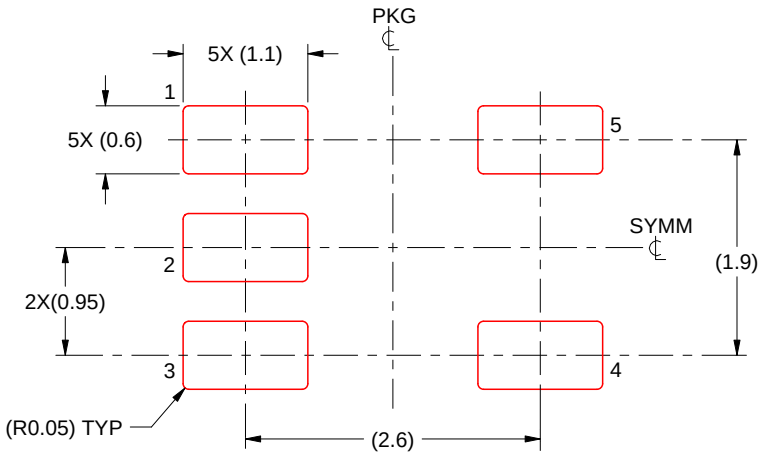


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

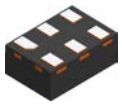
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

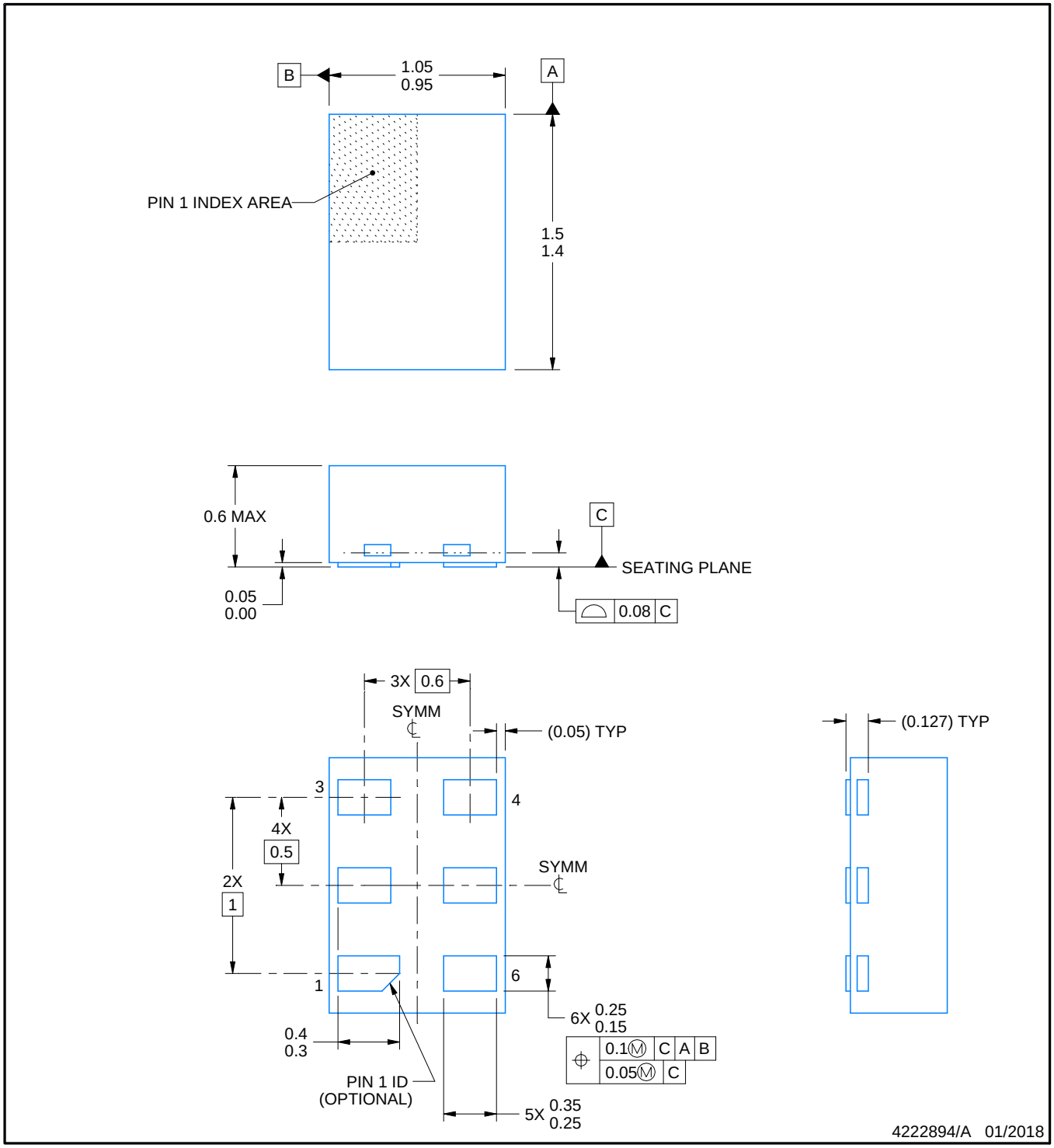
DRY0006A



PACKAGE OUTLINE

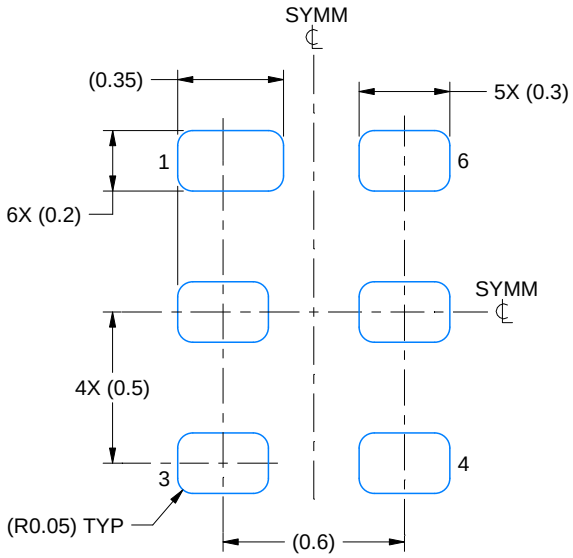
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

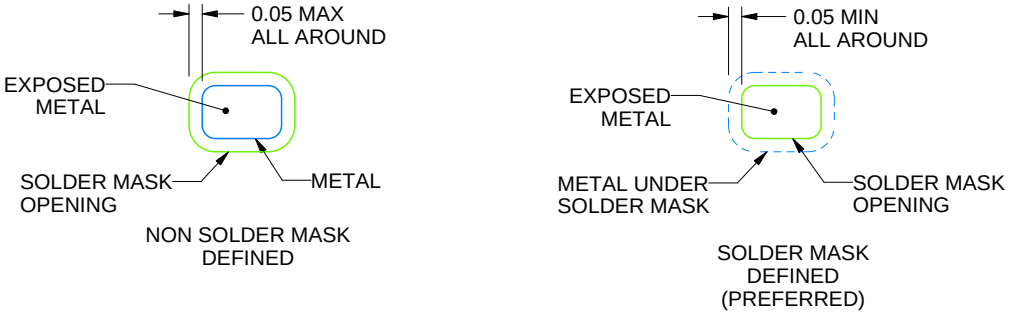


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

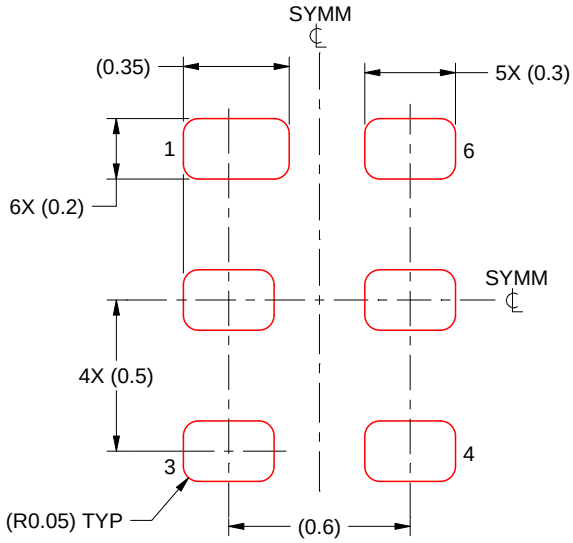
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

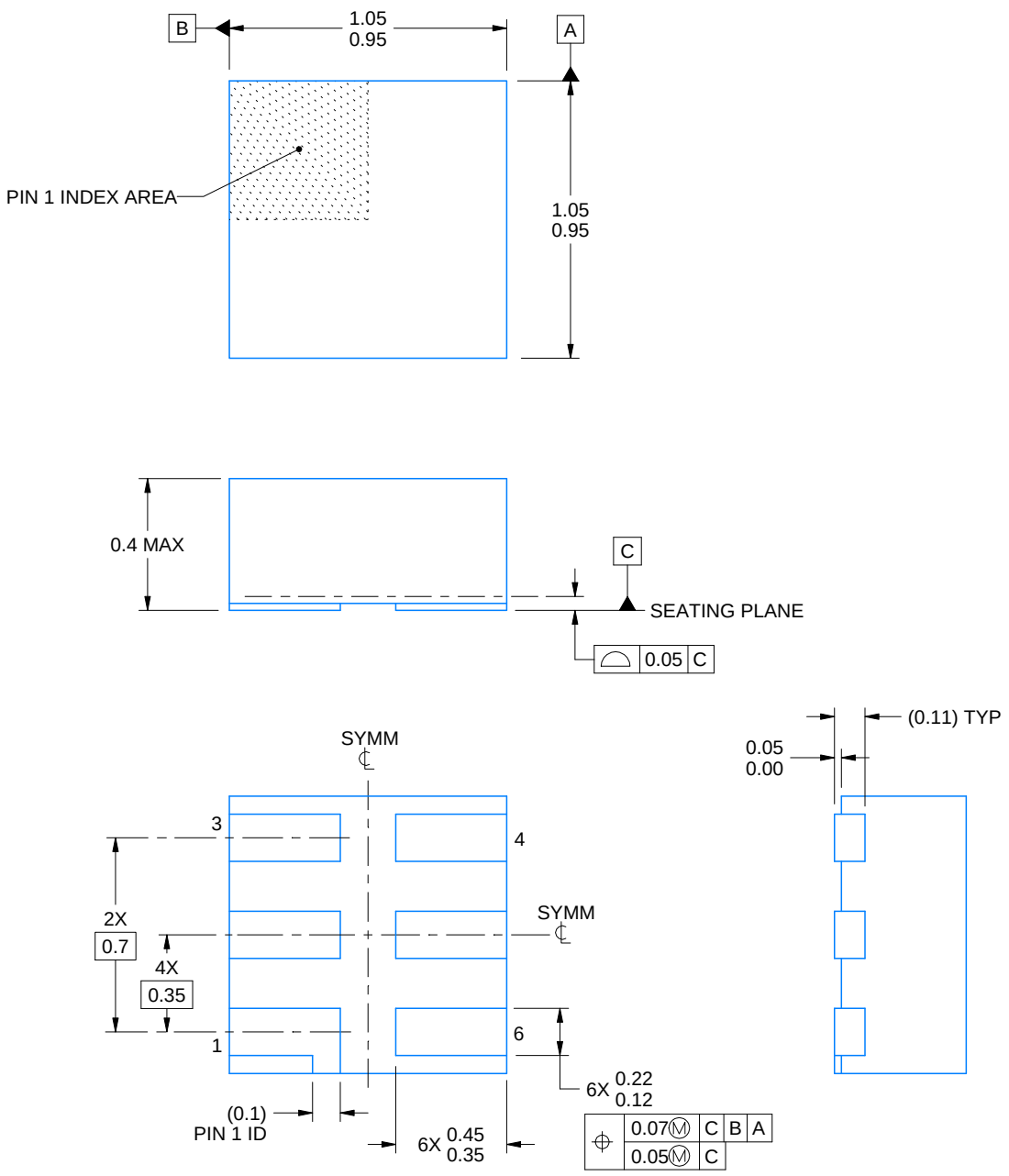
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

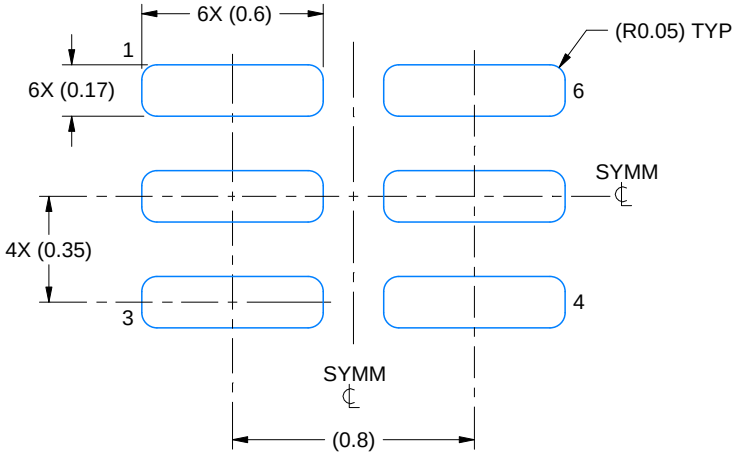
PLASTIC SMALL OUTLINE - NO LEAD



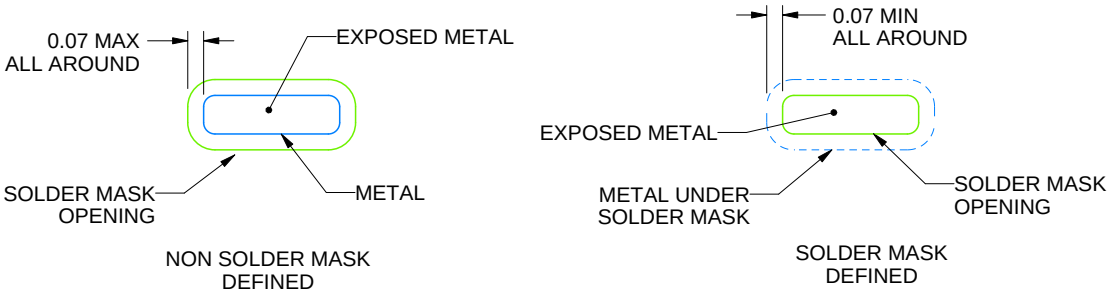
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

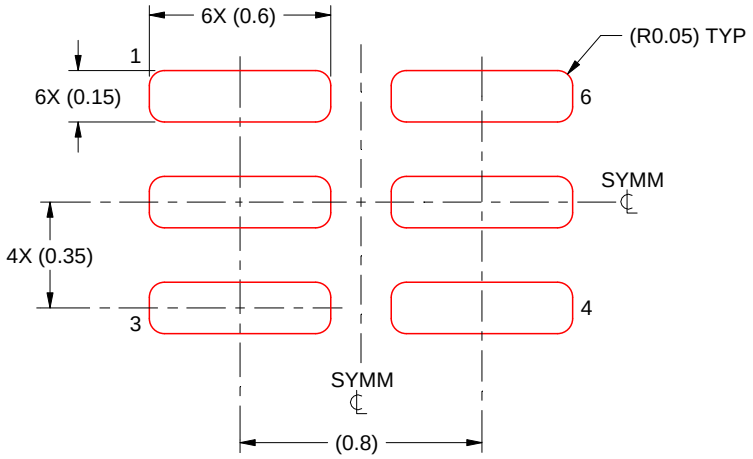
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

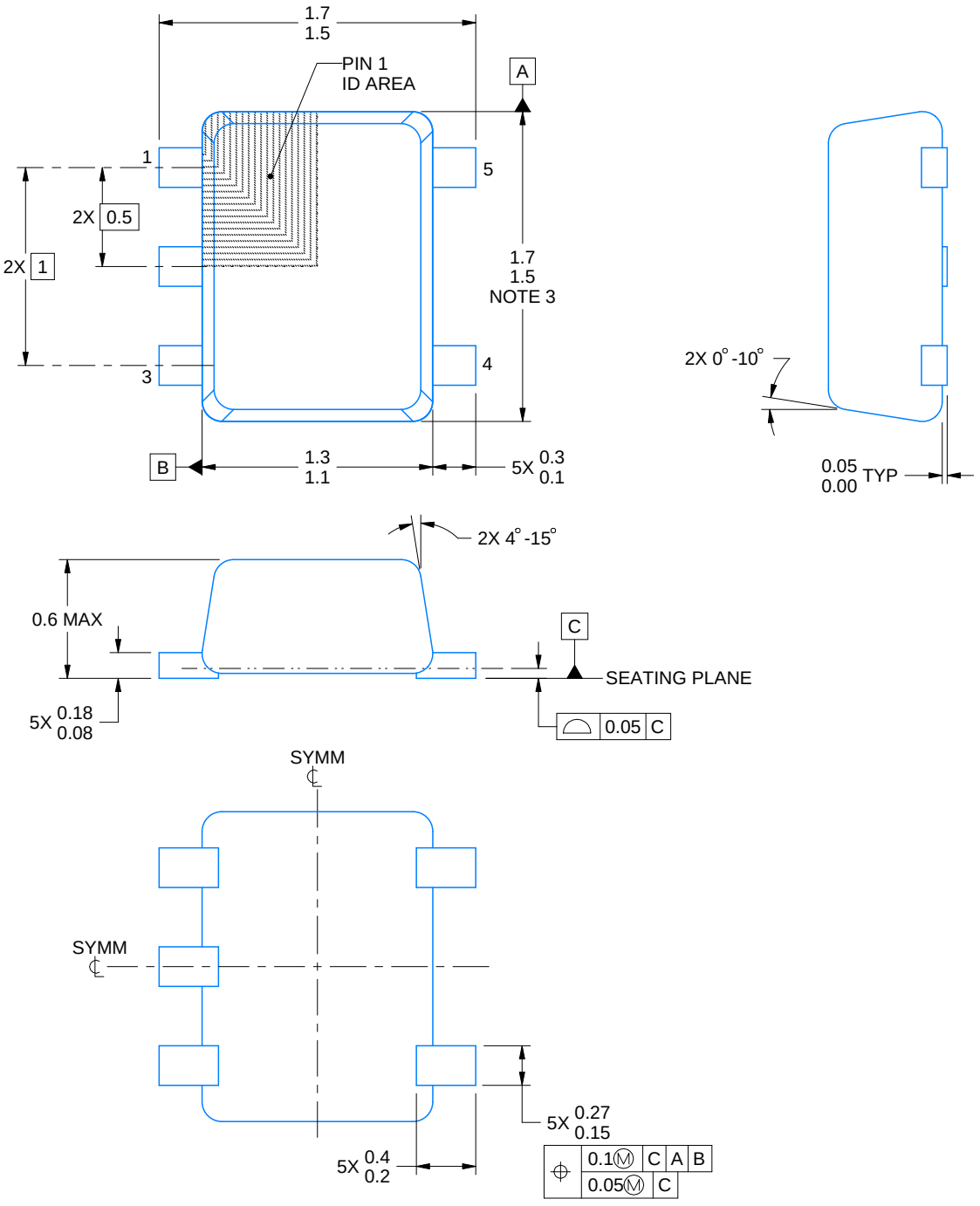
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

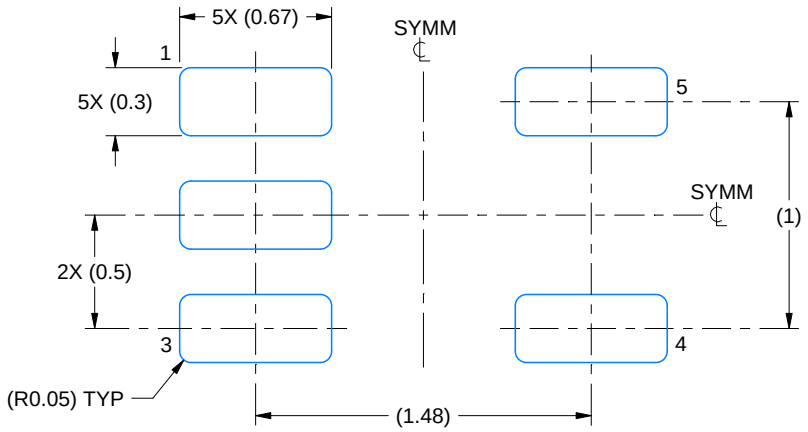
PLASTIC SMALL OUTLINE



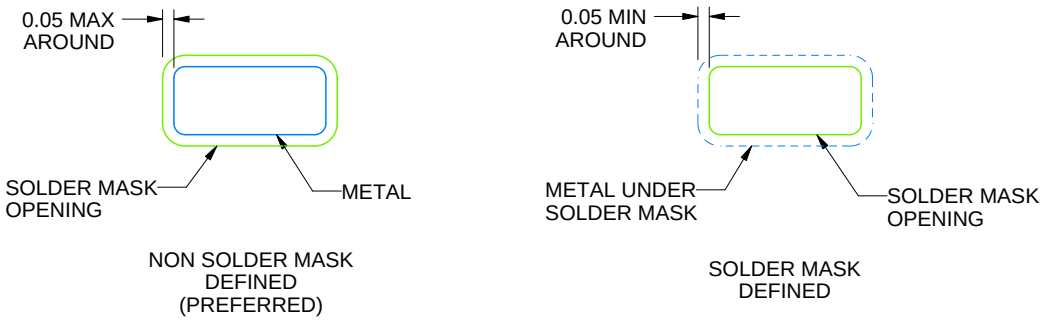
4220753/E 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

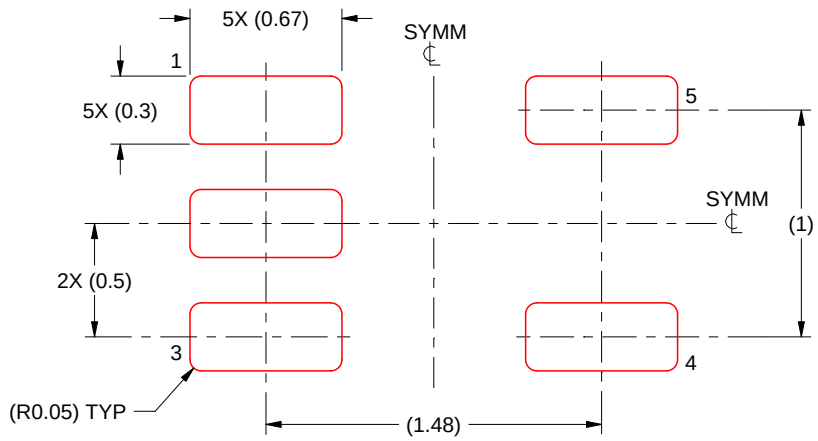


SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

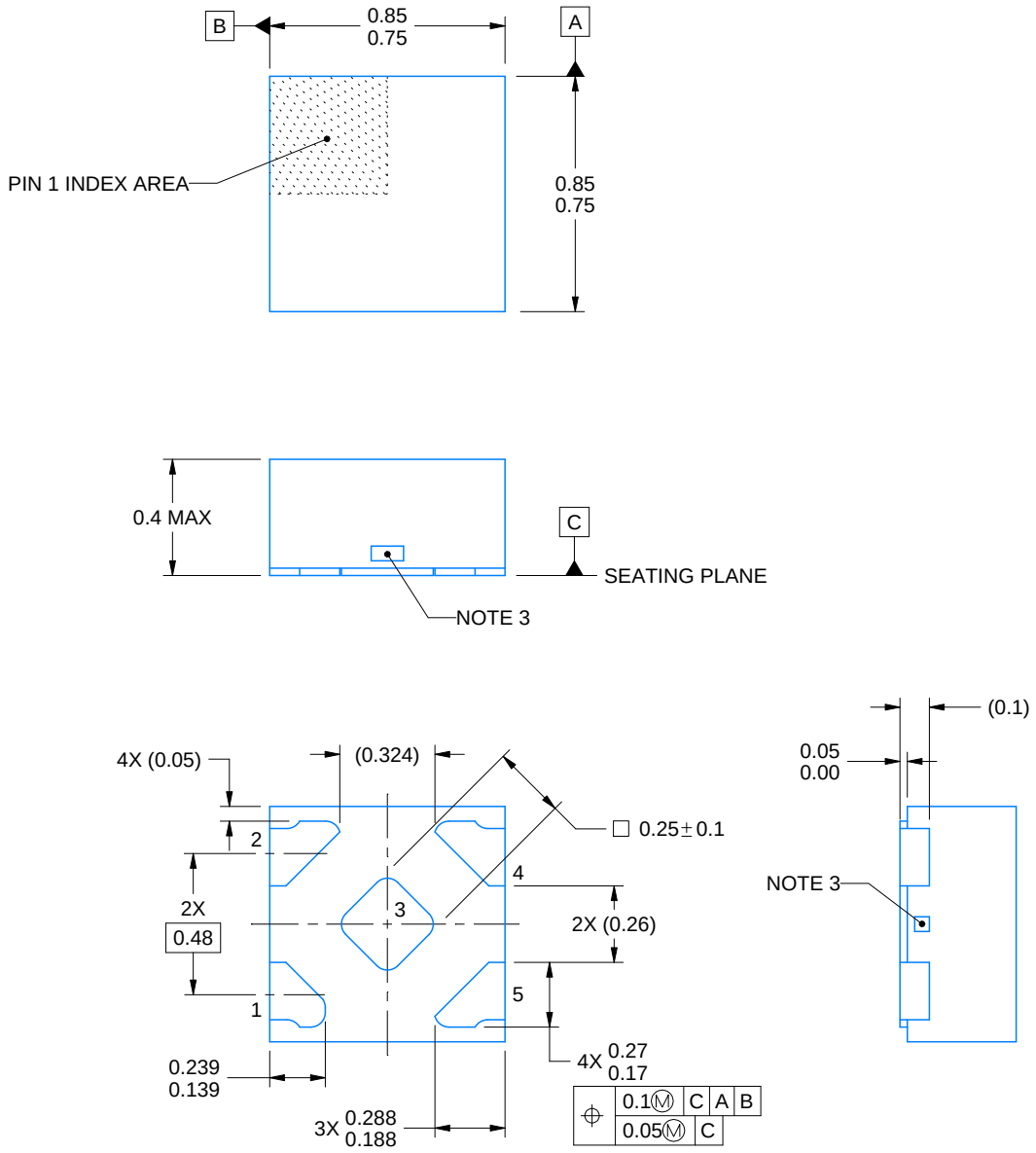
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

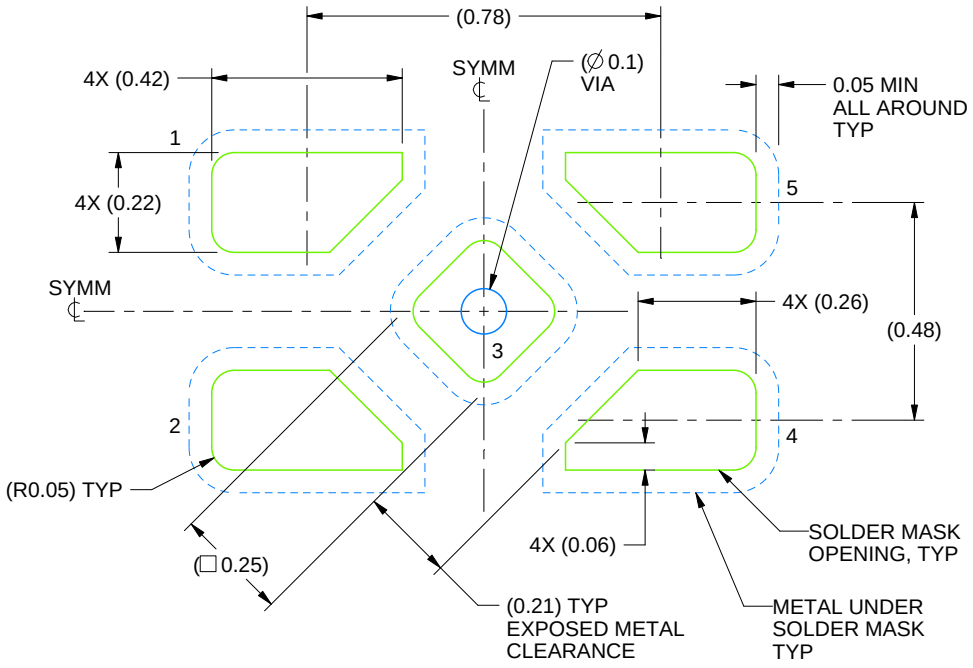
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

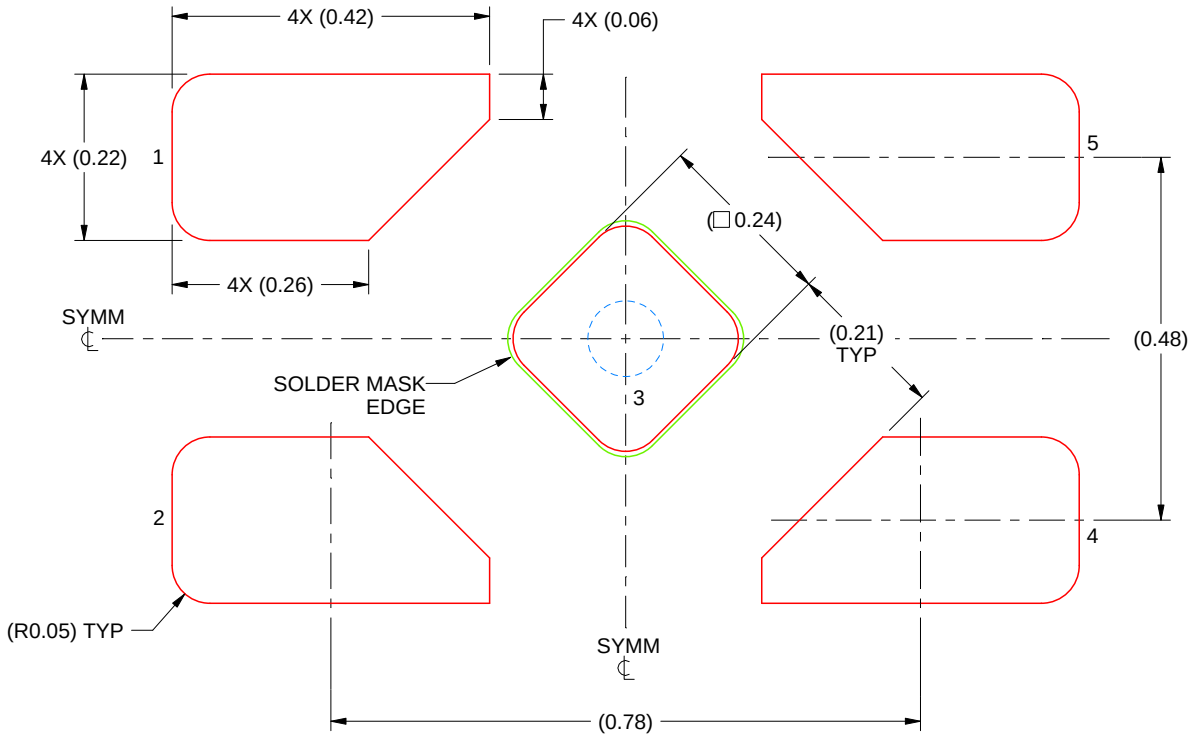
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

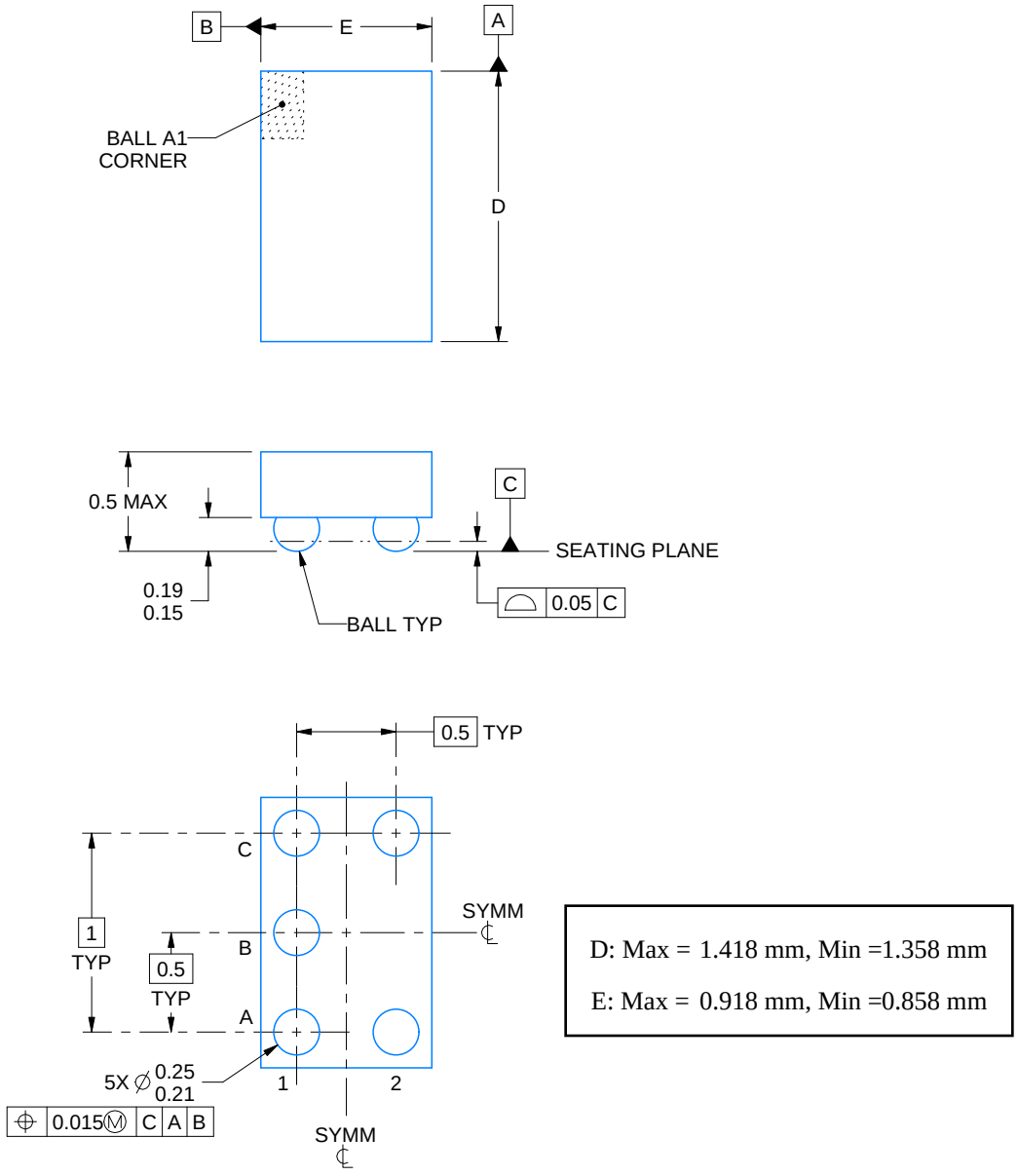
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



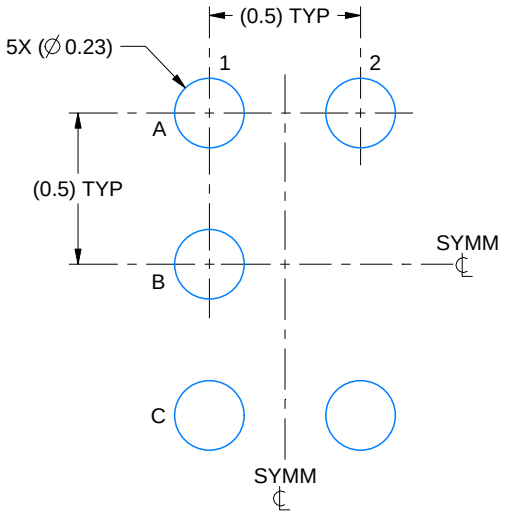
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

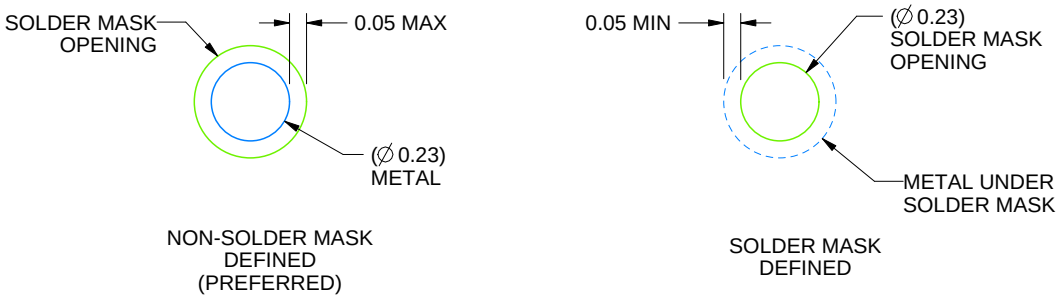
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

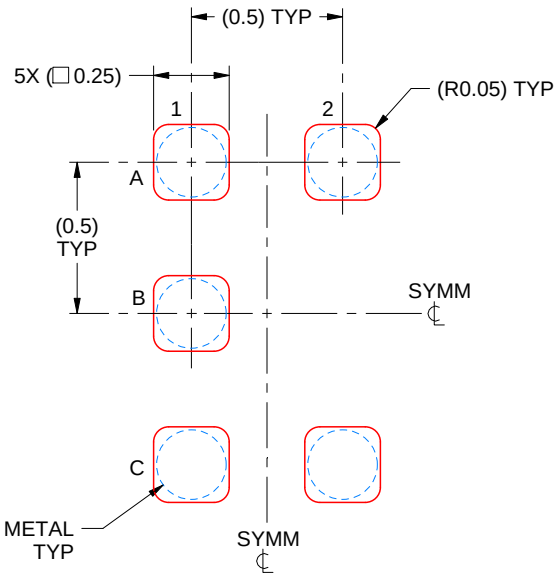


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



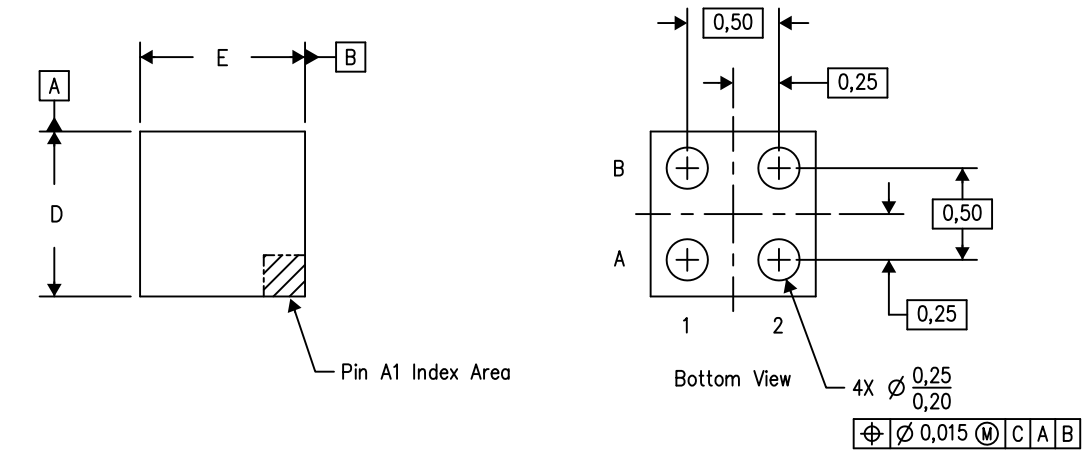
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

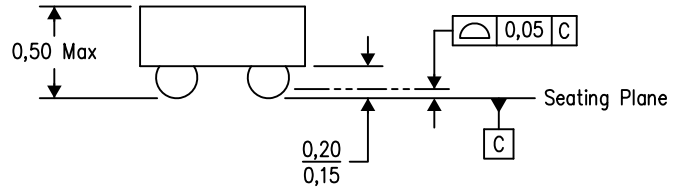
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY





D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4206083/C 07/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025