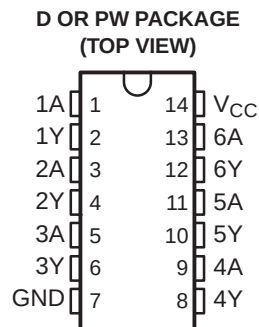


## HEX INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

### FEATURES

- Qualified for Automotive Applications
- Operate From 1.65 V to 3.6 V
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
- Max  $t_{pd}$  of 3.7 ns at 3.3 V
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17



### DESCRIPTION/ORDERING INFORMATION

This hex inverter buffer/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The outputs of the SN74LVC06A device are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION<sup>(1)</sup>

| $T_A$          | PACKAGE <sup>(2)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 125°C | SOIC – D               | Reel of 2500 | SN74LVC06AQDRQ1       | LVC06AQ          |
|                | TSSOP – PW             | Reel of 2000 | SN74LVC06AQPWRQ1      | LVC06AQ          |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

### FUNCTION TABLE (EACH INVERTER)

| INPUT<br>A | OUTPUT<br>Y |
|------------|-------------|
| H          | L           |
| L          | H           |

### LOGIC DIAGRAM, EACH INVERTER (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|               |                                            | MIN        | MAX  | UNIT |
|---------------|--------------------------------------------|------------|------|------|
| $V_{CC}$      | Supply voltage range                       | –0.5       | 6.5  | V    |
| $V_I$         | Input voltage range <sup>(2)</sup>         | –0.5       | 6.5  | V    |
| $V_O$         | Output voltage range                       | –0.5       | 6.5  | V    |
| $I_{IK}$      | Input clamp current                        | $V_I < 0$  | –50  | mA   |
| $I_{OK}$      | Output clamp current                       | $V_O < 0$  | –50  | mA   |
| $I_O$         | Continuous output current                  |            | ±50  | mA   |
|               | Continuous current through $V_{CC}$ or GND |            | ±100 | mA   |
| $\theta_{JA}$ | Package thermal impedance <sup>(3)</sup>   | D package  | 86   | °C/W |
|               |                                            | PW package | 113  |      |
| $T_{stg}$     | Storage temperature range                  | –65        | 150  | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

|          |                                | MIN                                          | MAX                  | UNIT |
|----------|--------------------------------|----------------------------------------------|----------------------|------|
| $V_{CC}$ | Supply voltage                 | Operating                                    | 1.65                 | 3.6  |
|          |                                | Data retention only                          | 1.5                  |      |
| $V_{IH}$ | High-level input voltage       | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.65 \times V_{CC}$ | V    |
|          |                                | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$   | 1.7                  |      |
|          |                                | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$   | 2                    |      |
| $V_{IL}$ | Low-level input voltage        | $V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$ | $0.35 \times V_{CC}$ | V    |
|          |                                | $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$   | 0.7                  |      |
|          |                                | $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$   | 0.8                  |      |
| $V_I$    | Input voltage                  | 0                                            | 5.5                  | V    |
| $V_O$    | Output voltage                 | 0                                            | 5.5                  | V    |
| $I_{OL}$ | Low-level output current       | $V_{CC} = 1.65 \text{ V}$                    | 4                    | mA   |
|          |                                | $V_{CC} = 2.3 \text{ V}$                     | 8                    |      |
|          |                                | $V_{CC} = 2.7 \text{ V}$                     | 12                   |      |
|          |                                | $V_{CC} = 3 \text{ V}$                       | 24                   |      |
| $T_A$    | Operating free-air temperature | –40                                          | 125                  | °C   |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS                                                              | V <sub>CC</sub> | MIN | TYP <sup>(1)</sup> | MAX  | UNIT |
|------------------|------------------------------------------------------------------------------|-----------------|-----|--------------------|------|------|
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 µA                                                     | 1.65 V to 3.6 V |     |                    | 0.2  | V    |
|                  | I <sub>OL</sub> = 4 mA                                                       | 1.65 V          |     |                    | 0.45 |      |
|                  | I <sub>OL</sub> = 8 mA                                                       | 2.3 V           |     |                    | 0.7  |      |
|                  | I <sub>OL</sub> = 12 mA                                                      | 2.7 V           |     |                    | 0.5  |      |
|                  | I <sub>OL</sub> = 24 mA                                                      | 3 V             |     |                    | 0.65 |      |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND                                                | 3.6 V           |     |                    | ±5   | µA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           |     |                    | 10   | µA   |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V  |     |                    | 1    | mA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           |     | 5                  |      | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## Switching Characteristics

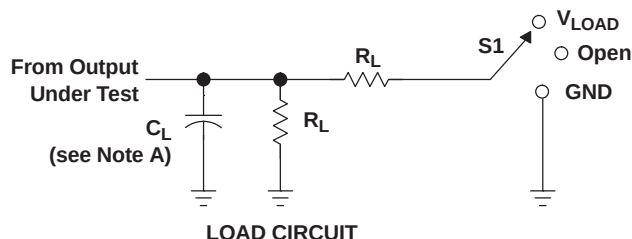
over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| PARAMETER       | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | UNIT |
|-----------------|-----------------|----------------|-------------------------|-----|------------------------------------|-----|------|
|                 |                 |                | MIN                     | MAX | MIN                                | MAX |      |
| t <sub>pd</sub> | A               | Y              |                         | 3.9 | 1                                  | 3.7 | ns   |

## Operating Characteristics, T<sub>A</sub> = 25°C

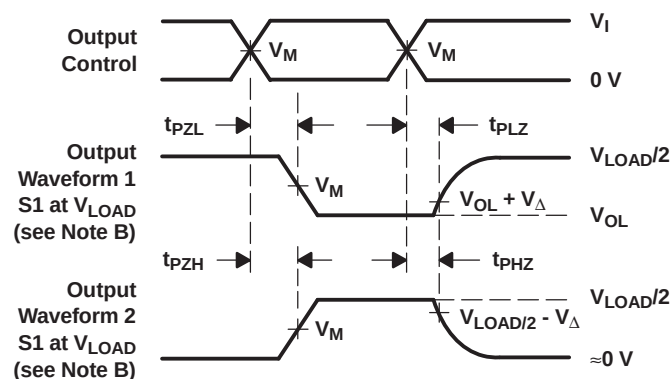
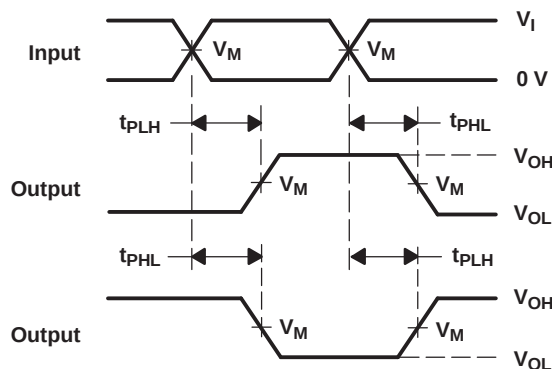
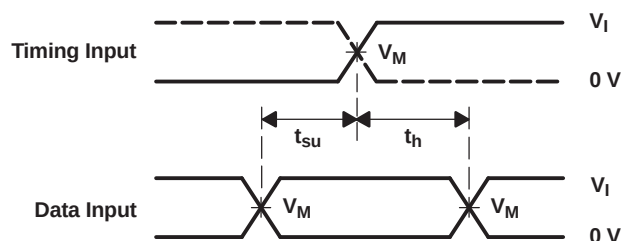
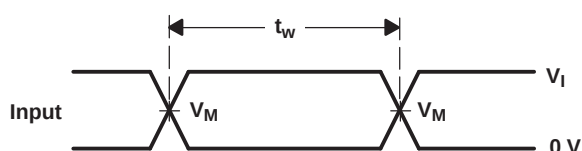
| PARAMETER                                                       | TEST CONDITIONS | V <sub>CC</sub> = 3.3 V | UNIT |
|-----------------------------------------------------------------|-----------------|-------------------------|------|
|                                                                 |                 | TYP                     |      |
| C <sub>pd</sub> Power dissipation capacitance per buffer/driver | f = 10 MHz      | 2.5                     | pF   |

## PARAMETER MEASUREMENT INFORMATION (OPEN DRAIN)



| TEST                          | S1         |
|-------------------------------|------------|
| $t_{PZL}$ (see Notes E and F) | $V_{LOAD}$ |
| $t_{PLZ}$ (see Notes E and G) | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$             | $V_{LOAD}$ |

| $V_{CC}$          | INPUT |               | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$        | $V_{\Delta}$ |
|-------------------|-------|---------------|-------|------------|-------|--------------|--------------|
|                   | $V_I$ | $t_r/t_f$     |       |            |       |              |              |
| 2.7 V             | 2.7 V | $\leq 2.5$ ns | 1.5 V | 6 V        | 50 pF | 500 $\Omega$ | 0.3 V        |
| 3.3 V $\pm$ 0.3 V | 2.7 V | $\leq 2.5$ ns | 1.5 V | 6 V        | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50$   $\Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .
  - $t_{PZL}$  is measured at  $V_M$ .
  - $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74LVC06AQDRG4Q1</a>  | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC06AQ             |
| SN74LVC06AQDRG4Q1.B                | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC06AQ             |
| <a href="#">SN74LVC06AQDRQ1</a>    | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC06AQ             |
| SN74LVC06AQDRQ1.B                  | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC06AQ             |
| <a href="#">SN74LVC06AQPWRG4Q1</a> | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC06AQ             |
| SN74LVC06AQPWRG4Q1.B               | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC06AQ             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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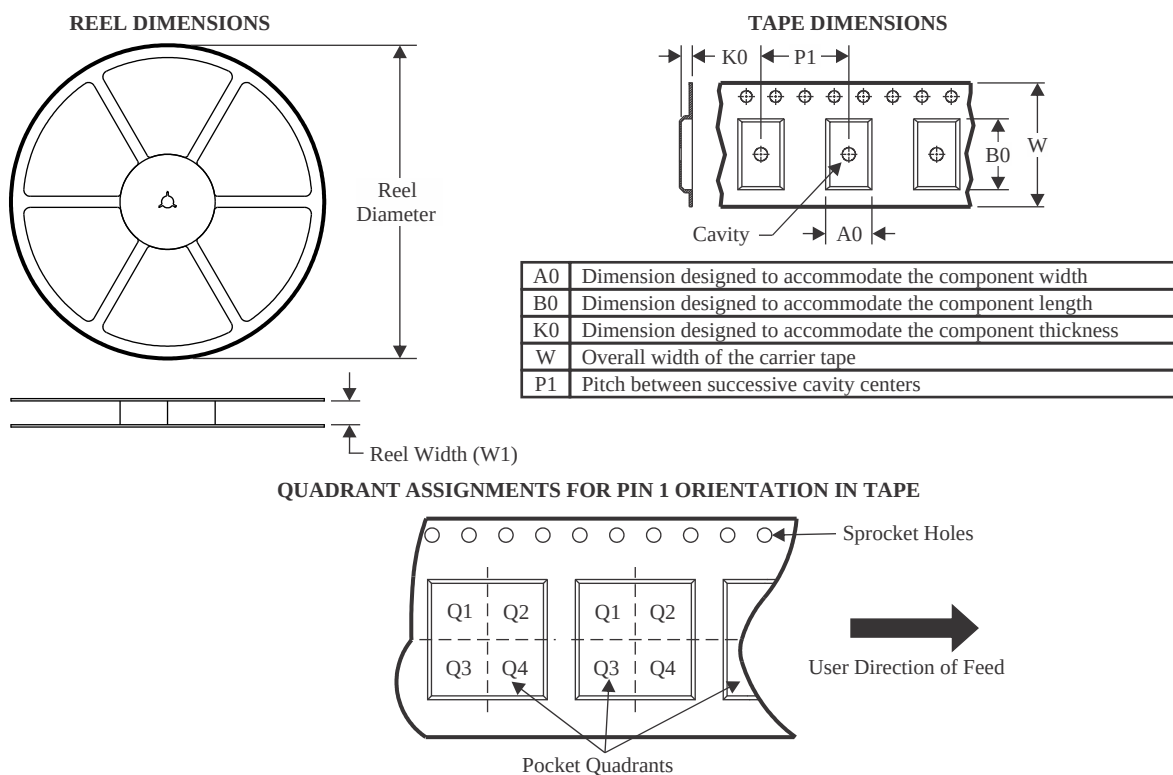
**OTHER QUALIFIED VERSIONS OF SN74LVC06A-Q1 :**

- Catalog : [SN74LVC06A](#)
- Enhanced Product : [SN74LVC06A-EP](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

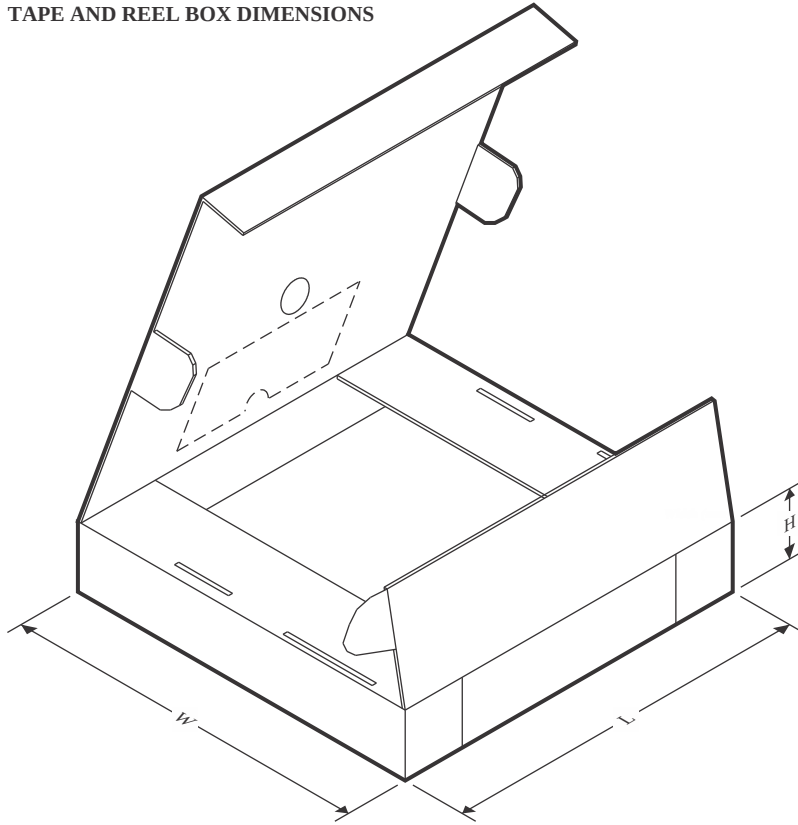
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

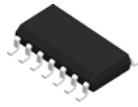
| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC06AQPWRG4Q1 | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

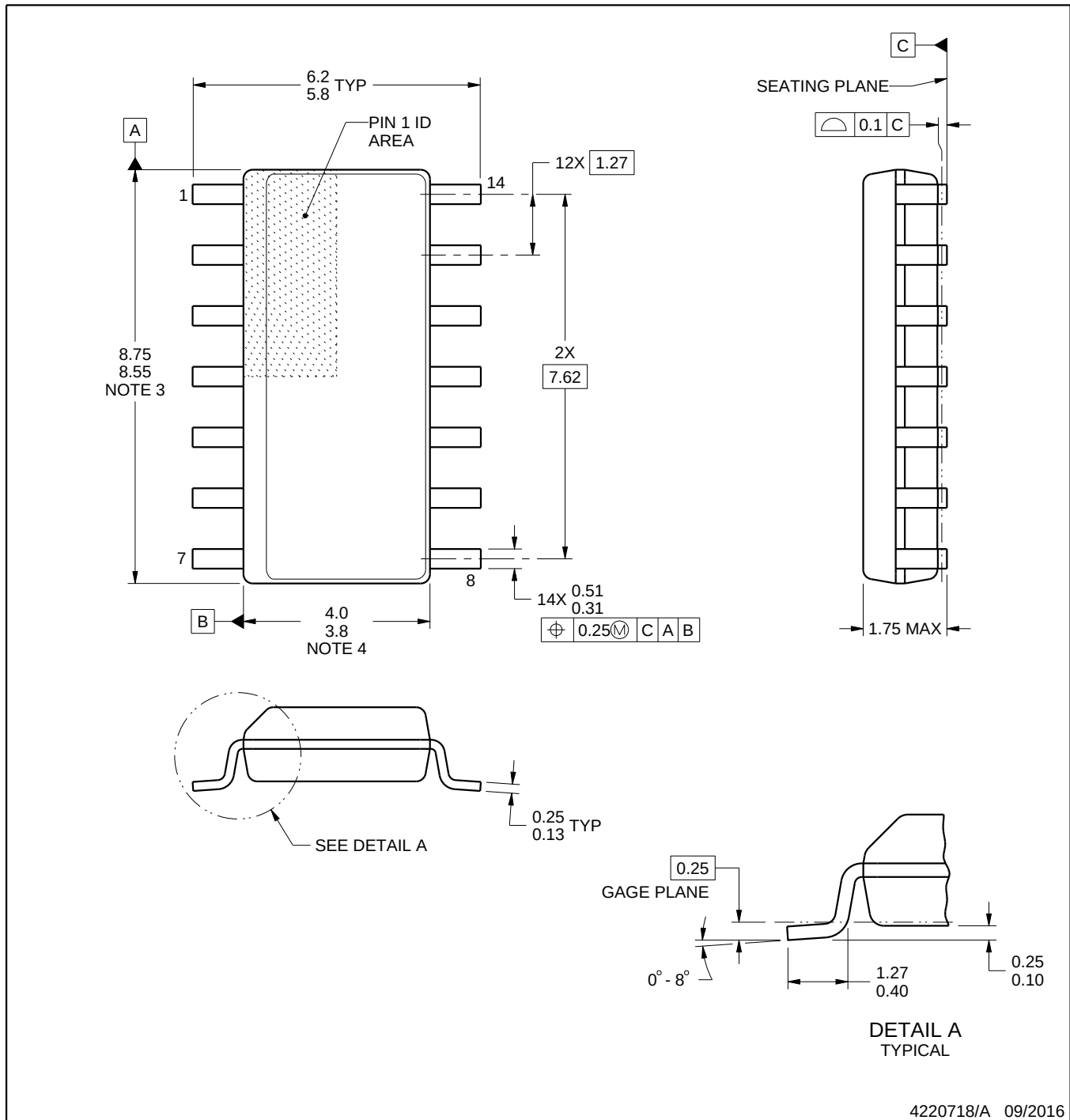


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC06AQPWRG4Q1 | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

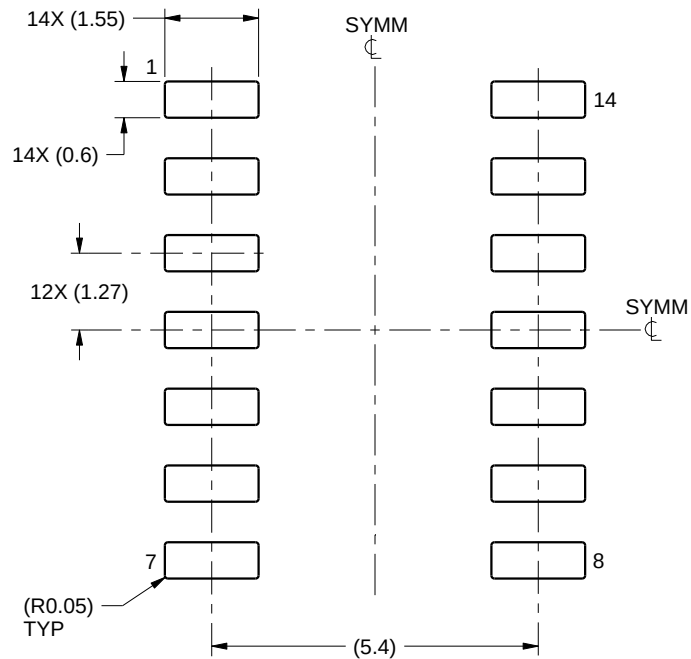


# EXAMPLE BOARD LAYOUT

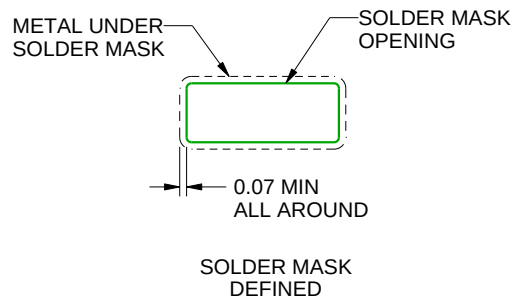
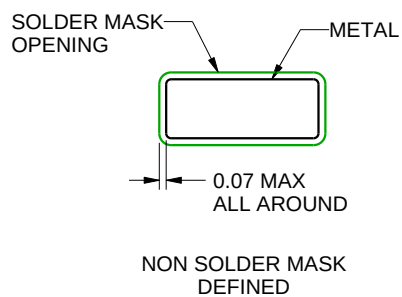
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

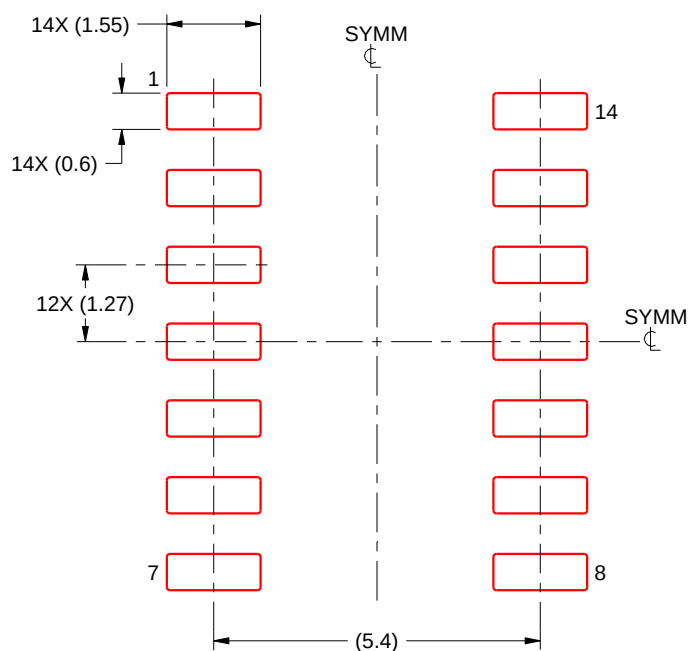
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

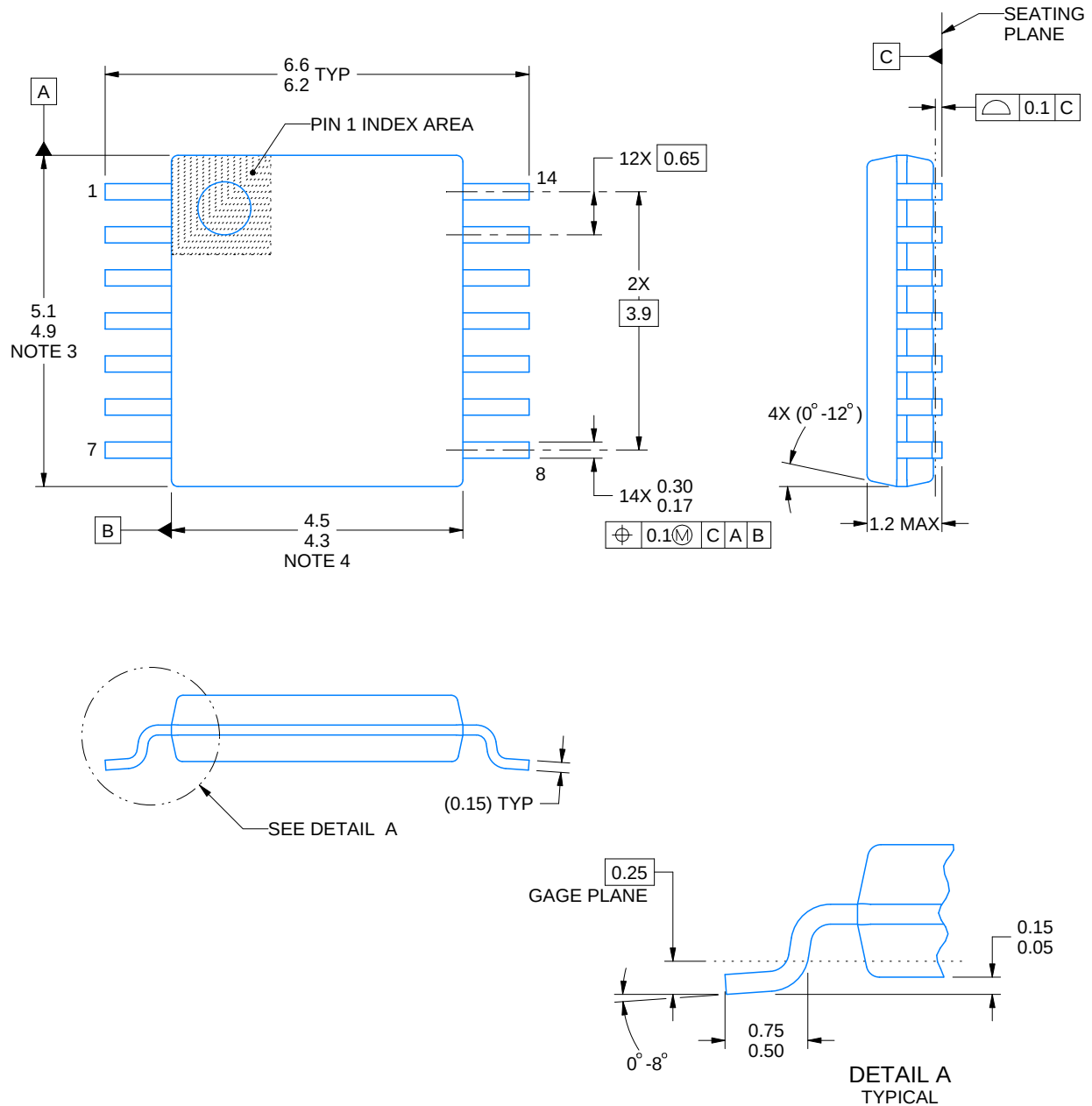
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**PW0014A**

## PACKAGE OUTLINE

**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

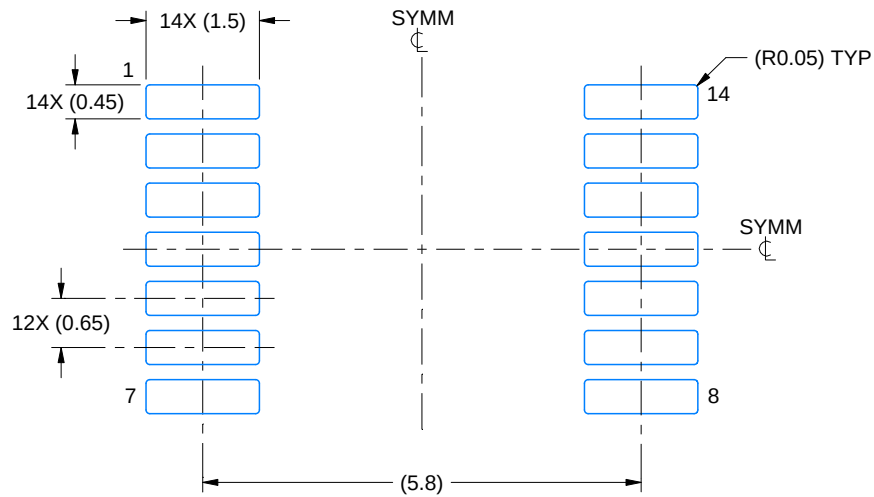
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

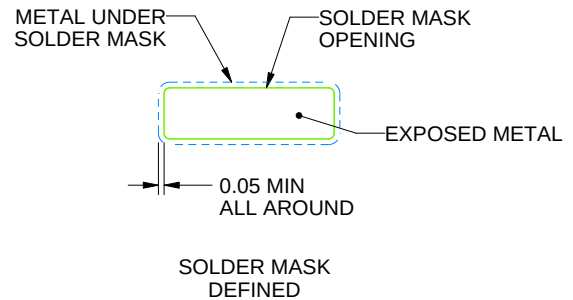
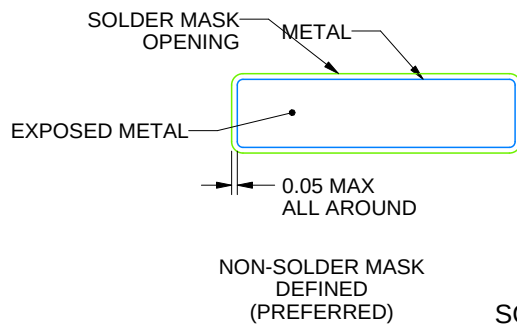
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

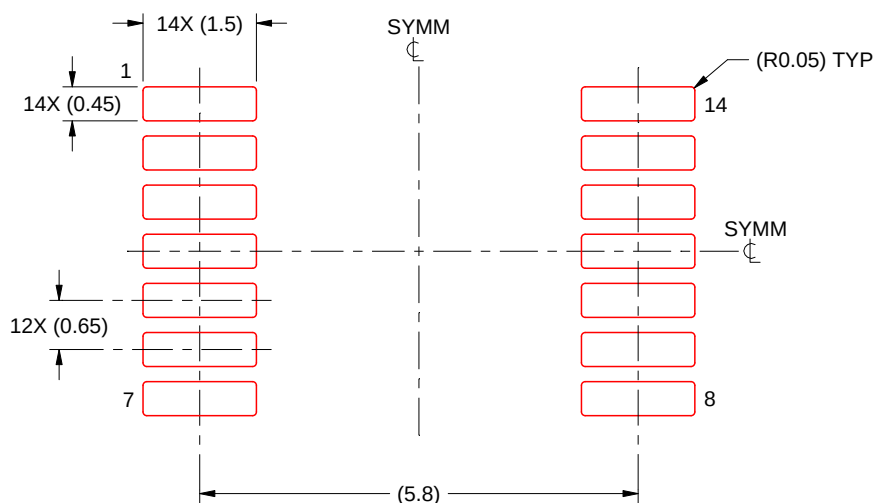
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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