SN74LV595B-EP Enhanced Product, 2-V to 5.5-V, Low-Noise, 8-bit Shift Register With 3-State Outputs

1 Features

- 2 V to 5.5 V V_{CC} operation
- Supports mixed-mode voltage operation on all ports
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 17
- Operating ambient temperature: -55°C to +125°C
- Supports defense, aerospace, and medical applications:
  - Controlled baseline
  - One assembly and test site
  - One fabrication site
  - Extended product life cycle
  - Product traceability

2 Applications

- Output expansion
- LED matrix control
- 7-segment display control

3 Description

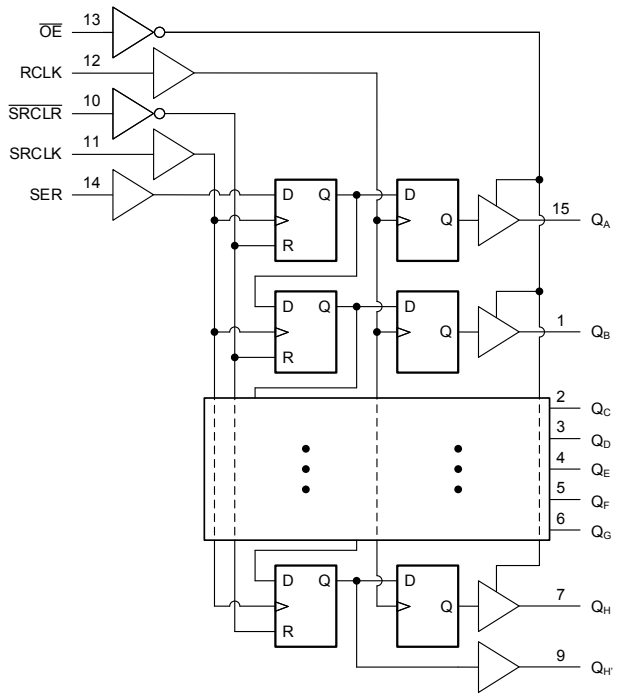
The SN74LV595B-EP contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{OE}$) input is high, all outputs except $Q_{H'}$ are in the high-impedance state.

The device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (2)
SN74LV595B-EP	PW (TSSOP, 16)	5.00 mm × 6.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial Release

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5 Pin Configuration and Functions

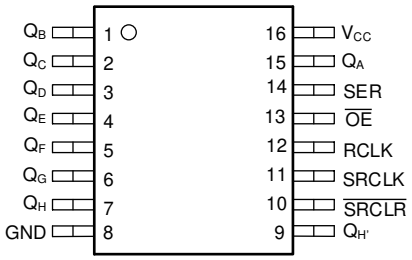


Figure 5-1. SN74LV595B-EP: PW Package, 16-Pin TSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
GND	8	G	Ground
$\overline{OE}$	13	I	Output Enable Pin
Q_A	15	O	Q_A Output
Q_B	1	O	Q_B Output
Q_C	2	O	Q_C Output
Q_D	3	O	Q_D Output
Q_E	4	O	Q_E Output
Q_F	5	O	Q_F Output
Q_G	6	O	Q_G Output
Q_H	7	O	Q_H Output
$Q_{H'}$	9	O	$Q_{H'}$ Output
$\overline{SRCLR}$	10	I	$\overline{SRCLR}$ Input
SRCLK	11	I	SRCLK Input
RCLK	12	I	RCLK Input
SER	14	I	SER Input
V_{CC}	16	P	Positive Supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage (2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–6	
		V_{CC} = 4.5 V to 5.5 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. See *Implications of Slow or Floating CMOS Inputs.*

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV595B-EP PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics.*

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 mA	2 V to 5.5 V	V_{CC} – 0.1			V
	I_{OH} = –2 mA	2.3 V	2			
	I_{OH} = –6 mA	3 V	2.48			
	I_{OH} = –12 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 50 mA	2 V to 5.5 V			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4	
	I_{OL} = 6 mA	3 V			0.44	
	I_{OL} = 12 mA	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0 V			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		3.5		pF

6.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

over operating free-air temperature range (unless otherwise noted)

			T_A = 25°C		T_A = –55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low	7		8.5		ns
		RCLK high or low	7		8.5		
		$\overline{SRCLR}$ low	6		7.5		
t_{su}	Setup time	SER before SRCLK↑	5.5		6.5		ns
		SRCLK↑ before RCLK↑(1)	8		10		
		$\overline{SRCLR}$ low before RCLK↑	8.5		10.5		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	4		5		
t_h	Hold time	SER after SRCLK↑	1.5		2.5		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

6.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over operating free-air temperature range (unless otherwise noted)

			T_A = 25°C		T_A = –55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low	5.5		6.5		ns
		RCLK high or low	5.5		6.5		
		$\overline{SRCLR}$ low	5		6		
t_{su}	Setup time	SER before SRCLK↑	3.5		4.5		ns
		SRCLK↑ before RCLK↑(1)	8		9.5		
		$\overline{SRCLR}$ low before RCLK↑	8		10		
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	3		4		
t_h	Hold time	SER after SRCLK↑	1.5		2.5		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

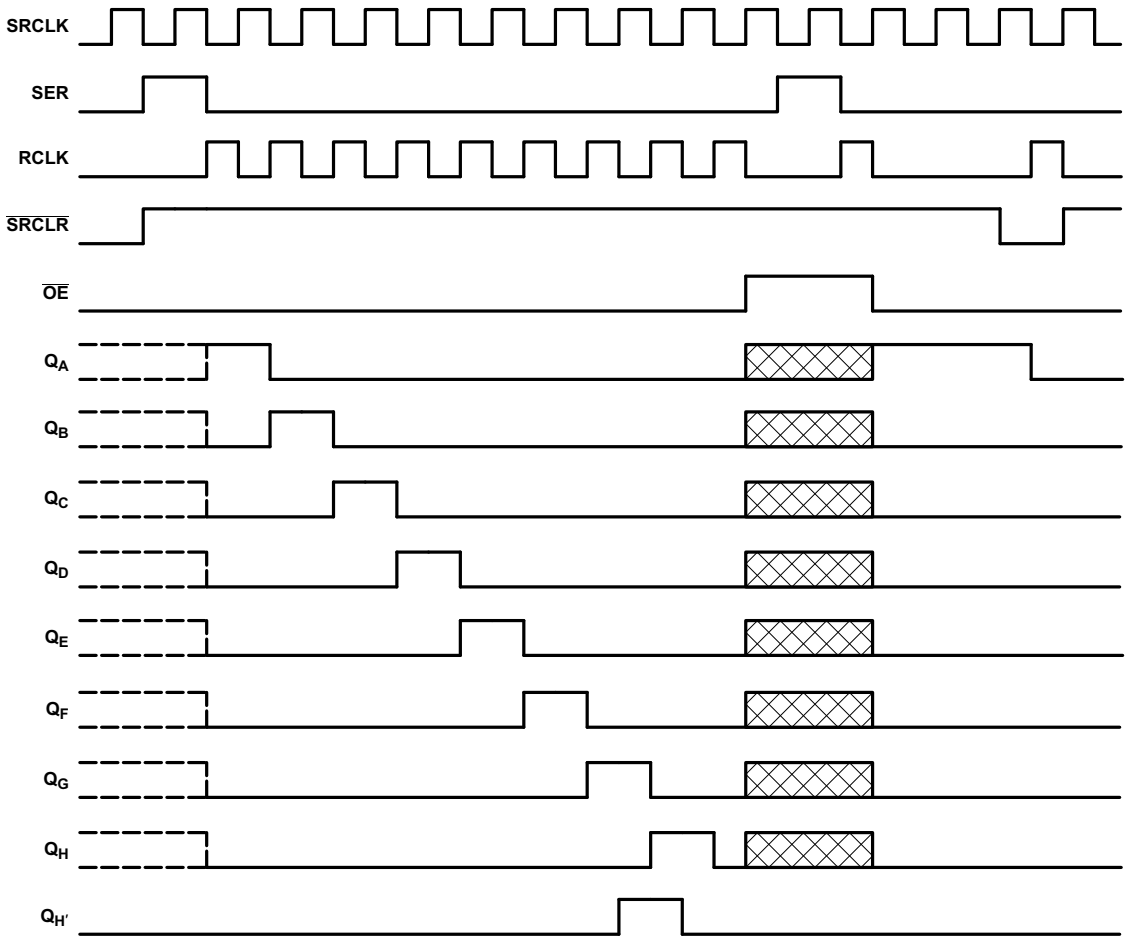
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6.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over operating free-air temperature range (unless otherwise noted)

			T_A = 25°C		T_A = −55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	SRCLK high or low	5		6		ns
		RCLK high or low	5		6		
		$\overline{\text{SRCLR}}$ low	5.2		6.2		
t_{su}	Setup time	SER before SRCLK↑	3		4		ns
		SRCLK↑ before RCLK↑(1)	5		6		
		$\overline{\text{SRCLR}}$ low before RCLK↑	5		6		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	2.5		3.5		
t_h	Hold time	SER after SRCLK↑	2		3		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.



NOTE: ⊠ implies that the output is in 3-State mode.

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Figure 6-1. Timing Diagram

6.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			T_A = −55°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			60	70		30		MHz
t_{PLH}	RCLK	Q_A–Q_H		11.2	17.2	1	22.3	ns
t_{PHL}				11.2	17.2	1	22.3	ns
t_{PLH}	SRCLK	$Q_{H'}$		13.1	22.5	1	28.5	ns
t_{PHL}				13.1	22.5	1	28.5	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$		12.4	18.8	1	24.1	ns
t_{PZH}	$\overline{OE}$	Q_A–Q_H		10.8	17	1	21.3	ns
t_{PZL}				13.4	21	1	26	ns
t_{PHZ}	$\overline{OE}$	Q_A–Q_H		12.2	18.3	1	22.5	ns
t_{PLZ}				14	20.9	1	25.6	ns

6.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			T_A = −55°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			55	105		40		MHz
t_{PLH}	RCLK	Q_A–Q_H		7.9	15.4	1	20	ns
t_{PHL}				7.9	15.4	1	20	ns
t_{PLH}	SRCLK	$Q_{H'}$		9.2	16.5	1	21.5	ns
t_{PHL}				9.2	16.5	1	21.5	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$		9	16.3	1	20.2	ns
t_{PZH}	$\overline{OE}$	Q_A–Q_H		7.8	15	1	20	ns
t_{PZL}				9.6	15	1	20	ns
t_{PHZ}	$\overline{OE}$	Q_A–Q_H		8.1	15.7	1	19.2	ns
t_{PLZ}				9.3	15.7	1	19.2	ns

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6.11 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			T_A = −55°C TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			95	140		75		MHz
t_{PLH}	RCLK	Q_A–Q_H		5.6	9.4	1	13.5	ns
t_{PHL}				5.6	9.4	1	13.5	ns
t_{PLH}	SRCLK	$Q_{H'}$		6.4	10.2	1	14.4	ns
t_{PHL}				6.4	10.2	1	14.4	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$		6.4	10	1	14.1	ns
t_{PZH}	$\overline{OE}$	Q_A–Q_H		5.7	10.6	1	15	ns
t_{PZL}				6.8	10.6	1	15	ns
t_{PHZ}	$\overline{OE}$	Q_A–Q_H		3.5	10.3	1	14	ns
t_{PLZ}				3.4	10.3	1	14	ns

6.12 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C(1)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.13 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF f = 10 MHz	3.3 V	111	pF
			5 V	114	

6.14 Typical Characteristics

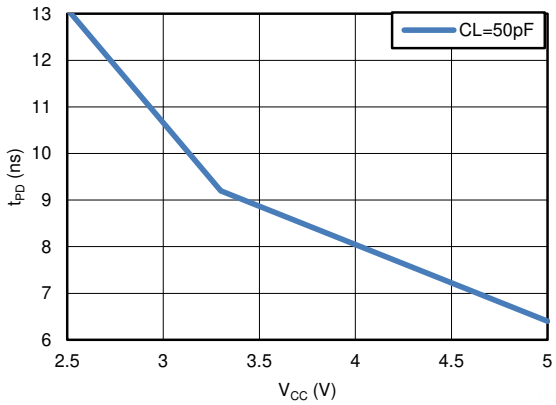
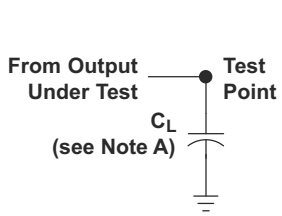
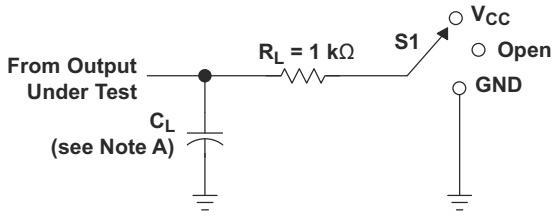


Figure 6-2. TPD vs V_{CC}

7 Parameter Measurement Information

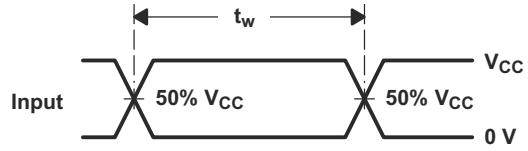


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

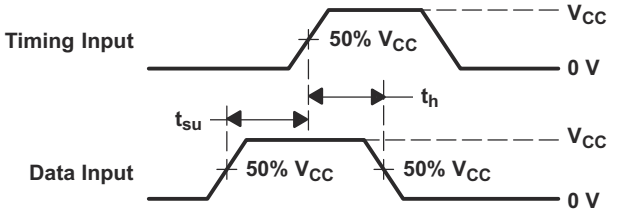


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

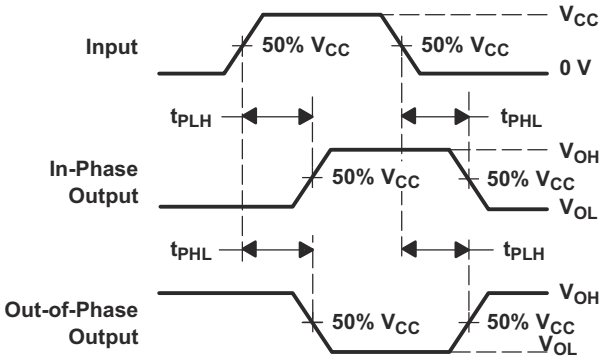
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



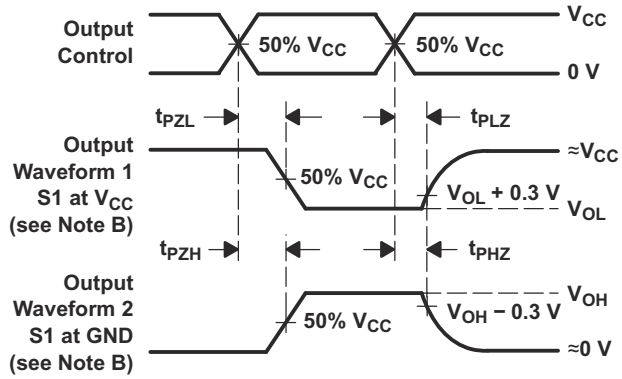
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, and t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

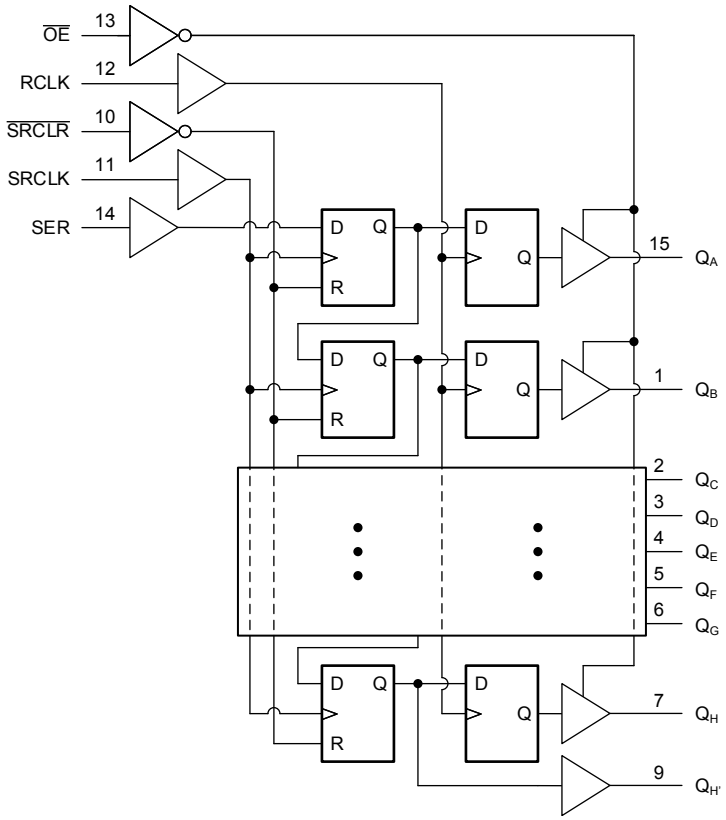
The SN74LV595B-EP contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{OE}$) input is high, all outputs except $Q_{H'}$ are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

For the high-impedance state during power up or power down, tie $\overline{OE}$ to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

8.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

8.3.3 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

8.3.4 Clamp Diode Structure

Figure 8-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

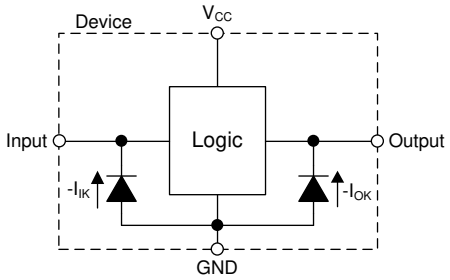


Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

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8.4 Device Functional Modes

Table 8-1 list the functional modes of the SN74LV595B-EP.

Table 8-1. Function Table

INPUTS(1)					FUNCTION
SER	SRCLK	$\overline{SRCLR}$	RCLK	$\overline{OE}$	
X	X	X	X	H	Outputs Q_A–Q_H are disabled. $Q_{H'}$ remains enabled.
X	X	X	X	L	Outputs Q_A–Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the storage register.

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, ↑ = Low to High transition, Z = High Impedance

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV595B-EP can be used to drive seven-segment displays from a singular serialized input. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74LV595B-EP does not need a communication interface for control. It can be easily operated with simple GPIO pins.

The $\overline{OE}$ pin is used to easily disable the outputs when the displays need to be turned off or connected to a PWM signal to control brightness. However, this pin can be tied low and the outputs of the SN74LV595B-EP can be controlled accordingly to turn off all the outputs reducing the I/O needed to three. There is no practical limitation to how many SN74LV595B-EP devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register.

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9.2 Typical Application

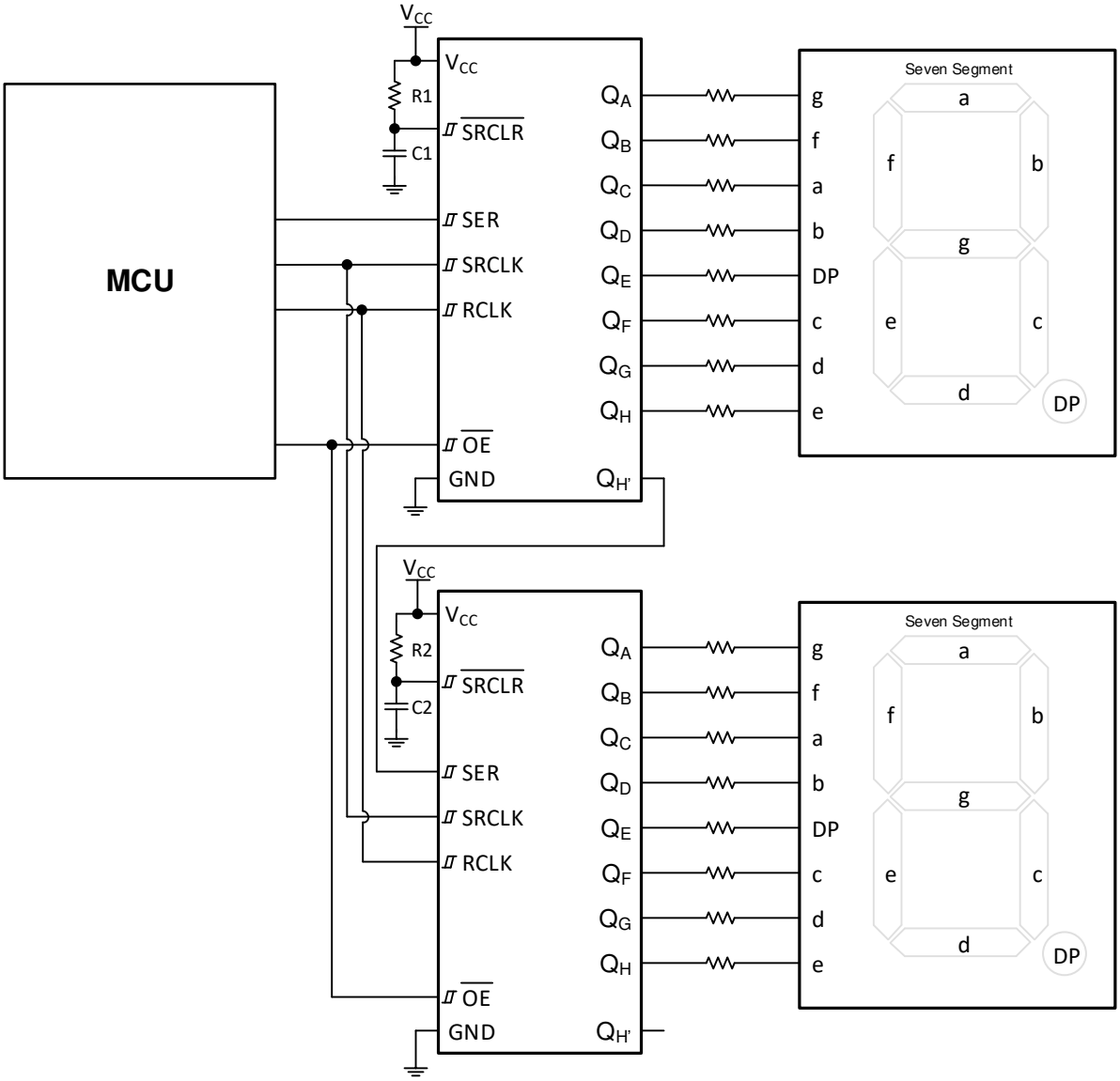


Figure 9-1. Input Expansion with Shift Registers

9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV595B-EP plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV595B-EP plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV595B-EP can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV595B-EP can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV595B-EP (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74LV595B-EP has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

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9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

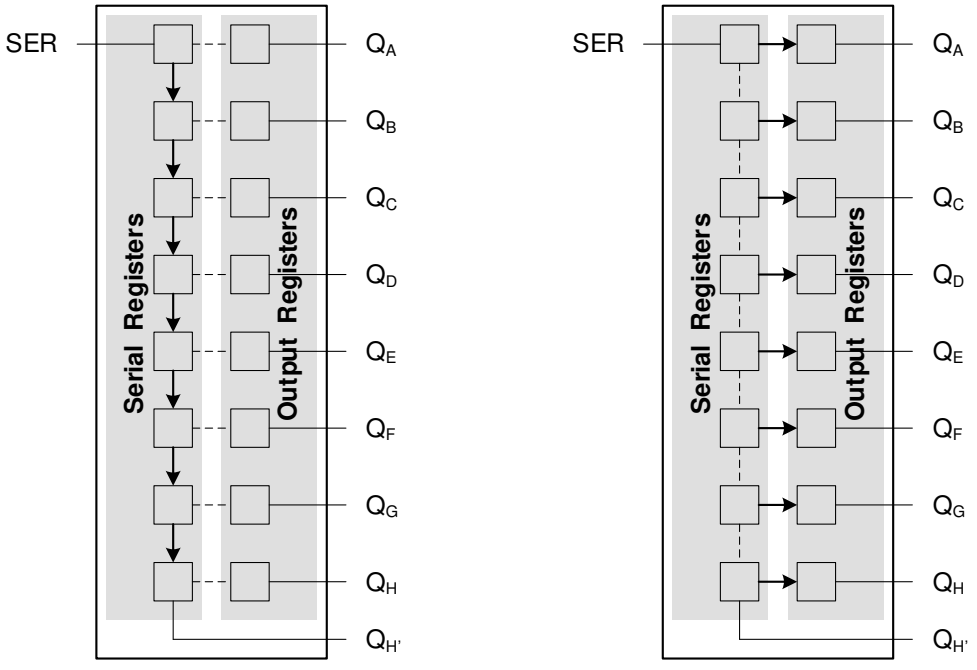
Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV595B-EP to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. which will not violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

9.2.5 Application Curves



SRCLK rising edge shifts data in the serial registers only

RCLK rising edge shifts data to the output registers

Figure 9-2. Application Curve

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9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor; if there are multiple V_{CC} terminals, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

9.4.2 Layout Example

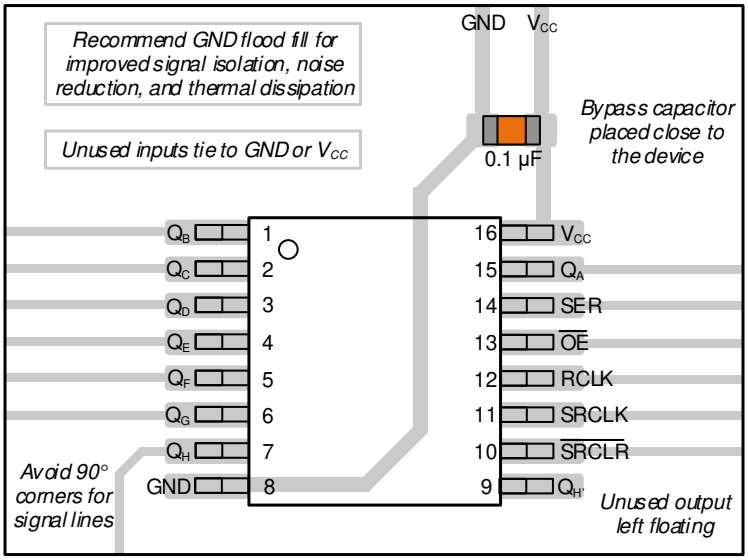


Figure 9-3. Layout Example for the SN74LV595B-EP in the PW Package

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation*
- Texas Instruments, *Introduction to Logic*
- Texas Instruments, *Power-Up Behavior of Clocked Devices*
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV595BMPWREP	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV595EP
SN74LV595BMPWREP.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV595EP
V62/23622-01XE	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See SN74LV595BMPWREP	LV595EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

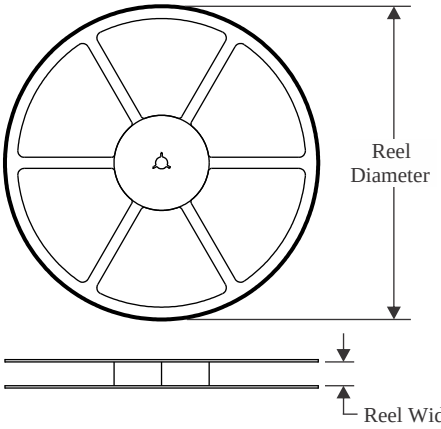
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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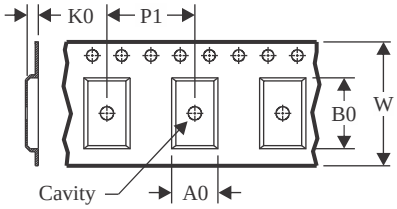
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

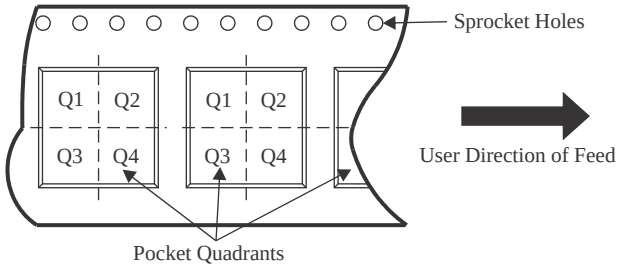


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

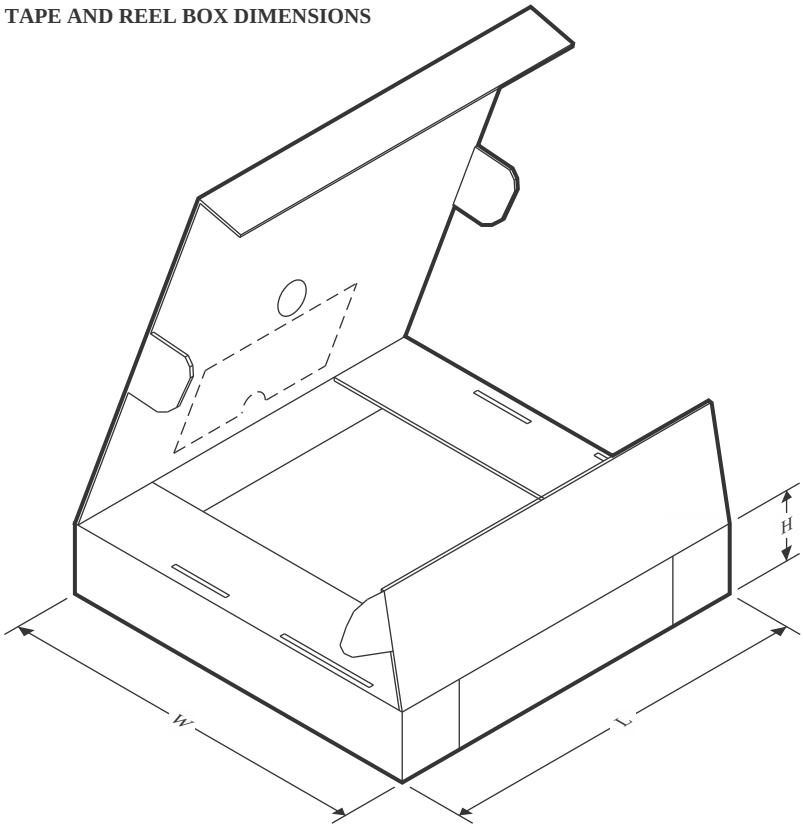
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV595BMPWREP	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

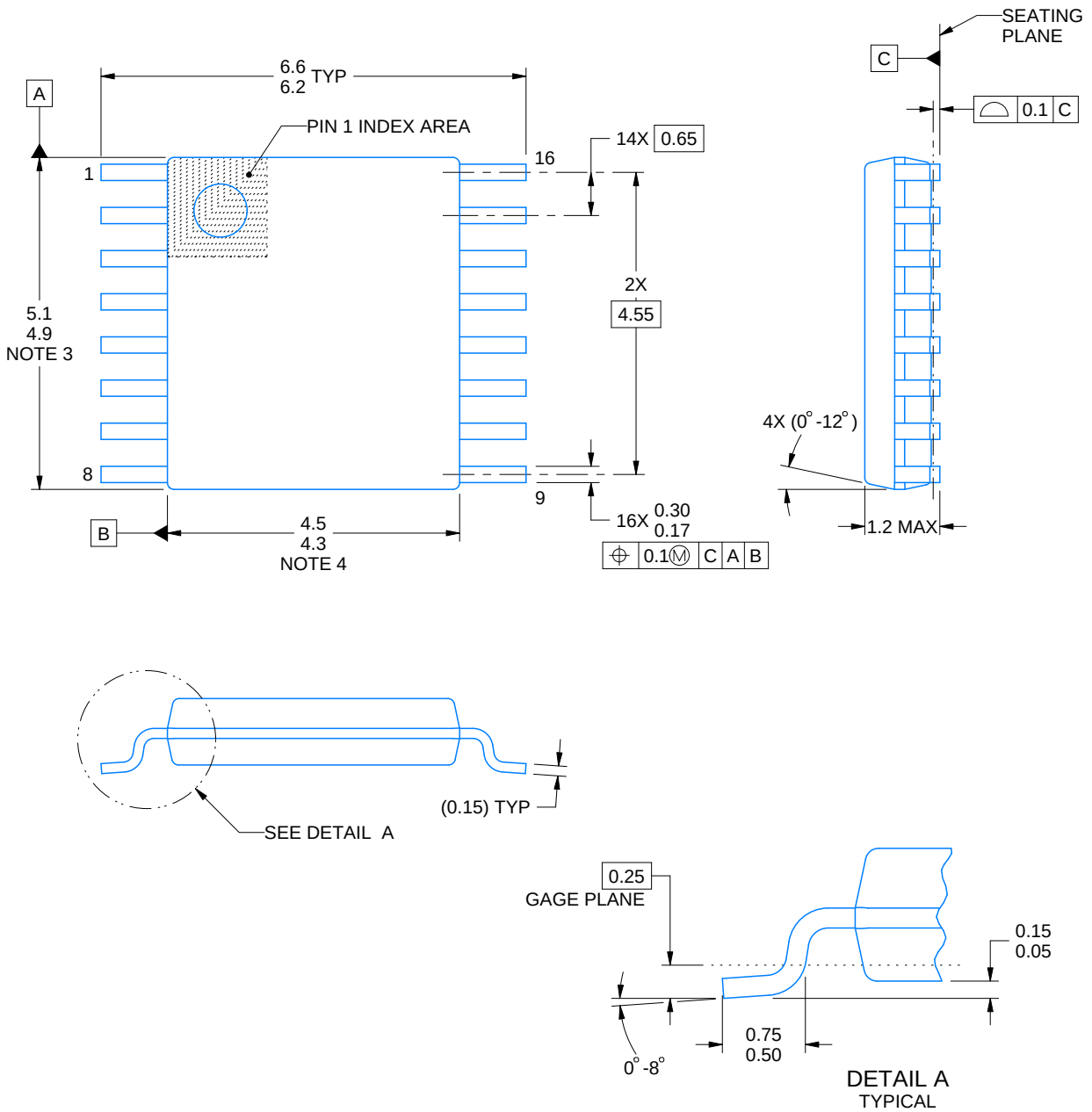
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV595BMPWREP	TSSOP	PW	16	3000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

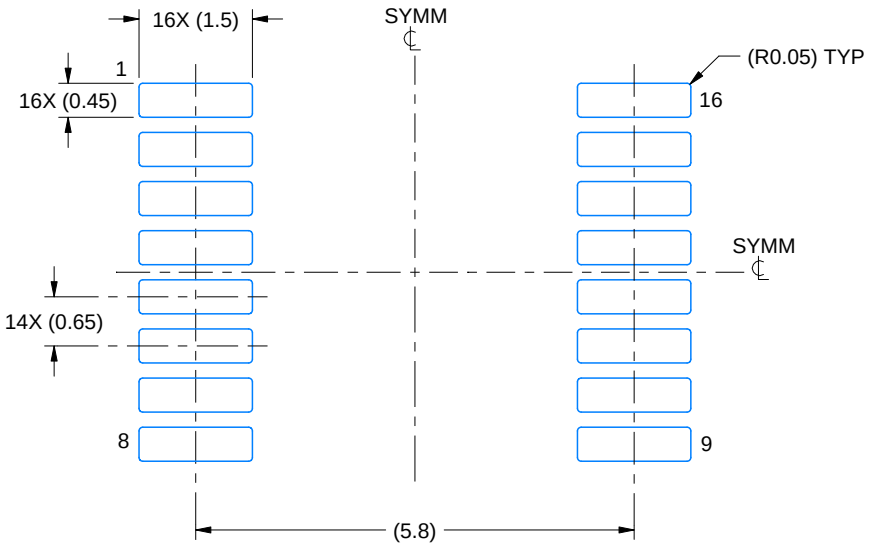
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

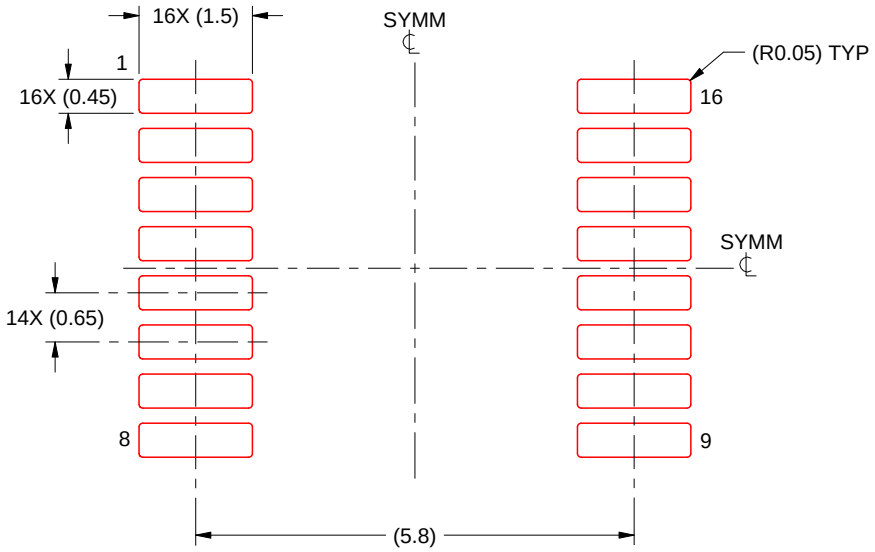


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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