

SN74LV166A 8-Bit Parallel-Load Shift Registers

1 Features

- Operation of 2 V to 5.5 V V_{CC}
- Max t_{pd} of 10.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} supports partial-power-down-mode operation
- Synchronous load
- Direct overriding clear
- Parallel-to-serial conversion
- Latch-up performance exceeds 100 mA per JESD 78, Class II

2 Application

- [Input expansion](#)
- 8-bit data storage

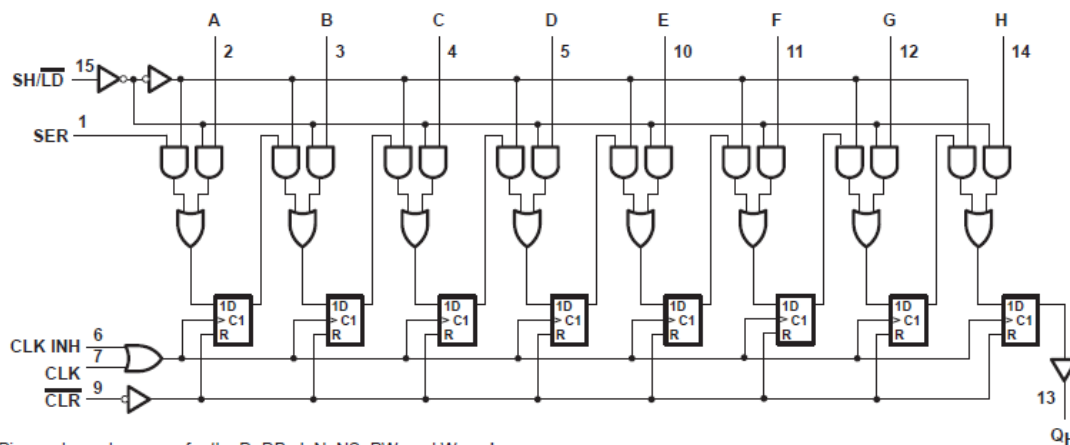
3 Description

The 'LV166A devices are 8-bit parallel-load shift registers, designed for 2 V to 5.5 V V_{CC} operation.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN74LV166A	D (SOIC, 16)	9.90 mm × 3.90 mm
	DB (SSOP, 16)	6.20 mm × 5.30 mm
	NS (SOP, 16)	10.3 mm × 5.30 mm
	PW (TSSOP, 16)	5.00 mm × 4.40 mm
	DGV (TVSOP, 16)	3.6 mm × 4.4 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

Functional Block Diagram



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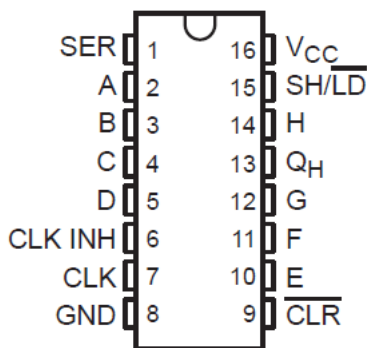
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2005) to Revision D (March 2023)	Page
<ul style="list-style-type: none"> Added <i>Applications</i>, <i>Package Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... 	1

5 Pin Configuration and Functions



**D, DB, DGV, NS, or PW Package
16-Pin SOP, SOIC, SSOP, TSSOP, TVSOP
(Top View)**

Table 5-1. Pin Functions

PIN			
NAME	NO.	I/O	DESCRIPTION
SER	1	I	Serial Output
A	2	I	Parallel Input
B	3	I	Parallel Input
C	4	I	Parallel Input
D	5	I	Parallel Input
CLK	7	I	Clock input
GND	8	—	Ground
CLR	9	I	Clear input, active low
E	10	I	Parallel Input
F	11	I	Parallel Input
G	12	I	Parallel Input
Q _H	13	O	Q _H output
H	14	I	Parallel input H
SH/ LD	15	I	Shift/ load input, enable shifting when input is high, load data when input is low
V _{CC}	16	—	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	7	V
V _I	Input voltage range ⁽¹⁾	–0.5	7	
V _O	Output voltage range applied in high or low state, ⁽¹⁾ ⁽¹⁾	–0.5 V	V _{CC} + 0.5 V	
V _O	Voltage range applied to any output in the power-off state ⁽¹⁾	–0.5	7	
I _{IK}	Input clamp current ⁽¹⁾	V _I < 0	–20	mA
I _{OK}	Output clamp current ⁽¹⁾	V _O < 0	–50	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Section 6.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-Body Model (A114-A) ⁽¹⁾	±2000
		Charged-Device Model (C101)	±1000
		Machine Model (A115-A)	±200

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			SN74LV166A		UNIT
			MIN	MAX	
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		– 50	μA
		V _{CC} = 2.3 V to 2.7 V		– 2	mA
		V _{CC} = 3 V to 3.6 V		– 6	
		V _{CC} = 4.5 V to 5.5 V		– 12	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	μA
		V _{CC} = 2.3 V to 2.7 V		2	mA
		V _{CC} = 3 V to 3.6 V		6	
		V _{CC} = 4.5 V to 5.5 V		12	

6.3 Recommended Operating Conditions (continued)

			SN74LV166A		UNIT
			MIN	MAX	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		200	ns/V
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		100	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		20	
T_A	Operating free-air temperature		-40	85	°C

6.4 Thermal Information

THERMAL METRIC		D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SO)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	73	82	120	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN74LV166A			UNIT
			MIN	TYP	MAX	
V_{OH}	$I_{OH} = -50 \mu A$	2 V to 5.5 V	$V_{CC}-0.1$			V
	$I_{OH} = -2 \text{ mA}$	2.3 V	2			
	$I_{OH} = -50 \mu A$	3 V	2.48			
	$I_{OH} = -6 \text{ mA}$	4.5 V	3.8			
V_{OL}	$I_{OH} = -12 \text{ mA}$	2 V to 5.5 V			0.1	V
		2.3 V			0.4	
		3 V			0.44	
	$I_{OL} = 4 \text{ mA}$	4.5 V			0.55	
I_I	$V_I = V_{CC}$ or 0	0 to 5.5 V			± 1	μA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V			20	μA
I_{off}		0			5	μA
C_i		3.3 V		1.6		pF

6.6 Timing Requirements, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

			$T_A = 25^\circ C$		SN74LV166A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLR low	8		9		ns
		CLK high or low	8.5		9		
t_{su}	Setup time	CLK INH before CLK $\uparrow$	7		7		ns
		Data before CLK $\uparrow$	6.5		8.5		
		SH/LD before CLK $\uparrow$	7		8.5		
		SER before CLK $\uparrow$	8.5		9.5		
		CLR $\uparrow$ inactive before CLK $\uparrow$	6		7		
t_h	Hold time	Data after CLK $\uparrow$	- 0.5		0		ns

6.7 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

			$T_A = 25^\circ\text{C}$		SN74LV166A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	6		7		ns
		CLK high or low	6		7		
t_{su}	Setup time	CLK INH before CLK $\uparrow$	5		5		ns
		Data before CLK $\uparrow$	5		6		
		SH/ $\overline{\text{LD}}$ before CLK $\uparrow$	5		6		
		SER before CLK $\uparrow$	5		6		
		$\overline{\text{CLR}}\uparrow$ inactive before CLK $\uparrow$	4		4		
t_h	Hold time	Data after CLK $\uparrow$	0		0		ns

6.8 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

			$T_A = 25^\circ\text{C}$		SN74LV166A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	5		5		ns
		CLK high or low	4		4		
t_{su}	Setup time	CLK INH before CLK $\uparrow$	3.5		3.5		ns
		Data before CLK $\uparrow$	4.5		4.5		
		SH/ $\overline{\text{LD}}$ before CLK $\uparrow$	4		4		
		SER before CLK $\uparrow$	4		4		
		$\overline{\text{CLR}}\uparrow$ inactive before CLK $\uparrow$	3.5		3.5		
t_h	Hold time	Data after CLK $\uparrow$	1		1		ns

6.9 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN74LV166A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	50 ¹	105 ¹		45		MHz
			$C_L = 50\text{ pF}$	40	80		35		
t_{PHL}	$\overline{\text{CLR}}$	Q_H	$C_L = 15\text{ pF}$		8.8 ¹	16 ¹	1	18	ns
t_{pd}	CLK				9.2 ¹	19.8 ¹	1	22	
t_{PHL}	$\overline{\text{CLR}}$	Q_H	$C_L = 50\text{ pF}$		11.3	19.5	1	22	ns
t_{pd}	CLK				11.8	23.3	1	26	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.10 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN74LV166A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{\max}$			$C_L = 15\text{ pF}$	65 ¹	150 ¹		55		MHz
			$C_L = 50\text{ pF}$	60	120		50		
t_{PHL}	$\overline{\text{CLR}}$	Q_H	$C_L = 15\text{ pF}$		6.3 ¹	12.5 ¹	1	15	ns
t_{pd}	CLK				6.6 ¹	15.4 ¹	1	18	
t_{PHL}	$\overline{\text{CLR}}$	Q_H	$C_L = 50\text{ pF}$		7.9	16.3	1	18.5	ns
t_{pd}	CLK				8.3	18.9	1	21.5	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.11 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN74LV166A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{\max}$			$C_L = 15\text{ pF}$	110 ¹	205 ¹		90		MHz
			$C_L = 50\text{ pF}$	95	160		85		
t_{PHL}	$\overline{\text{CLR}}$	Q_H	$C_L = 15\text{ pF}$		4.6 ¹	8.6 ¹	1	10	ns
t_{pd}	CLK				4.8 ¹	9.9 ¹	1	11.5	
t_{PHL}	$\overline{\text{CLR}}$	Q_H	$C_L = 50\text{ pF}$		5.7	10.6	1	12	ns
t_{pd}	CLK				6.1	11.9	1	13.5	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

Timing Diagram

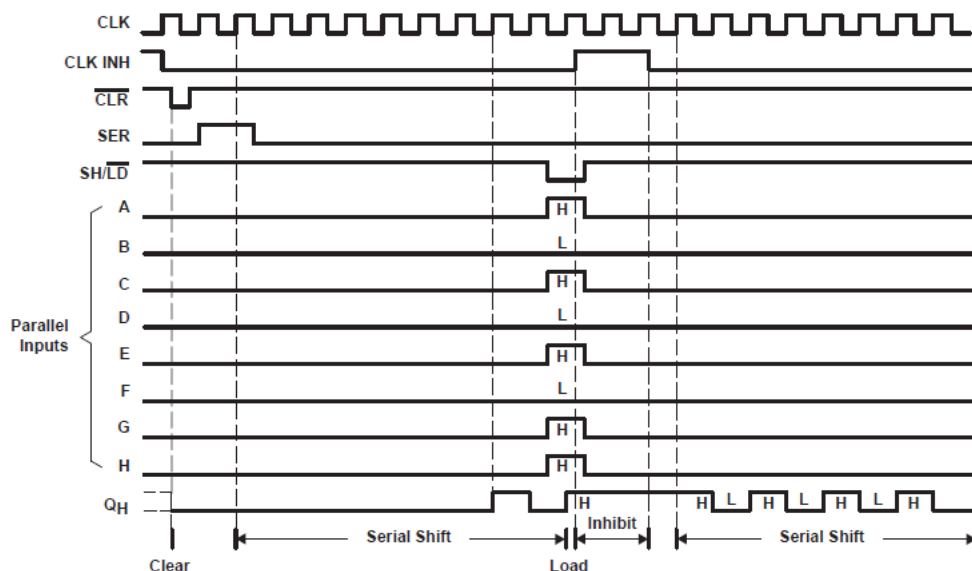


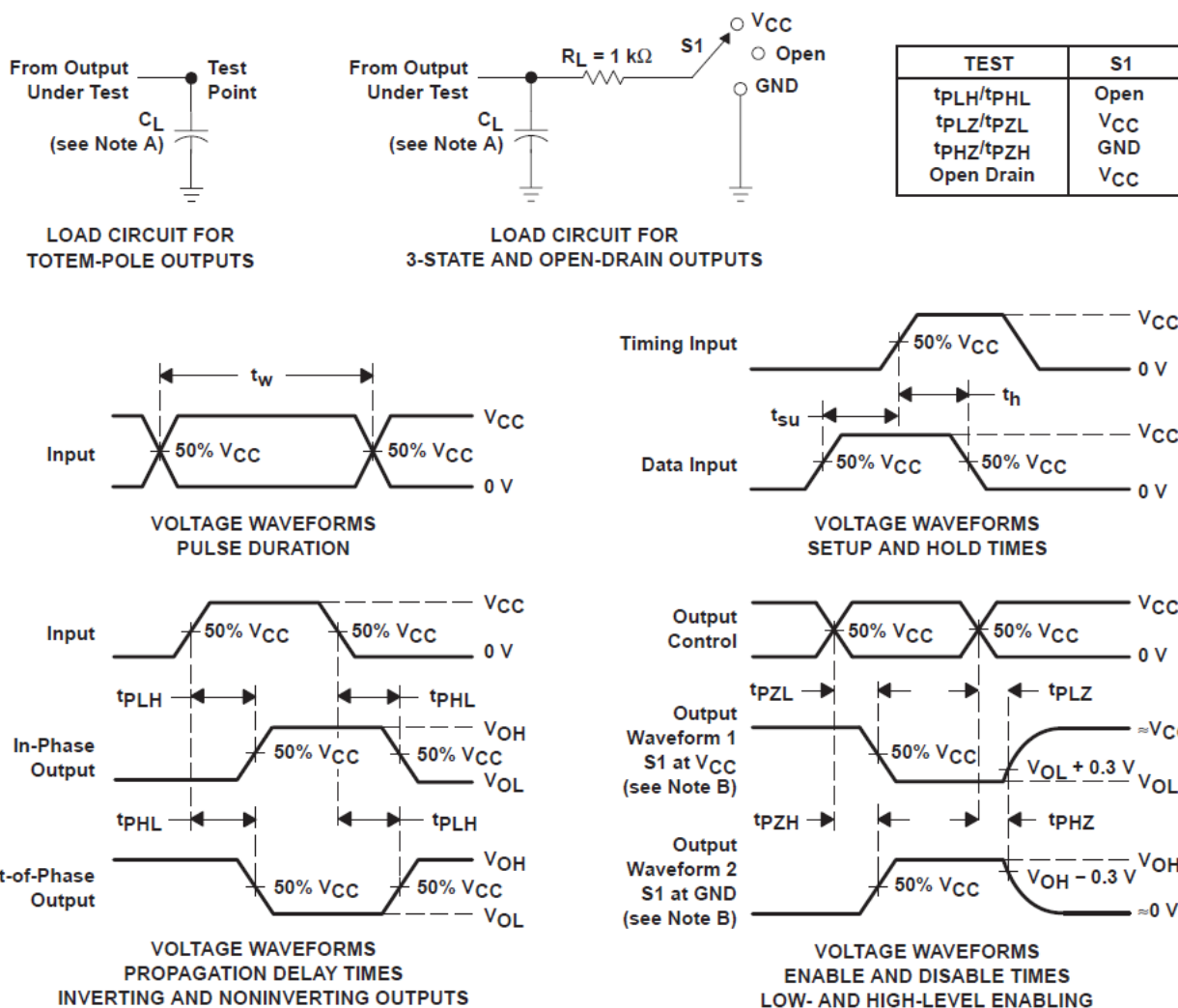
Figure 6-1. Typical Clear, Shift, Load, Inhibit, and Shift Sequence

6.12 Operating Characteristics

 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$	$f = 10\text{ MHz}$	3.3 V	39.1	pF
				5 V	44.5	

7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 6\text{ ns}$, $t_f = 6\text{ ns}$.

C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PHL} and t_{PLH} are the same as t_{pd} .

H. All parameters and waveforms are not applicable to all devices.

8 Detailed Description

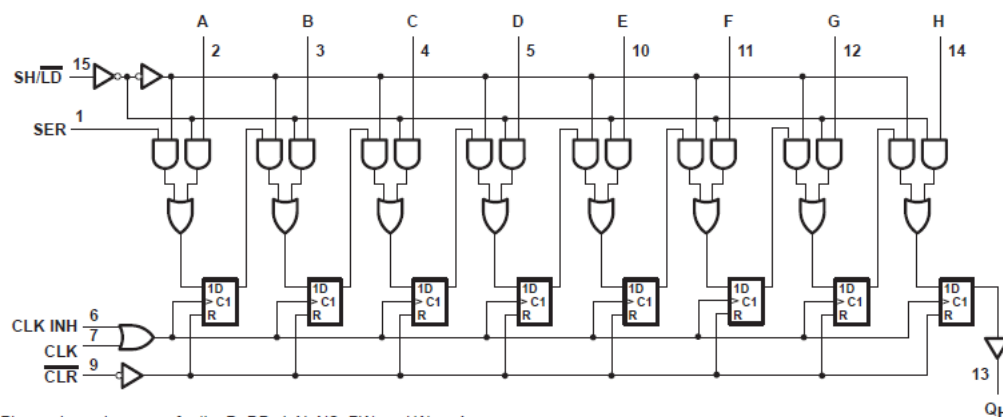
8.1 Overview

These parallel-in or serial-in, serial-out registers feature gated clock (CLK, CLK INH) inputs and an overriding clear ($\overline{\text{CLR}}$) input. The parallel-in or serial-in modes are established by the shift/load ($\text{SH}/\overline{\text{LD}}$) input. When high, $\text{SH}/\overline{\text{LD}}$ enables the serial (SER) data input and couples the eight flip-flops for serial shifting with each clock (CLK) pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited.

Clocking is accomplished on the low-to-high-level edge of CLK through a 2-input positive-NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either CLK or CLK INH high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. CLK INH should be changed to the high level only when CLK is high. $\overline{\text{CLR}}$ overrides all other inputs, including CLK, and resets all flip-flops to zero.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram



8.3 Device Functional Modes

Table 8-1. Function Table

INPUTS						OUTPUTS		
$\overline{\text{CLR}}$	$\text{SH}/\overline{\text{LD}}$	CLK INH	CLK	SER	PARALLEL A...H	INTERNAL		Q_H
						Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	$\uparrow$	X	a...h	a	b	h
H	H	L	$\uparrow$	H	X	H	Q_{An}	Q_{Gn}
H	H	L	$\uparrow$	L	X	L	Q_{An}	Q_{Gn}
H	X	H	$\uparrow$	X	X	Q_{A0}	Q_{B0}	Q_{H0}

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Section 6.1](#) table. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. For this device, a 0.1- μ F capacitor is recommended. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminals as possible for best results.

9.2 Layout

9.2.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 channels are used. Such input pins should not be left completely unconnected because the unknown voltages result in undefined operational states.

Specified in [Section 9.2.1.1](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is recommended to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This pin keeps the input section of the I/Os from being disabled and floated.

9.2.1.1 Layout Example

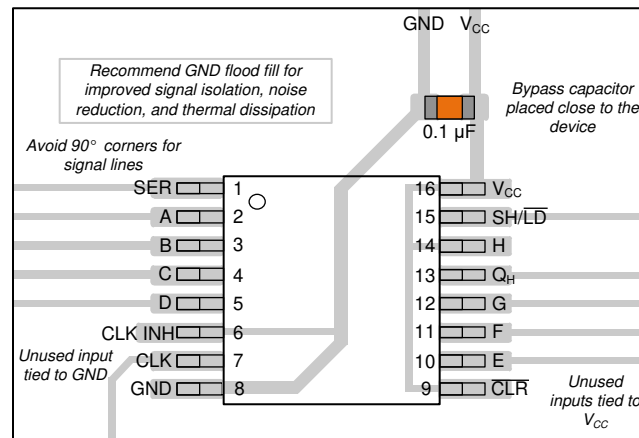


Figure 9-1. Layout Example

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV166A	Click here	Click here	Click here	Click here	Click here

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV166AD	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	LV166A
SN74LV166ADBR	Last Time Buy	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV166A
SN74LV166ADBR.A	Last Time Buy	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV166A
SN74LV166ADGVR	Last Time Buy	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV166A
SN74LV166ADGVR.A	Last Time Buy	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV166A
SN74LV166ADR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV166A
SN74LV166ADR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV166A
SN74LV166ANSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV166A
SN74LV166ANSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV166A
SN74LV166APW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	LV166A
SN74LV166APWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	LV166A
SN74LV166APWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV166A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

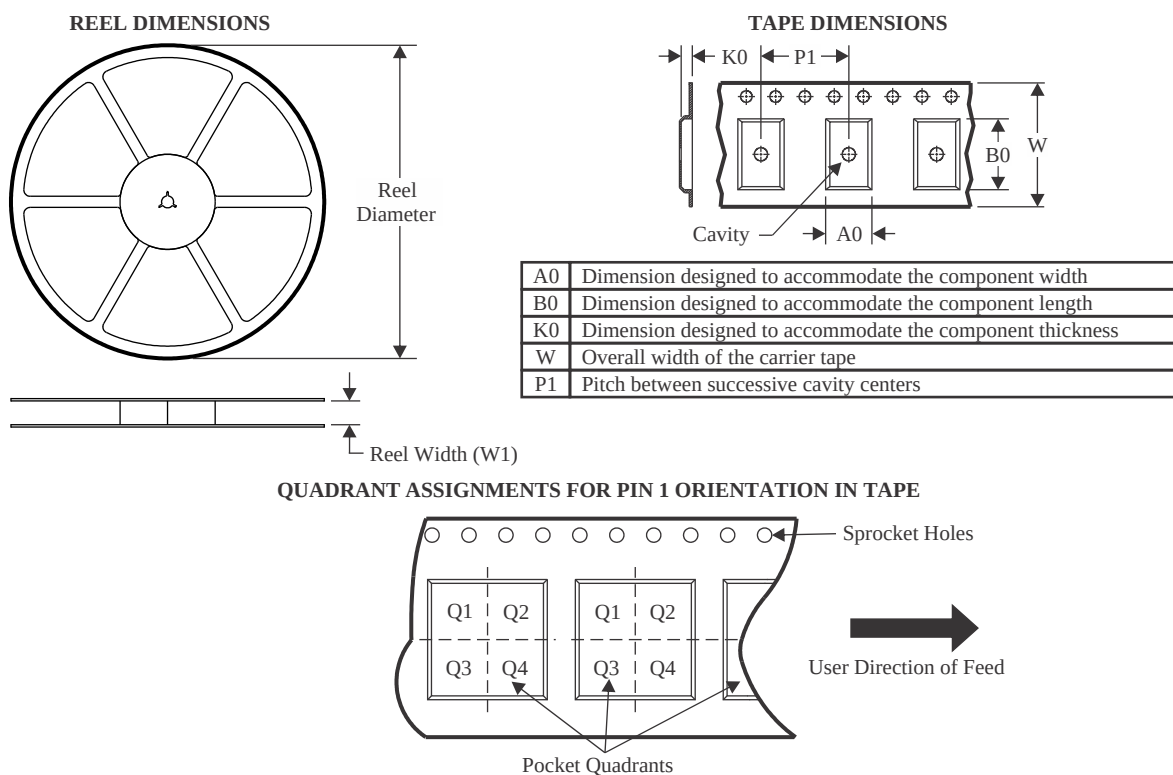
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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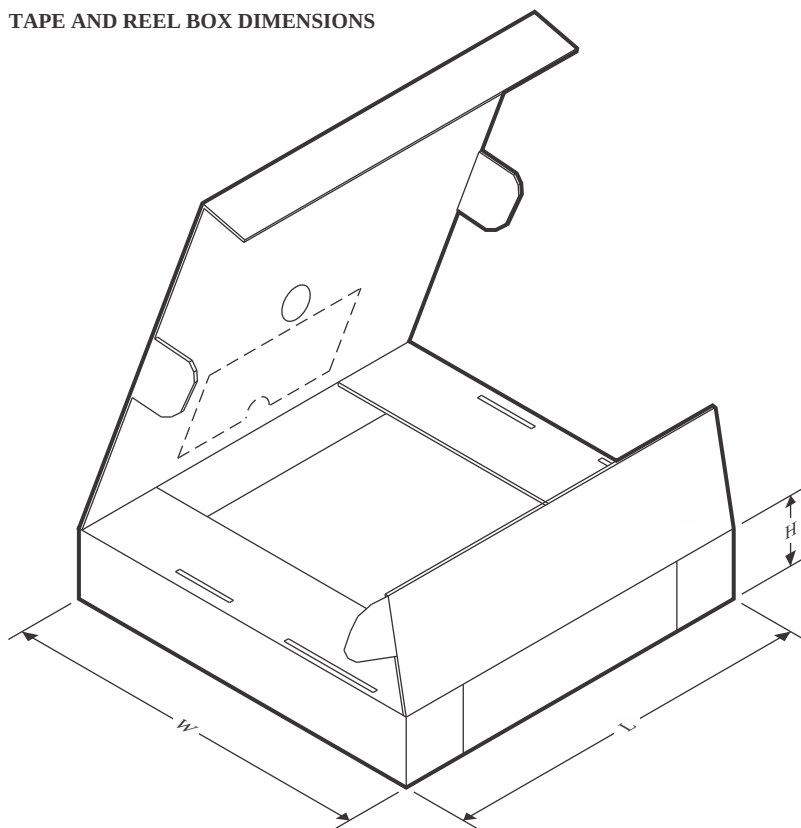
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV166ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV166ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV166ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV166ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV166APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

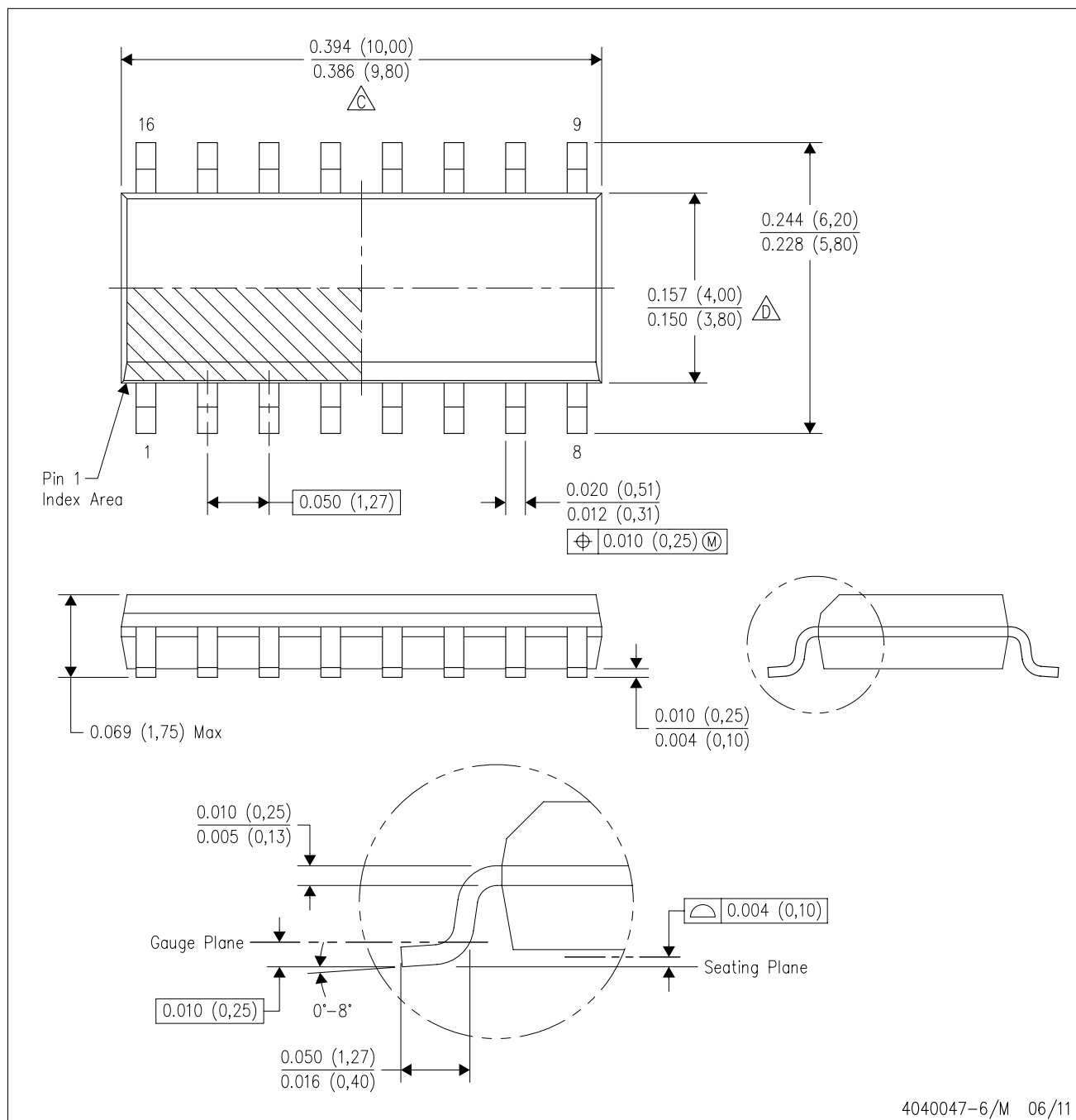


*All dimensions are nominal

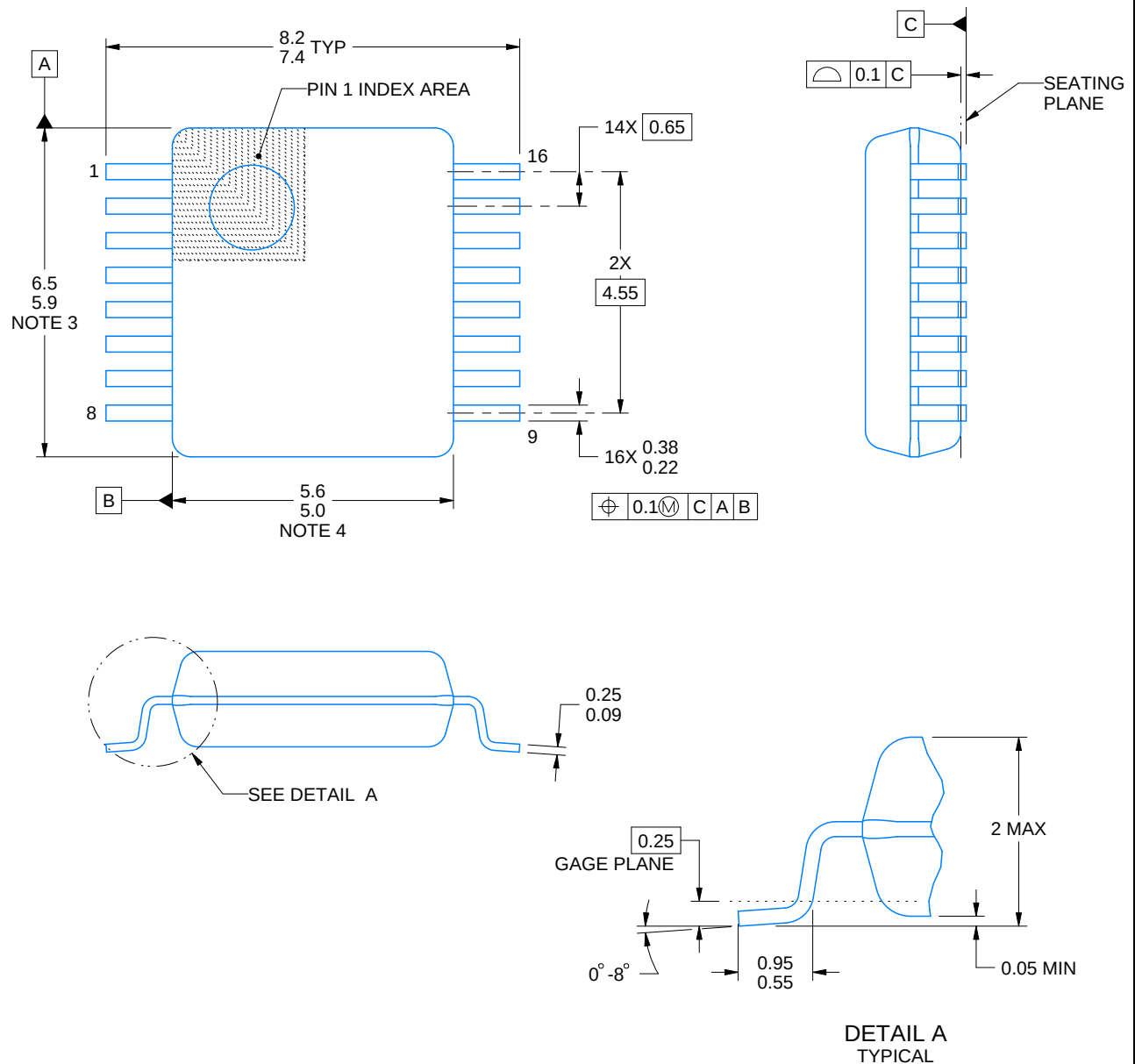
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV166ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74LV166ADGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74LV166ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV166ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LV166APWR	TSSOP	PW	16	2000	353.0	353.0	32.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220763/A 05/2022

NOTES:

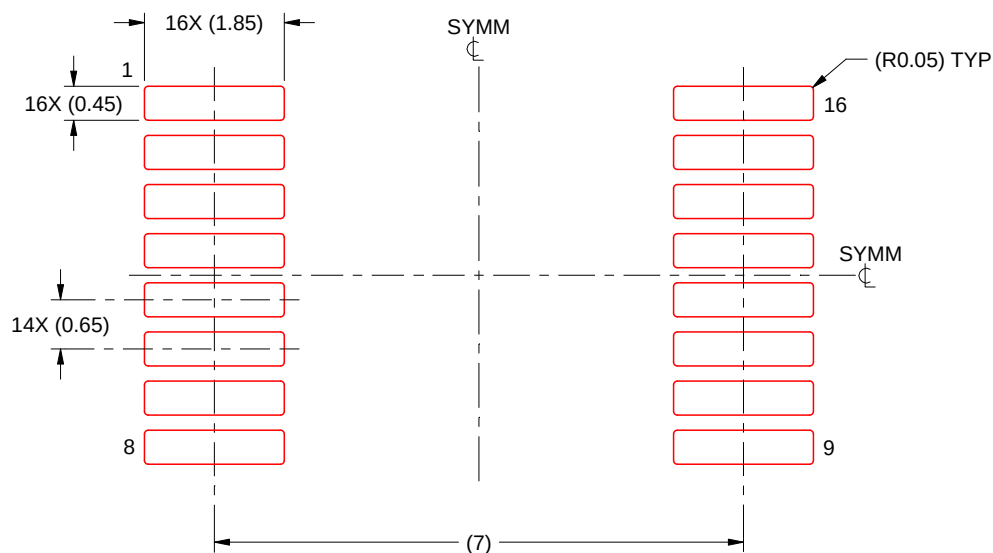
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

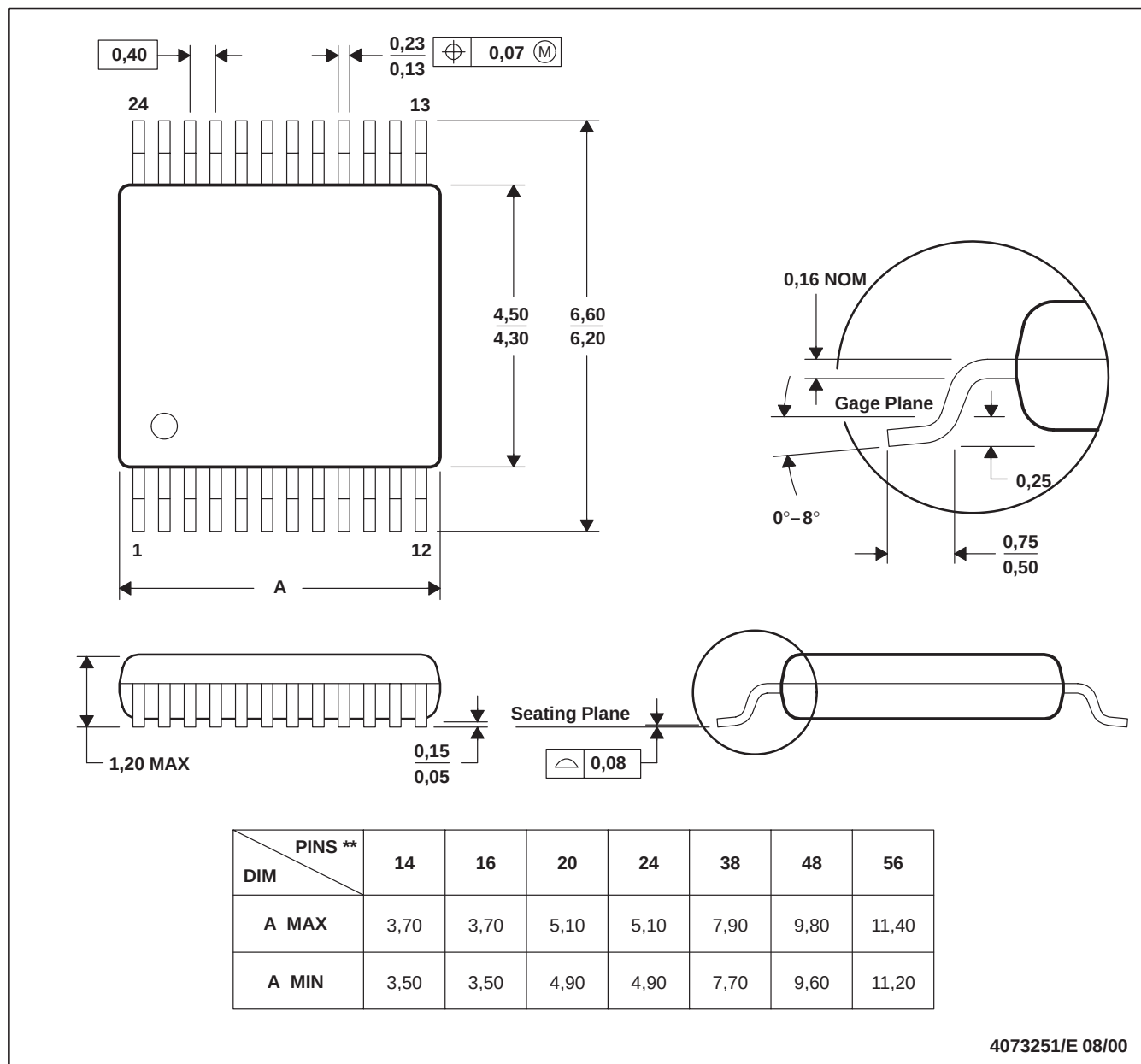
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



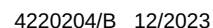
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



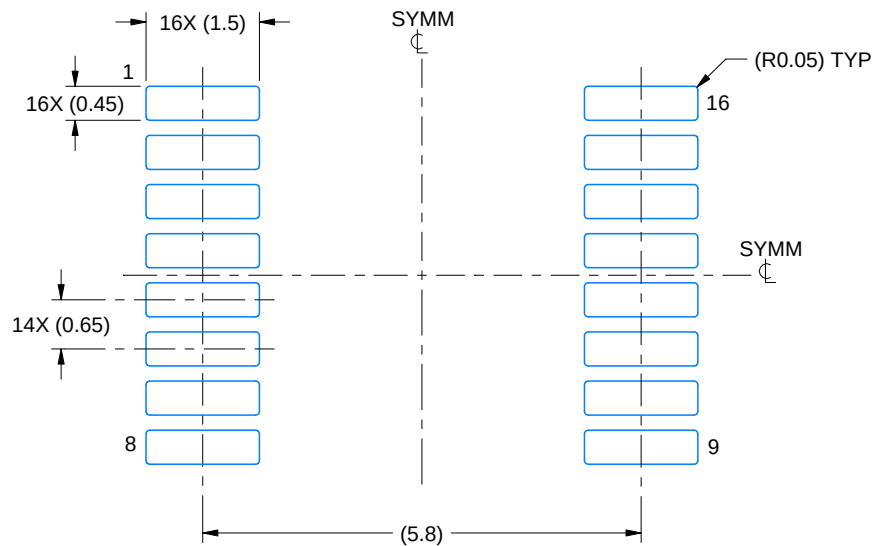
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

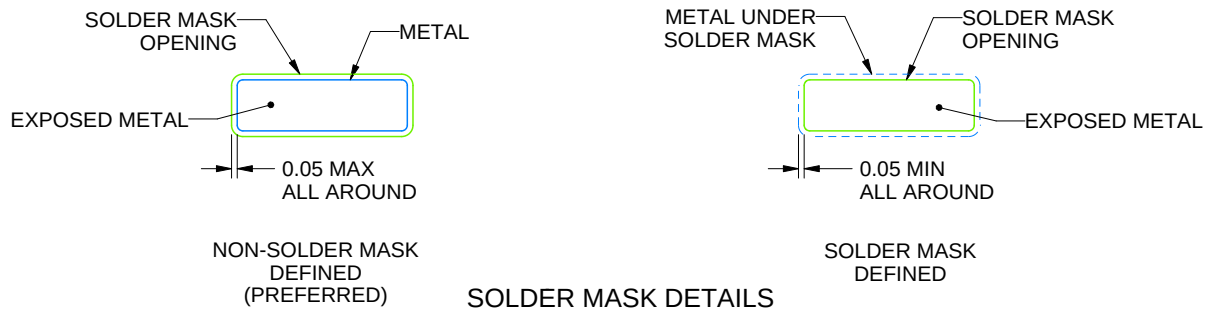
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

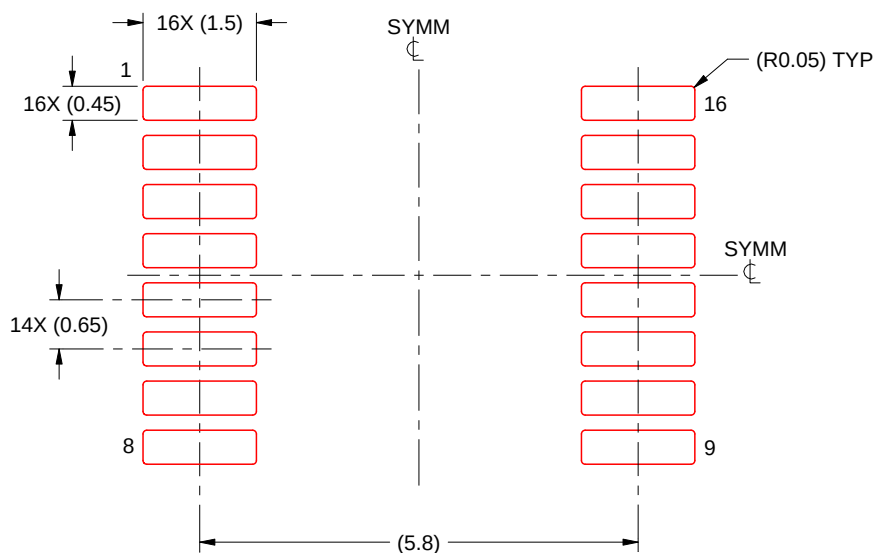
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

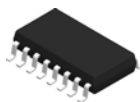


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

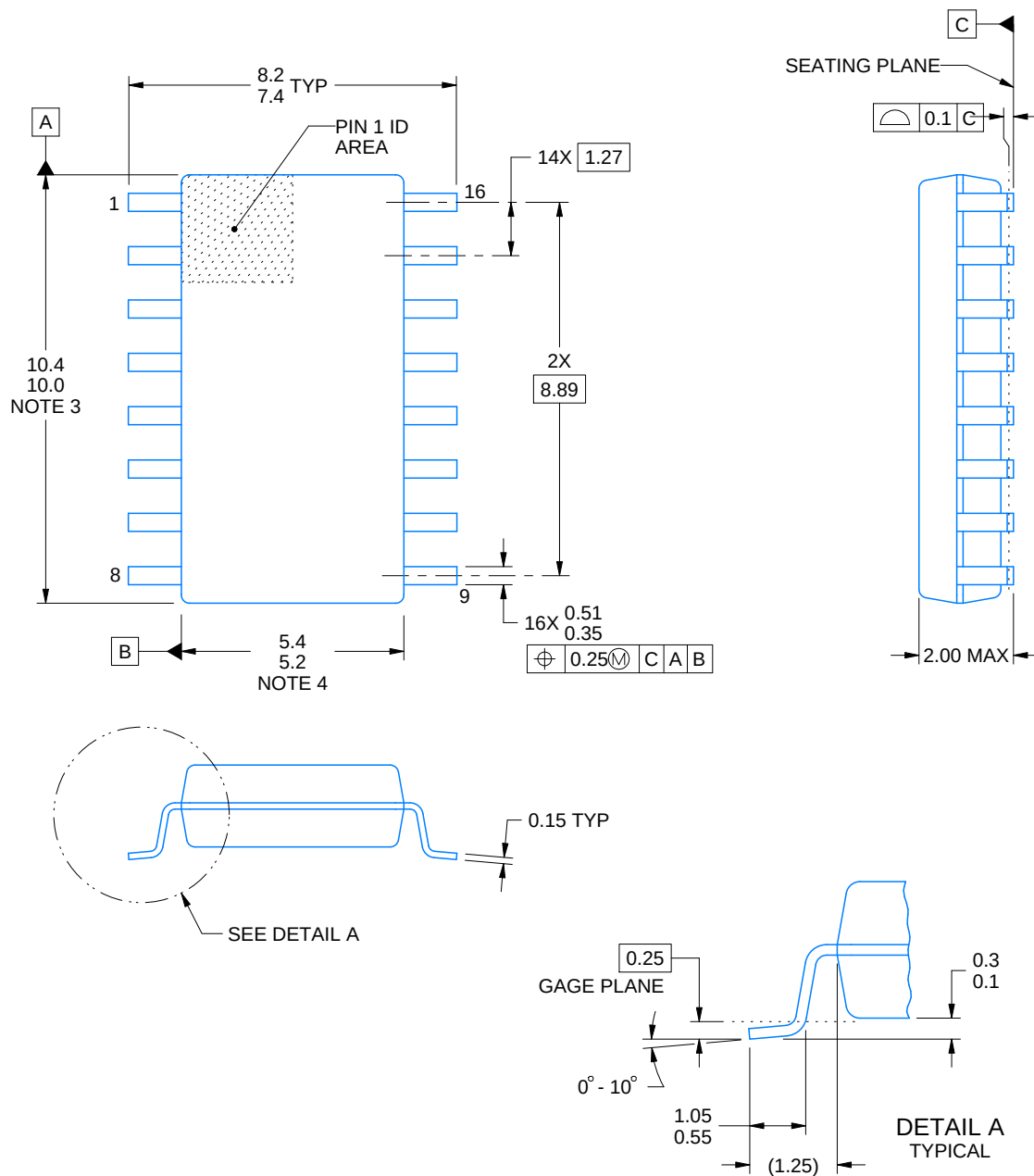


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

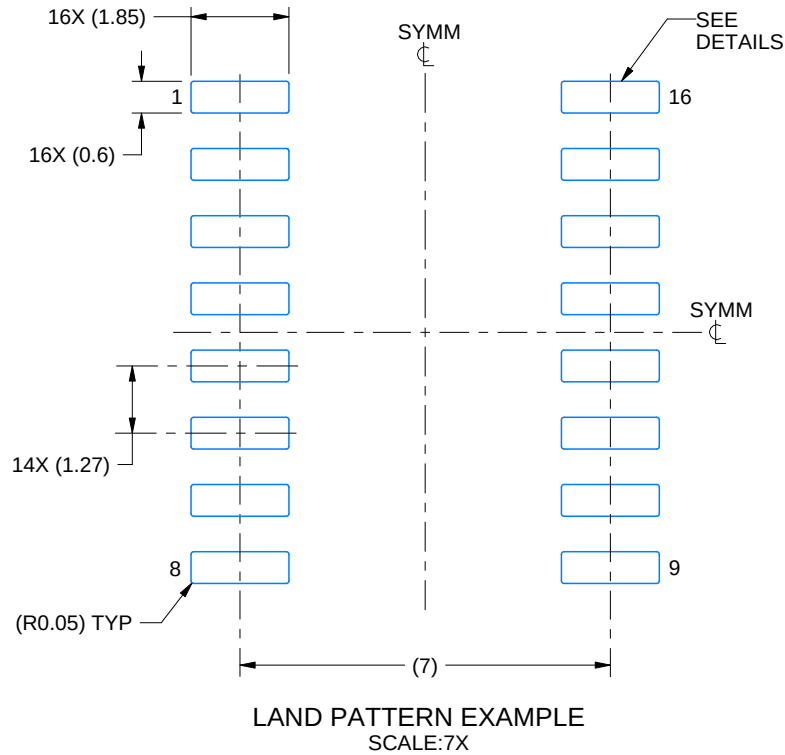
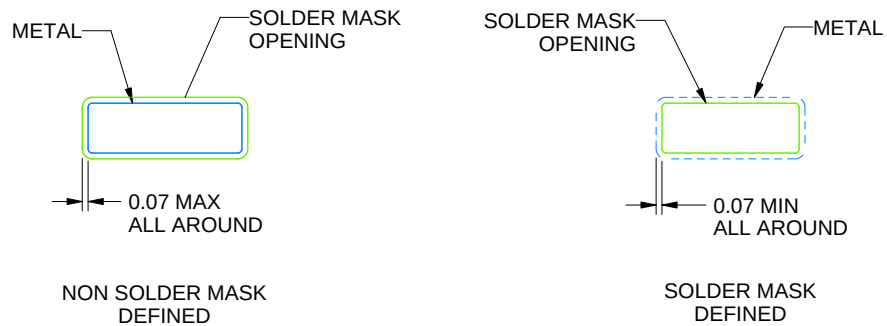
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



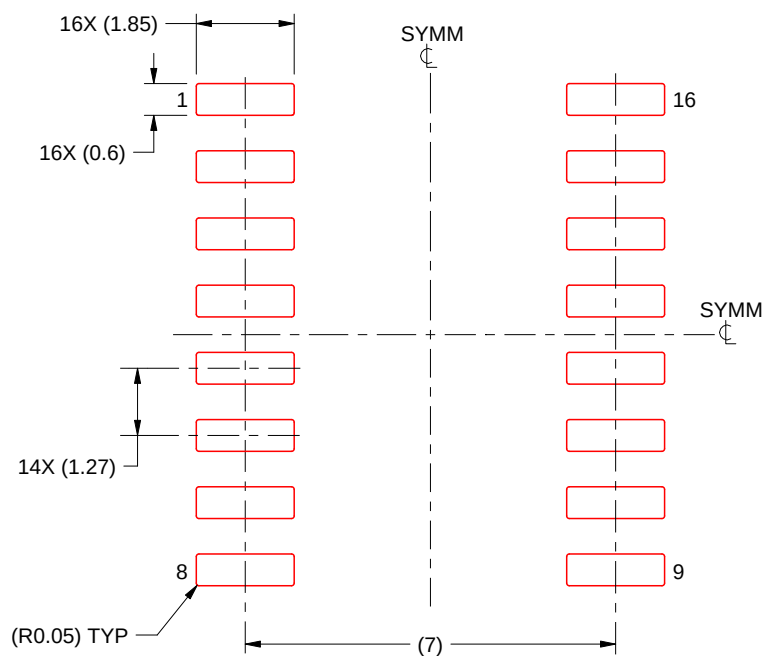
SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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