

# SN74LV125AT Quadruple Bus Buffer Gates With 3-State Outputs

## 1 Features

- Inputs Are TTL-Voltage Compatible
- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Typical  $t_{pd}$  of 3.8 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2.3 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17

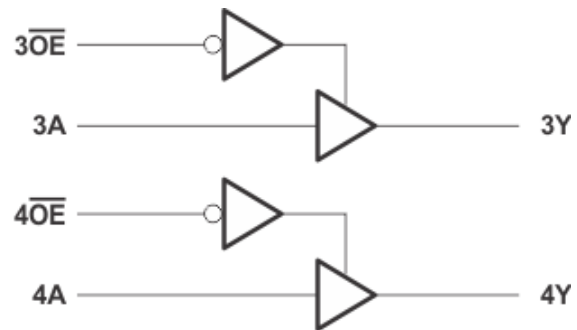
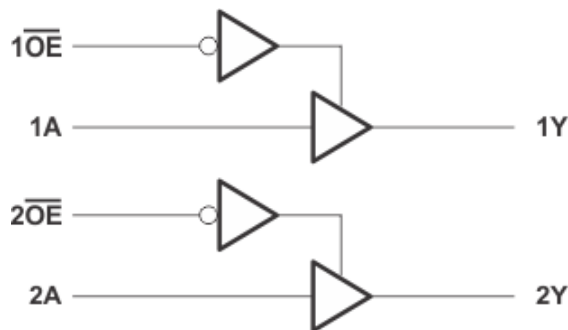
## 2 Description

The SN74LV125AT is a quadruple bus buffer gate. This device features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

### Package Information

| PART NUMBER | PACKAGE <sup>1</sup> | PACKAGE SIZE <sup>2</sup> |
|-------------|----------------------|---------------------------|
| SN74LV125AT | RGY (VQFN, 14)       | 3.50 mm x 3.50 mm         |
|             | D (SOIC, 14)         | 8.65 mm x 6 mm            |
|             | NS (SO, 14)          | 10.20 mm x 7.8 mm         |
|             | DB (SSOP, 14)        | 6.20 mm x 7.8 mm          |
|             | PW (TSSOP, 14)       | 5.00 mm x 6.4 mm          |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length x width) is a nominal value and includes pins, where applicable.



Simplified Schematic



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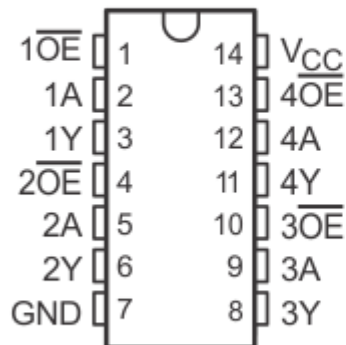
|                                                |          |                                                             |           |
|------------------------------------------------|----------|-------------------------------------------------------------|-----------|
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## 3 Revision History

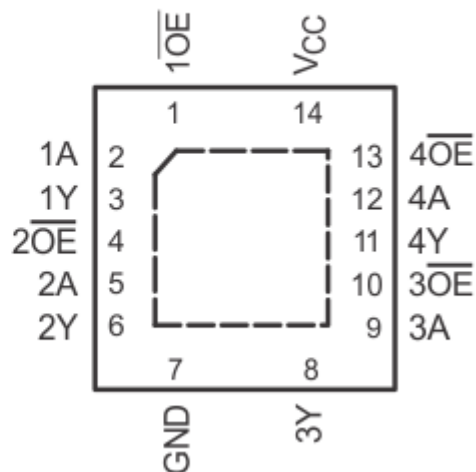
| Changes from Revision A (May 2023) to Revision B (July 2023)                                                                                                                                                                                                                                                                                 | Page |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| <ul style="list-style-type: none"> <li>Added <i>Package Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i>, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul> | 1    |

## 4 Pin Configuration and Functions

SN74LV125A . . . D, DB, DGV, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LV125A . . . RGY PACKAGE  
(TOP VIEW)



| PIN |      | TYPE <sup>(1)</sup> | DESCRIPTION                 |
|-----|------|---------------------|-----------------------------|
| NO. | NAME |                     |                             |
| 1   | 1OE  | I                   | Output Enable 1, Active Low |
| 2   | 1A   | I                   | 1A Input                    |
| 3   | 1Y   | O                   | 1Y Output                   |
| 4   | 2OE  | I                   | Output Enable 2, Active Low |
| 5   | 2A   | I                   | 2A Input                    |
| 6   | 2Y   | O                   | 2Y Output                   |
| 7   | GND  | —                   | Ground Pin                  |
| 8   | 3Y   | O                   | 3Y Output                   |
| 9   | 3A   | I                   | 3A Input                    |
| 10  | 3OE  | I                   | Output Enable 3, Active Low |
| 11  | 4Y   | O                   | 4Y Output                   |
| 12  | 4A   | I                   | 4A Input                    |
| 13  | 4OE  | I                   | Output Enable 4, Active Low |
| 14  | VCC  | —                   | Power Pin                   |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                                                             |                                       | MIN  | MAX                   | UNIT |
|------------------|---------------------------------------------------------------------------------------------|---------------------------------------|------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage                                                                              |                                       | –0.5 | 7                     | V    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                                                          |                                       | –0.5 | 7                     | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> |                                       | –0.5 | 7                     | V    |
| V <sub>O</sub>   | Output voltage range <sup>(2) (3)</sup>                                                     |                                       | –0.5 | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current                                                                         | V <sub>I</sub> < 0                    |      | –20                   | mA   |
| I <sub>OK</sub>  | Output clamp current                                                                        | V <sub>O</sub> < 0                    |      | ±50                   | mA   |
| I <sub>O</sub>   | Continuous output current                                                                   | V <sub>O</sub> = 0 to V <sub>CC</sub> |      | ±35                   | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND                                           |                                       |      | ±70                   | mA   |
| T <sub>stg</sub> | Storage temperature                                                                         |                                       | –65  | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

### 5.2 ESD Ratings

|                    |                         |                                                                                          | MAX   | UNIT |
|--------------------|-------------------------|------------------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    |                                  | SN74LV125AT |                 | UNIT |
|-----------------|------------------------------------|----------------------------------|-------------|-----------------|------|
|                 |                                    |                                  | MIN         | MAX             |      |
| V <sub>CC</sub> | Supply voltage                     |                                  | 4.5         | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 4.5 V to 5.5 V | 2           |                 | V    |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 4.5 V to 5.5 V |             | 0.8             | V    |
| V <sub>I</sub>  | Input voltage                      |                                  | 0           | 5.5             | V    |
| V <sub>O</sub>  | Output voltage                     | High or low state                | 0           | V <sub>CC</sub> | V    |
|                 |                                    | 3-state                          | 0           | 5.5             |      |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 4.5 V to 5.5 V |             | –16             | mA   |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 4.5 V to 5.5 V |             | 16              | mA   |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 4.5 V to 5.5 V |             | 20              | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     |                                  | –40         | 125             | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                        | SN74LV125AT |    |    |     |     | UNIT |
|-------------------------------|----------------------------------------|-------------|----|----|-----|-----|------|
|                               |                                        | D           | DB | NS | PW  | RGY |      |
|                               |                                        | 14 PINS     |    |    |     |     |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 86          | 96 | 76 | 113 | 47  | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                        | TEST CONDITIONS                                             | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |       | –40°C to 85°C |      | –40°C to 125°C |      | UNIT |
|------------------------------------------------------------------|-------------------------------------------------------------|-----------------|-----------------------|-----|-------|---------------|------|----------------|------|------|
|                                                                  |                                                             |                 | MIN                   | TYP | MAX   | MIN           | MAX  | MIN            | MAX  |      |
| V <sub>OH</sub> High-level output voltage                        | I <sub>OH</sub> = –50 µA                                    | 4.5 V           | 4.4                   | 4.5 |       | 4.4           |      | 4.4            |      | V    |
|                                                                  | I <sub>OH</sub> = –16 mA                                    | 4.5 V           | 3.8                   |     |       | 3.8           |      | 3.8            |      |      |
| V <sub>OL</sub> Low-level output voltage                         | I <sub>OL</sub> = 50 µA                                     | 4.5 V           |                       | 0   | 0.1   |               | 0.1  |                | 0.1  | V    |
|                                                                  | I <sub>OL</sub> = 16 mA                                     | 4.5 V           |                       |     | 0.55  |               | 0.55 |                | 0.55 |      |
| I <sub>I</sub> Input leakage current                             | V <sub>I</sub> = 5.5 V or GND                               | 0 to 5.5 V      |                       |     | ±1    |               | ±1   |                | ±1   | µA   |
| I <sub>OZ</sub> Off-State (High-Impedance State) Output Current  | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5 V           |                       |     | ±0.25 |               | ±2.5 |                | ±2.5 | µA   |
| I <sub>CC</sub> Static supply current                            | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           |                       |     | 2     |               | 20   |                | 20   | µA   |
| ΔI <sub>CC</sub> <sup>(1)</sup> Additional static supply current | One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  | 5.5 V           |                       |     | 1.35  |               | 1.5  |                | 1.5  |      |
| I <sub>off</sub> Input/Output Power-Off Leakage Current          | V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V               | 0               |                       |     | 0.5   |               | 5    |                | 5    | µA   |
| C <sub>i</sub> Input capacitance                                 | V <sub>I</sub> = V <sub>CC</sub> or GND                     |                 |                       |     | 2     |               |      |                |      | pF   |

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit And Voltage Waveforms](#))

| PARAMETER          | FROM (INPUT)           | TO (OUTPUT) | LOAD CAPACITANCE       | T <sub>A</sub> = 25°C |     |     | –40°C to 85°C |     | –40°C to 125°C |      | UNIT |
|--------------------|------------------------|-------------|------------------------|-----------------------|-----|-----|---------------|-----|----------------|------|------|
|                    |                        |             |                        | MIN                   | TYP | MAX | MIN           | MAX | MIN            | MAX  |      |
| t <sub>pd</sub>    | A                      | Y           | C <sub>L</sub> = 15 pF | 1.9                   | 3.8 | 5.5 | 1             | 6.5 | 1              | 8.5  | ns   |
| t <sub>en</sub>    | $\overline{\text{OE}}$ | Y           |                        | 2                     | 3.6 | 5.1 | 1             | 6   | 1              | 7.5  |      |
| t <sub>dis</sub>   | $\overline{\text{OE}}$ | Y           |                        | 1.5                   | 3.2 | 6.8 | 1             | 8   | 1              | 10   |      |
| t <sub>pd</sub>    | A                      | Y           | C <sub>L</sub> = 50 pF | 2.9                   | 5.3 | 7.5 | 1             | 8.5 | 1              | 10.5 | ns   |
| t <sub>en</sub>    | $\overline{\text{OE}}$ | Y           |                        | 2.8                   | 5.1 | 7.1 | 1             | 8   | 1              | 9.5  |      |
| t <sub>dis</sub>   | $\overline{\text{OE}}$ | Y           |                        | 2.8                   | 6.1 | 8.8 | 1             | 10  | 1              | 10   |      |
| t <sub>sk(o)</sub> |                        |             |                        |                       |     | 1   |               | 1   |                | 1    |      |

## 5.7 Noise Characteristics

V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C

| PARAMETER <sup>(1)</sup> |                                               | SN74LV125AT |      |      | UNIT |
|--------------------------|-----------------------------------------------|-------------|------|------|------|
|                          |                                               | MIN         | TYP  | MAX  |      |
| V <sub>OL(P)</sub>       | Quiet output, maximum dynamic V <sub>OL</sub> |             | 1.1  | 1.5  | V    |
| V <sub>OL(V)</sub>       | Quiet output, minimum dynamic V <sub>OL</sub> |             | –0.3 | –0.8 | V    |
| V <sub>OH(V)</sub>       | Quiet output, minimum dynamic V <sub>OH</sub> |             | 3    |      | V    |
| V <sub>IH(D)</sub>       | High-level dynamic input voltage              | 2           |      |      | V    |
| V <sub>IL(D)</sub>       | Low-level dynamic input voltage               |             |      | 0.8  | V    |

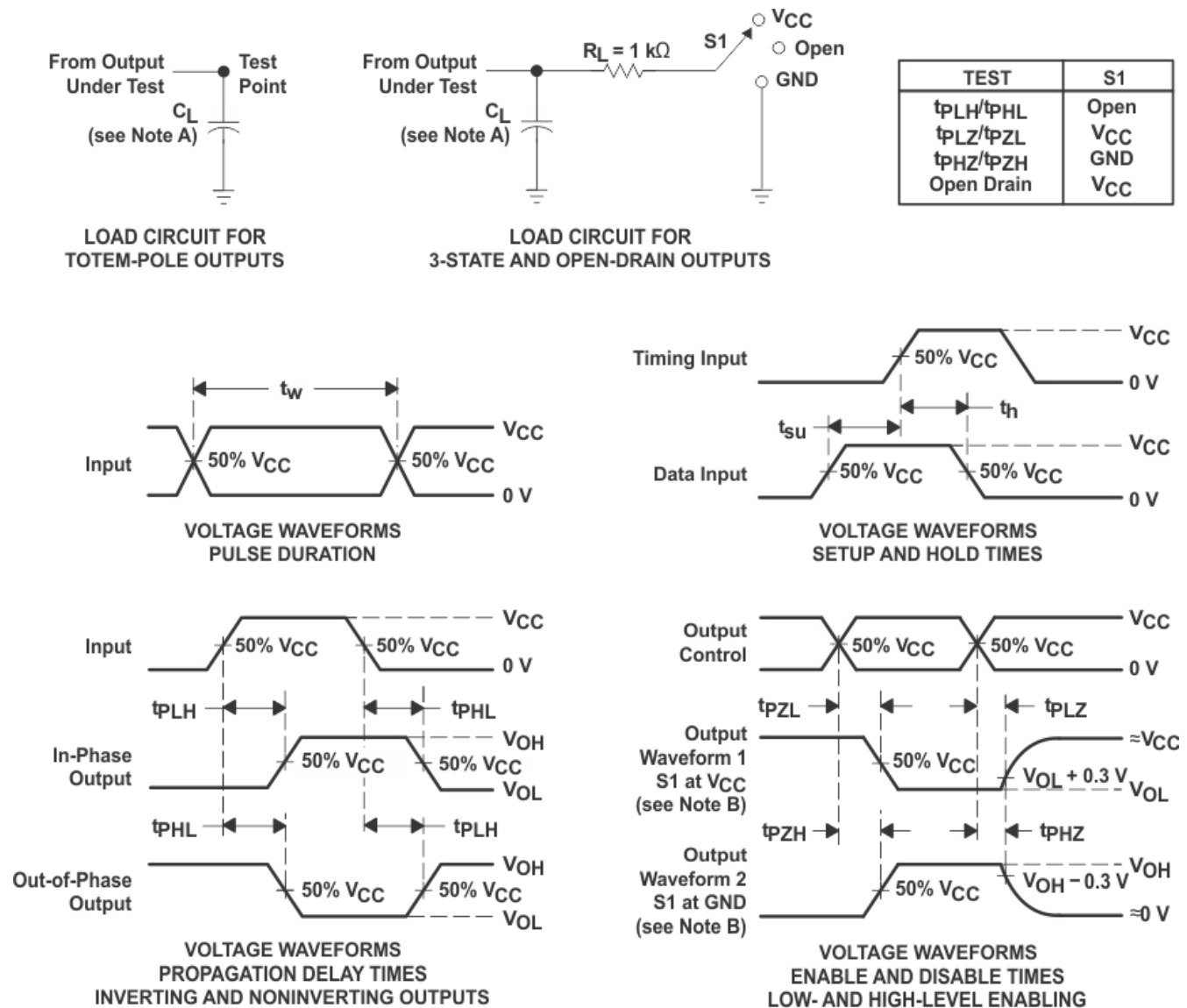
(1) Characteristics are for surface-mount packages only.

## 5.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = -25^\circ\text{C}$

| PARAMETER |                               |                 | TEST CONDITIONS                            | TYP | UNIT |
|-----------|-------------------------------|-----------------|--------------------------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | Outputs enabled | $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$ | 16  | pF   |

## 6 Parameter Measurement Information



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit And Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

The SN74LV125AT is a quadruple bus buffer gate. This device features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 7.2 Functional Block Diagram

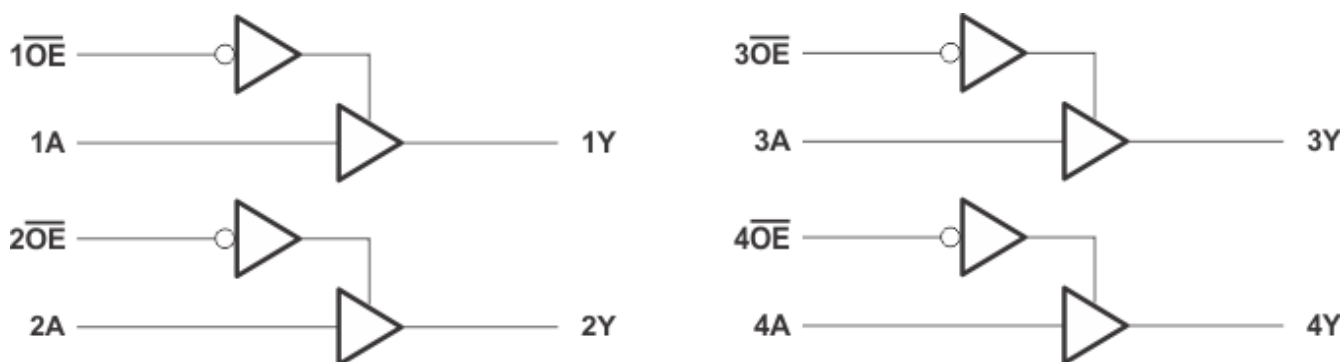


Figure 7-1. Logic Diagram (Positive Logic)

### 7.3 Device Functional Modes

Table 7-1. Function Table  
(Each Buffer)

| INPUTS <sup>(1)</sup> |   | OUTPUT <sup>(2)</sup><br>Y |
|-----------------------|---|----------------------------|
| $\overline{OE}$       | A |                            |
| L                     | H | H                          |
| L                     | L | L                          |
| H                     | X | Z                          |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

| PARTS       | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN74LV125AT | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74LV125ATD</a>    | Obsolete      | Production           | SOIC (D)   14   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | LV125AT             |
| <a href="#">SN74LV125ATDBR</a>  | Active        | Production           | SSOP (DB)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV125AT             |
| SN74LV125ATDBR.A                | Active        | Production           | SSOP (DB)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV125AT             |
| <a href="#">SN74LV125ATDR</a>   | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | LV125AT             |
| SN74LV125ATDR.A                 | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV125AT             |
| <a href="#">SN74LV125ATNSR</a>  | Active        | Production           | SOP (NS)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV125AT             |
| SN74LV125ATNSR.A                | Active        | Production           | SOP (NS)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV125AT             |
| <a href="#">SN74LV125ATPWR</a>  | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV125AT             |
| SN74LV125ATPWR.A                | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LV125AT             |
| <a href="#">SN74LV125ATPWT</a>  | Obsolete      | Production           | TSSOP (PW)   14 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | LV125AT             |
| <a href="#">SN74LV125ATRGYR</a> | Active        | Production           | VQFN (RGY)   14 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | VV125               |
| SN74LV125ATRGYR.A               | Active        | Production           | VQFN (RGY)   14 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | VV125               |
| SN74LV125ATRGYRG4               | Active        | Production           | VQFN (RGY)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VV125               |
| SN74LV125ATRGYRG4.A             | Active        | Production           | VQFN (RGY)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VV125               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV125ATDBR    | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74LV125ATDR     | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LV125ATNSR    | SOP          | NS              | 14   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LV125ATPWR    | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LV125ATRGYR   | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |
| SN74LV125ATRGYRG4 | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV125ATDBR    | SSOP         | DB              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV125ATDR     | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74LV125ATNSR    | SOP          | NS              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV125ATPWR    | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LV125ATRGRYR  | VQFN         | RGY             | 14   | 3000 | 360.0       | 360.0      | 36.0        |
| SN74LV125ATRGRYG4 | VQFN         | RGY             | 14   | 3000 | 360.0       | 360.0      | 36.0        |

## GENERIC PACKAGE VIEW

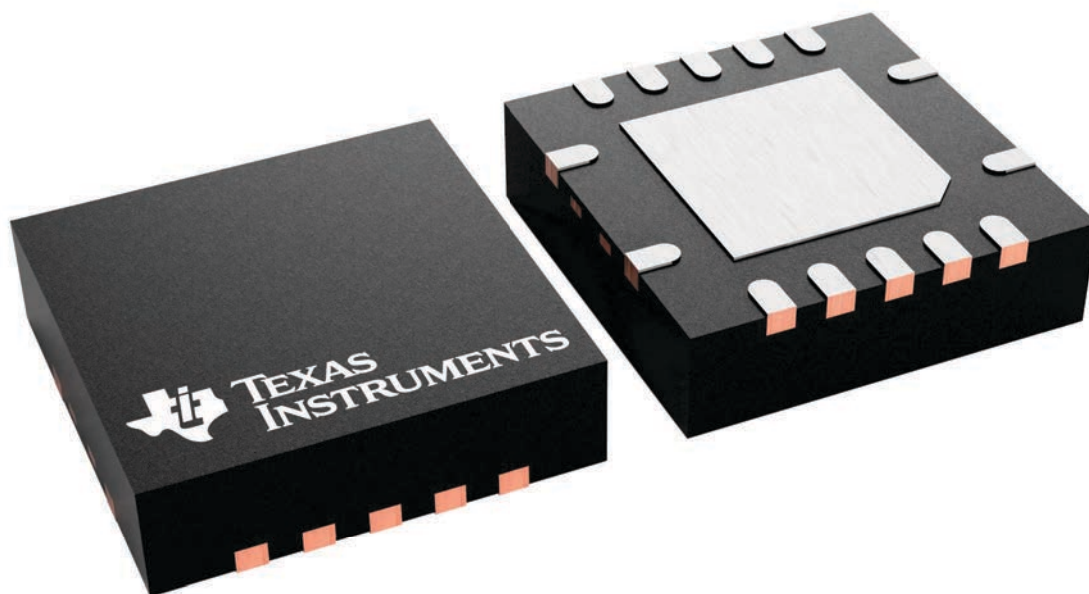
**RGY 14**

**VQFN - 1 mm max height**

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231541/A

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



4220762/A 05/2024

## NOTES:

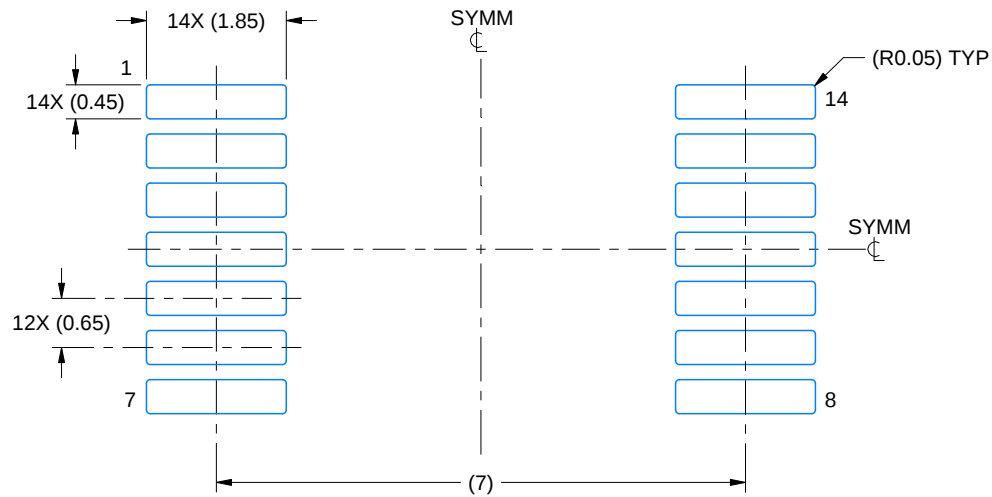
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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