

SN74HCS367-Q1 Automotive Hex Buffers and Line Drivers With Schmitt-Trigger Inputs and 3-State Outputs

1 Features

- Wide operating voltage range: 2V to 6V
- **Schmitt-trigger inputs** allow for slow or noisy input signals
- Low power consumption
 - Typical I_{CC} of 100nA
 - Typical input leakage current of ± 100 nA
- ± 7.8 mA output drive at 6V

2 Applications

- **Enable or disable a digital signal**
- **Eliminate slow or noisy input signals**
- **Hold a signal during controller reset**
- **Debounce a switch**

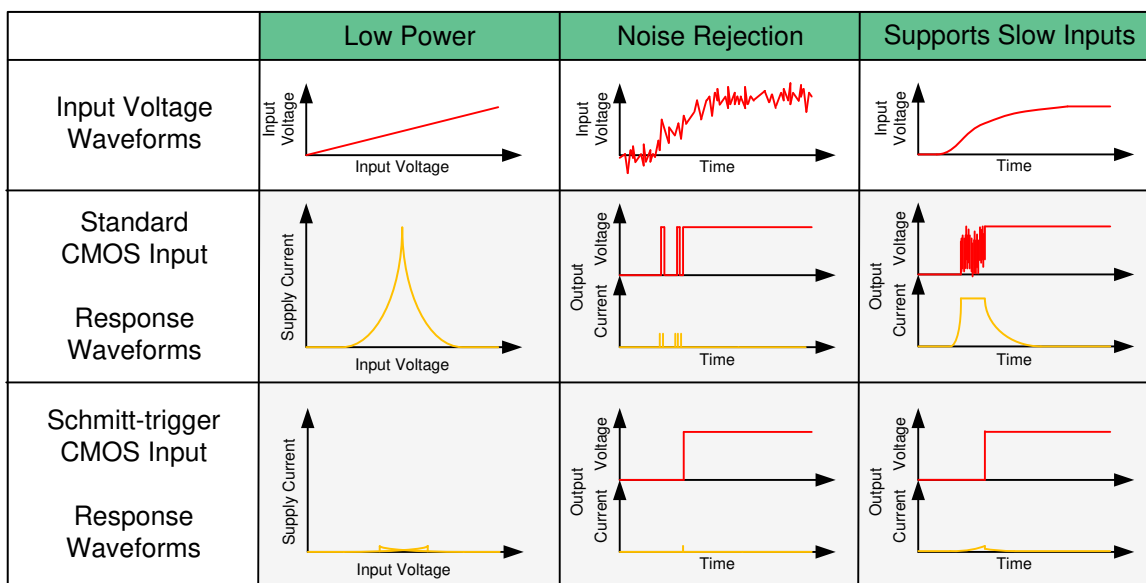
3 Description

The SN74HCS367-Q1 is a hex buffer with 3-state outputs and Schmitt-trigger inputs. The device is configured into two banks, one with four drivers and one with two drivers, each controlled by its own output enable pin.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
SN74HCS367PW-Q1	TSSOP (16)	5.00mm × 4.40mm
SN74HCS367D-Q1	SOIC (16)	9.90mm × 3.90mm
SN74HCS367WBQB-Q1	WQFN (16)	3.60mm × 2.60mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



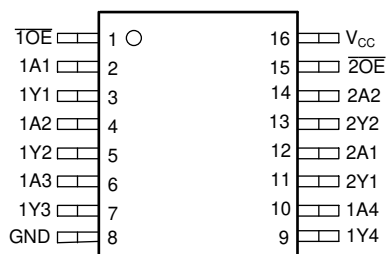
Benefits of Schmitt-Trigger Inputs



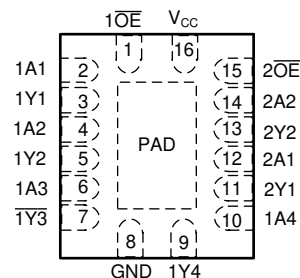
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4 Pin Configuration and Functions



D or PW Package
20-Pin SOIC or TSSOP
Top View



WBQB Package
20-Pin WQFN
Top View

Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
SOIC or TSSOP NO.	NAME		
1	1OE	I	Bank 1, output enable, active low
2	1A1	I	Bank 1, channel 1 input
3	1Y1	O	Bank 1, channel 1 output
4	1A2	I	Bank 1, channel 2 input
5	1Y2	O	Bank 1, channel 2 output
6	1A3	I	Bank 1, channel 3 input
7	1Y3	O	Bank 1, channel 3 output
8	GND	—	Ground
9	1Y4	O	Bank 1, channel 4 output
10	1A4	I	Bank 1, channel 4 input
11	2Y1	O	Bank 2, channel 1 output
12	2A1	I	Bank 2, channel 1 input
13	2Y2	O	Bank 2, channel 2 output
14	2A2	I	Bank 2, channel 2 input
15	2OE	I	Bank 2, output enable, active low
16	VCC	—	Positive supply
Thermal Pad ⁽²⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

(2) WBQB package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < −0.5V or V _I > V _{CC} + 0.5V		±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _I < −0.5V or V _I > V _{CC} + 0.5V		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±35	mA
	Continuous current through V _{CC} or GND			±70	mA
T _J	Junction temperature ⁽³⁾			150	°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings can be exceeded if the input and output current ratings are observed.
- (3) Verified by design.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2	5	6	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
T _A	Ambient temperature	−40		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74HCS367-Q1			UNIT
		PW (TSSOP)	D (SOIC)	WBQB (WQFN)	
		16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	141.2	122.2	97.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	78.8	80.9	93.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	85.8	80.6	66.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	27.7	40.4	14.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	85.5	80.3	66.4	°C/W

5.4 Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		SN74HCS367-Q1			UNIT
		PW (TSSOP)	D (SOIC)	WBQB (WQFN)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	44.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

5.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2V	1.13	1.26	1.37	V
				4.5V	2.31	2.47	2.66	
				6V	2.99	3.18	3.44	
V_{T-}	Negative switching threshold			2V	0.55	0.62	0.71	V
				4.5V	1.21	1.36	1.5	
				6V	1.56	1.79	1.99	
ΔV_T	$V_{T+} - V_{T-}$			2V	0.54	0.64	0.71	V
				4.5V	0.94	1.11	1.27	
				6V	1.20	1.38	1.57	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2V to 6V	$V_{CC} - \frac{V_{CC}}{0.1} - 0.002$			V
			$I_{OH} = -6\text{mA}$	4.5V	4.0	4.3		
			$I_{OH} = -7.8\text{mA}$	6V	5.4	5.75		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2V to 6V		0.002	0.1	V
			$I_{OL} = 4\text{mA}$	4.5V		0.18	0.30	
			$I_{OL} = 7.8\text{mA}$	6V		0.22	0.33	
I_I	Input leakage current	$V_I = V_{CC}$ or 0		6V		± 100	± 1000	nA
I_{OZ}	Output leakage current (3-state only)	$V_O = V_{CC}$ or 0		6V		0.01	2	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0, $I_O = 0$		6V		0.1	2	μA
C_i	Input capacitance			2V to 6V			5	pF

5.6 Switching Characteristics

$C_L = 50\text{pF}$; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER		FROM	TO	V _{CC}	Operating free-air temperature (T _A)						UNIT
					25°C			−40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
t _{pd}	Propagation delay	A	Y	2V	14	21	32	ns			
				4.5V	6	10	15				
				6V	5	9	12				
t _{en}	Enable time	OE	Y	2V	14	21	36	ns			
				4.5V	7	12	15				
				6V	6	9	13				

5.6 Switching Characteristics (continued)

$C_L = 50\text{pF}$; over operating free-air temperature range (unless otherwise noted). See *Parameter Measurement Information*.

PARAMETER		FROM	TO	V _{CC}	Operating free-air temperature (T _A)						UNIT
					25°C			−40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
t _{dis}	Disable time	OE	Y	2V	13		21	24			ns
				4.5V	9		13	16			
				6V	8		12	15			
t _t	Transition-time		Any output	2V			9	16			ns
				4.5V			5	9			
				6V			4	8			

5.7 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load		15		pF

5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$

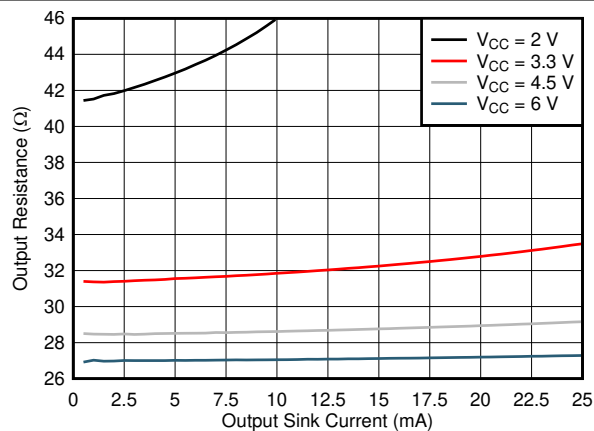


Figure 5-1. Output Driver Resistance in LOW State

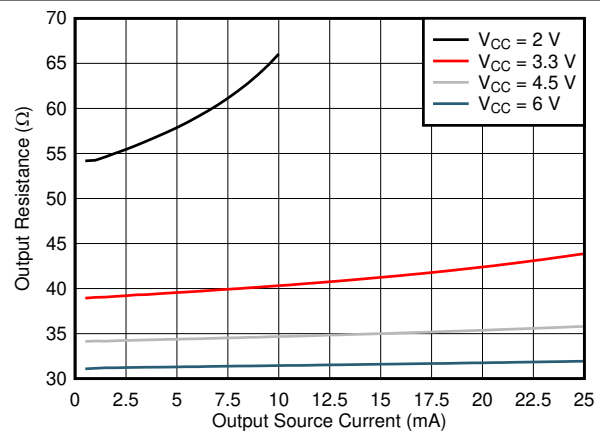


Figure 5-2. Output Driver Resistance in HIGH State.

5.8 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$

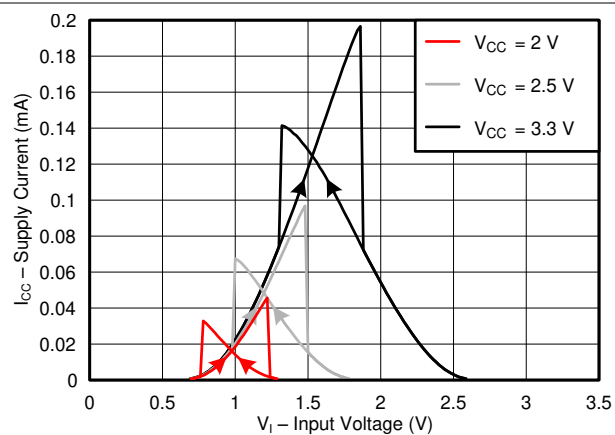


Figure 5-3. Supply Current Across Input Voltage, 2-, 2.5-, and 3.3V Supply

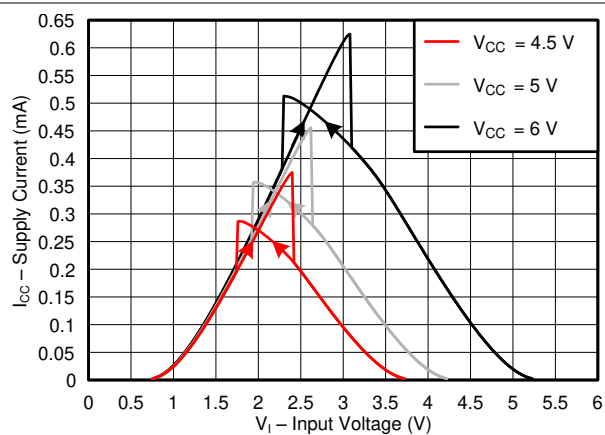


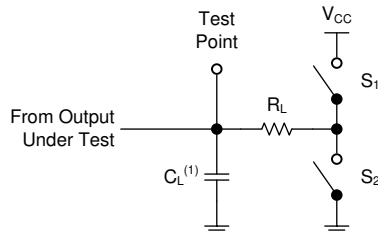
Figure 5-4. Supply Current Across Input Voltage, 4.5-, 5-, and 6V Supply

6 Parameter Measurement Information

Phase relationships between waveforms are selected arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_t < 2.5\text{ns}$.

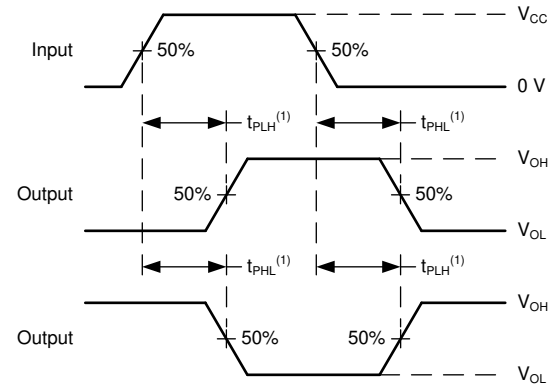
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between $t_{PLH}^{(1)}$ and $t_{PHL}^{(1)}$ is the same as t_{pd} .

Figure 6-2. Voltage Waveforms Propagation Delays

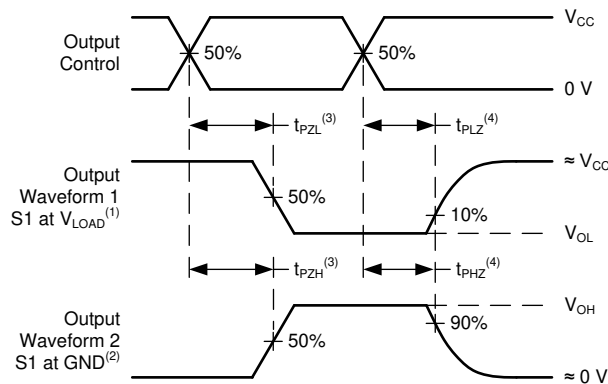
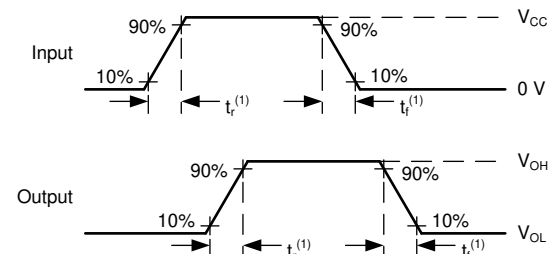


Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

Figure 6-4. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74HCS367-Q1 contains 6 individual high speed CMOS buffers with Schmitt-trigger inputs and 3-state outputs.

Each buffer performs the boolean logic function $xY_n = xA_n$, with x being the bank number and n being the channel number.

The first bank includes four buffers, and the second bank includes two buffers.

Each output enable ($\overline{xOE}$) controls one bank of buffers. When the $\overline{xOE}$ pin is in the low state, the outputs of all buffers in the bank x are enabled. When the $\overline{xOE}$ pin is in the high state, the outputs of all buffers in the bank x are disabled. All disabled output are placed into the high-impedance state.

To ensure the high-impedance state during power up or power down, both $\overline{xOE}$ pins should be tied to V_{CC} through a pull-up resistor. The value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table. Typically a 10k Ω resistor will be sufficient.

7.2 Functional Block Diagram

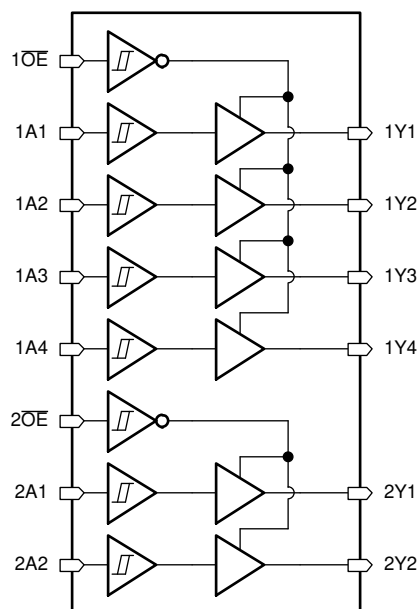


Figure 7-1. Logic Diagram (Positive Logic) for SN74HCS367-Q1

7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs: driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without damage. Limit the output power of the device to avoid damage from overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output does not source or sink current except minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the device does not control the output voltage. The output current is dependent on external factors. A floating node is a node that has no other drivers connected, and the voltage is unknown. A pull-up or pull-down resistor can be connected to the

output to provide a known voltage at the output while the device is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor meets these requirements.

Leave unused 3-state CMOS outputs disconnected.

7.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, properly terminating unused inputs is still recommended. Driving the inputs with slow transitioning signals increases dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

7.3.3 Clamp Diode Structure

As shown in [Figure 7-2](#), the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

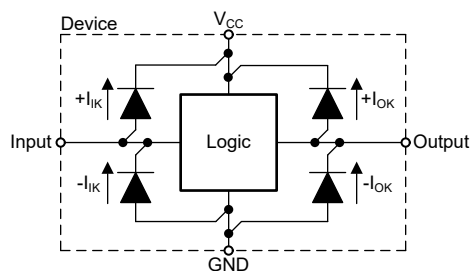


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the datasheet where packages include this feature.

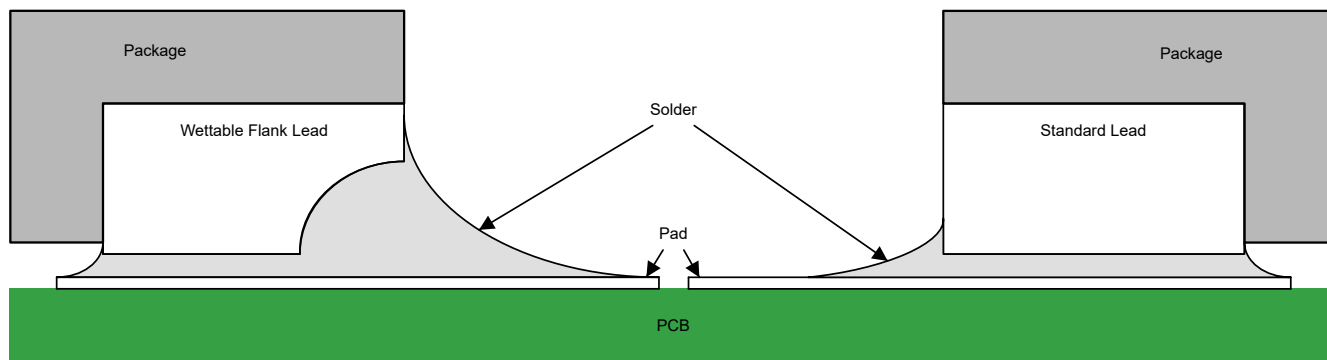


Figure 7-3. Simplified Cutaway View of Wetable-Flank QFN Package and Standard QFN Package After Soldering

Wetable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in [Figure 7-3](#), a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.4 Device Functional Modes

[Function Table](#) lists the functional modes of the SN74HCS367-Q1.

Table 7-1. Function Table

INPUTS ⁽¹⁾⁽²⁾		OUTPUTS ⁽¹⁾⁽²⁾
xOE	xAn	xYn
L	L	L
L	H	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High-Impedance State

(2) x = bank number, n = channel number

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74HCS367-Q1 can be used to drive signals over relatively long traces or transmission lines. A series damping resistor placed in series with the transmitter's output can be used to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

8.2 Typical Application

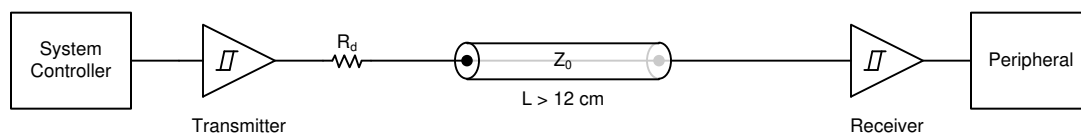


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS367-Q1 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS367-Q1 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74HCS367-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied; however, TI recommends adding a series resistor between the output and capacitor to prevent excessive current.

The SN74HCS367-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{t(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74HCS367-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k Ω resistor value is often used due to these factors.

The SN74HCS367-Q1 has no input signal transition rate requirements because the device has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, see the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value provides the peak-to-peak limit.

Unlike what occurs with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

See the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50 pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SN74HCS367-Q1 to the receiving device.
3. Verify that the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

8.2.3 Application Curves

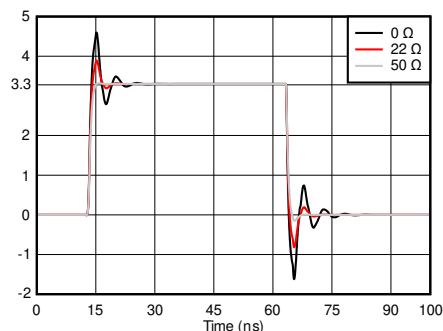


Figure 8-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor (R_d) Values

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A $0.1\mu\text{F}$ capacitor is recommended for this device. Multiple bypass capacitors can be placed in parallel to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

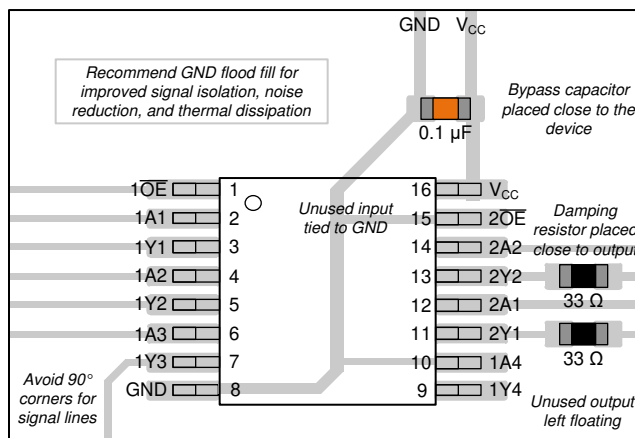


Figure 8-3. Example Layout for the SN74HCS367-Q1 in the PW Package

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [HCMOS Design Considerations application note](#)
- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 16, 2021 to September 29, 2026 (from Revision A (December 2021) to Revision B (October 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed V_{T+} limits at 2V V_{CC} from 0.7V (min), 1.5V (max) to 1.13V (min), 1.37V (max)	5
• Added V_{T+} typical values at 2V V_{CC}	5
• Changed V_{T+} limits at 4.5V V_{CC} from 1.7V (min), 3.15V (max) to 2.31V (min), 2.66V (max)	5
• Added V_{T+} typical values at 4.5V V_{CC}	5
• Changed V_{T+} limits at 6V V_{CC} from 2.1V (min), 4.2V (max) to 2.99V (min), 3.44V (max)	5
• Added V_{T+} typical values at 6V V_{CC}	5
• Changed V_{T-} limits at 2V V_{CC} from 0.3V (min), 1.0V (max) to 0.55V (min), 0.71V (max).....	5
• Added V_{T-} typical values at 2V V_{CC}	5
• Changed V_{T-} limits at 4.5V V_{CC} from 0.9V (min), 2.2V (max) to 1.21V (min), 1.50V (max)	5

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SCLS816B – SEPTEMBER 2020 – REVISED OCTOBER 2026

• Added V_{T-} typical values at 4.5V V_{CC}	5
• Changed V_{T-} limits at 6V V_{CC} from 1.2V (min), 3.0V (max) to 1.56V (min), 1.99V (max).....	5
• Added V_{T-} typical values at 6V V_{CC}	5
• Changed ΔV_T limits at 2V V_{CC} from 0.2V (min), 1.0V (max) to 0.54V (min), 0.71V (max).....	5
• Added ΔV_T typical values at 2V V_{CC}	5
• Changed ΔV_T limits at 4.5V V_{CC} from 0.4V (min), 1.4V (max) to 0.94V (min), 1.27V (max).....	5
• Added ΔV_T typical values at 4.5V V_{CC}	5
• Changed ΔV_T limits at 6V V_{CC} from 0.6V (min), 1.6V (max) to 1.20V (min), 1.57V (max).....	5
• Added ΔV_T typical values at 6V V_{CC}	5
• Added Section 7.3.4	10

Changes from Revision * (September 2020) to Revision A (December 2021)	Page
• Added WBQB package to <i>Pin Configuration and Functions</i>	3
• Added WBQB package to Thermal Information table.....	4
• Added Wettable Flanks section to <i>Feature Description</i>	9

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCS367QDRQ1	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS367Q
SN74HCS367QDRQ1.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS367Q
SN74HCS367QPWRQ1	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HCS367Q
SN74HCS367QPWRQ1.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS367Q
SN74HCS367QWBQBRQ1	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS367Q
SN74HCS367QWBQBRQ1.A	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS367Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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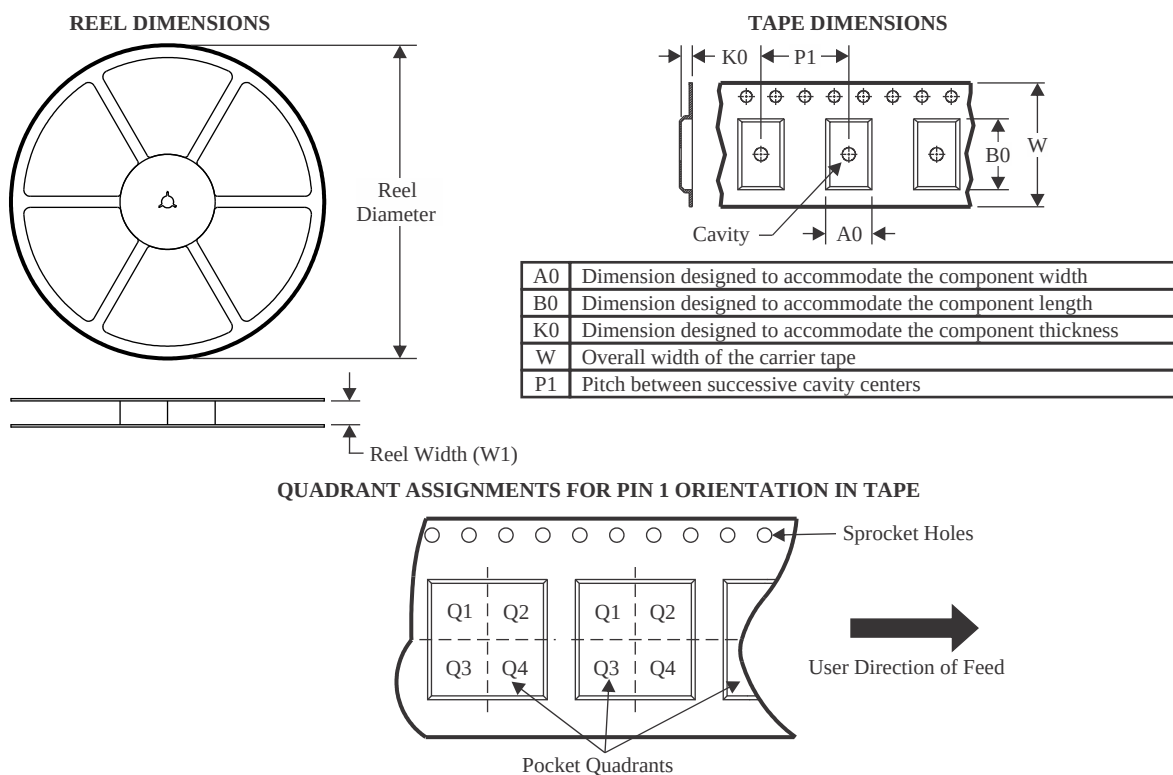
OTHER QUALIFIED VERSIONS OF SN74HCS367-Q1 :

- Catalog : [SN74HCS367](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

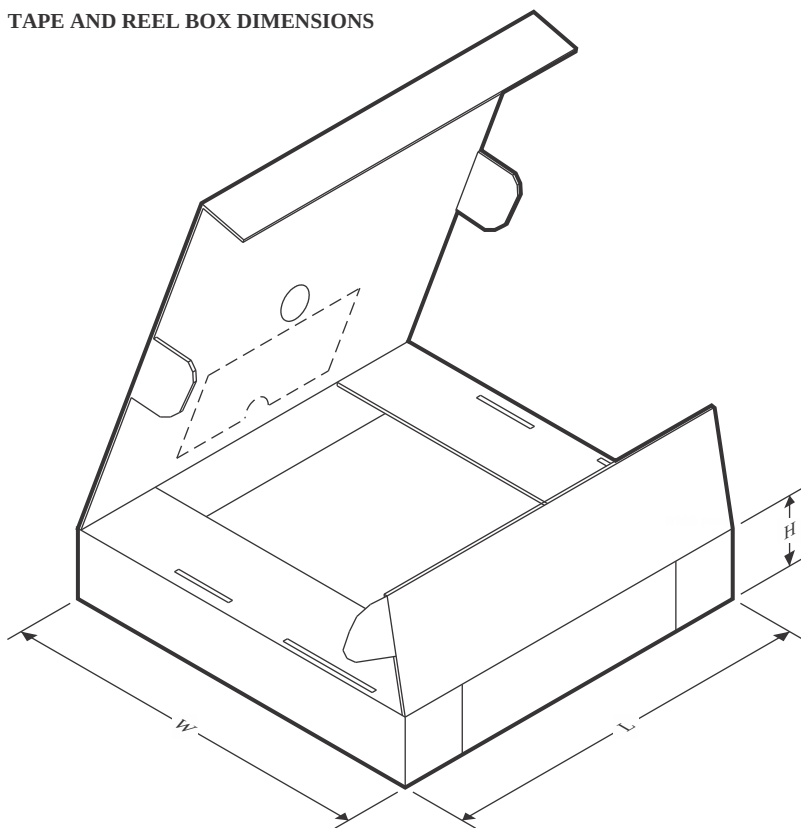
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS367QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCS367QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS367QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

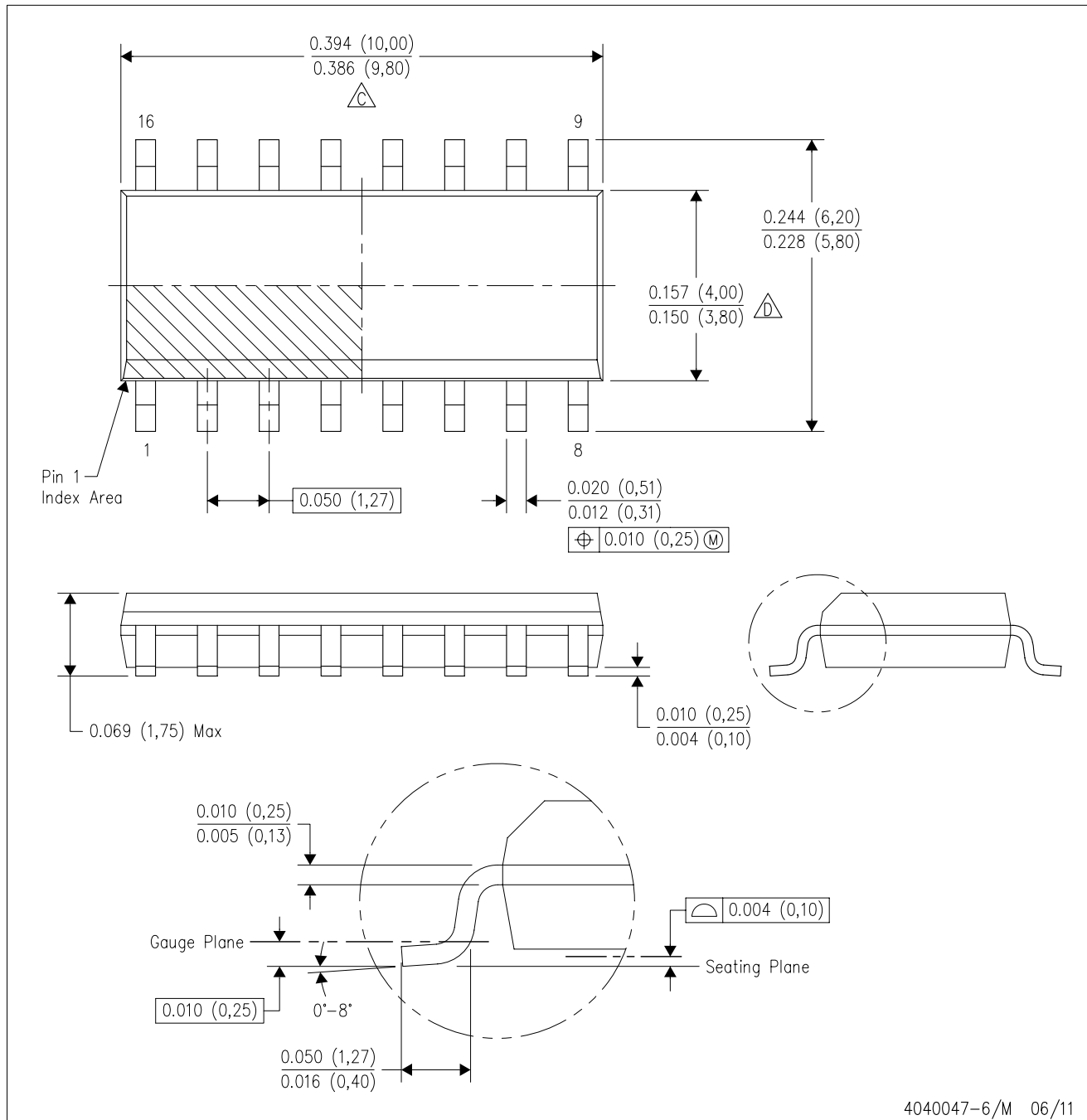


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS367QDRQ1	SOIC	D	16	2500	353.0	353.0	32.0
SN74HCS367QPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HCS367QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

GENERIC PACKAGE VIEW

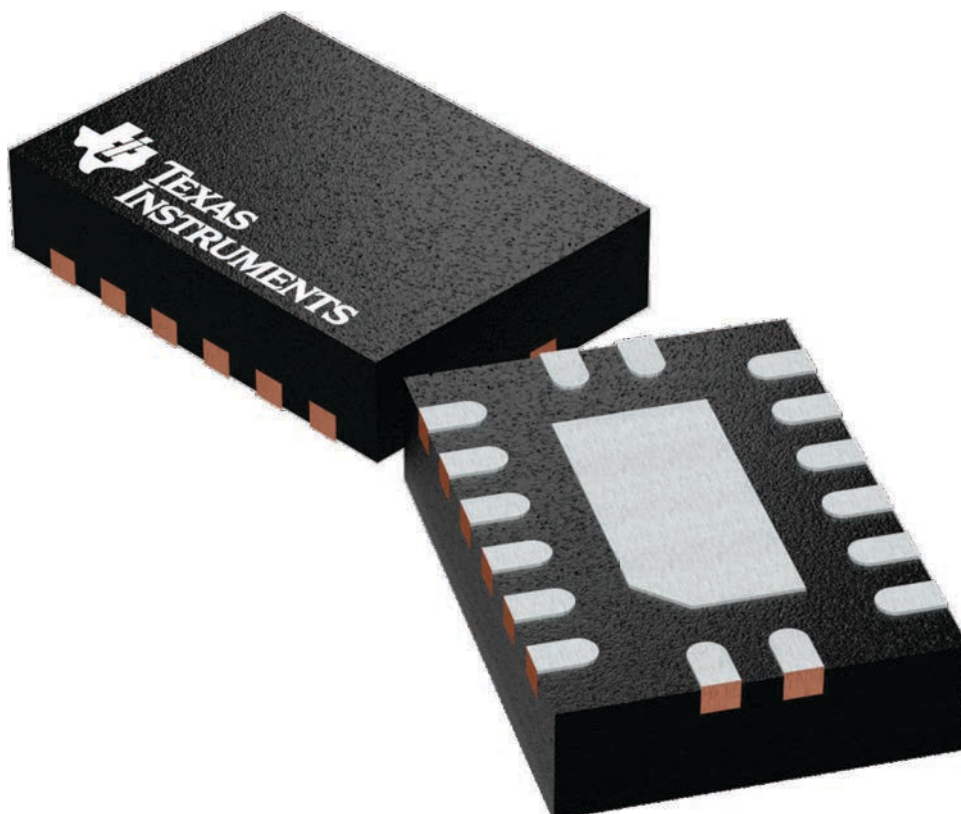
BQB 16

WQFN - 0.8 mm max height

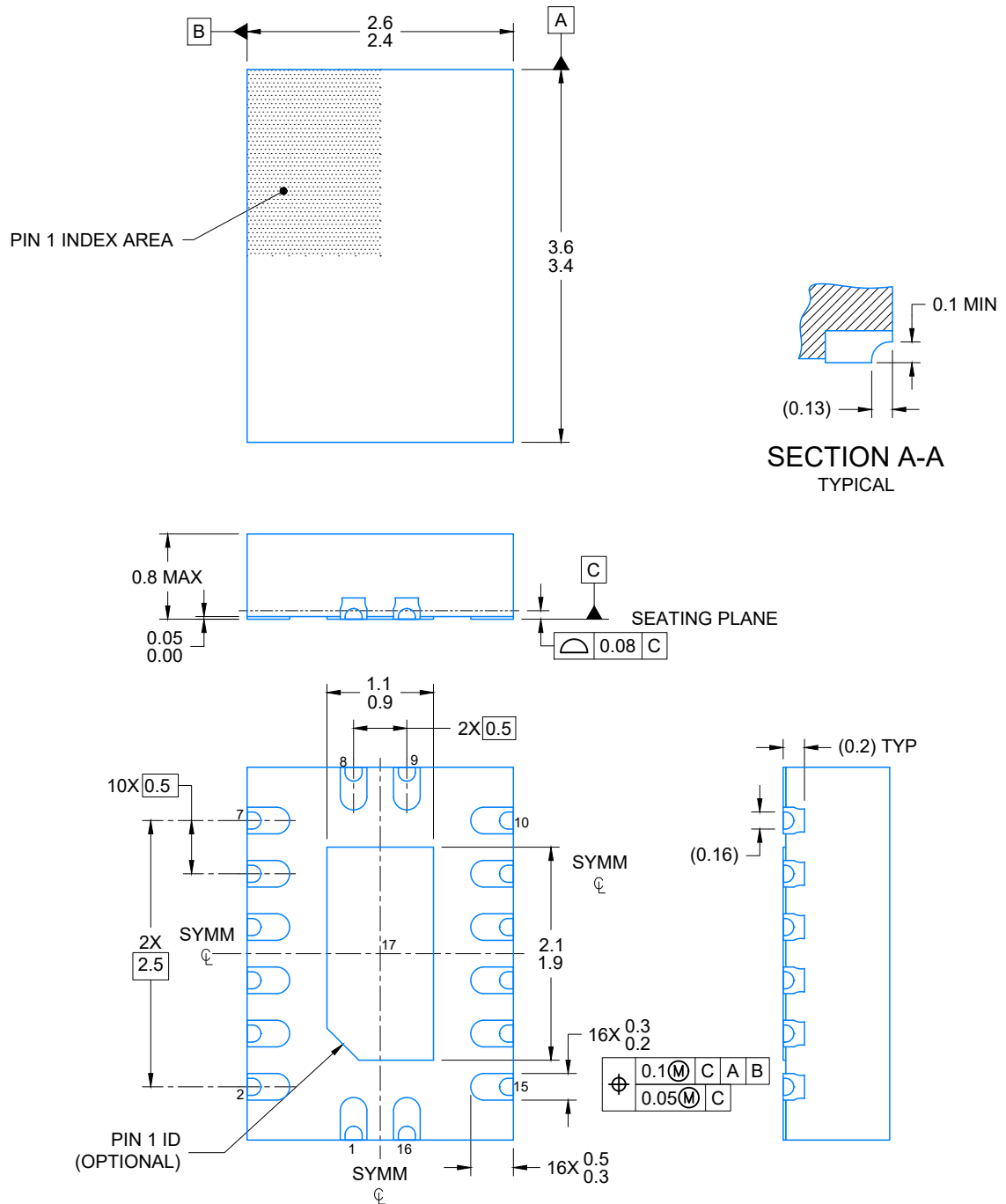
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226161/A

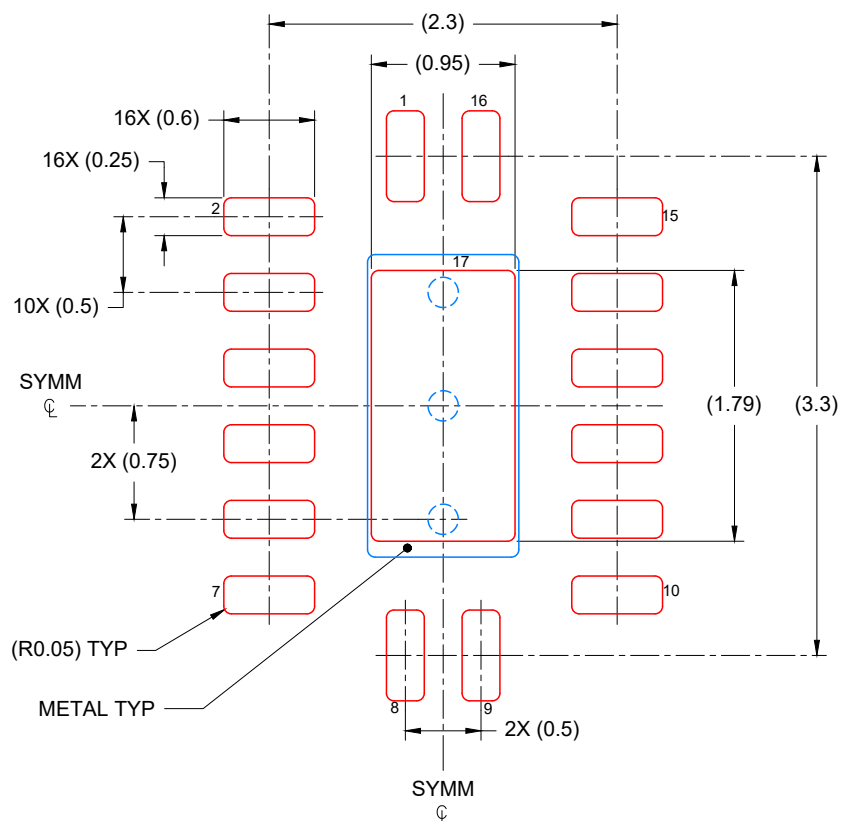


4226135/A 08/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

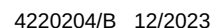
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



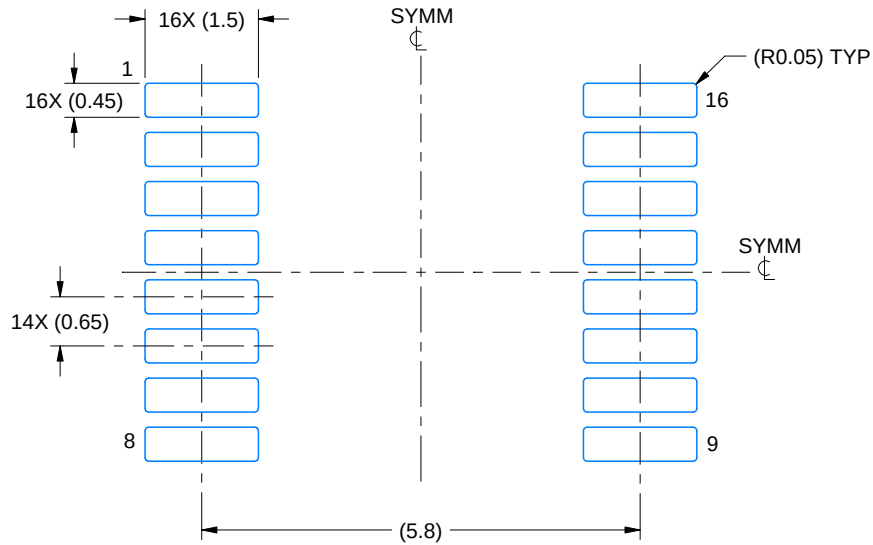
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

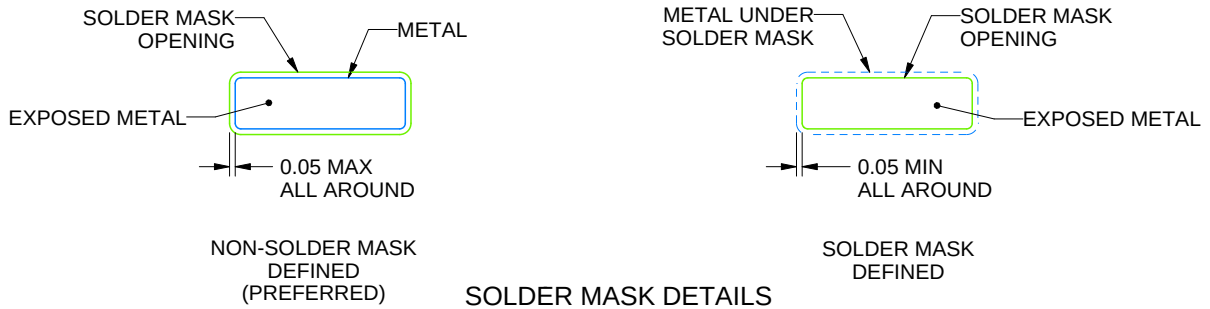
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

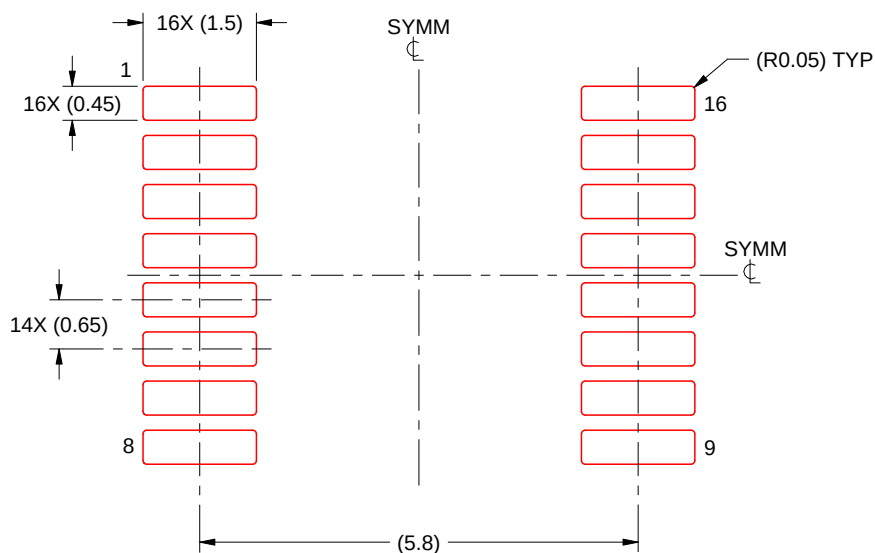
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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