

# SN74CBT3245C

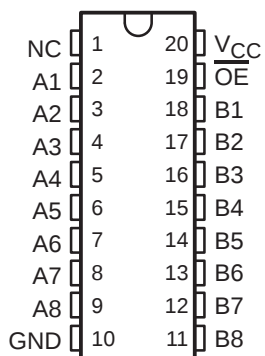
## 8-BIT FET BUS SWITCH

### 5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

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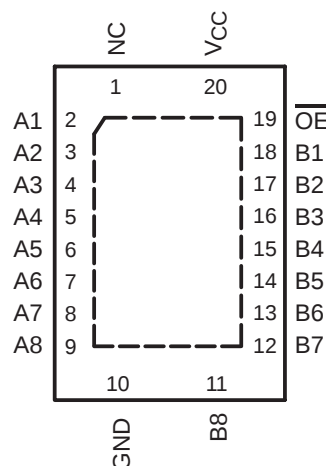
- Undershoot Protection for Off-Isolation on A and B Ports Up To –2 V
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{ON}$ ) Characteristics ( $r_{ON} = 3\ \Omega$  Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{IO(OFF)} = 5.5\ \text{pF}$  Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 3\ \mu\text{A}$  Max)
- $V_{CC}$  Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{OFF}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: USB Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

RGY PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The SN74CBT3245C is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{ON}$ ), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3245C provides protection for undershoot up to –2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3245C is organized as an 8-bit bus switch with a single output-enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is low, the bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the bus switch is OFF, and the high-impedance state exists between the A and B ports.



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description/ordering information (continued)

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

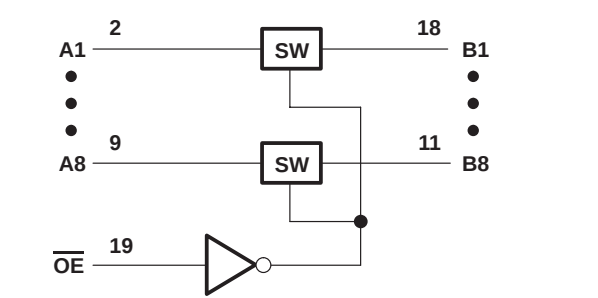
| T <sub>A</sub> | PACKAGE†          |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------------|---------------|-----------------------|------------------|
| –40°C to 85°C  | QFN – RGY         | Tape and reel | SN74CBT3245CRGYR      | CU245C           |
|                | SOIC – DW         | Tube          | SN74CBT3245CDW        | CBT3245C         |
|                |                   | Tape and reel | SN74CBT3245CDWR       |                  |
|                | SSOP – DB         | Tube          | SN74CBT3245CDB        | CU245C           |
|                |                   | Tape and reel | SN74CBT3245CDBR       |                  |
|                | SSOP (QSOP) – DBQ | Tape and reel | SN74CBT3245CDBQR      | CBT3245C         |
|                | TSSOP – PW        | Tube          | SN74CBT3245CPW        | CU245C           |
|                |                   | Tape and reel | SN74CBT3245CPWR       |                  |
|                | TVSOP – DGV       | Tape and reel | SN74CBT3245CDGVR      | CU245C           |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

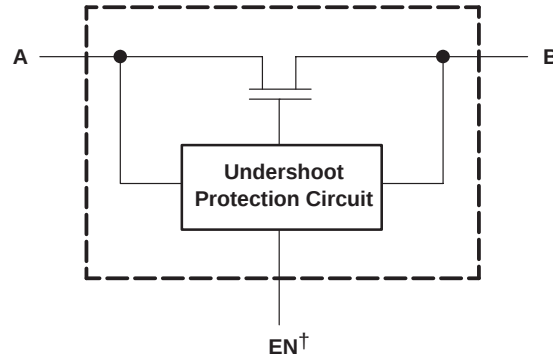
FUNCTION TABLE

| INPUT $\overline{OE}$ | INPUT/OUTPUT A | FUNCTION        |
|-----------------------|----------------|-----------------|
| L                     | B              | A port = B port |
| H                     | Z              | Disconnect      |

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

|                                                                   |                |
|-------------------------------------------------------------------|----------------|
| Supply voltage range, $V_{CC}$                                    | –0.5 V to 7 V  |
| Control input voltage range, $V_{IN}$ (see Notes 1 and 2)         | –0.5 V to 7 V  |
| Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)       | –0.5 V to 7 V  |
| Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ )            | –50 mA         |
| I/O port clamp current, $I_{I/OK}$ ( $V_{I/O} < 0$ )              | –50 mA         |
| ON-state switch current, $I_{I/O}$ (see Note 4)                   | ±128 mA        |
| Continuous current through $V_{CC}$ or GND terminals              | ±100 mA        |
| Package thermal impedance, $\theta_{JA}$ (see Note 5): DB package | 70°C/W         |
| (see Note 5): DBQ package                                         | 68°C/W         |
| (see Note 5): DGV package                                         | 92°C/W         |
| (see Note 5): DW package                                          | 58°C/W         |
| (see Note 5): PW package                                          | 83°C/W         |
| (see Note 6): RGY package                                         | 37°C/W         |
| Storage temperature range, $T_{stg}$                              | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
  2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  3.  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
  4.  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
  5. The package thermal impedance is calculated in accordance with JESD 51-7.
  6. The package thermal impedance is calculated in accordance with JESD 51-5.

**recommended operating conditions (see Note 7)**

|                                           | MIN | MAX | UNIT |
|-------------------------------------------|-----|-----|------|
| $V_{CC}$ Supply voltage                   | 4   | 5.5 | V    |
| $V_{IH}$ High-level control input voltage | 2   | 5.5 | V    |
| $V_{IL}$ Low-level control input voltage  | 0   | 0.8 | V    |
| $V_{I/O}$ Data input/output voltage       | 0   | 5.5 | V    |
| $T_A$ Operating free-air temperature      | –40 | 85  | °C   |

NOTE 7: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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## 8-BIT FET BUS SWITCH

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                     |                | TEST CONDITIONS                                        |                                                                                                             | MIN | TYP <sup>†</sup> | MAX  | UNIT |
|-------------------------------|----------------|--------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|-----|------------------|------|------|
| V <sub>IK</sub>               | Control inputs | V <sub>CC</sub> = 4.5 V,                               | I <sub>IN</sub> = -18 mA                                                                                    |     |                  | -1.8 | V    |
| V <sub>IKU</sub>              | Data inputs    | V <sub>CC</sub> = 5 V,                                 | 0 mA > I <sub>I</sub> ≥ -50 mA,<br>V <sub>IN</sub> = V <sub>CC</sub> or GND, Switch OFF                     |     |                  | -2   | V    |
| I <sub>IN</sub>               | Control inputs | V <sub>CC</sub> = 5.5 V,                               | V <sub>IN</sub> = V <sub>CC</sub> or GND                                                                    |     |                  | ±1   | μA   |
| I <sub>OZ</sub> <sup>‡</sup>  |                | V <sub>CC</sub> = 5.5 V,                               | V <sub>O</sub> = 0 to 5.5 V,<br>V <sub>I</sub> = 0, Switch OFF,<br>V <sub>IN</sub> = V <sub>CC</sub> or GND |     |                  | ±10  | μA   |
| I <sub>off</sub>              |                | V <sub>CC</sub> = 0,                                   | V <sub>O</sub> = 0 to 5.5 V,<br>V <sub>I</sub> = 0                                                          |     |                  | 10   | μA   |
| I <sub>CC</sub>               |                | V <sub>CC</sub> = 5.5 V,                               | I <sub>I/O</sub> = 0,<br>V <sub>IN</sub> = V <sub>CC</sub> or GND, Switch ON or OFF                         |     |                  | 3    | μA   |
| ΔI <sub>CC</sub> <sup>§</sup> | Control inputs | V <sub>CC</sub> = 5.5 V,                               | One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND                                                  |     |                  | 2.5  | mA   |
| C <sub>in</sub>               | Control inputs | V <sub>IN</sub> = 3 V or 0                             |                                                                                                             |     | 4                |      | pF   |
| C <sub>io</sub> (OFF)         |                | V <sub>I/O</sub> = 3 V or 0, Switch OFF,               | V <sub>IN</sub> = V <sub>CC</sub> or GND                                                                    |     | 5.5              |      | pF   |
| C <sub>io</sub> (ON)          |                | V <sub>I/O</sub> = 3 V or 0, Switch ON,                | V <sub>IN</sub> = V <sub>CC</sub> or GND                                                                    |     | 14               |      | pF   |
| r <sub>on</sub> <sup>¶</sup>  |                | V <sub>CC</sub> = 4 V,<br>TYP at V <sub>CC</sub> = 4 V | V <sub>I</sub> = 2.4 V, I <sub>O</sub> = -15 mA                                                             |     | 8                | 12   | Ω    |
|                               |                | V <sub>CC</sub> = 4.5 V                                | V <sub>I</sub> = 0, I <sub>O</sub> = 64 mA                                                                  |     | 3                | 6    |      |
|                               |                |                                                        | I <sub>O</sub> = 30 mA                                                                                      |     | 3                | 6    |      |
|                               |                |                                                        | V <sub>I</sub> = 2.4 V, I <sub>O</sub> = -15 mA                                                             |     | 5                | 10   |      |

V<sub>IN</sub> and I<sub>IN</sub> refer to control inputs. V<sub>I</sub>, V<sub>O</sub>, I<sub>I</sub>, and I<sub>O</sub> refer to data pins.

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), T<sub>A</sub> = 25°C.

<sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

<sup>§</sup> This is the increase in supply current for each input that is at the specified voltage level, rather than V<sub>CC</sub> or GND.

<sup>¶</sup> Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER                    | FROM<br>(INPUT)        | TO<br>(OUTPUT) | V <sub>CC</sub> = 4 V |      | V <sub>CC</sub> = 5 V<br>± 0.5 V |      | UNIT |
|------------------------------|------------------------|----------------|-----------------------|------|----------------------------------|------|------|
|                              |                        |                | MIN                   | MAX  | MIN                              | MAX  |      |
| t <sub>pd</sub> <sup>#</sup> | A or B                 | B or A         |                       | 0.24 |                                  | 0.15 | ns   |
| t <sub>en</sub>              | $\overline{\text{OE}}$ | A or B         |                       | 5.1  | 1.5                              | 4.7  | ns   |
| t <sub>dis</sub>             | $\overline{\text{OE}}$ | A or B         |                       | 4.9  | 1.5                              | 5.3  | ns   |

<sup>#</sup> The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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**8-BIT FET BUS SWITCH**  
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undershoot characteristics (see Figures 1 and 2)

| PARAMETER  | TEST CONDITIONS                                                 | MIN | TYP <sup>†</sup> | MAX | UNIT |
|------------|-----------------------------------------------------------------|-----|------------------|-----|------|
| $V_{OUTU}$ | $V_{CC} = 5.5 \text{ V}$ , Switch OFF, $V_{IN} = V_{CC}$ or GND | 2   | $V_{OH} - 0.3$   |     | V    |

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

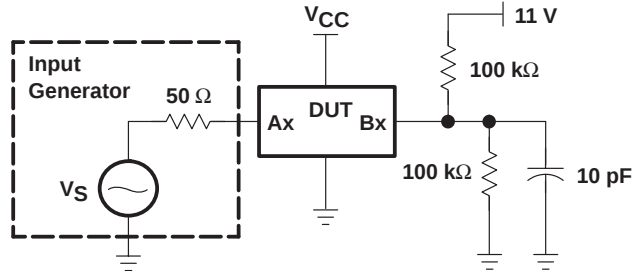


Figure 1. Device Test Setup

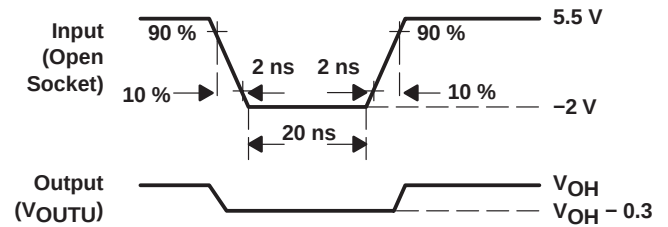


Figure 2. Transient Input Voltage ( $V_I$ ) and Output Voltage ( $V_{OUTU}$ ) Waveforms (Switch OFF)

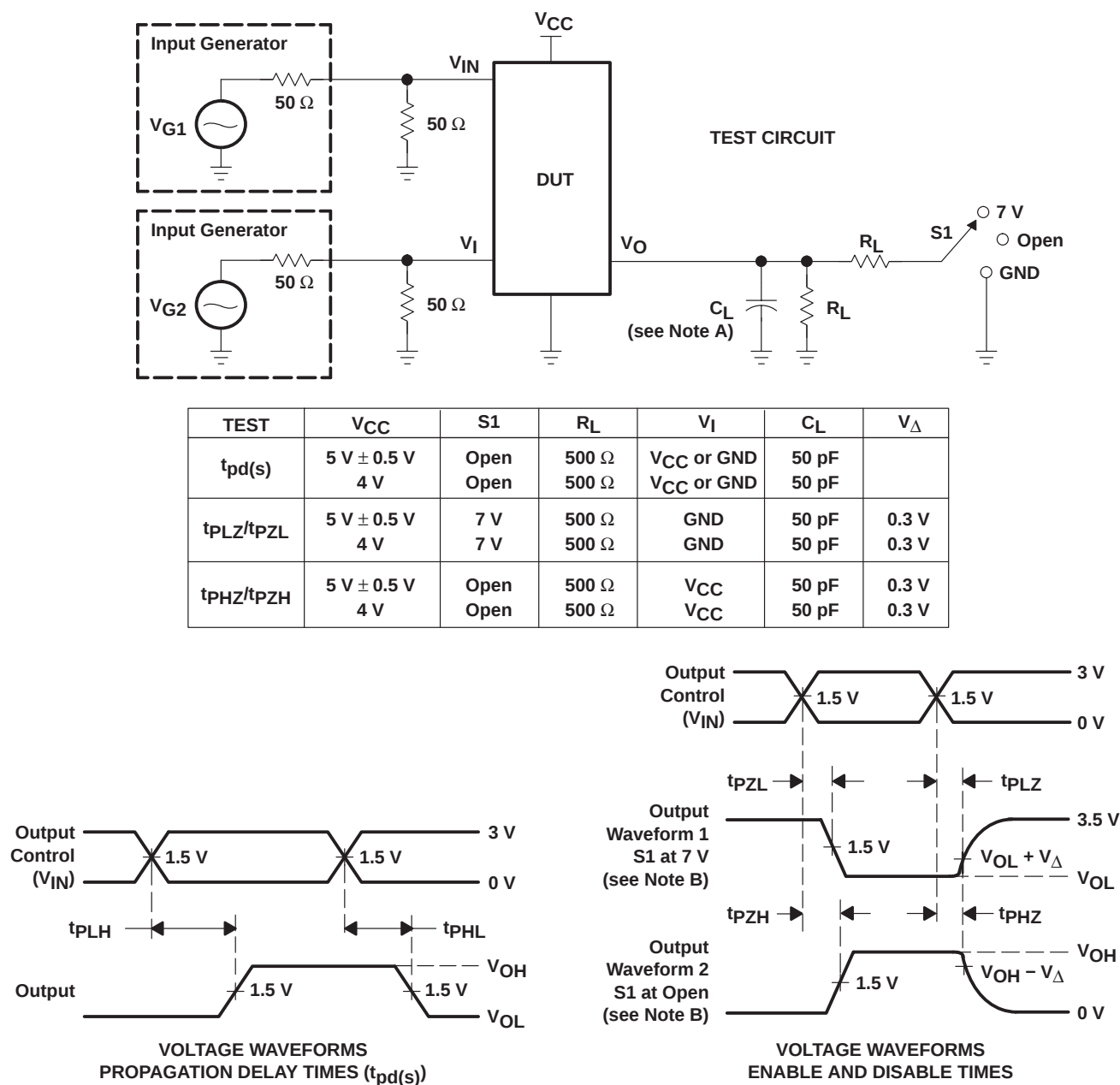
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#### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>(s). The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74CBT3245CDBQR</a> | Active        | Production           | SSOP (DBQ)   20  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CBT3245C            |
| SN74CBT3245CDBQR.B               | Active        | Production           | SSOP (DBQ)   20  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CBT3245C            |
| <a href="#">SN74CBT3245CDBR</a>  | Active        | Production           | SSOP (DB)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CU245C              |
| SN74CBT3245CDBR.B                | Active        | Production           | SSOP (DB)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CU245C              |
| <a href="#">SN74CBT3245CDGVR</a> | Active        | Production           | TVSOP (DGV)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CU245C              |
| SN74CBT3245CDGVR.B               | Active        | Production           | TVSOP (DGV)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CU245C              |
| SN74CBT3245CDGVRG4               | Active        | Production           | TVSOP (DGV)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CU245C              |
| SN74CBT3245CDGVRG4.B             | Active        | Production           | TVSOP (DGV)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CU245C              |
| <a href="#">SN74CBT3245CDW</a>   | Active        | Production           | SOIC (DW)   20   | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBT3245C            |
| SN74CBT3245CDW.B                 | Active        | Production           | SOIC (DW)   20   | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBT3245C            |
| <a href="#">SN74CBT3245CDWR</a>  | Active        | Production           | SOIC (DW)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBT3245C            |
| SN74CBT3245CDWR.B                | Active        | Production           | SOIC (DW)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CBT3245C            |
| <a href="#">SN74CBT3245CPW</a>   | Active        | Production           | TSSOP (PW)   20  | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CU245C              |
| SN74CBT3245CPW.B                 | Active        | Production           | TSSOP (PW)   20  | 70   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CU245C              |
| <a href="#">SN74CBT3245CPWR</a>  | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CU245C              |
| SN74CBT3245CPWR.B                | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | CU245C              |
| <a href="#">SN74CBT3245CRGYR</a> | Active        | Production           | VQFN (RGY)   20  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CU245C              |
| SN74CBT3245CRGYR.B               | Active        | Production           | VQFN (RGY)   20  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CU245C              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

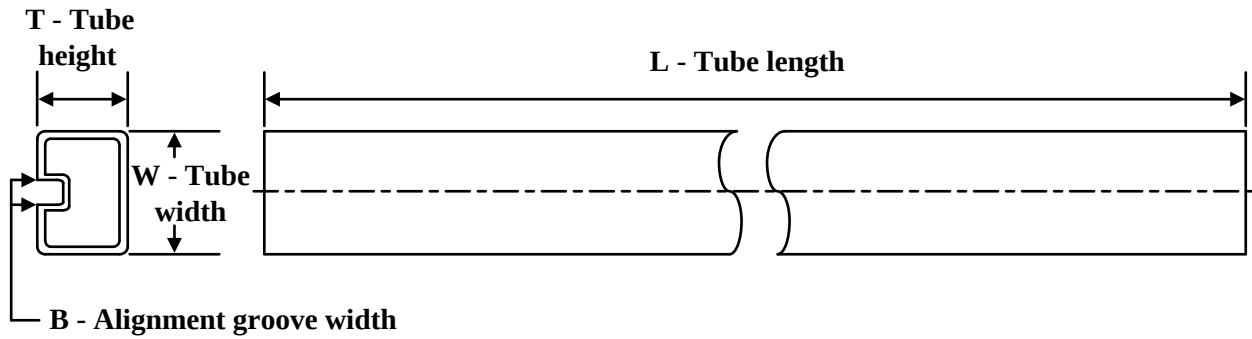
| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBT3245CDBQR   | SSOP         | DBQ             | 20   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74CBT3245CDBR    | SSOP         | DB              | 20   | 2000 | 330.0              | 16.4               | 8.2     | 7.5     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74CBT3245CDGVR   | TVSOP        | DGV             | 20   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBT3245CDGVRG4 | TVSOP        | DGV             | 20   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBT3245CDWR    | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74CBT3245CPWR    | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74CBT3245CRGYR   | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.71    | 4.71    | 1.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBT3245CDBQR   | SSOP         | DBQ             | 20   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74CBT3245CDBR    | SSOP         | DB              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CBT3245CDGVR   | TVSOP        | DGV             | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CBT3245CDGVRG4 | TVSOP        | DGV             | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CBT3245CDWR    | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74CBT3245CPWR    | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CBT3245CRGYR   | VQFN         | RGY             | 20   | 3000 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device           | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74CBT3245CDW   | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74CBT3245CDW.B | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74CBT3245CPW   | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |
| SN74CBT3245CPW.B | PW           | TSSOP        | 20   | 70  | 530    | 10.2   | 3600   | 3.5    |



4220206/A 02/2017

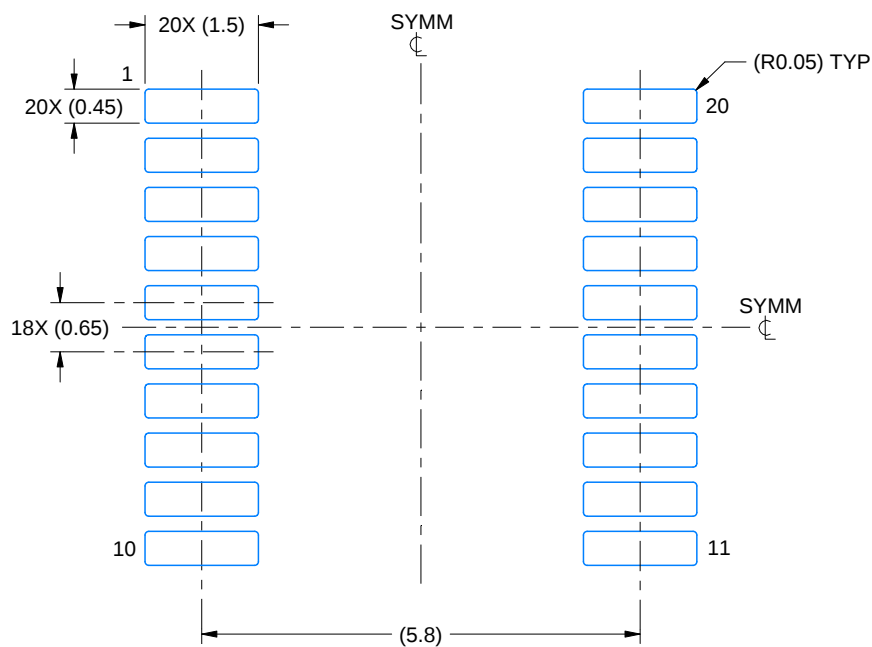
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

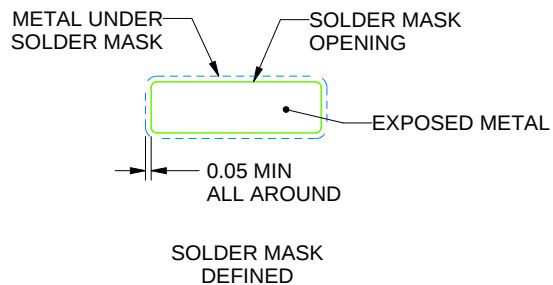
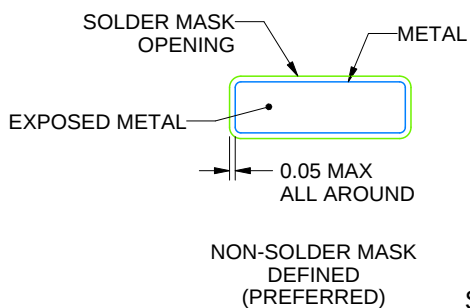
**PW0020A**

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

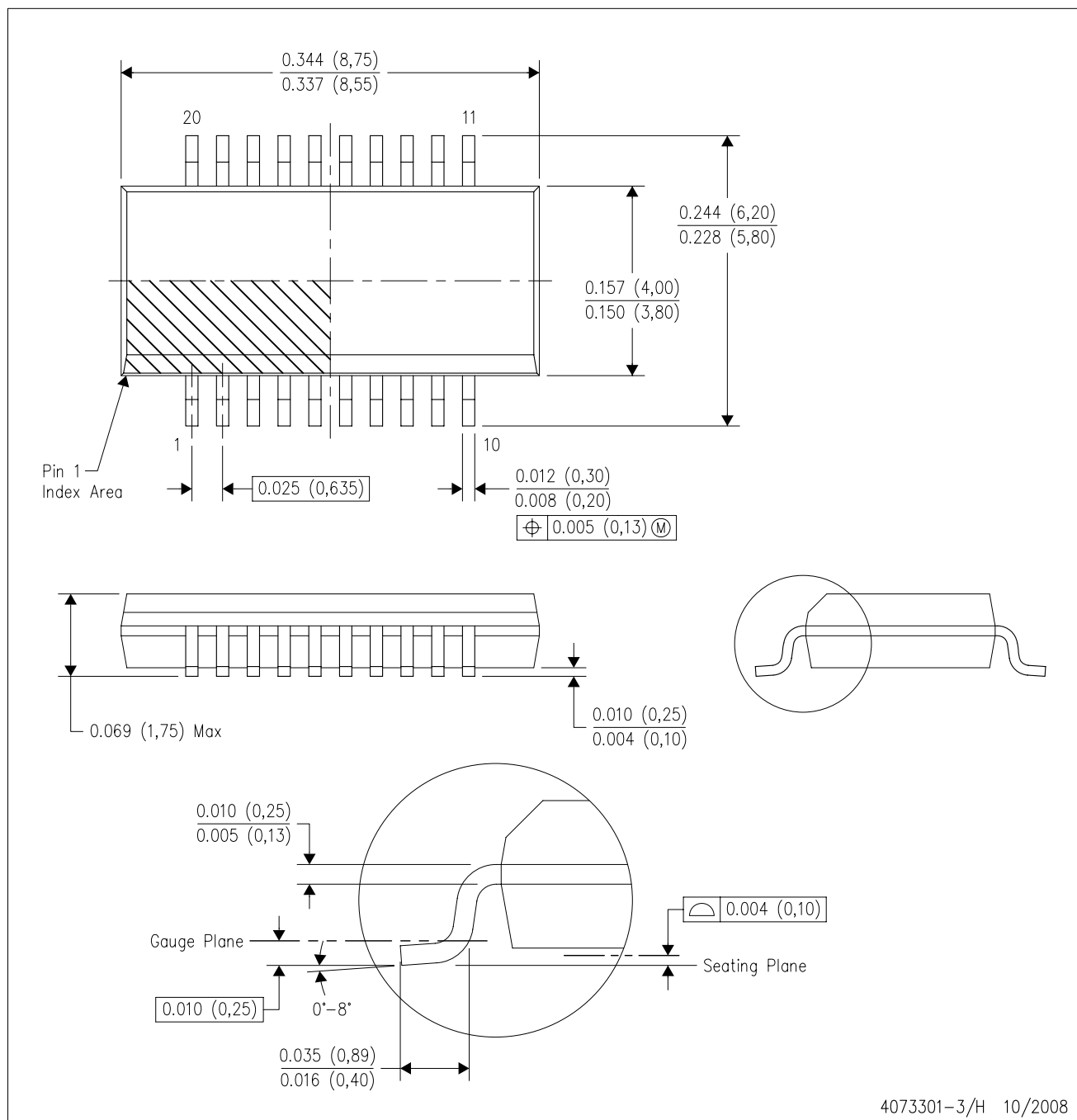
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

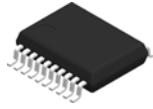
DBQ (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



4073301-3/H 10/2008

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AD.



4214851/B 08/2019

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

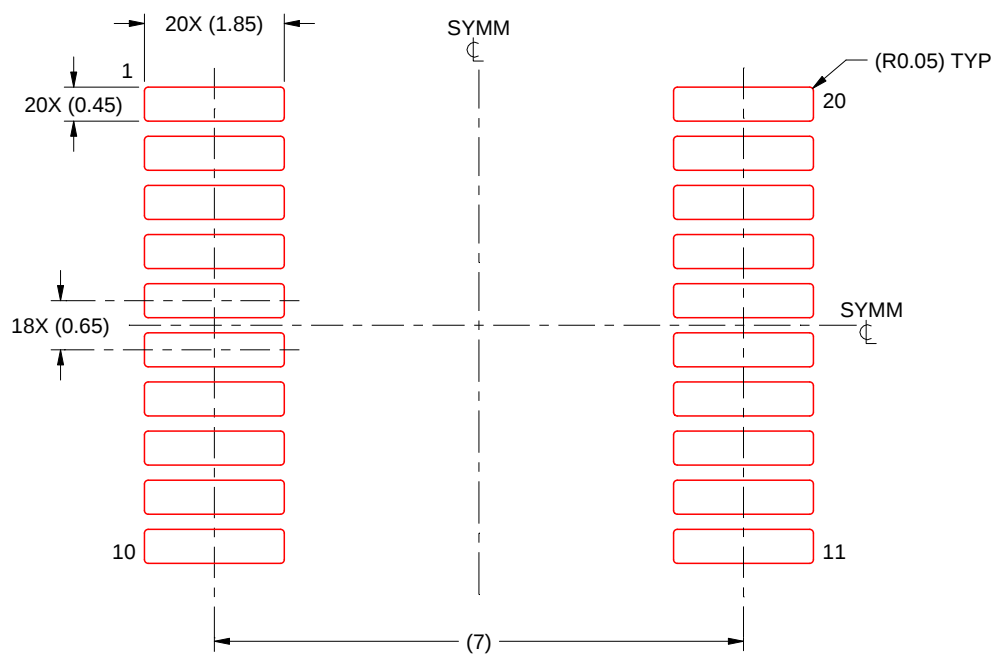
6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**DB0020A**

**SSOP - 2 mm max height**

## SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## GENERIC PACKAGE VIEW

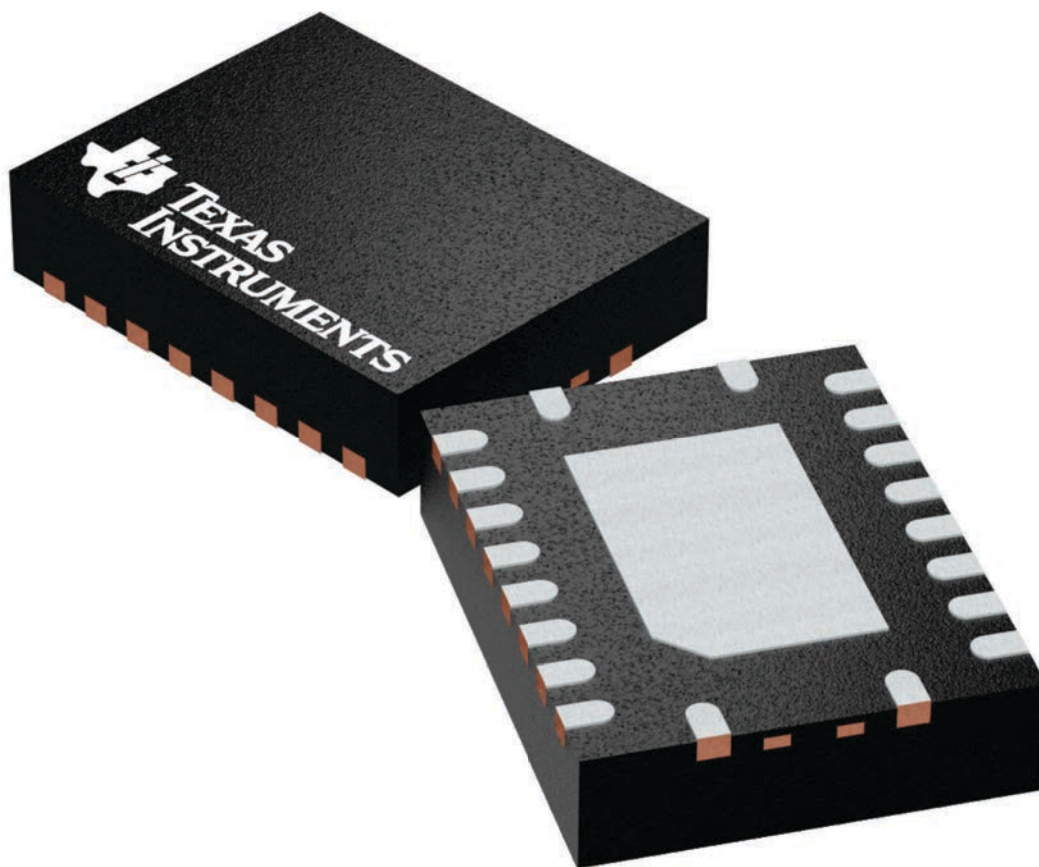
**RGY 20**

**VQFN - 1 mm max height**

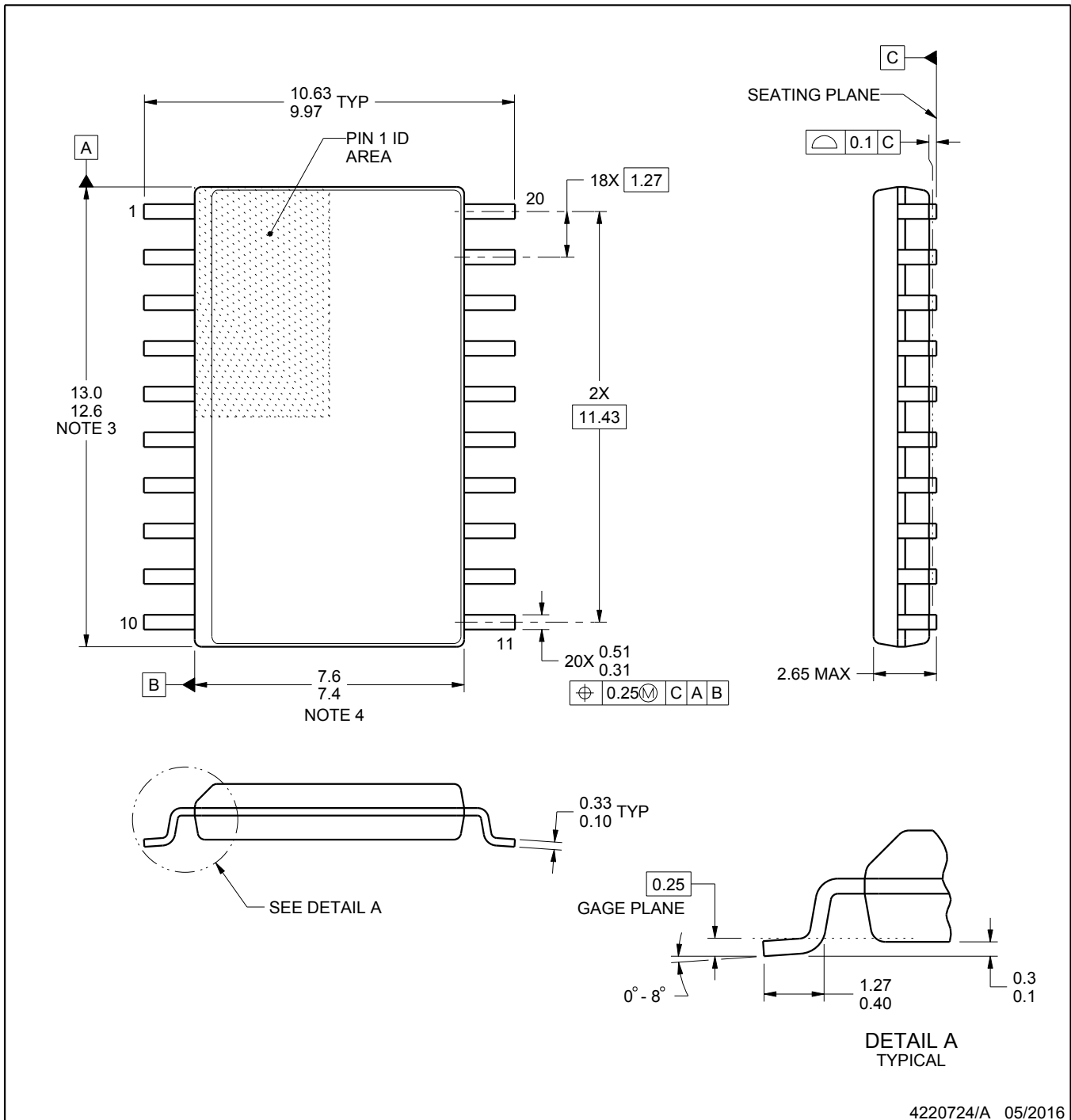
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4220724/A 05/2016

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025