

SN74CBT16292

12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER WITH INTERNAL PULLDOWN RESISTORS

SCDS053E – MARCH 1998 – REVISED OCTOBER 2000

- Member of Texas Instruments' Widebus™ Family
- 4-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Make-Before-Break Feature
- Internal 500-Ω Pulldown Resistors to Ground
- Latch-Up Performance Exceeds 250 mA Per JESD 17

description

The SN74CBT16292 is a 12-bit 1-of-2 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When the select (S) input is low, port A is connected to port B1, and R_{INT} is connected to port B2. When S is high, port A is connected to port B2, and R_{INT} is connected to port B1.

DGG, DGV, OR DL PACKAGE (TOP VIEW)

S	1	56	NC
1A	2	55	NC
NC	3	54	1B1
2A	4	53	1B2
NC	5	52	2B1
3A	6	51	2B2
NC	7	50	3B1
GND	8	49	GND
4A	9	48	3B2
NC	10	47	4B1
5A	11	46	4B2
NC	12	45	5B1
6A	13	44	5B2
NC	14	43	6B1
7A	15	42	6B2
NC	16	41	7B1
V _{CC}	17	40	7B2
8A	18	39	8B1
GND	19	38	GND
NC	20	37	8B2
9A	21	36	9B1
NC	22	35	9B2
10A	23	34	10B1
NC	24	33	10B2
11A	25	32	11B1
NC	26	31	11B2
12A	27	30	12B1
NC	28	29	12B2

NC – No internal connection

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBT16292DL	CBT16292
		Tape and reel	SN74CBT16292DLR	
	TSSOP – DGG	Tape and reel	SN74CBT16292DGGR	CBT16292
	TVSOP – DGV	Tape and reel	SN74CBT16292DGVR	CY292

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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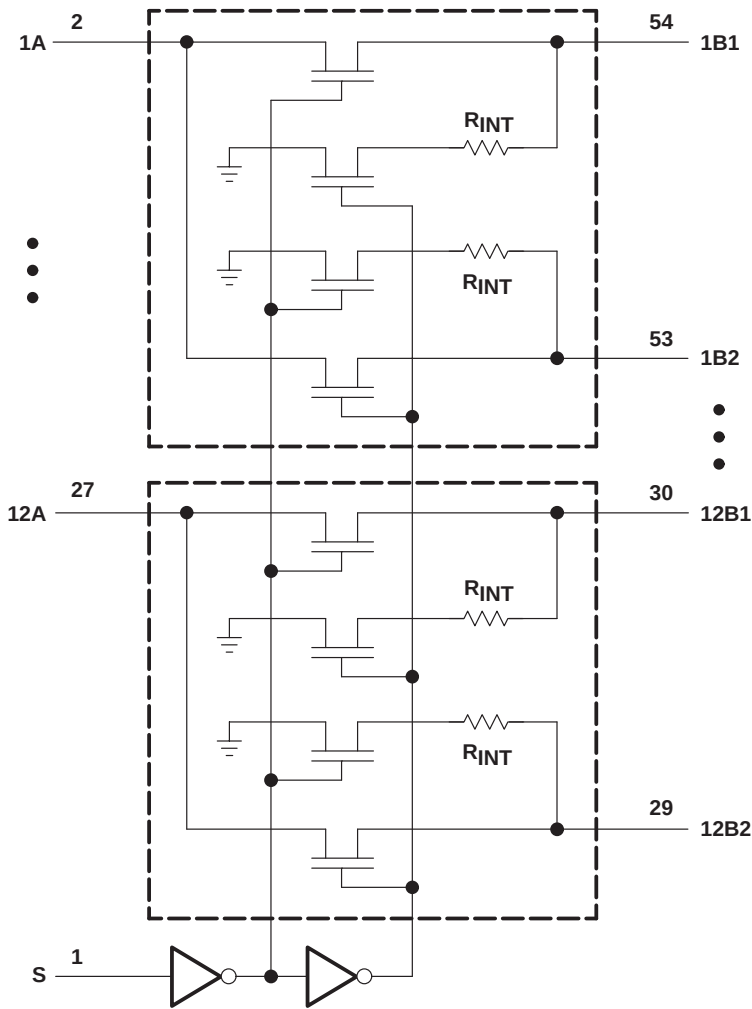
SN74CBT16292
12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER
WITH INTERNAL PULLDOWN RESISTORS

SCDS053E – MARCH 1998 – REVISED OCTOBER 2000

FUNCTION TABLE

INPUT S	FUNCTION
L	A port = B1 port R _{INT} = B2 port
H	A port = B2 port R _{INT} = B1 port

logic diagram (positive logic)



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12-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER
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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\dagger$	A or B	B or A		0.5		0.25	ns
t_{en}	S	A or B		6.8	1	6	ns
t_{dis}	S	A or B		7	1	6.3	ns

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

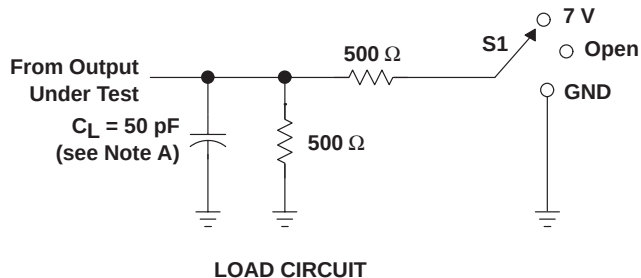
PARAMETER	DESCRIPTION	$V_{CC} = 4$ V		$V_{CC} = 5$ V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	
$t_{mbb}^\ddagger$	Make-before-break time	0	2	0	2	ns

[‡] The make-before-break time is the time interval between make and break, during the transition from one selected port to the other.

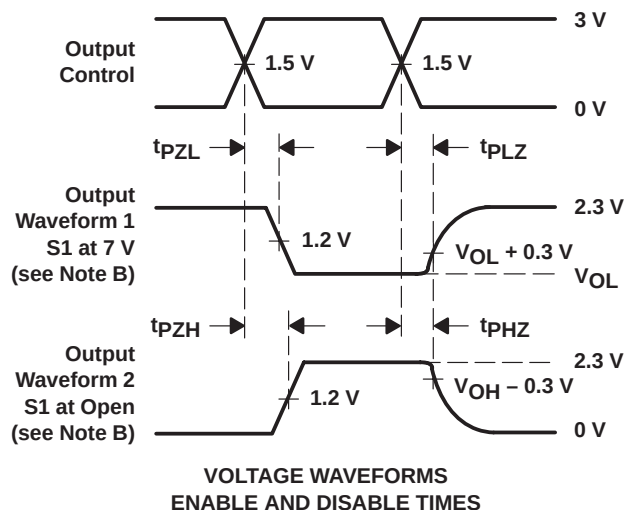
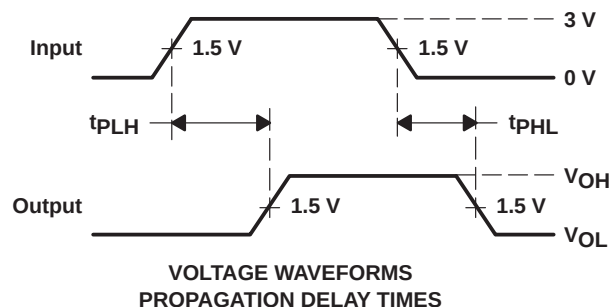
SN74CBT16292
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PZL}/t_{PLZ}	7 V
t_{PZH}/t_{PHZ}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when connected to the internal 500- Ω pulldown resistor. Waveform 2 is for an output with internal conditions such that the output is high except when connected to the internal 500- Ω pulldown resistor.
 - All pulse inputs and DC inputs are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} . $Z = R_{INT} = 500 \Omega$
 - t_{PZL} and t_{PZH} are the same as t_{en} . $Z = R_{INT} = 500 \Omega$
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CBT16292DGGR	NRND	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292
SN74CBT16292DGGR.A	NRND	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292
SN74CBT16292DGVR	NRND	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY292
SN74CBT16292DGVR.A	NRND	Production	TVSOP (DGV) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY292
SN74CBT16292DL	NRND	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292
SN74CBT16292DL.A	NRND	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292
SN74CBT16292DLR	NRND	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292
SN74CBT16292DLR.A	NRND	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16292

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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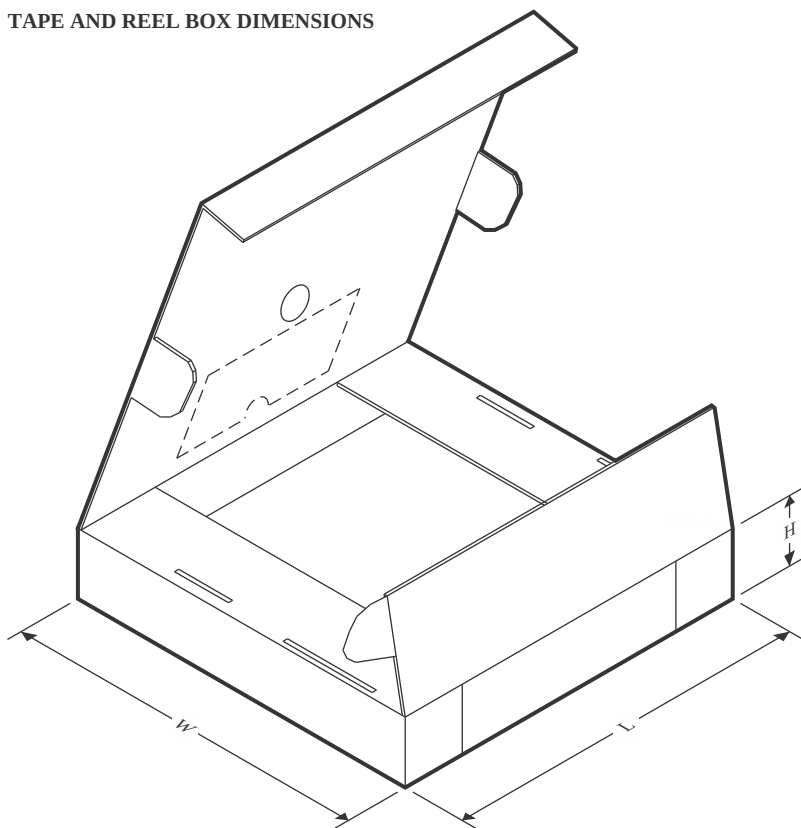
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16292DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74CBT16292DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74CBT16292DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16292DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74CBT16292DGVR	TVSOP	DGV	56	2000	367.0	367.0	45.0
SN74CBT16292DLR	SSOP	DL	56	1000	356.0	356.0	53.0

TUBE



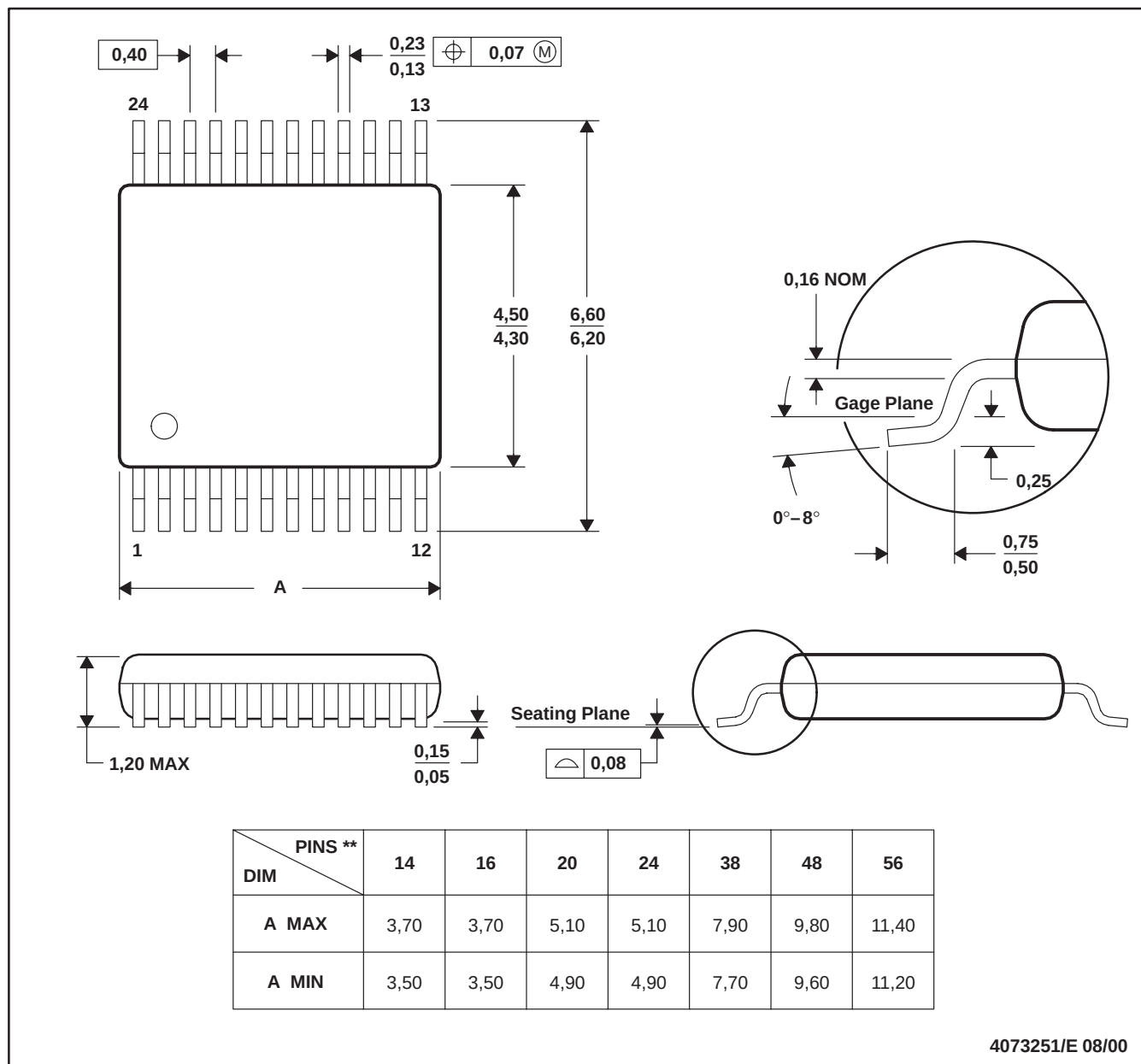
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT16292DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74CBT16292DL.A	DL	SSOP	56	20	473.7	14.24	5110	7.87

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



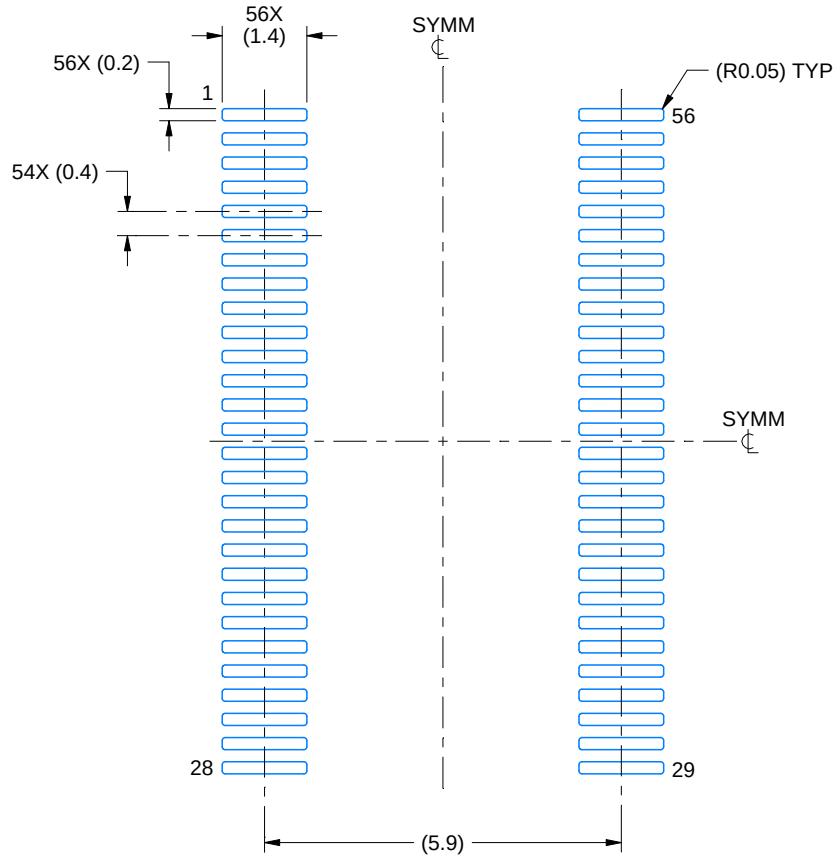
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-194.

EXAMPLE BOARD LAYOUT

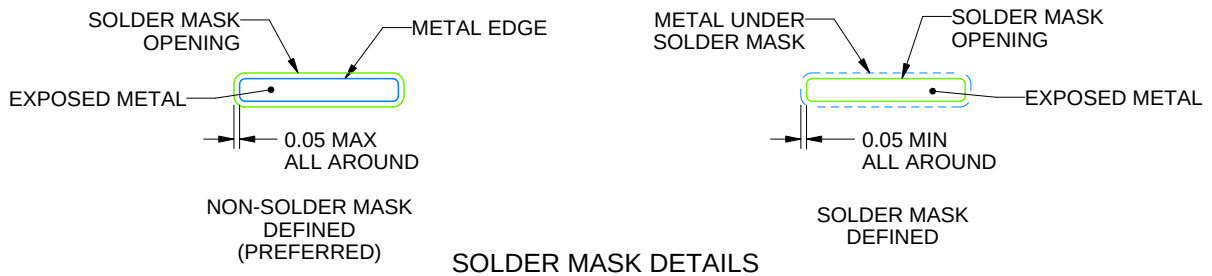
DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

4220240/B 12/2020

NOTES: (continued)

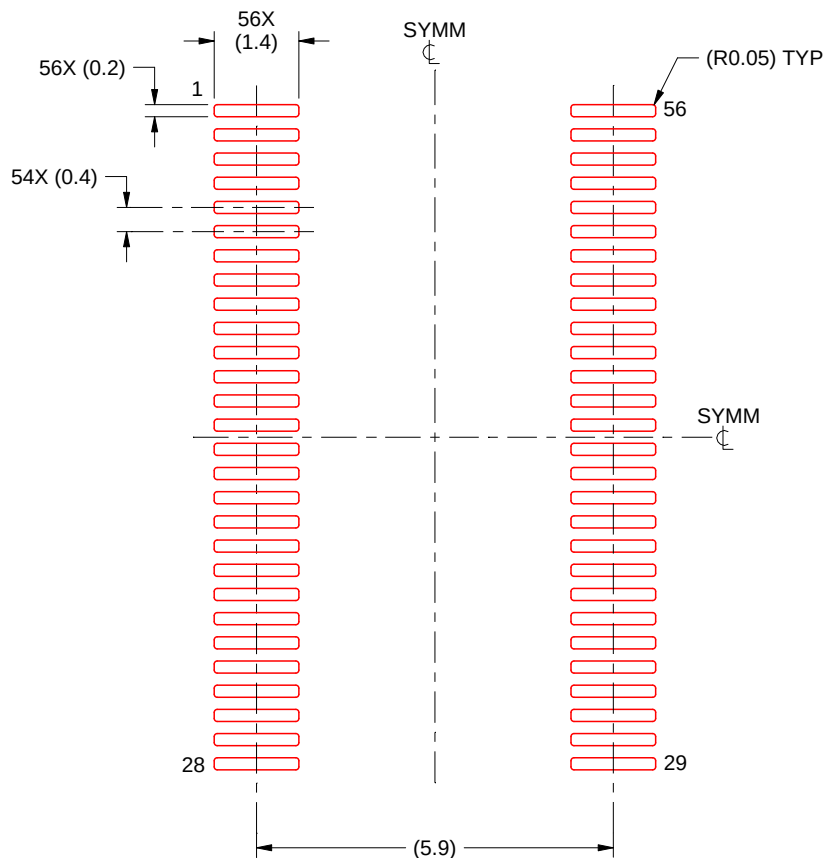
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

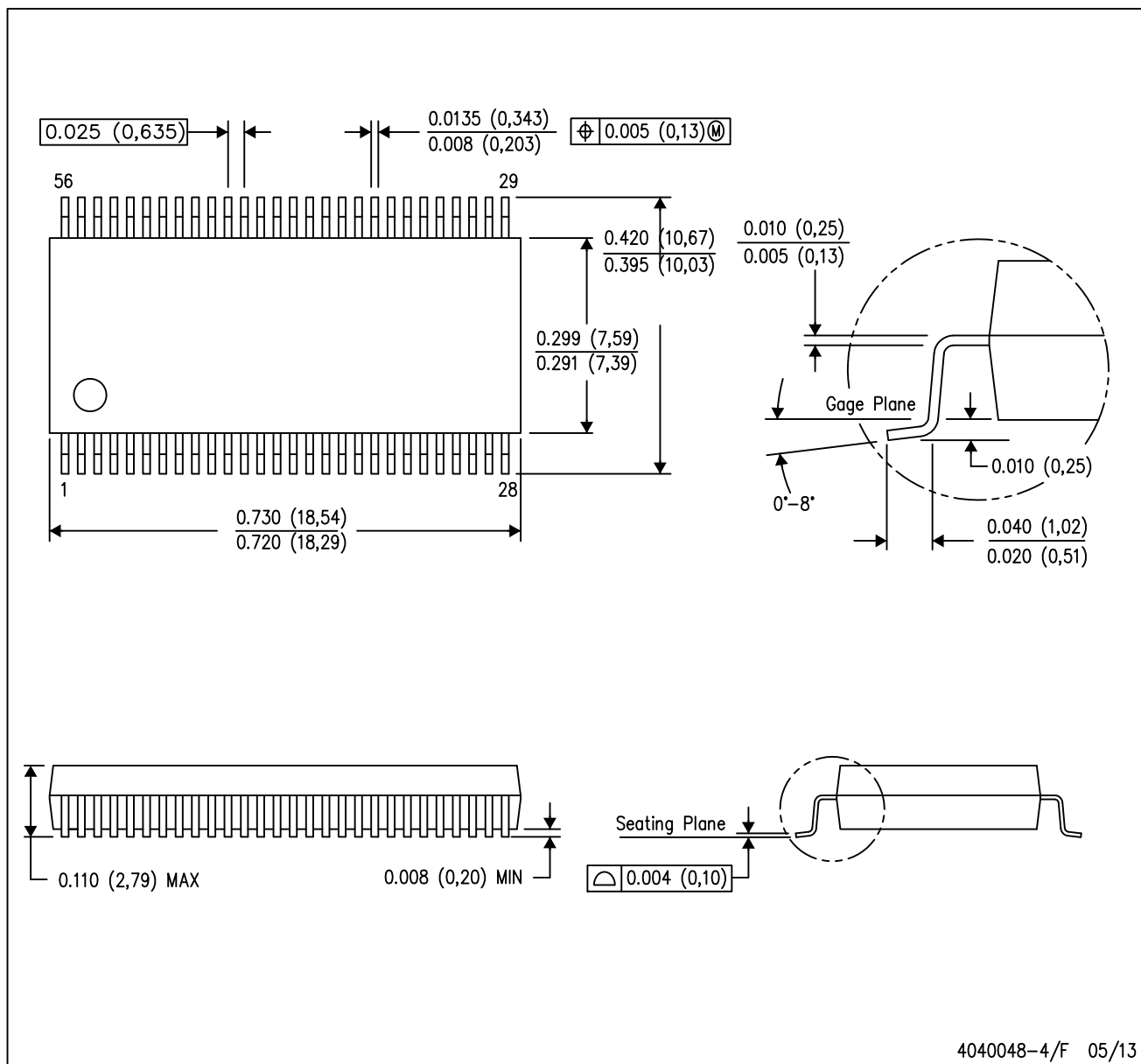
4220240/B 12/2020

NOTES: (continued)

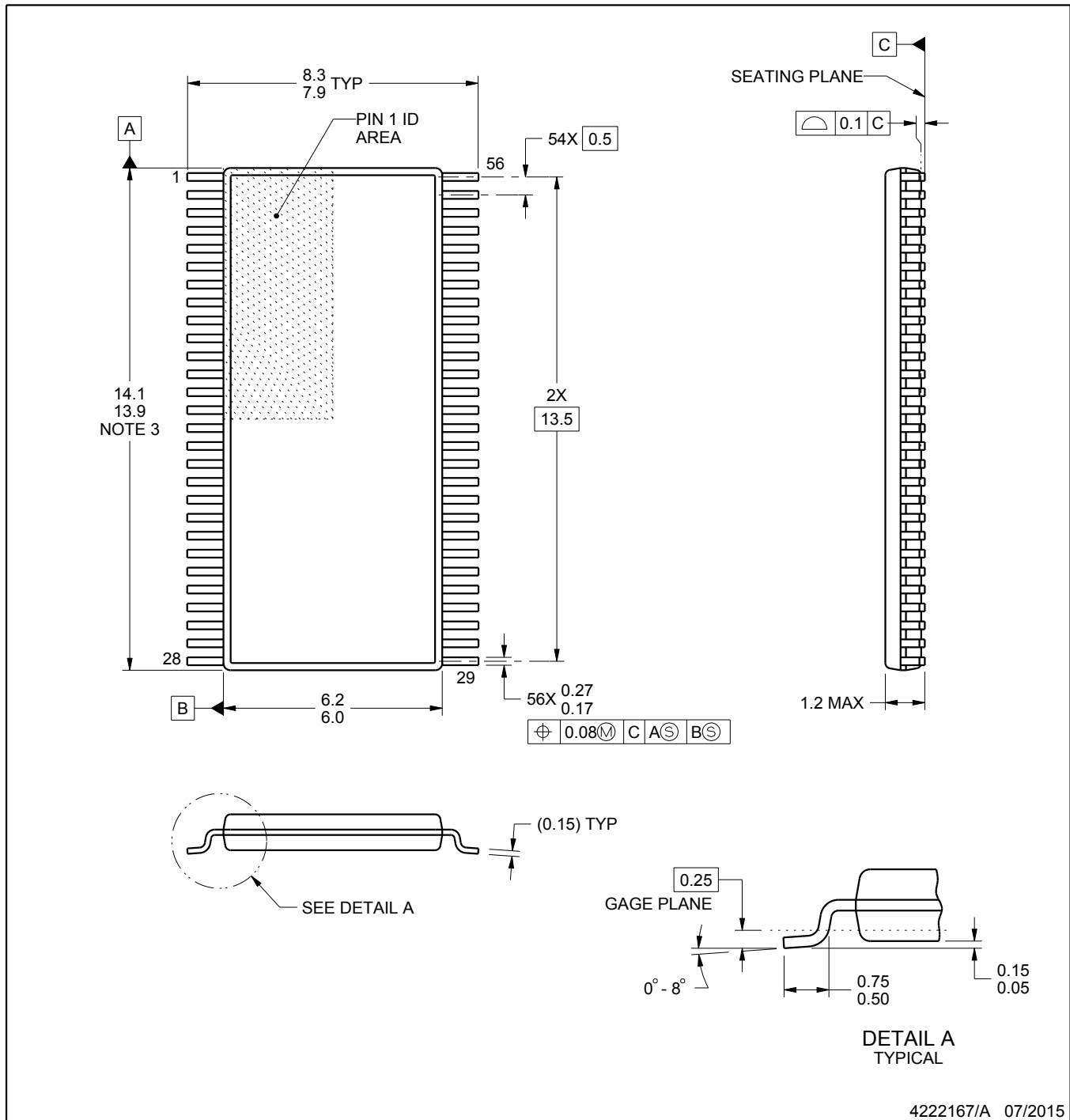
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118



4222167/A 07/2015

NOTES:

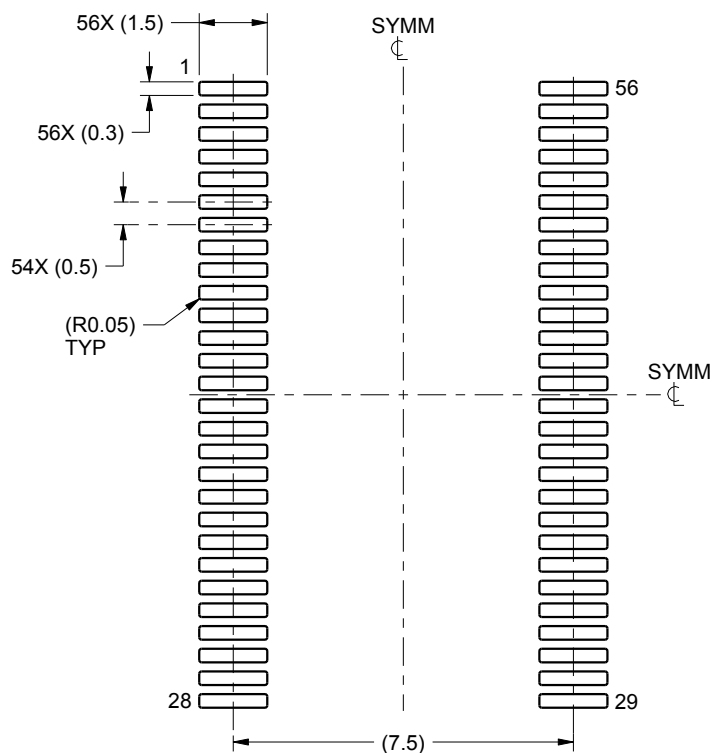
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

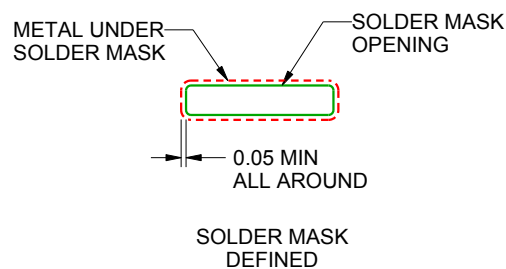
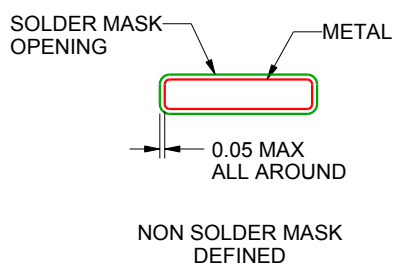
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

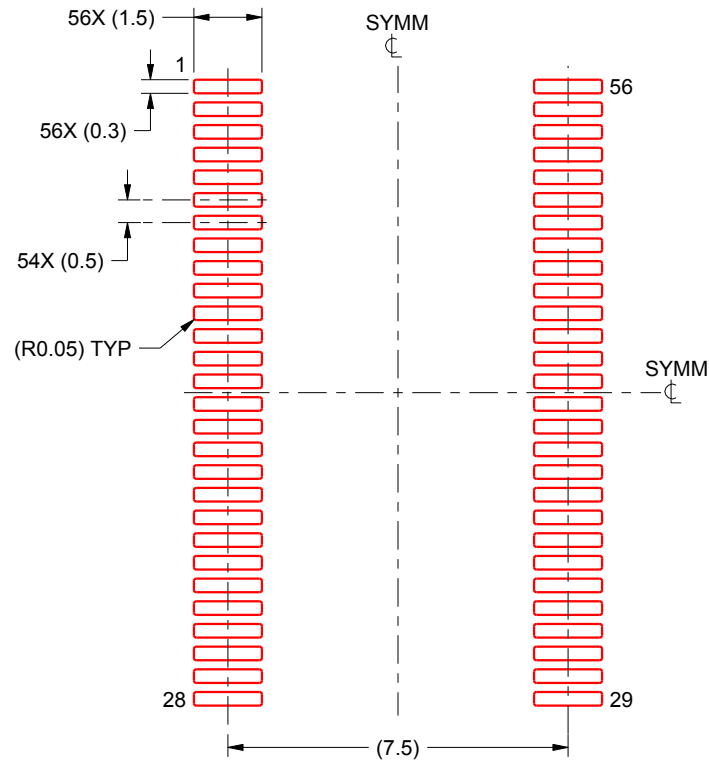
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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