# SN74AXC4T774 4-Bit Dual-Supply Bus Transceiver with Independent Direction Control, Configurable Voltage Translation, and Tri-State Outputs

## 1 Features

- Fully configurable dual-rail design allows each port to operate with a power supply range from 0.65 V to 3.6 V
- Operating temperature from –40°C to +125°C
- Independent direction control pins to allow configurable up and down translation
- Glitch-free power supply sequencing
- Up to 310 Mbps support when translating from 1.8 V to 3.3 V
- $V_{CC}$ isolation feature
  - If either $V_{CC}$ input is below 100 mV, all I/Os outputs are disabled and become high-impedance
- $I_{off}$ supports partial-power-down mode operation
- Compatible with AVC family level shifters
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 8000-V human-body model
  - 1000-V charged-device model

## 2 Applications

- Enterprise and communications
- Industrial
- Personal electronics
- Wireless infrastructure
- Building automation
- Point of sale

## 3 Description

The SN74AXC4T774 is a four-bit non-inverting bus transceiver that uses two individually configurable power-supply rails. The device is operational with both $V_{CCA}$ and $V_{CCB}$ supplies as low as 0.65 V. The A port is designed to track $V_{CCA}$, which accepts any supply voltage from 0.65 V to 3.6 V. The B port is designed to track $V_{CCB}$, which also accepts any supply voltage from 0.65 V to 3.6 V. Additionally the SN74AXC4T774 is compatible with a single-supply system.

The SN74AXC4T774 device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level of the direction-control inputs (DIRx). The output-enable input ($\overline{OE}$) is used to disable the outputs so the buses are effectively isolated. The SN74AXC4T774 device is designed so the control pins (DIRx and $\overline{OE}$) are referenced to $V_{CCA}$.

To put the level shifter I/Os in the high-impedance state during power up or power down, tie the $\overline{OE}$ pin to $V_{CCA}$ through a pullup resistor.

This device is fully specified for partial-power-down applications using the $I_{off}$ current. The $I_{off}$ protection circuitry is designed so that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specific voltage while the device is powered down.

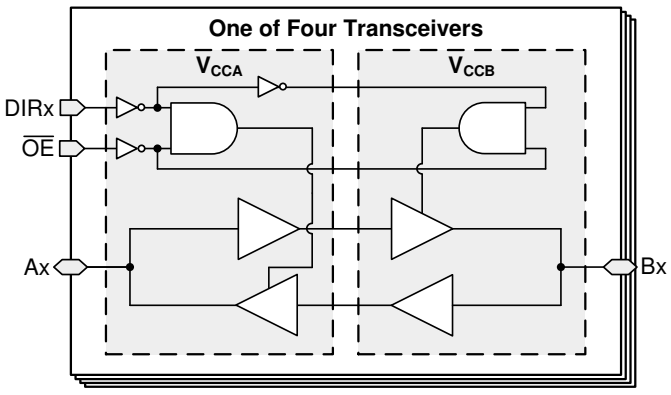
The $V_{CC}$ isolation feature is designed so that if either $V_{CCA}$ or $V_{CCB}$ is less than 100 mV, both I/O ports are set to the high-impedance state by disabling their outputs.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| SN74AXC4T774 | PW (TSSOP, 16) | 5mm × 6.4mm |
| | BQB (WQFN, 16) | 3.5mm × 2.5mm |
| | RSV (UQFN ,16) | 2.6mm × 1.8mm |

(1) For more information, see Section 11
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Functional Block Diagram**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Pin Configuration and Functions

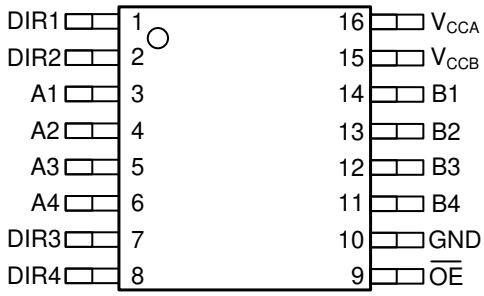



**Figure 4-1. PW Package, 16-Pin TSSOP (Top View)**

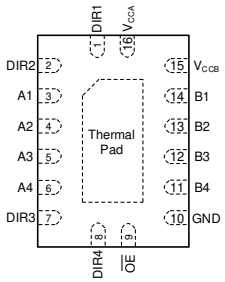



**Figure 4-2. BQB Package, 16-Pin WQFN (Transparent Top View)**

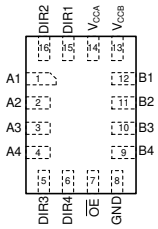



**Figure 4-3. RSV Package, 16-Pin UQFN (Transparent Top View)**

**Table 4-1. Pin Functions**

| PIN | | | | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PW | RSV | BQB | | |
| A1 | 3 | 1 | 3 | I/O | Input/output A1. Referenced to $V_{CCA}$. |
| A2 | 4 | 2 | 4 | I/O | Input/output A2. Referenced to $V_{CCA}$. |
| A3 | 5 | 3 | 5 | I/O | Input/output A3. Referenced to $V_{CCA}$. |
| A4 | 6 | 4 | 6 | I/O | Input/output A4. Referenced to $V_{CCA}$. |
| B1 | 14 | 12 | 14 | I/O | Input/output B1. Referenced to $V_{CCB}$. |
| B2 | 13 | 11 | 13 | I/O | Input/output B2. Referenced to $V_{CCB}$. |
| B3 | 12 | 10 | 12 | I/O | Input/output B3. Referenced to $V_{CCB}$. |
| B4 | 11 | 9 | 11 | I/O | Input/output B4. Referenced to $V_{CCB}$. |
| DIR1 | 1 | 15 | 1 | I | Direction-control input for port 1. Referenced to $V_{CCA}$. |
| DIR2 | 2 | 16 | 2 | I | Direction-control input for port 2. Referenced to $V_{CCA}$. |
| DIR3 | 7 | 5 | 7 | I | Direction-control input for port 3. Referenced to $V_{CCA}$. |
| DIR4 | 8 | 6 | 8 | I | Direction-control input for port 4. Referenced to $V_{CCA}$. |
| $\overline{OE}$ | 9 | 7 | 9 | I | Tri-state output enable. Pull $\overline{OE}$ high to place all outputs in tri-state mode. Referenced to $V_{CCA}$. |
| GND | 10 | 8 | 10 | — | Ground |
| $V_{CCA}$ | 16 | 14 | 16 | — | A-port power supply voltage. 0.65 V ≤ $V_{CCA}$ ≤ 3.6 V |
| $V_{CCB}$ | 15 | 13 | 15 | — | B-port power supply voltage. 0.65 V ≤ $V_{CCB}$ ≤ 3.6 V |

(1) I = input, O = output

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage A | | –0.5 | 4.2 | V |
| $V_{CCB}$ | Supply voltage B | | –0.5 | 4.2 | V |
| $V_I$ | Input Voltage(2) | I/O Ports (A Port) | –0.5 | 4.2 | V |
| | | I/O Ports (B Port) | –0.5 | 4.2 | |
| | | Control Inputs | –0.5 | 4.2 | |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state(2) | A Port | –0.5 | 4.2 | V |
| | | B Port | –0.5 | 4.2 | |
| $V_O$ | Voltage applied to any output in the high or low state(2) (3) | A Port | –0.5 | $V_{CCA}$ + 0.2 | V |
| | | B Port | –0.5 | $V_{CCB}$ + 0.2 | |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | –50 | | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | –50 | | mA |
| $I_O$ | Continuous output current | | –50 | 50 | mA |
| | Continuous current through $V_{CC}$ or GND | | –100 | 100 | mA |
| $T_j$ | Junction Temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±8000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.


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## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) 2

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage A | | | 0.65 | 3.6 | V |
| $V_{CCB}$ | Supply voltage B | | | 0.65 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | Data Inputs | $V_{CCI}$ = 0.65 V - 0.75 V | $V_{CCI}$ x 0.70 | | |
| | | | $V_{CCI}$ = 0.76 V - 1 V | $V_{CCI}$ x 0.70 | | |
| | | | $V_{CCI}$ = 1.1 V - 1.95 V | $V_{CCI}$ x 0.65 | | |
| | | | $V_{CCI}$ = 2.3 V - 2.7 V | 1.6 | | |
| | | | $V_{CCI}$ = 3 V - 3.6 V | 2 | | |
| | | Control Inputs(DIRx, $\overline{OE}$), Referenced to $V_{CCA}$ | $V_{CCA}$ = 0.65 V - 0.75 V | $V_{CCA}$ x 0.70 | | |
| | | | $V_{CCA}$ = 0.76 V - 1 V | $V_{CCA}$ x 0.70 | | |
| | | | $V_{CCA}$ = 1.1 V - 1.95 V | $V_{CCA}$ x 0.65 | | |
| | | | $V_{CCA}$ = 2.3 V - 2.7 V | 1.6 | | |
| | | | $V_{CCA}$ = 3 V - 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | Data Inputs | $V_{CCI}$ = 0.65 V - 0.75 V | | $V_{CCI}$ x 0.30 | V |
| | | | $V_{CCI}$ = 0.76 V - 1 V | | $V_{CCI}$ x 0.30 | |
| | | | $V_{CCI}$ = 1.1 V - 1.95 V | | $V_{CCI}$ x 0.35 | |
| | | | $V_{CCI}$ = 2.3 V - 2.7 V | | 0.7 | |
| | | | $V_{CCI}$ = 3 V - 3.6 V | | 0.8 | |
| | | Control Inputs(DIRx, $\overline{OE}$), Referenced to $V_{CCA}$ | $V_{CCA}$ = 0.65 V - 0.75 V | | $V_{CCA}$ x 0.30 | |
| | | | $V_{CCA}$ = 0.76 V - 1 V | | $V_{CCA}$ x 0.30 | |
| | | | $V_{CCA}$ = 1.1 V - 1.95 V | | $V_{CCA}$ x 0.35 | |
| | | | $V_{CCA}$ = 2.3 V - 2.7 V | | 0.7 | |
| | | | $V_{CCA}$ = 3 V - 3.6 V | | 0.8 | |
| $V_I$ | Input voltage 1 | | | 0 | 3.6 | V |
| $V_O$ | Output voltage | Active State | | 0 | $V_{CCO}$ | V |
| | | Tri-State | | 0 | 3.6 | |
| $\Delta t/\Delta v$2 | Input transition rise and fall time | | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | | –40 | 125 | °C |

(1) $V_{CCI}$ is the $V_{CC}$ associated with the input port.$V_{CCO}$ is the $V_{CC}$ associated with the output port.
(2) All unused inputs of the device must be held at $V_{CC}$ or GND for proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.

## 5.4 Thermal Information

| THERMAL METRIC(1) | | SN74AXC4T774 | | | UNIT |
|---|---|---|---|---|---|
| | | PW (TSSOP) | RSV (UQFN) | BQB (WQFN) | |
| | | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 118.2 | 130.8 | 73.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 48.6 | 69.1 | 70.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 64.5 | 59.9 | 43.5 | °C/W |
| $Y_{JT}$ | Junction-to-top characterization parameter | 7.3 | 3.9 | 4.9 | °C/W |
| $Y_{JB}$ | Junction-to-board characterization parameter | 63.9 | 58.3 | 43.5 | °C/W |
| $R_{\theta JC(bottom)}$ | Junction-to-case (bottom) thermal resistance | NA | NA | 21.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1) (2)

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | $V_{CCB}$ | Operating free-air temperature ($T_A$) | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | -40°C to 85°C | | -40°C to 125°C | | |
| | | | | | | MIN TYP(4) | MAX | MIN TYP(4) | MAX | |
| $V_{OH}$ | High-level output voltage | $V_I = V_{IH}$ | $I_{OH}$ = -100 µA | 0.7 V - 3.6 V | 0.7 V - 3.6 V | $V_{CCO}$ – 0.1 | | $V_{CCO}$ – 0.1 | | V |
| | | | $I_{OH}$ = -50 µA | 0.65 V | 0.65 V | 0.55 | | 0.55 | | |
| | | | $I_{OH}$ = -200 µA | 0.76 V | 0.76 V | 0.58 | | 0.58 | | |
| | | | $I_{OH}$ = -500 µA | 0.85 V | 0.85 V | 0.65 | | 0.65 | | |
| | | | $I_{OH}$ = -3 mA | 1.1 V | 1.1 V | 0.85 | | 0.85 | | |
| | | | $I_{OH}$ = -6 mA | 1.4 V | 1.4 V | 1.05 | | 1.05 | | |
| | | | $I_{OH}$ = -8 mA | 1.65 V | 1.65 V | 1.2 | | 1.2 | | |
| | | | $I_{OH}$ = -9 mA | 2.3 V | 2.3 V | 1.75 | | 1.75 | | |
| | | | $I_{OH}$ = -12 mA | 3 V | 3 V | 2.3 | | 2.3 | | |
| $V_{OL}$ | Low-level output voltage | $V_I = V_{IL}$ | $I_{OL}$ = 100 µA | 0.7 V - 3.6 V | 0.7 V - 3.6 V | | 0.1 | | 0.1 | V |
| | | | $I_{OL}$ = 50 µA | 0.65 V | 0.65 V | | 0.1 | | 0.1 | |
| | | | $I_{OL}$ = 200 µA | 0.76 V | 0.76 V | | 0.18 | | 0.18 | |
| | | | $I_{OL}$ = 500 µA | 0.85 V | 0.85 V | | 0.2 | | 0.2 | |
| | | | $I_{OL}$ = 3 mA | 1.1 V | 1.1 V | | 0.25 | | 0.25 | |
| | | | $I_{OL}$ = 6 mA | 1.4 V | 1.4 V | | 0.35 | | 0.35 | |
| | | | $I_{OL}$ = 8 mA | 1.65 V | 1.65 V | | 0.45 | | 0.45 | |
| | | | $I_{OL}$ = 9 mA | 2.3 V | 2.3 V | | 0.55 | | 0.55 | |
| | | | $I_{OL}$ = 12 mA | 3 V | 3 V | | 0.7 | | 0.7 | |
| $I_I$ | Input leakage current | Control inputs (DIRx, $\overline{OE}$):$V_I$ = $V_{CCA}$ or GND | | 0.65 V- 3.6 V | 0.65 V- 3.6 V | –0.5 | 0.5 | –1 | 1 | µA |
| | | Data Inputs (Ax, Bx),$V_I$ = $V_{CCI}$ or GND | | 0.65 V- 3.6 V | 0.65 V- 3.6 V | –4 | 4 | –8 | 8 | µA |
| $I_{off}$ | Partial power down current | A Port: $V_I$ or $V_O$ = 0 V - 3.6 V | | 0 V | 0 V - 3.6 V | –4 | 4 | –8 | 8 | µA |
| | | B Port: $V_I$ or $V_O$ = 0 V - 3.6 V | | 0 V - 3.6 V | 0 V | –4 | 4 | –8 | 8 | |
| $I_{OZ}$ | Tri-state output current (3) | A or B Port, $V_I$ = $V_{CCI}$ or GND, $V_O$ = $V_{CCO}$ or GND, $\overline{OE}$ = $V_{IH}$ | | 3.6 V | 3.6 V | –4 | 4 | –8 | 8 | µA |
| $I_{CCA}$ | $V_{CCA}$ supply current | $V_I$ = $V_{CCI}$ or GND | $I_O$ = 0 | 0.65 V- 3.6 V | 0.65 V- 3.6 V | | 15 | | 27 | µA |
| | | | | 0 V | 3.6 V | –2 | | –12 | | |
| | | | | 3.6 V | 0 V | | 10 | | 18 | |
| $I_{CCB}$ | $V_{CCB}$ supply current | $V_I$ = $V_{CCI}$ or GND | $I_O$ = 0 | 0.65 V- 3.6 V | 0.65 V- 3.6 V | | 15 | | 27 | µA |
| | | | | 0 V | 3.6 V | | 10 | | 18 | |
| | | | | 3.6 V | 0 V | –2 | | –12 | | |
| $I_{CCA}$ + $I_{CCB}$ | Combined supply current | $V_I$ = $V_{CCI}$ or GND | $I_O$ = 0 | 0.65 V- 3.6 V | 0.65 V- 3.6 V | | 21 | | 40 | µA |
| $C_i$ | Control Input Capacitance | $V_I$ = 3.3 V or GND | | 3.3 V | 3.3 V | 4.5 | | 4.5 | | pF |
| $C_{io}$ | Data I/O Capacitance | $\overline{OE}$ = $V_{CCA}$, $V_O$ = 1.65V DC +1 MHz -16 dBm sine wave | | 3.3 V | 3.3 V | 6.5 | | 6.5 | | pF |

(1) $V_{CCI}$ is the $V_{CC}$ associated with the input port.
(2) $V_{CCO}$ is the $V_{CC}$ associated with the output port.
(3) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(4) All typical data is taken at 25°C.


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## 5.6 Switching Characteristics, $V_{CCA}$ = 0.7 ± 0.05 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

| PARAMETER | | FROM | TO | Test Conditions | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0.7 ± 0.05 V | | 0.8 ± 0.04 V | | 0.9 ± 0.045 V | | 1.2 ± 0.1 V | | 1.5 ± 0.1 V | | 1.8 ± 0.15 V | | 2.5 ± 0.2 V | | 3.3 ± 0.3 V | | |
| | | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Propagation delay | A | B | -40°C to 85°C | 0.5 | 172 | 0.5 | 120 | 0.5 | 88 | 0.5 | 51 | 0.5 | 46 | 0.5 | 56 | 0.5 | 78 | 0.5 | 221 | ns |
| | | | | -40°C to 125°C | 0.5 | 172 | 0.5 | 120 | 0.5 | 88 | 0.5 | 51 | 0.5 | 46 | 0.5 | 56 | 0.5 | 78 | 0.5 | 221 | |
| | | B | A | -40°C to 85°C | 0.5 | 172 | 0.5 | 141 | 0.5 | 109 | 0.5 | 51 | 0.5 | 16 | 0.5 | 12 | 0.5 | 9 | 0.5 | 9 | |
| | | | | -40°C to 125°C | 0.5 | 172 | 0.5 | 141 | 0.5 | 109 | 0.5 | 51 | 0.5 | 16 | 0.5 | 12 | 0.5 | 9 | 0.5 | 9 | |
| $t_{dis}$ | Disable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | ns |
| | | | | -40°C to 125°C | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | 0.5 | 205 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 189 | 0.5 | 161 | 0.5 | 145 | 0.5 | 102 | 0.5 | 99 | 0.5 | 102 | 0.5 | 113 | 0.5 | 176 | |
| | | | | -40°C to 125°C | 0.5 | 189 | 0.5 | 161 | 0.5 | 145 | 0.5 | 102 | 0.5 | 99 | 0.5 | 102 | 0.5 | 113 | 0.5 | 176 | |
| $t_{en}$ | Enable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | ns |
| | | | | -40°C to 125°C | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | 0.5 | 287 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 309 | 0.5 | 219 | 0.5 | 177 | 0.5 | 133 | 0.5 | 127 | 0.5 | 132 | 0.5 | 165 | 0.5 | 418 | |
| | | | | -40°C to 125°C | 0.5 | 309 | 0.5 | 219 | 0.5 | 177 | 0.5 | 133 | 0.5 | 127 | 0.5 | 132 | 0.5 | 165 | 0.5 | 418 | |

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## 5.7 Switching Characteristics, $V_{CCA}$ = 0.8 ± 0.04 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

| PARAMETER | | FROM | TO | Test Conditions | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0.7 ± 0.05 V | | 0.8 ± 0.04 V | | 0.9 ± 0.045 V | | 1.2 ± 0.1 V | | 1.5 ± 0.1 V | | 1.8 ± 0.15 V | | 2.5 ± 0.2 V | | 3.3 ± 0.3 V | | |
| | | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Propagation delay | A | B | -40°C to 85°C | 0.5 | 141 | 0.5 | 96 | 0.5 | 73 | 0.5 | 39 | 0.5 | 29 | 0.5 | 28 | 0.5 | 29 | 0.5 | 40 | ns |
| | | | | -40°C to 125°C | 0.5 | 141 | 0.5 | 96 | 0.5 | 73 | 0.5 | 39 | 0.5 | 29 | 0.5 | 28 | 0.5 | 29 | 0.5 | 40 | |
| | | B | A | -40°C to 85°C | 0.5 | 120 | 0.5 | 96 | 0.5 | 76 | 0.5 | 39 | 0.5 | 16 | 0.5 | 11 | 0.5 | 9 | 0.5 | 9 | |
| | | | | -40°C to 125°C | 0.5 | 120 | 0.5 | 96 | 0.5 | 76 | 0.5 | 39 | 0.5 | 16 | 0.5 | 12 | 0.5 | 9 | 0.5 | 9 | |
| $t_{dis}$ | Disable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | ns |
| | | | | -40°C to 125°C | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | 0.5 | 114 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 156 | 0.5 | 131 | 0.5 | 116 | 0.5 | 71 | 0.5 | 67 | 0.5 | 68 | 0.5 | 70 | 0.5 | 84 | |
| | | | | -40°C to 125°C | 0.5 | 156 | 0.5 | 131 | 0.5 | 116 | 0.5 | 71 | 0.5 | 67 | 0.5 | 68 | 0.5 | 70 | 0.5 | 84 | |
| $t_{en}$ | Enable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | ns |
| | | | | -40°C to 125°C | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | 0.5 | 161 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 258 | 0.5 | 174 | 0.5 | 137 | 0.5 | 90 | 0.5 | 73 | 0.5 | 71 | 0.5 | 77 | 0.5 | 106 | |
| | | | | -40°C to 125°C | 0.5 | 258 | 0.5 | 174 | 0.5 | 137 | 0.5 | 90 | 0.5 | 73 | 0.5 | 71 | 0.5 | 77 | 0.5 | 106 | |


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## 5.8 Switching Characteristics, $V_{CCA}$ = 0.9 ± 0.045 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

| PARAMETER | | FROM | TO | Test Conditions | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0.7 ± 0.05 V | | 0.8 ± 0.04 V | | 0.9 ± 0.045 V | | 1.2 ± 0.1 V | | 1.5 ± 0.1 V | | 1.8 ± 0.15 V | | 2.5 ± 0.2 V | | 3.3 ± 0.3 V | | |
| | | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Propagation delay | A | B | -40°C to 85°C | 0.5 | 109 | 0.5 | 76 | 0.5 | 60 | 0.5 | 33 | 0.5 | 23 | 0.5 | 21 | 0.5 | 21 | 0.5 | 24 | ns |
| | | | | -40°C to 125°C | 0.5 | 109 | 0.5 | 76 | 0.5 | 60 | 0.5 | 33 | 0.5 | 23 | 0.5 | 21 | 0.5 | 21 | 0.5 | 24 | |
| | | B | A | -40°C to 85°C | 0.5 | 88 | 0.5 | 73 | 0.5 | 60 | 0.5 | 33 | 0.5 | 16 | 0.5 | 11 | 0.5 | 9 | 0.5 | 9 | |
| | | | | -40°C to 125°C | 0.5 | 88 | 0.5 | 73 | 0.5 | 60 | 0.5 | 33 | 0.5 | 16 | 0.5 | 12 | 0.5 | 9 | 0.5 | 9 | |
| $t_{dis}$ | Disable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | ns |
| | | | | -40°C to 125°C | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | 0.5 | 83 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 138 | 0.5 | 112 | 0.5 | 97 | 0.5 | 51 | 0.5 | 46 | 0.5 | 46 | 0.5 | 46 | 0.5 | 54 | |
| | | | | -40°C to 125°C | 0.5 | 138 | 0.5 | 112 | 0.5 | 97 | 0.5 | 51 | 0.5 | 46 | 0.5 | 46 | 0.5 | 46 | 0.5 | 54 | |
| $t_{en}$ | Enable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | ns |
| | | | | -40°C to 125°C | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | 0.5 | 94 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 203 | 0.5 | 140 | 0.5 | 110 | 0.5 | 70 | 0.5 | 52 | 0.5 | 45 | 0.5 | 43 | 0.5 | 51 | |
| | | | | -40°C to 125°C | 0.5 | 203 | 0.5 | 140 | 0.5 | 110 | 0.5 | 74 | 0.5 | 54 | 0.5 | 47 | 0.5 | 43 | 0.5 | 51 | |

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## 5.9 Switching Characteristics, $V_{CCA}$ = 1.2 ± 0.1 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

| PARAMETER | | FROM | TO | Test Conditions | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0.7 ± 0.05 V | | 0.8 ± 0.04 V | | 0.9 ± 0.045 V | | 1.2 ± 0.1 V | | 1.5 ± 0.1 V | | 1.8 ± 0.15 V | | 2.5 ± 0.2 V | | 3.3 ± 0.3 V | | |
| | | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Propagation delay | A | B | -40°C to 85°C | 0.5 | 50 | 0.5 | 39 | 0.5 | 33 | 0.5 | 20 | 0.5 | 14 | 0.5 | 12 | 0.5 | 10 | 0.5 | 12 | ns |
| | | | | -40°C to 125°C | 0.5 | 50 | 0.5 | 39 | 0.5 | 33 | 0.5 | 20 | 0.5 | 14 | 0.5 | 12 | 0.5 | 10 | 0.5 | 12 | |
| | | B | A | -40°C to 85°C | 0.5 | 51 | 0.5 | 39 | 0.5 | 33 | 0.5 | 20 | 0.5 | 15 | 0.5 | 11 | 0.5 | 8 | 0.5 | 7 | |
| | | | | -40°C to 125°C | 0.5 | 51 | 0.5 | 39 | 0.5 | 33 | 0.5 | 20 | 0.5 | 15 | 0.5 | 12 | 0.5 | 8 | 0.5 | 7 | |
| $t_{dis}$ | Disable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 28 | 0.5 | 28 | 0.5 | 28 | 0.5 | 28 | 0.5 | 28 | 0.5 | 28 | 0.5 | 28 | 0.5 | 28 | ns |
| | | | | -40°C to 125°C | 0.5 | 29 | 0.5 | 29 | 0.5 | 29 | 0.5 | 29 | 0.5 | 29 | 0.5 | 29 | 0.5 | 29 | 0.5 | 29 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 123 | 0.5 | 95 | 0.5 | 78 | 0.5 | 33 | 0.5 | 26 | 0.5 | 25 | 0.5 | 23 | 0.5 | 26 | |
| | | | | -40°C to 125°C | 0.5 | 124 | 0.5 | 95 | 0.5 | 79 | 0.5 | 34 | 0.5 | 27 | 0.5 | 26 | 0.5 | 24 | 0.5 | 26 | |
| $t_{en}$ | Enable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 39 | 0.5 | 39 | 0.5 | 39 | 0.5 | 39 | 0.5 | 39 | 0.5 | 39 | 0.5 | 39 | 0.5 | 39 | ns |
| | | | | -40°C to 125°C | 0.5 | 40 | 0.5 | 40 | 0.5 | 40 | 0.5 | 40 | 0.5 | 40 | 0.5 | 40 | 0.5 | 40 | 0.5 | 40 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 124 | 0.5 | 87 | 0.5 | 70 | 0.5 | 51 | 0.5 | 38 | 0.5 | 33 | 0.5 | 26 | 0.5 | 25 | |
| | | | | -40°C to 125°C | 0.5 | 124 | 0.5 | 87 | 0.5 | 70 | 0.5 | 55 | 0.5 | 42 | 0.5 | 36 | 0.5 | 28 | 0.5 | 26 | |


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## 5.10 Switching Characteristics, $V_{CCA}$ = 1.5 ± 0.1 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

| PARAMETER | | FROM | TO | Test Conditions | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0.7 ± 0.05 V | | 0.8 ± 0.04 V | | 0.9 ± 0.045 V | | 1.2 ± 0.1 V | | 1.5 ± 0.1 V | | 1.8 ± 0.15 V | | 2.5 ± 0.2 V | | 3.3 ± 0.3 V | | |
| | | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Propagation delay | A | B | -40°C to 85°C | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 15 | 0.5 | 11 | 0.5 | 10 | 0.5 | 8 | 0.5 | 10 | ns |
| | | | | -40°C to 125°C | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 15 | 0.5 | 11 | 0.5 | 10 | 0.5 | 8 | 0.5 | 10 | |
| | | B | A | -40°C to 85°C | 0.5 | 47 | 0.5 | 29 | 0.5 | 23 | 0.5 | 14 | 0.5 | 11 | 0.5 | 9 | 0.5 | 7 | 0.5 | 6 | |
| | | | | -40°C to 125°C | 0.5 | 47 | 0.5 | 29 | 0.5 | 23 | 0.5 | 14 | 0.5 | 11 | 0.5 | 9 | 0.5 | 7 | 0.5 | 6 | |
| $t_{dis}$ | Disable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | ns |
| | | | | -40°C to 125°C | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 120 | 0.5 | 91 | 0.5 | 74 | 0.5 | 29 | 0.5 | 22 | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | |
| | | | | -40°C to 125°C | 0.5 | 120 | 0.5 | 92 | 0.5 | 75 | 0.5 | 30 | 0.5 | 23 | 0.5 | 22 | 0.5 | 19 | 0.5 | 20 | |
| $t_{en}$ | Enable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 24 | 0.5 | 24 | 0.5 | 24 | 0.5 | 24 | 0.5 | 24 | 0.5 | 24 | 0.5 | 24 | 0.5 | 24 | ns |
| | | | | -40°C to 125°C | 0.5 | 25 | 0.5 | 25 | 0.5 | 25 | 0.5 | 25 | 0.5 | 25 | 0.5 | 25 | 0.5 | 25 | 0.5 | 25 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 28 | 0.5 | 29 | 0.5 | 33 | 0.5 | 41 | 0.5 | 31 | 0.5 | 27 | 0.5 | 22 | 0.5 | 19 | |
| | | | | -40°C to 125°C | 0.5 | 29 | 0.5 | 30 | 0.5 | 33 | 0.5 | 42 | 0.5 | 33 | 0.5 | 29 | 0.5 | 24 | 0.5 | 21 | |

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## 5.11 Switching Characteristics, $V_{CCA}$ = 1.8 ± 0.15 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

| PARAMETER | | FROM | TO | Test Conditions | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0.7 ± 0.05 V | | 0.8 ± 0.04 V | | 0.9 ± 0.045 V | | 1.2 ± 0.1 V | | 1.5 ± 0.1 V | | 1.8 ± 0.15 V | | 2.5 ± 0.2 V | | 3.3 ± 0.3 V | | |
| | | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Propagation delay | A | B | -40°C to 85°C | 0.5 | 12 | 0.5 | 11 | 0.5 | 11 | 0.5 | 11 | 0.5 | 9 | 0.5 | 8 | 0.5 | 7 | 0.5 | 7 | ns |
| | | | | -40°C to 125°C | 0.5 | 12 | 0.5 | 12 | 0.5 | 12 | 0.5 | 12 | 0.5 | 9 | 0.5 | 9 | 0.5 | 7 | 0.5 | 7 | |
| | | B | A | -40°C to 85°C | 0.5 | 56 | 0.5 | 28 | 0.5 | 21 | 0.5 | 12 | 0.5 | 10 | 0.5 | 8 | 0.5 | 6 | 0.5 | 5 | |
| | | | | -40°C to 125°C | 0.5 | 56 | 0.5 | 28 | 0.5 | 21 | 0.5 | 12 | 0.5 | 10 | 0.5 | 9 | 0.5 | 7 | 0.5 | 6 | |
| $t_{dis}$ | Disable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 17 | 0.5 | 17 | 0.5 | 17 | 0.5 | 17 | 0.5 | 17 | 0.5 | 17 | 0.5 | 17 | 0.5 | 17 | ns |
| | | | | -40°C to 125°C | 0.5 | 18 | 0.5 | 18 | 0.5 | 18 | 0.5 | 18 | 0.5 | 18 | 0.5 | 18 | 0.5 | 18 | 0.5 | 18 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 117 | 0.5 | 90 | 0.5 | 73 | 0.5 | 28 | 0.5 | 21 | 0.5 | 19 | 0.5 | 16 | 0.5 | 18 | |
| | | | | -40°C to 125°C | 0.5 | 119 | 0.5 | 90 | 0.5 | 74 | 0.5 | 29 | 0.5 | 22 | 0.5 | 20 | 0.5 | 17 | 0.5 | 18 | |
| $t_{en}$ | Enable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | 0.5 | 19 | ns |
| | | | | -40°C to 125°C | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | 0.5 | 20 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 21 | 0.5 | 20 | 0.5 | 20 | 0.5 | 32 | 0.5 | 27 | 0.5 | 24 | 0.5 | 20 | 0.5 | 18 | |
| | | | | -40°C to 125°C | 0.5 | 22 | 0.5 | 22 | 0.5 | 22 | 0.5 | 34 | 0.5 | 29 | 0.5 | 26 | 0.5 | 22 | 0.5 | 19 | |


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## 5.12 Switching Characteristics, $V_{CCA}$ = 2.5 ± 0.2 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

| PARAMETER | | FROM | TO | Test Conditions | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0.7 ± 0.05 V | | 0.8 ± 0.04 V | | 0.9 ± 0.045 V | | 1.2 ± 0.1 V | | 1.5 ± 0.1 V | | 1.8 ± 0.15 V | | 2.5 ± 0.2 V | | 3.3 ± 0.3 V | | |
| | | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Propagation delay | A | B | -40°C to 85°C | 0.5 | 10 | 0.5 | 10 | 0.5 | 9 | 0.5 | 8 | 0.5 | 7 | 0.5 | 6 | 0.5 | 6 | 0.5 | 6 | ns |
| | | | | -40°C to 125°C | 0.5 | 10 | 0.5 | 10 | 0.5 | 9 | 0.5 | 8 | 0.5 | 7 | 0.5 | 7 | 0.5 | 6 | 0.5 | 6 | |
| | | B | A | -40°C to 85°C | 0.5 | 78 | 0.5 | 30 | 0.5 | 21 | 0.5 | 10 | 0.5 | 8 | 0.5 | 7 | 0.5 | 6 | 0.5 | 5 | |
| | | | | -40°C to 125°C | 0.5 | 78 | 0.5 | 30 | 0.5 | 21 | 0.5 | 10 | 0.5 | 8 | 0.5 | 7 | 0.5 | 6 | 0.5 | 5 | |
| $t_{dis}$ | Disable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | ns |
| | | | | -40°C to 125°C | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 115 | 0.5 | 89 | 0.5 | 72 | 0.5 | 26 | 0.5 | 19 | 0.5 | 18 | 0.5 | 14 | 0.5 | 17 | |
| | | | | -40°C to 125°C | 0.5 | 117 | 0.5 | 89 | 0.5 | 72 | 0.5 | 28 | 0.5 | 21 | 0.5 | 19 | 0.5 | 15 | 0.5 | 17 | |
| $t_{en}$ | Enable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | 0.5 | 14 | ns |
| | | | | -40°C to 125°C | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 15 | 0.5 | 14 | 0.5 | 13 | 0.5 | 14 | 0.5 | 15 | 0.5 | 16 | 0.5 | 15 | 0.5 | 15 | |
| | | | | -40°C to 125°C | 0.5 | 16 | 0.5 | 15 | 0.5 | 15 | 0.5 | 16 | 0.5 | 17 | 0.5 | 18 | 0.5 | 17 | 0.5 | 16 | |

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## 5.13 Switching Characteristics, $V_{CCA}$ = 3.3 ± 0.3 V

See Figure 5 and Table 1 for test circuit and loading. See Figure 6, Figure 7, and Figure 8 for measurement waveforms.

| PARAMETER | | FROM | TO | Test Conditions | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 0.7 ± 0.05 V | | 0.8 ± 0.04 V | | 0.9 ± 0.045 V | | 1.2 ± 0.1 V | | 1.5 ± 0.1 V | | 1.8 ± 0.15 V | | 2.5 ± 0.2 V | | 3.3 ± 0.3 V | | |
| | | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | Propagation delay | A | B | -40°C to 85°C | 0.5 | 10 | 0.5 | 9 | 0.5 | 9 | 0.5 | 8 | 0.5 | 6 | 0.5 | 6 | 0.5 | 5 | 0.5 | 5 | ns |
| | | | | -40°C to 125°C | 0.5 | 10 | 0.5 | 9 | 0.5 | 9 | 0.5 | 8 | 0.5 | 6 | 0.5 | 6 | 0.5 | 5 | 0.5 | 5 | |
| | | B | A | -40°C to 85°C | 0.5 | 221 | 0.5 | 40 | 0.5 | 24 | 0.5 | 12 | 0.5 | 10 | 0.5 | 7 | 0.5 | 6 | 0.5 | 5 | |
| | | | | -40°C to 125°C | 0.5 | 221 | 0.5 | 40 | 0.5 | 24 | 0.5 | 12 | 0.5 | 10 | 0.5 | 7 | 0.5 | 6 | 0.5 | 5 | |
| $t_{dis}$ | Disable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | ns |
| | | | | -40°C to 125°C | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | 0.5 | 16 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 115 | 0.5 | 89 | 0.5 | 72 | 0.5 | 26 | 0.5 | 19 | 0.5 | 17 | 0.5 | 14 | 0.5 | 16 | |
| | | | | -40°C to 125°C | 0.5 | 117 | 0.5 | 89 | 0.5 | 72 | 0.5 | 27 | 0.5 | 20 | 0.5 | 18 | 0.5 | 14 | 0.5 | 16 | |
| $t_{en}$ | Enable time | $\overline{OE}$ | A | -40°C to 85°C | 0.5 | 12 | 0.5 | 12 | 0.5 | 12 | 0.5 | 12 | 0.5 | 12 | 0.5 | 12 | 0.5 | 12 | 0.5 | 12 | ns |
| | | | | -40°C to 125°C | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | |
| | | $\overline{OE}$ | B | -40°C to 85°C | 0.5 | 13 | 0.5 | 12 | 0.5 | 11 | 0.5 | 11 | 0.5 | 11 | 0.5 | 12 | 0.5 | 12 | 0.5 | 12 | |
| | | | | -40°C to 125°C | 0.5 | 14 | 0.5 | 12 | 0.5 | 12 | 0.5 | 12 | 0.5 | 12 | 0.5 | 13 | 0.5 | 13 | 0.5 | 13 | |


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## 5.14 Operating Characteristics: $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $C_{pdA}$ | Power Dissipation Capacitance per transceiver (A to B: outputs enabled) | $C_L$ = 0, $R_L$ = Open<br>f = 1 MHz<br>$t_{rise}$ = $t_{fall}$ = 1 ns | 0.7 V | 0.7 V | | 2.4 | | pF |
| | | | 0.8 V | 0.8 V | | 2.3 | | |
| | | | 0.9 V | 0.9 V | | 2.2 | | |
| | | | 1.2 V | 1.2 V | | 2.2 | | |
| | | | 1.5 V | 1.5 V | | 2.2 | | |
| | | | 1.8 V | 1.8 V | | 2.2 | | |
| | | | 2.5 V | 2.5 V | | 2.4 | | |
| | | | 3.3 V | 3.3 V | | 3.0 | | |
| | Power Dissipation Capacitance per transceiver (A to B: outputs disabled) | $C_L$ = 0, $R_L$ = Open<br>f = 1 MHz<br>$t_{rise}$ = $t_{fall}$ = 1 ns | 0.7 V | 0.7 V | | 1.5 | | pF |
| | | | 0.8 V | 0.8 V | | 1.5 | | |
| | | | 0.9 V | 0.9 V | | 1.5 | | |
| | | | 1.2 V | 1.2 V | | 1.5 | | |
| | | | 1.5 V | 1.5 V | | 1.5 | | |
| | | | 1.8 V | 1.8 V | | 1.5 | | |
| | | | 2.5 V | 2.5 V | | 1.6 | | |
| | | | 3.3 V | 3.3 V | | 2.0 | | |
| | Power Dissipation Capacitance per transceiver (B to A: outputs enabled) | $C_L$ = 0, $R_L$ = Open<br>f = 1 MHz<br>$t_{rise}$ = $t_{fall}$ = 1 ns | 0.7 V | 0.7 V | | 13.4 | | pF |
| | | | 0.8 V | 0.8 V | | 15.0 | | |
| | | | 0.9 V | 0.9 V | | 14.0 | | |
| | | | 1.2 V | 1.2 V | | 20.7 | | |
| | | | 1.5 V | 1.5 V | | 29.6 | | |
| | | | 1.8 V | 1.8 V | | 40.2 | | |
| | | | 2.5 V | 2.5 V | | 65.8 | | |
| | | | 3.3 V | 3.3 V | | 91.7 | | |
| | Power Dissipation Capacitance per transceiver (B to A: outputs disabled) | $C_L$ = 0, $R_L$ = Open<br>f = 1 MHz<br>$t_{rise}$ = $t_{fall}$ = 1 ns | 0.7 V | 0.7 V | | 1.3 | | pF |
| | | | 0.8 V | 0.8 V | | 1.1 | | |
| | | | 0.9 V | 0.9 V | | 1.1 | | |
| | | | 1.2 V | 1.2 V | | 1.0 | | |
| | | | 1.5 V | 1.5 V | | 1.0 | | |
| | | | 1.8 V | 1.8 V | | 1.0 | | |
| | | | 2.5 V | 2.5 V | | 1.0 | | |
| | | | 3.3 V | 3.3 V | | 1.0 | | |

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## 5.14 Operating Characteristics: $T_A$ = 25°C (continued)

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $C_{pdB}$ | Power Dissipation Capacitance per transceiver (A to B: outputs enabled) | $C_L$ = 0, $R_L$ = Open<br>f = 1 MHz<br>$t_{rise}$ = $t_{fall}$ = 1 ns | 0.7 V | 0.7 V | | 13.4 | | pF |
| | | | 0.8 V | 0.8 V | | 13.8 | | |
| | | | 0.9 V | 0.9 V | | 14.9 | | |
| | | | 1.2 V | 1.2 V | | 20.6 | | |
| | | | 1.5 V | 1.5 V | | 29.6 | | |
| | | | 1.8 V | 1.8 V | | 40.3 | | |
| | | | 2.5 V | 2.5 V | | 66.2 | | |
| | | | 3.3 V | 3.3 V | | 92.5 | | |
| | Power Dissipation Capacitance per transceiver (A to B: outputs disabled) | $C_L$ = 0, $R_L$ = Open<br>f = 1 MHz<br>$t_{rise}$ = $t_{fall}$ = 1 ns | 0.7 V | 0.7 V | | 1.3 | | pF |
| | | | 0.8 V | 0.8 V | | 1.2 | | |
| | | | 0.9 V | 0.9 V | | 1.1 | | |
| | | | 1.2 V | 1.2 V | | 1.1 | | |
| | | | 1.5 V | 1.5 V | | 1.1 | | |
| | | | 1.8 V | 1.8 V | | 1.1 | | |
| | | | 2.5 V | 2.5 V | | 1.1 | | |
| | | | 3.3 V | 3.3 V | | 1.1 | | |
| | Power Dissipation Capacitance per transceiver (B to A: outputs enabled) | $C_L$ = 0, $R_L$ = Open<br>f = 1 MHz<br>$t_{rise}$ = $t_{fall}$ = 1 ns | 0.7 V | 0.7 V | | 2.5 | | pF |
| | | | 0.8 V | 0.8 V | | 2.4 | | |
| | | | 0.9 V | 0.9 V | | 2.3 | | |
| | | | 1.2 V | 1.2 V | | 2.2 | | |
| | | | 1.5 V | 1.5 V | | 2.3 | | |
| | | | 1.8 V | 1.8 V | | 2.3 | | |
| | | | 2.5 V | 2.5 V | | 2.5 | | |
| | | | 3.3 V | 3.3 V | | 3.0 | | |
| | Power Dissipation Capacitance per transceiver (B to A: outputs disabled) | $C_L$ = 0, $R_L$ = Open<br>f = 1 MHz<br>$t_{rise}$ = $t_{fall}$ = 1 ns | 0.7 V | 0.7 V | | 1.6 | | pF |
| | | | 0.8 V | 0.8 V | | 1.5 | | |
| | | | 0.9 V | 0.9 V | | 1.5 | | |
| | | | 1.2 V | 1.2 V | | 1.5 | | |
| | | | 1.5 V | 1.5 V | | 1.5 | | |
| | | | 1.8 V | 1.8 V | | 1.5 | | |
| | | | 2.5 V | 2.5 V | | 1.6 | | |
| | | | 3.3 V | 3.3 V | | 2.0 | | |


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## 5.15 Typical Characteristics

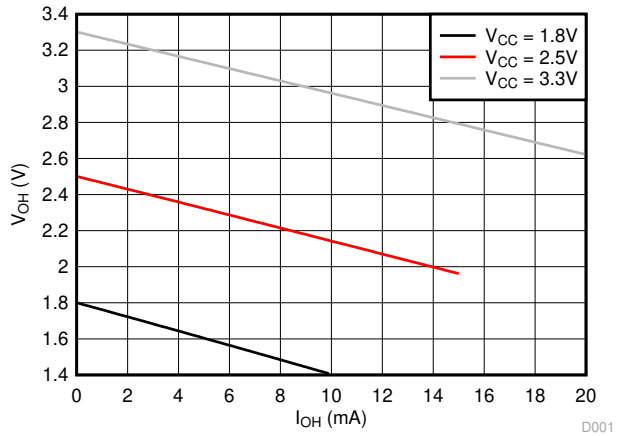



**Figure 5-1. Typical ($T_A$=25°C) Output High Voltage ($V_{OH}$) vs Source Current ($I_{OH}$)**

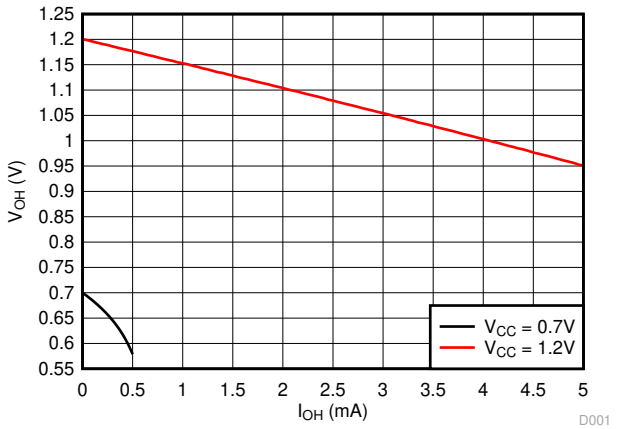



**Figure 5-2. Typical ($T_A$=25°C) Output High Voltage ($V_{OH}$) vs Source Current ($I_{OH}$)**

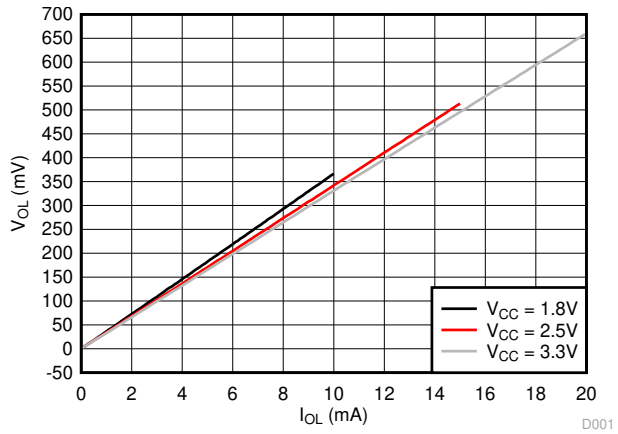



**Figure 5-3. Typical ($T_A$=25°C) Output High Voltage ($V_{OL}$) vs Sink Current ($I_{OL}$)**

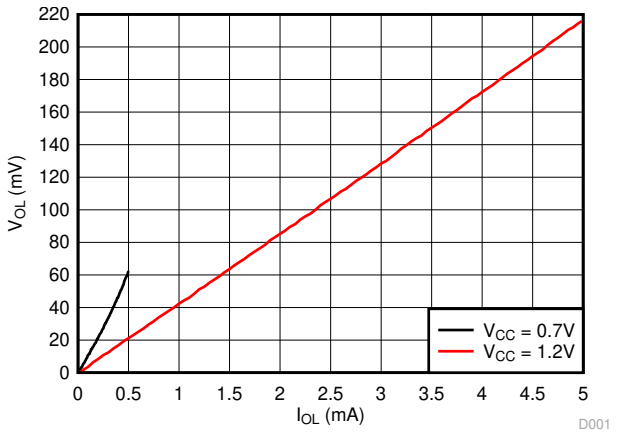



**Figure 5-4. Typical ($T_A$=25°C) Output High Voltage ($V_{OL}$) vs Sink Current ($I_{OL}$)**

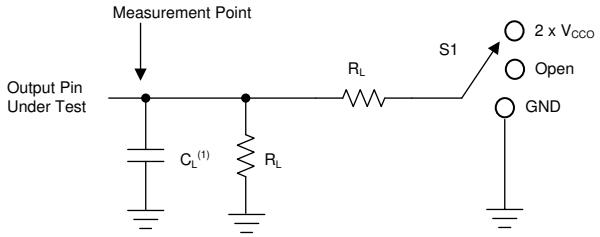
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# 6 Parameter Measurement Information

## 6.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1 MHz
- $Z_O$ = 50 Ω
- dv/dt ≤ 1 ns/V

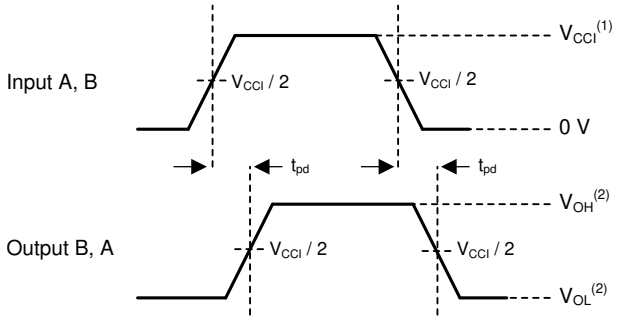



A. $C_L$ includes probe and jig capacitance.

**Figure 6-1. Load Circuit**

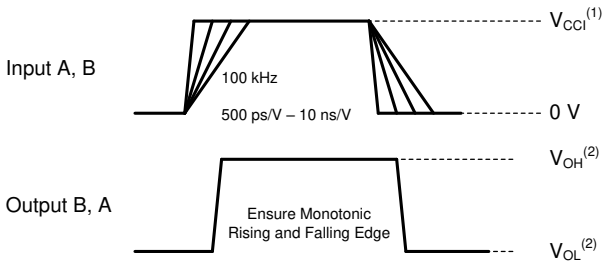
**Table 6-1. Load Circuit Conditions**

| Parameter | | $V_{CCO}$ | $R_L$ | $C_L$ | $S_1$ | $V_{TP}$ |
|---|---|---|---|---|---|---|
| Δt/Δv | Input transition rise or fall rate | 0.65 V – 3.6 V | 1 MΩ | 15 pF | Open | N/A |
| $t_{pd}$ | Propagation (delay) time | 1.1 V – 3.6 V | 2 kΩ | 15 pF | Open | N/A |
| | | 0.65 V – 0.95 V | 20 kΩ | 15 pF | Open | N/A |
| $t_{en}$, $t_{dis}$ | Enable time, disable time | 3 V – 3.6 V | 2 kΩ | 15 pF | 2 × $V_{CCO}$ | 0.3 V |
| | | 1.65 V – 2.7 V | 2 kΩ | 15 pF | 2 × $V_{CCO}$ | 0.15 V |
| | | 1.1 V – 1.6 V | 2 kΩ | 15 pF | 2 × $V_{CCO}$ | 0.1 V |
| | | 0.65 V – 0.95 V | 20 kΩ | 15 pF | 2 × $V_{CCO}$ | 0.1 V |
| $t_{en}$, $t_{dis}$ | Enable time, disable time | 3 V – 3.6 V | 2 kΩ | 15 pF | GND | 0.3 V |
| | | 1.65 V – 2.7 V | 2 kΩ | 15 pF | GND | 0.15 V |
| | | 1.1 V – 1.6 V | 2 kΩ | 15 pF | GND | 0.1 V |
| | | 0.65 V – 0.95 V | 20 kΩ | 15 pF | GND | 0.1 V |




1. $V_{CCI}$ is the supply pin associated with the input port.
2. $V_{OH}$ and $V_{OL}$ are typical output voltage levels that occur with specified $R_L$, $C_L$, and $S_1$

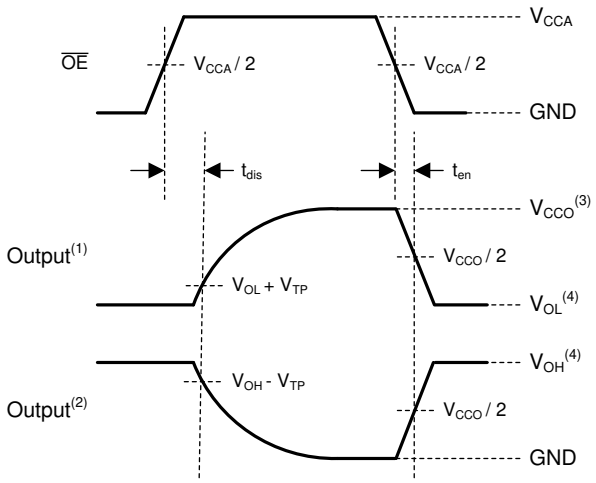
**Figure 6-2. Propagation Delay**




1. $V_{CCI}$ is the supply pin associated with the input port.
2. $V_{OH}$ and $V_{OL}$ are typical output voltage levels that occur with specified $R_L$, $C_L$, and $S_1$

**Figure 6-3. Input Transition Rise or Fall Rate**


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A. Output waveform on the condition that input is driven to a valid Logic Low.
B. Output waveform on the condition that input is driven to a valid Logic High.
C. $V_{CCO}$ is the supply pin associated with the output port.
D. $V_{OH}$ and $V_{OL}$ are typical output voltage levels with specified $R_L$, $C_L$, and $S_1$.

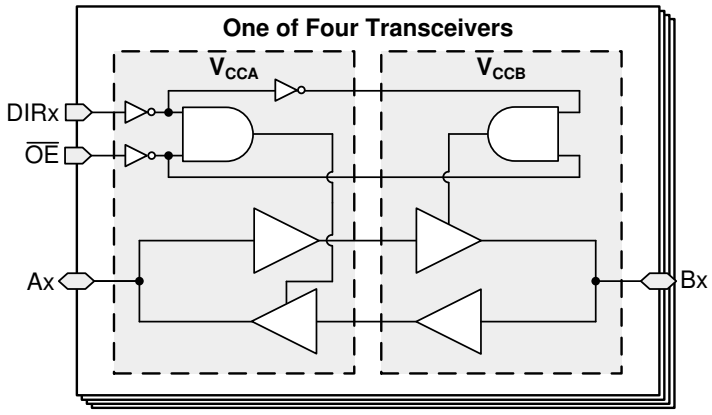
**Figure 6-4. Enable Time And Disable Time**

# 7 Detailed Description

## 7.1 Overview

The SN74AXC4T774 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (DIRx and $\overline{OE}$) are reference to $V_{CCA}$ logic levels, and Bx pins are referenced to $V_{CCB}$ logic levels. The A port is able to accept I/O voltages ranging from 0.65 V to 3.6 V, while the B port can accept I/O voltages from 0.65 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both Ax and Bx pins are in the high-impedance state. See *Device Functional Modes* for a summary of the operation of the control logic.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the Electrical Characteristics. The worst case resistance is calculated with the maximum input voltage, given in the Absolute Maximum Ratings, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

### 7.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

### 7.3.3 Partial Power Down ($I_{off}$)

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by $I_{off}$ in the Electrical Characteristics.

### 7.3.4 $V_{CC}$ Isolation

The inputs and outputs for this device enter a high-impedance state when either supply is <100mV.

### 7.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.


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### 7.3.6 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low). Glitches of this nature can be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report

### 7.3.7 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in Figure 7-1.

**CAUTION**

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

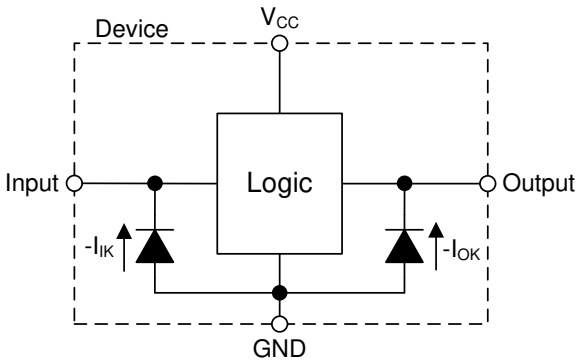



**Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output**

### 7.3.8 Fully Configurable Dual-Rail Design

Both the $V_{CCA}$ and $V_{CCB}$ pins can be supplied at any voltage from 0.65 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V and 3.3 V).

### 7.3.9 I/Os with Integrated Static Pull-Down Resistors

To help avoid floating inputs on the I/Os, this device has 71kΩ typical integrated weak pull-downs on all data I/Os. This feature allows all inputs to be left floating without the concern for unstable outputs or increased current consumption. This also helps to reduce external component count for applications where not all channels are used or need to be fixed low. If an external pull-up is required, it should be no larger than 7kΩ to avoid contention with the 71kΩ internal pull-down.

### 7.3.10 Supports High-Speed Translation

The SN74AXC4T774 device can support high data-rate applications. The translated signal data rate can be up to 310 Mbps when the signal is translated from 1.8 V to 3.3 V.

## 7.4 Device Functional Modes

**Table 7-1. Function Table (Each Transceiver)**

| CONTROL INPUTS(1) (2) | | PORT STATUS | | OPERATION |
|---|---|---|---|---|
| $\overline{OE}$ | DIR | A PORT | B PORT | |
| L | L | Output (Enabled) | Input (Hi-Z) | B data to A bus |
| L | H | Input (Hi-Z) | Output (Enabled) | A data to B bus |

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**Table 7-1. Function Table (Each Transceiver) (continued)**

| CONTROL INPUTS(1) (2) | | PORT STATUS | | OPERATION |
|---|---|---|---|---|
| $\overline{OE}$ | DIR | A PORT | B PORT | |
| H | X | Input (Hi-Z) | Input (Hi-Z) | Isolation |

(1) Input circuits of the data I/Os are always active.
(2) Pins configured as inputs should not be left floating.


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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The SN74AXC4T774 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AXC4T774 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 310 Mbps when device translates a signal from 1.8 V to 3.3 V.

One example application is shown in Figure 8-1, where the SN74AXC4T774 device is used to translate a low voltage SPI signal from an SoC to a higher voltage signal to properly drive the inputs of a GPS module, and vice versa.

## 8.2 Typical Application

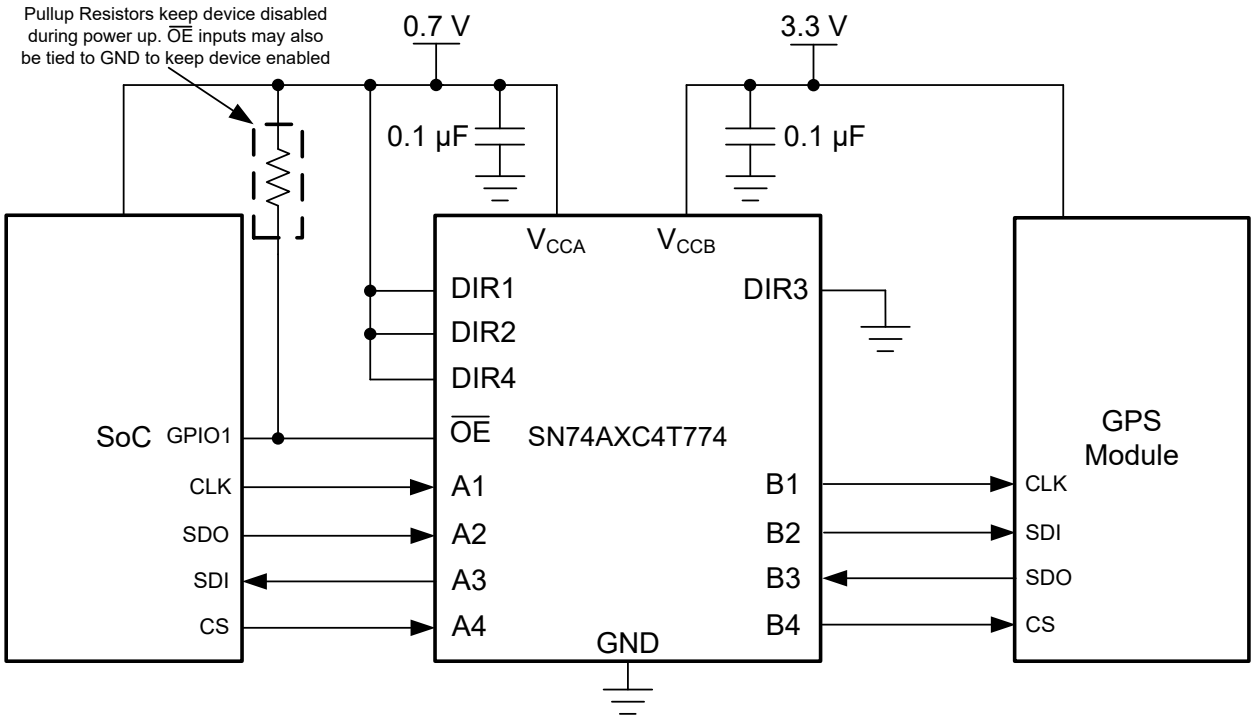



**Figure 8-1. Serial Peripheral Interface (SPI) Application**

### 8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

**Table 8-1. Design Parameters**

| DESIGN PARAMETERS | EXAMPLE VALUES |
|---|---|
| Input voltage range | 0.65 V to 3.6 V |
| Output voltage range | 0.65 V to 3.6 V |

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### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXC4T774 device to determine the input voltage range. For a valid logic-high, the value must exceed the high-level input voltage ($V_{IH}$) of the input port. For a valid logic low the value must be less than the low-level input voltage ($V_{IL}$) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXC4T774 device is driving to determine the output voltage range.

### 8.2.3 Application Curve

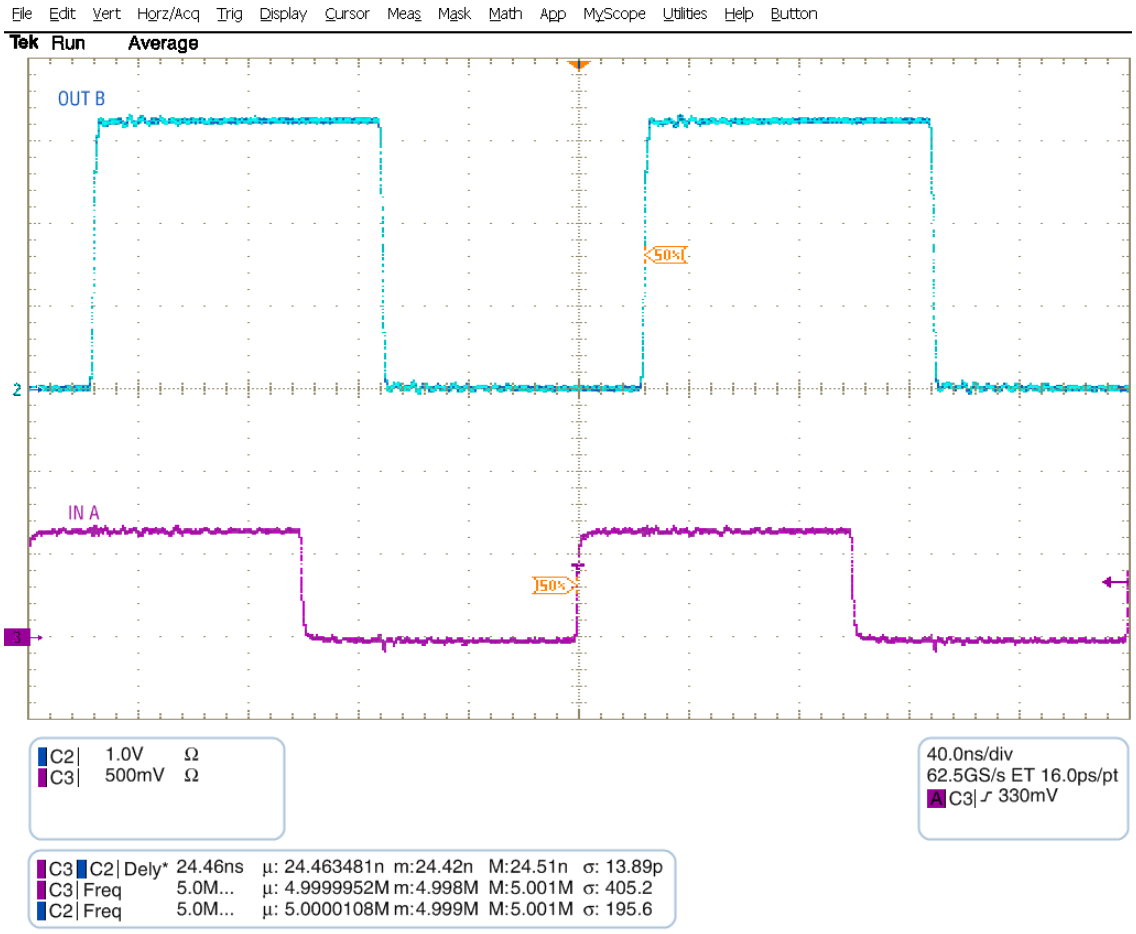



**Figure 8-2. Up Translation at 2.5 MHz (0.7 V to 3.3 V)**

## 8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Glitch Free Power Sequencing With AXC Level Translators* application report


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## 8.4 Layout

### 8.4.1 Layout Guidelines

For device reliability, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1µF capacitor is recommended, but transient performance can be improved by having both 1µF and 0.1µF capacitors in parallel as bypass capacitors.
- The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

### 8.4.2 Layout Example

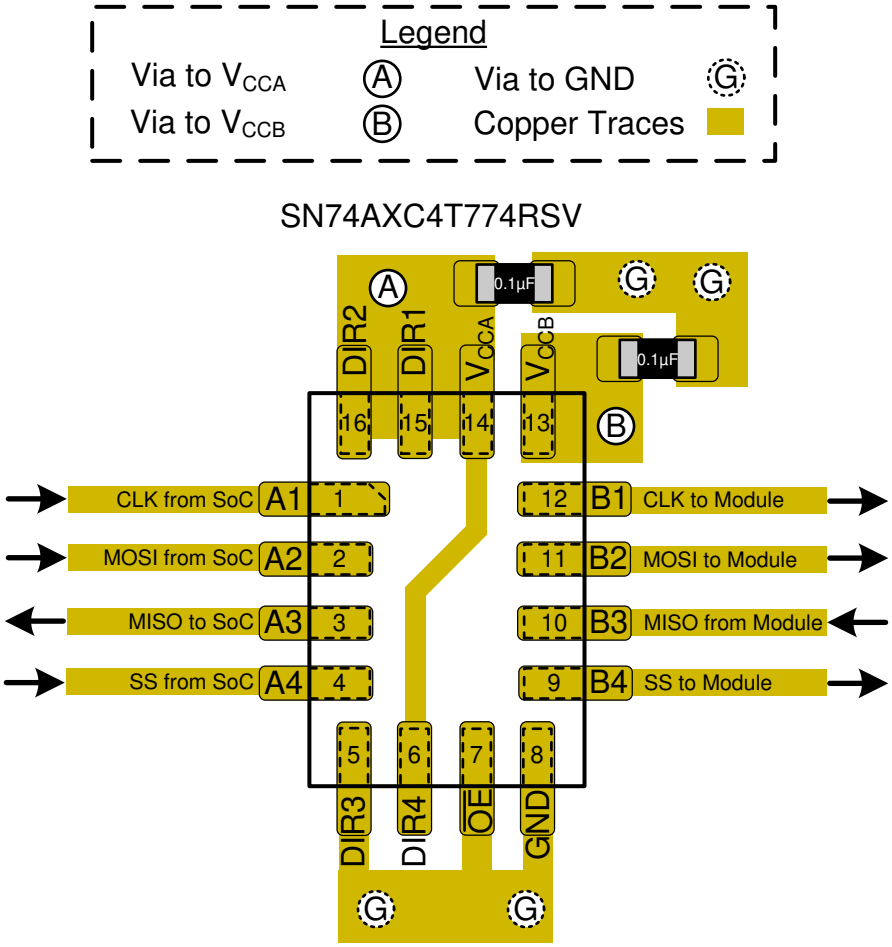



**Figure 8-3. Layout Example**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Power Sequencing for AXC Family of Devices* application report
- Texas Instruments, *SN74AXC4T774 Evaluation Module Tool Folder*

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

| Changes from Revision B (May 2021) to Revision C (May 2022) | Page |
|---|---|
| • Added the *I/Os with Integrated Static Pull-Down Resistors* section | 20 |

| Changes from Revision A (July 2020) to Revision B (May 2021) | Page |
|---|---|
| • Updated the *Serial Peripheral Interface (SPI) Application* figure in the *Typical Application* section | 23 |

| Changes from Revision * (July 2019) to Revision A (July 2020) | Page |
|---|---|
| • Updated the numbering format for tables, figures and cross-references throughout the document | 1 |
| • Added BQB (WQFN) package option to *Device Information* table | 1 |


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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AXC4T774BQBR | Active | Production | WQFN (BQB) \| 16 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 4T774 |
| SN74AXC4T774BQBR.A | Active | Production | WQFN (BQB) \| 16 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 4T774 |
| SN74AXC4T774BQBRG4 | Active | Production | WQFN (BQB) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 4T774 |
| SN74AXC4T774BQBRG4.A | Active | Production | WQFN (BQB) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 4T774 |
| SN74AXC4T774PWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | SN4T774 |
| SN74AXC4T774PWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SN4T774 |
| SN74AXC4T774PWRG4 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SN4T774 |
| SN74AXC4T774PWRG4.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | SN4T774 |
| SN74AXC4T774RSVR | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1UXR |
| SN74AXC4T774RSVR.A | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1UXR |
| SN74AXC4T774RSVRG4.A | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1UXR |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AXC4T774 :**

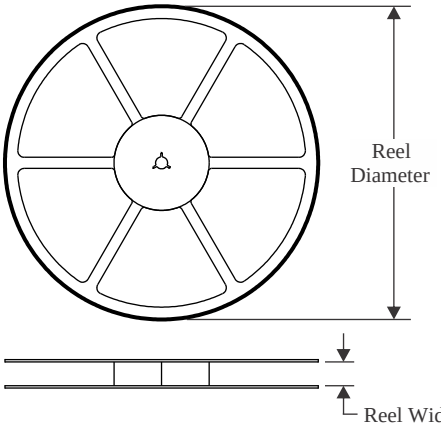
- Automotive : SN74AXC4T774-Q1

NOTE: Qualified Version Definitions:

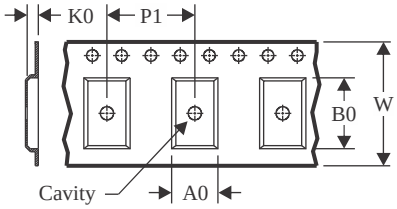
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

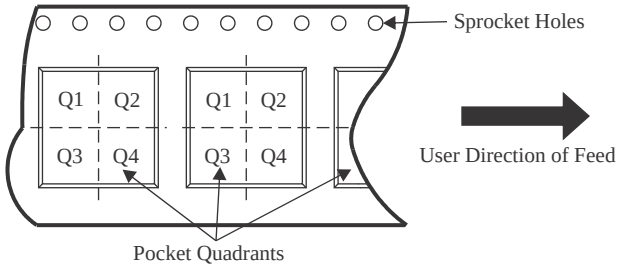



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

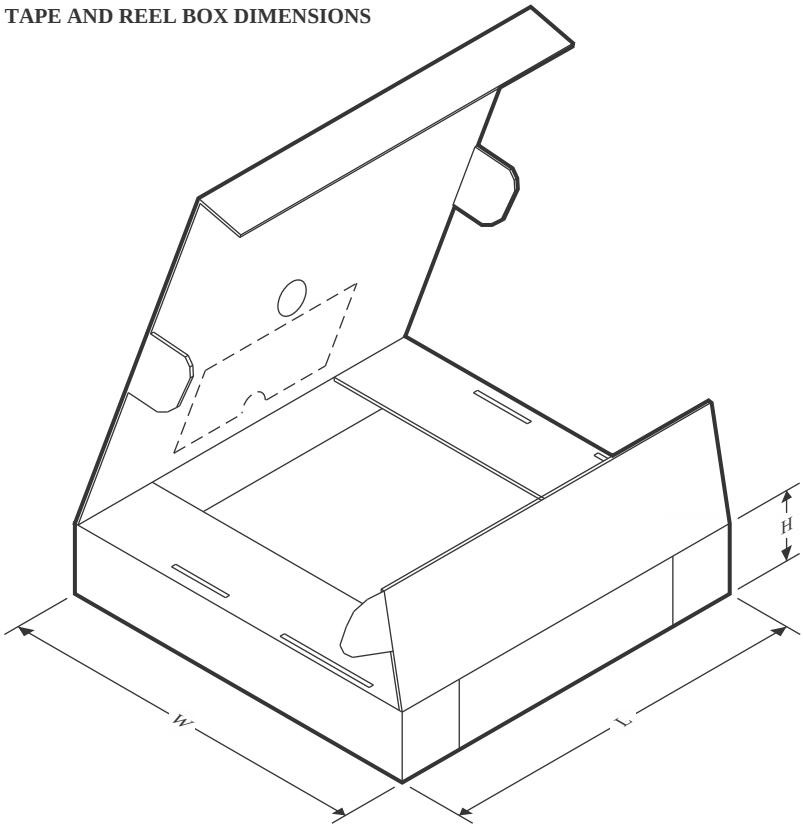
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AXC4T774BQBR | WQFN | BQB | 16 | 3000 | 180.0 | 12.4 | 2.8 | 3.8 | 1.2 | 4.0 | 12.0 | Q1 |
| SN74AXC4T774BQBRG4 | WQFN | BQB | 16 | 3000 | 180.0 | 12.4 | 2.8 | 3.8 | 1.2 | 4.0 | 12.0 | Q1 |
| SN74AXC4T774PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.3 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AXC4T774PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AXC4T774PWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AXC4T774RSVR | UQFN | RSV | 16 | 3000 | 178.0 | 13.5 | 2.1 | 2.9 | 0.75 | 4.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AXC4T774BQBR | WQFN | BQB | 16 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AXC4T774BQBRG4 | WQFN | BQB | 16 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AXC4T774PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74AXC4T774PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AXC4T774PWRG4 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AXC4T774RSVR | UQFN | RSV | 16 | 3000 | 189.0 | 185.0 | 36.0 |

# GENERIC PACKAGE VIEW

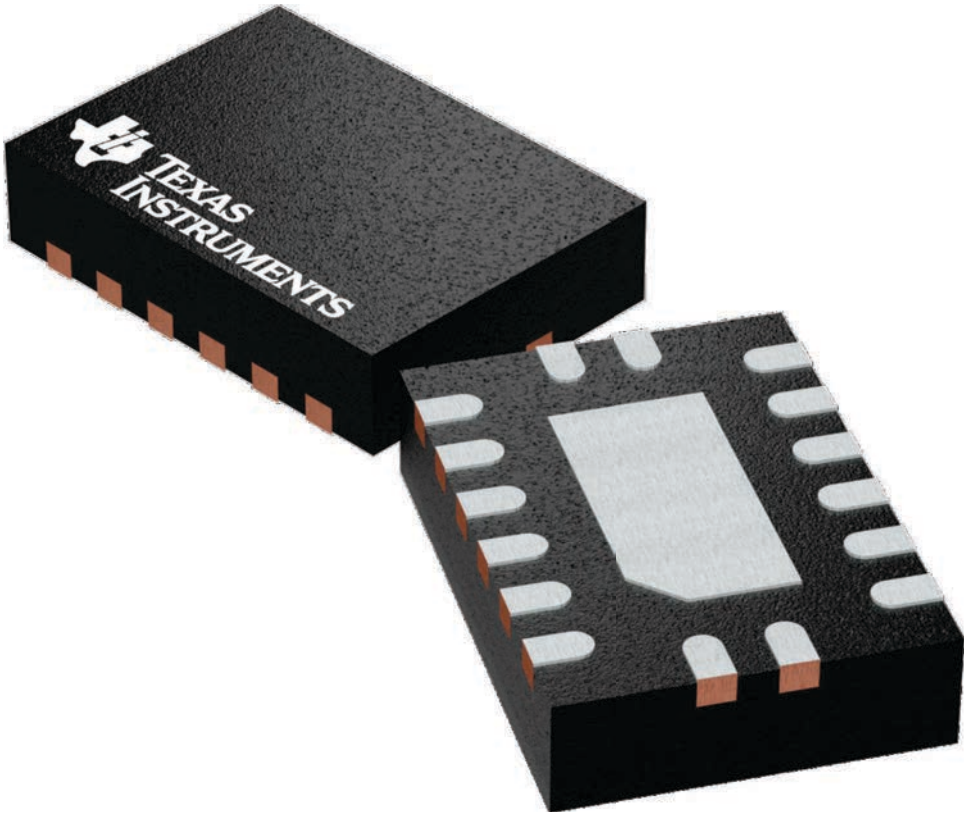
## BQB 16

## WQFN - 0.8 mm max height

**2.5 x 3.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



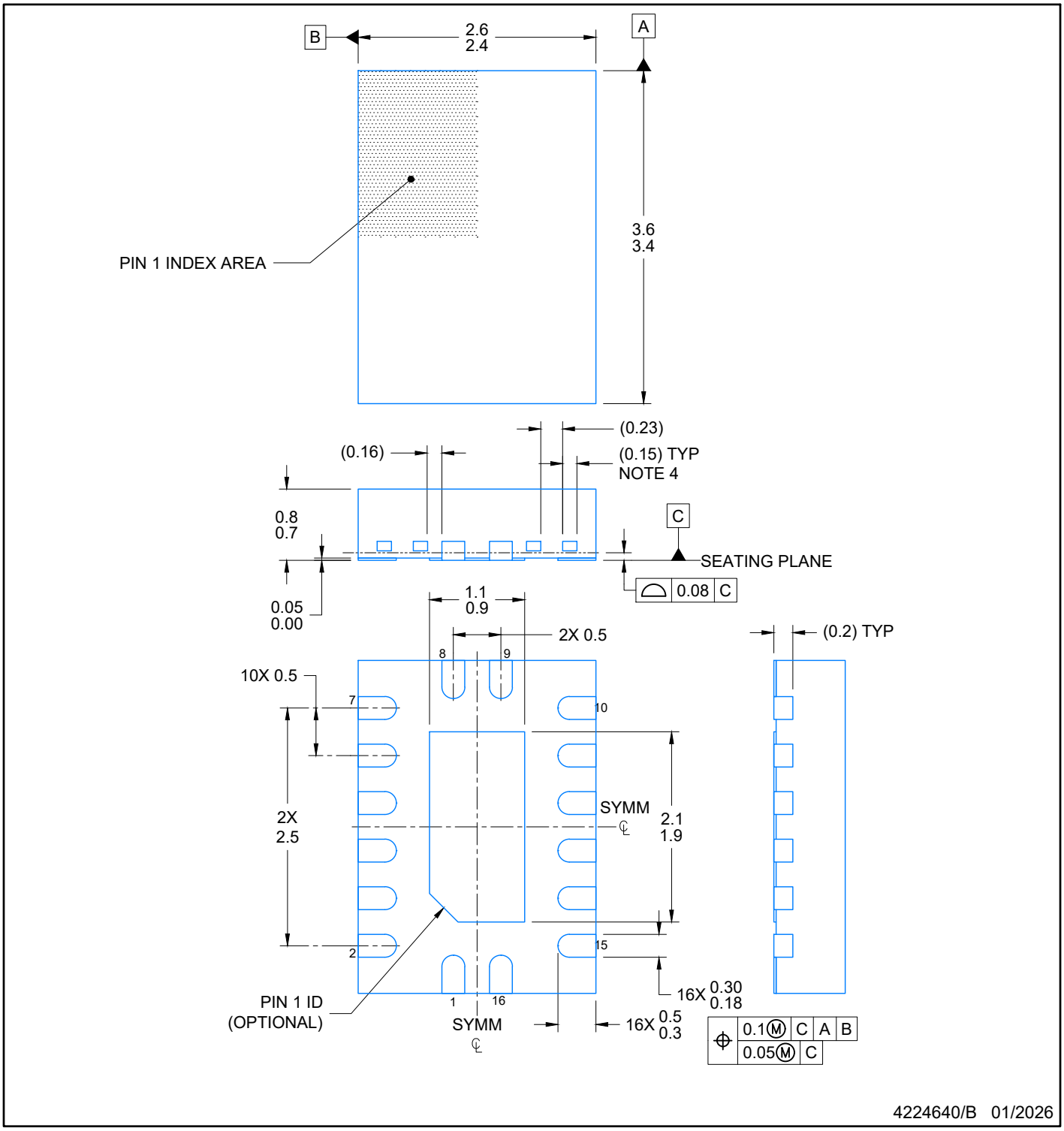

4226161/A

# PACKAGE OUTLINE

## BQB0016A

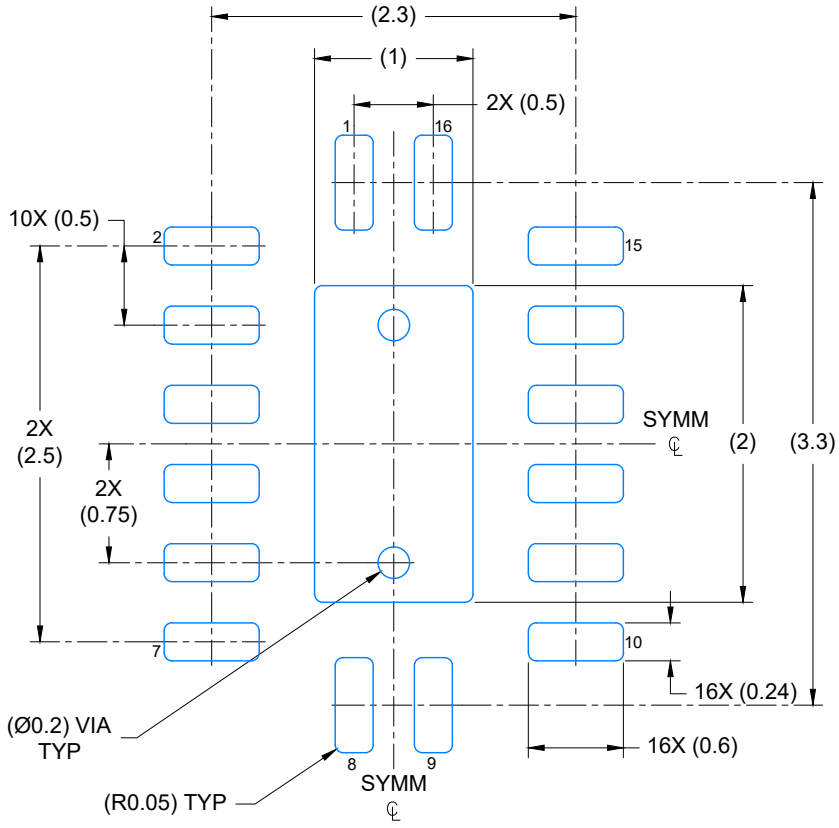
## WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

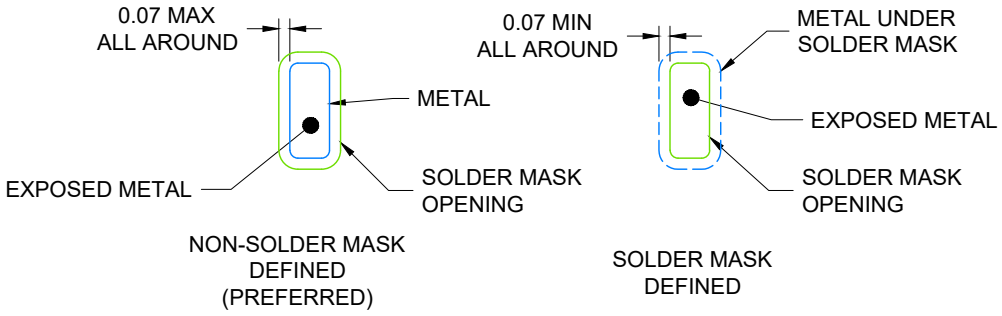



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

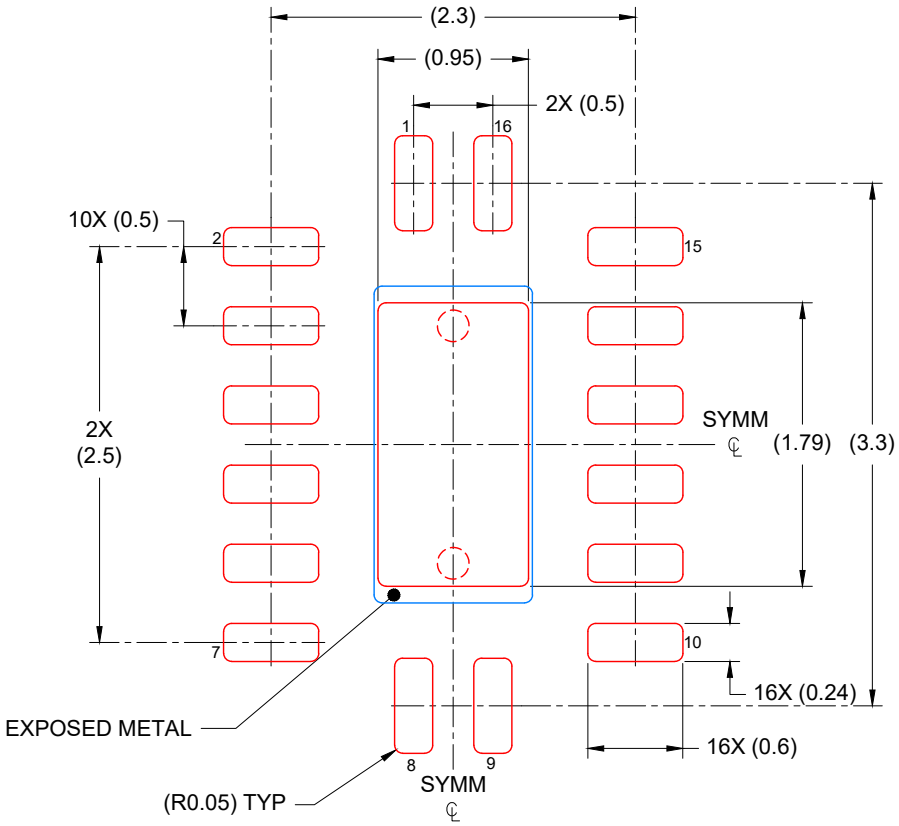



4224640/B 01/2026

1. NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/B 01/2026

NOTES: (continued)

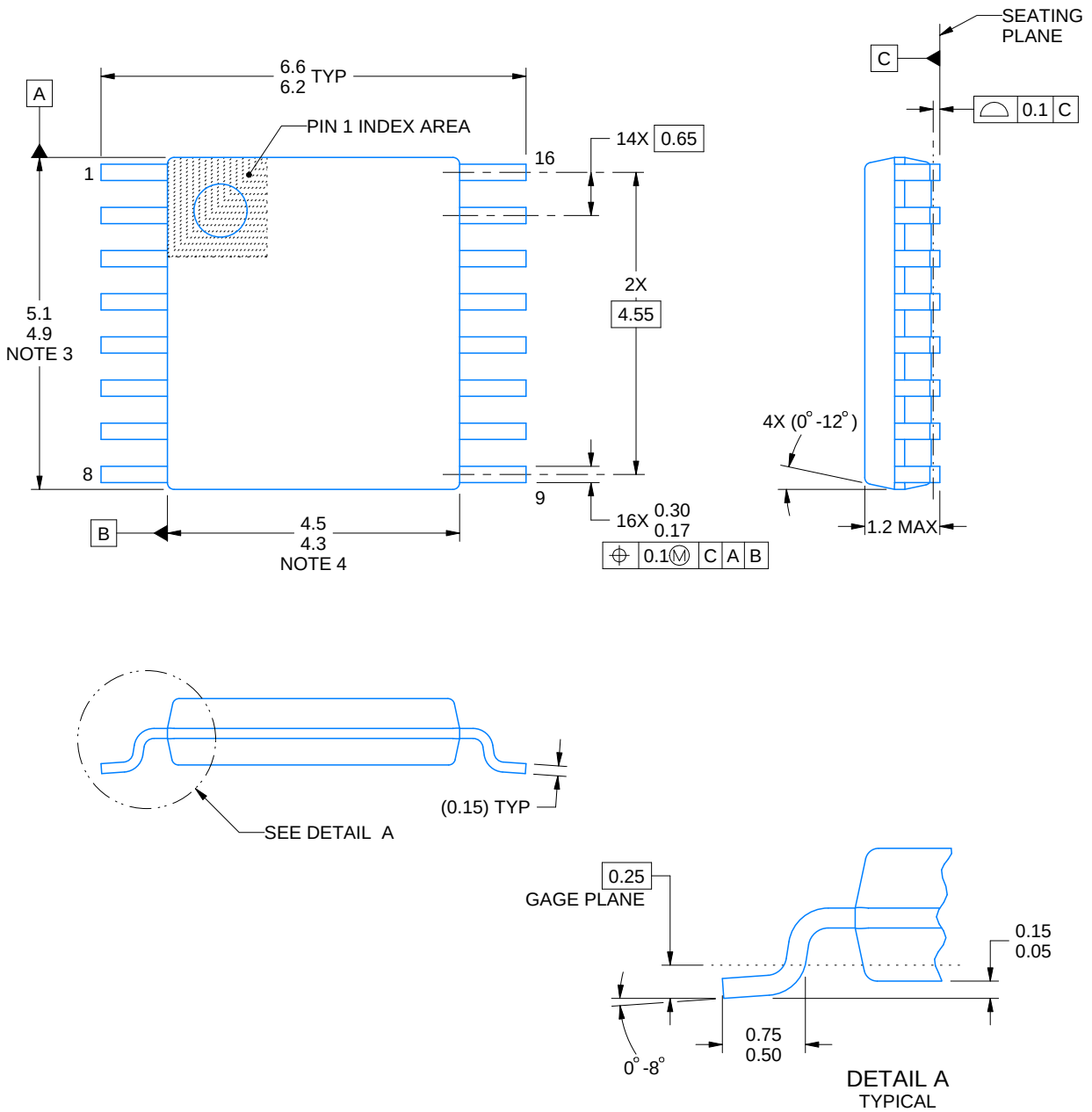
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## PW0016A

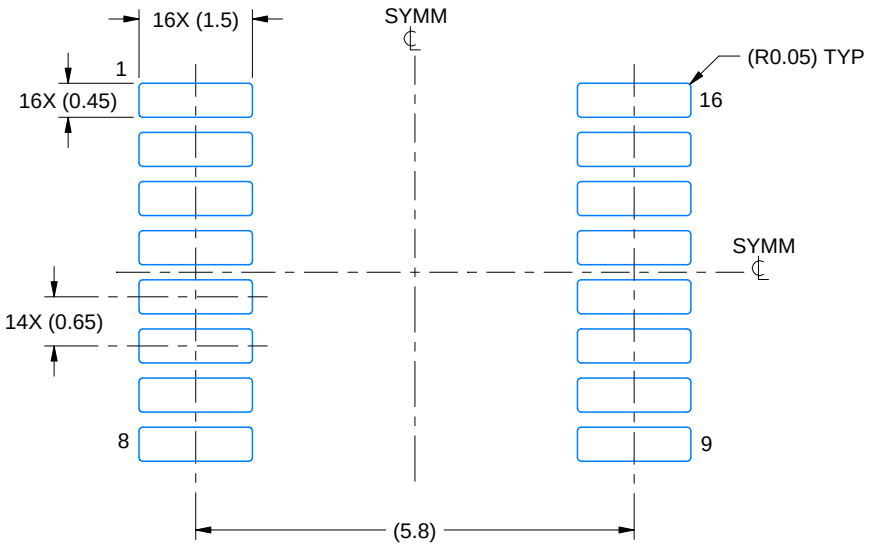
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

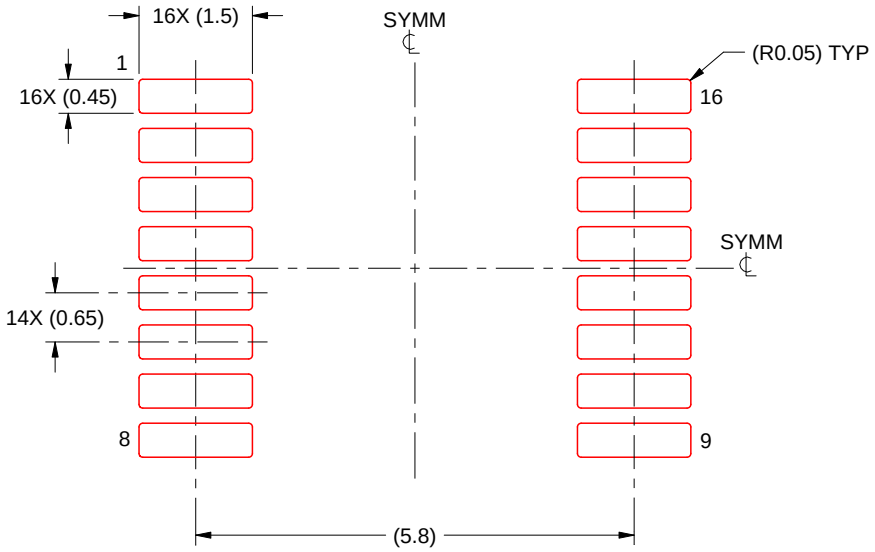



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

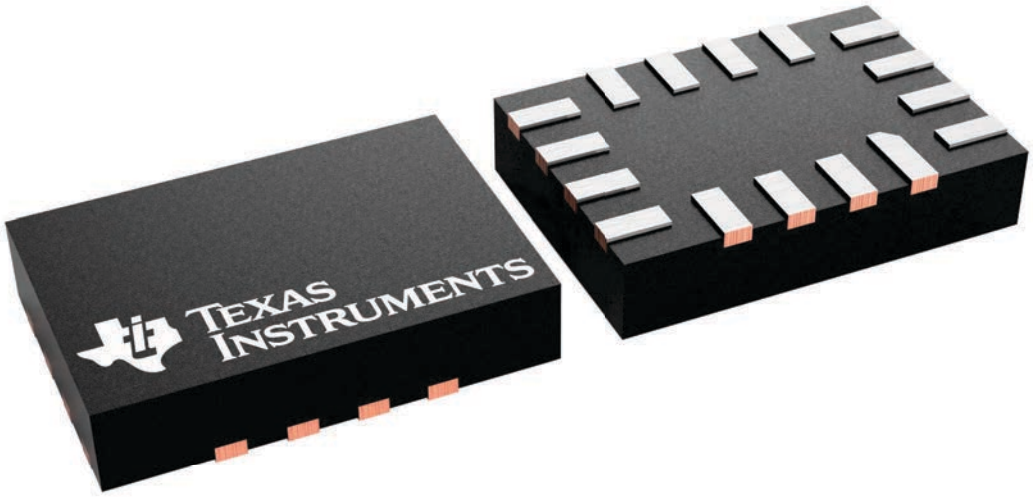
## RSV 16

## UQFN - 0.55 mm max height

**1.8 x 2.6, 0.4 mm pitch**

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



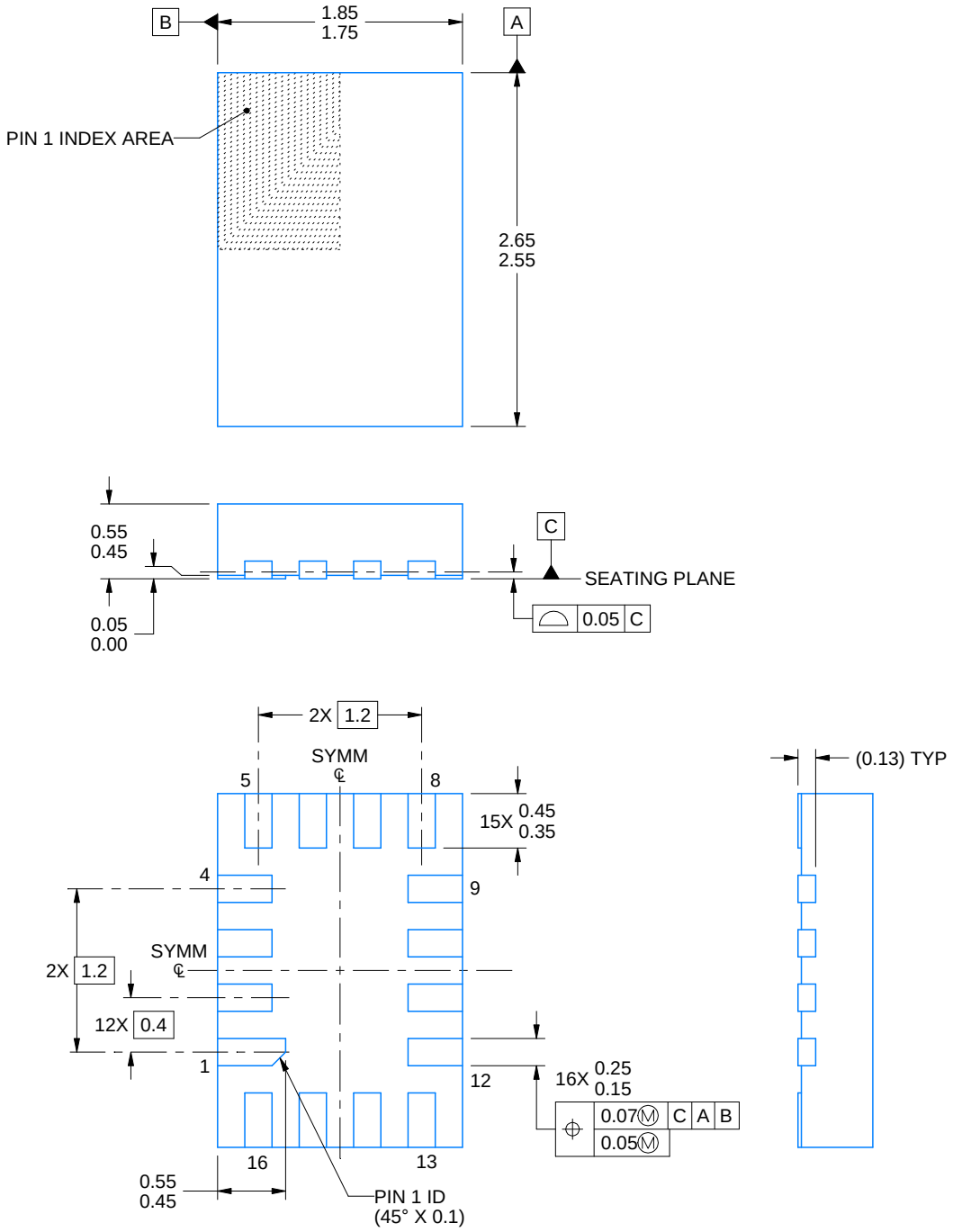

4231225/A

# RSV0016A

# PACKAGE OUTLINE

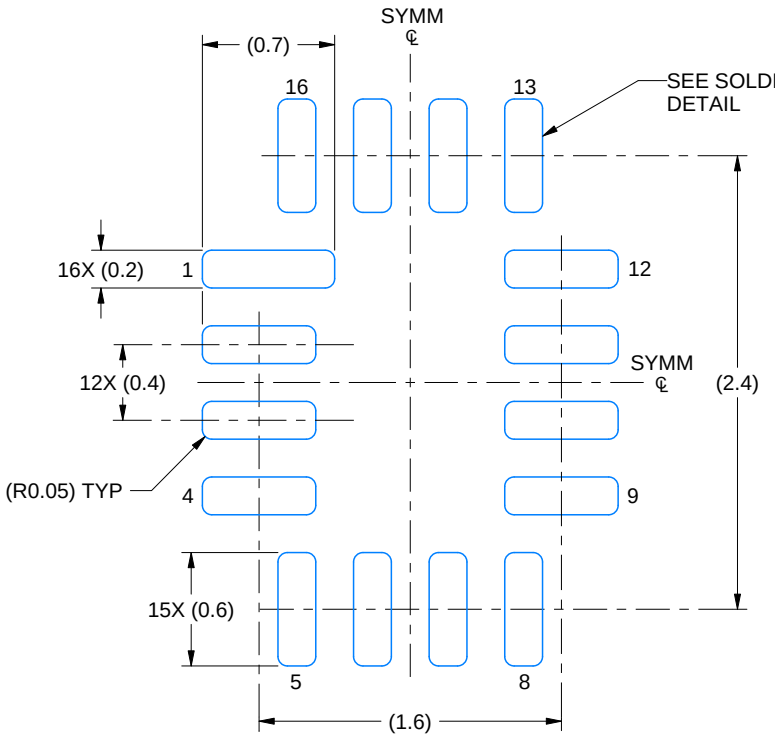
## UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

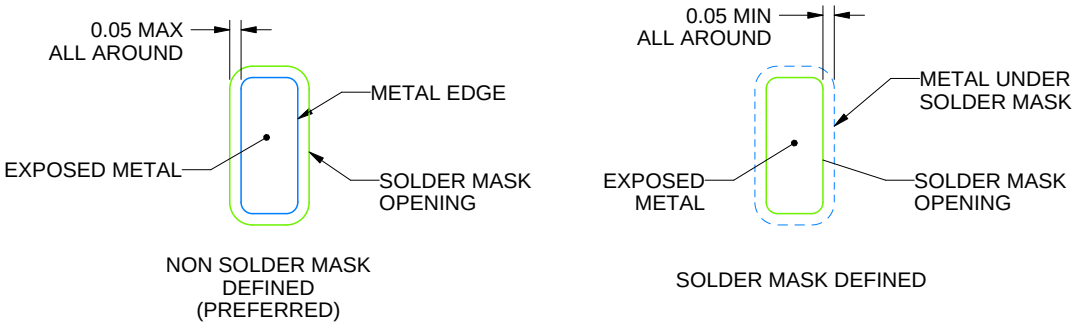



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

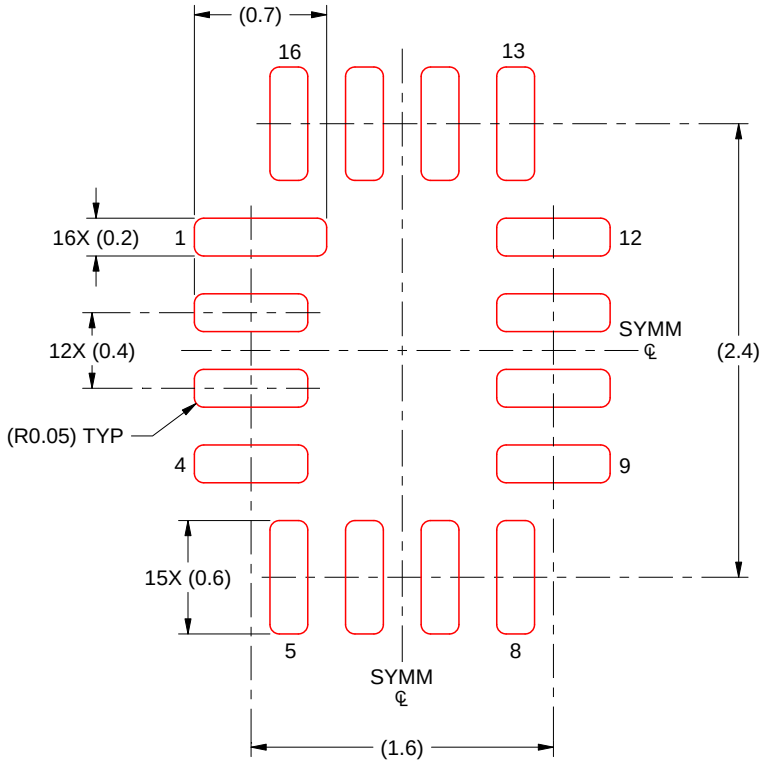



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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