

SN74AUP1G126 Low-Power Single Bus Buffer Gate With Tri-State Output

1 Features

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22–
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption ($I_{CC} = 0.9 \mu\text{A}$ Maximum)
- Low Dynamic-Power Consumption ($C_{pd} = 4 \text{ pF}$ Typical at 3.3 V)
- Low Input Capacitance ($C_i = 1.5 \text{ pF}$ Typical)
- Low Noise – Overshoot and Undershoot $<10\%$ of V_{CC}
- Input-Disable Feature Allows Floating Input Conditions
- I_{off} Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4.6 \text{ ns}$ Maximum at 3.3 V
- Suitable for Point-to-Point Applications

2 Applications

- Audio Dock: Portable
- BluRay™ Players and Home Theaters
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid-State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Wireless Headsets, Keyboards, and Mice

3 Description

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family assures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see [AUP – The Lowest-Power Family](#) and [Excellent Signal Integrity](#)).

This bus buffer gate is a single line driver with a 3-state output. The output is disabled when the output-enable (OE) input is low. This device has the input-disable feature, which allows floating input signals.

To assure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G126DRL	SOT-5X3 (5)	1.60 mm × 1.20 mm
SN74AUP1G126DBV	SOT-23 (5)	1.60 mm × 2.90 mm
SN74AUP1G126DCK	SC70 (5)	1.25 mm × 2.00 mm
SN74AUP1G126DRY	SON (6)	1.00 mm × 1.45 mm
SN74AUP1G126DSF	SON (6)	1.00 mm × 1.00 mm
SN74AUP1G126YFP	DSBGA (6)	0.76 mm × 1.16 mm
SN74AUP1G126YZP	DSBGA (5)	0.89 mm × 1.39 mm
SN74AUP1G126DPW	X2SON (5)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

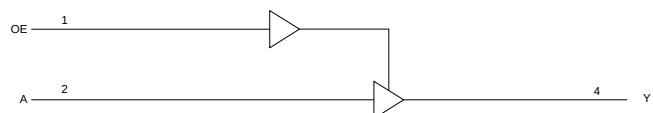


Table of Contents

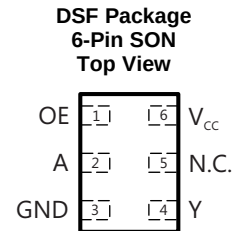
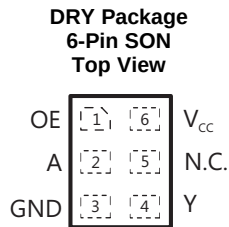
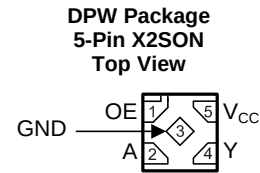
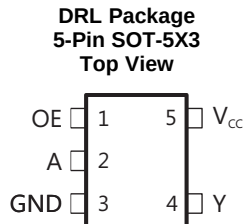
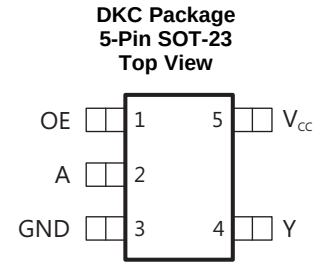
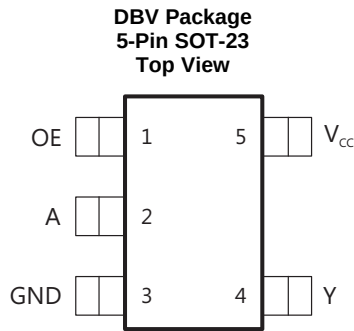
1 Features	1	8 Detailed Description	14
2 Applications	1	8.1 Overview	14
3 Description	1	8.2 Functional Block Diagram	14
4 Revision History	2	8.3 Feature Description	14
5 Pin Configuration and Functions	3	8.4 Device Functional Modes	15
6 Specifications	4	9 Application and Implementation	16
6.1 Absolute Maximum Ratings	4	9.1 Application Information	16
6.2 ESD Ratings	4	9.2 Typical Application	16
6.3 Recommended Operating Conditions	4	10 Power Supply Recommendations	17
6.4 Thermal Information	5	11 Layout	17
6.5 Electrical Characteristics	5	11.1 Layout Guidelines	17
6.6 Switching Characteristics: $C_L = 5\text{ pF}$	7	11.2 Layout Example	17
6.7 Switching Characteristics: $C_L = 10\text{ pF}$	8	12 Device and Documentation Support	18
6.8 Switching Characteristics: $C_L = 15\text{ pF}$	9	12.1 Documentation Support	18
6.9 Switching Characteristics: $C_L = 30\text{ pF}$	10	12.2 Receiving Notification of Documentation Updates	18
6.10 Operating Characteristics	11	12.3 Community Resources	18
6.11 Typical Characteristics	11	12.4 Trademarks	18
7 Parameter Measurement Information	12	12.5 Electrostatic Discharge Caution	18
7.1 (Propagation Delays, Setup and Hold Times, and Pulse Width)	12	12.6 Glossary	18
7.2 (Enable and Disable Times)	13	13 Mechanical, Packaging, and Orderable Information	18

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

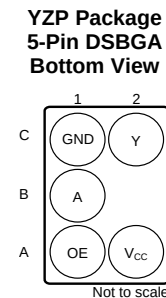
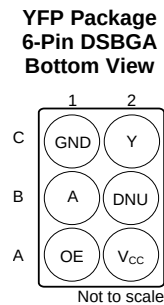
Changes from Revision F (May 2010) to Revision G	Page
Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Application and Implementation</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
Deleted <i>Ordering Information</i> table, see <i>Mechanical, Packaging, and Orderable Information</i> at the end of the data sheet	1

5 Pin Configuration and Functions



N.C. – No internal connection.

See mechanical drawings for dimensions.



Pin Functions

NAME	PIN				I/O	DESCRIPTION
	DBV, DCK, DRL, DPW	DRY, DSF	YFP	YZP		
A	2	2	B1	B1	I	Input
DNU	—	—	—	B2	—	Do not use
GND	3	3	C1	C1	—	Ground
N.C.	—	5	B2	—	—	No Internal Connection
OE	1	1	A1	A1	I	Output enable (active high)
V _{CC}	5	6	A2	A2	—	Positive supply
Y	4	4	C2	C2	O	Buffered output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	4.6	V
V _I	Input voltage ⁽²⁾		−0.5	4.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		−0.5	4.6	V
V _O	Output voltage range in the high or low state ⁽²⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50		mA
I _{OK}	Output clamp current	V _O < 0	−50		mA
I _O	Continuous output current		±20		mA
	Continuous current through V _{CC} or GND		±50		mA
T _j	Junction Temperature		150		°C
T _{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	0.8	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}	V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}	
		V _{CC} = 2.3 V to 2.7 V	1.6	
		V _{CC} = 3 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0	V
		V _{CC} = 1.1 V to 1.95 V	0	
		V _{CC} = 2.3 V to 2.7 V	0	
		V _{CC} = 3 V to 3.6 V	0	
V _O	Output voltage	Active state	0	V
		3-state	0	
I _{OH}	High-level output current	V _{CC} = 0.8 V	−20	mA
		V _{CC} = 1.1 V	−1.1	
		V _{CC} = 1.4 V	−1.7	
		V _{CC} = 1.65 V	−1.9	
		V _{CC} = 2.3 V	−3.1	
		V _{CC} = 3 V	−4	

(1) All unused inputs of the device must be held at V_{CC} or GND to assure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#).

Recommended Operating Conditions (continued)

See⁽¹⁾

		MIN	MAX	UNIT
I_{OL} Low-level output current	$V_{CC} = 0.8\text{ V}$		20	μA
	$V_{CC} = 1.1\text{ V}$		1.1	mA
	$V_{CC} = 1.4\text{ V}$		1.7	
	$V_{CC} = 1.65\text{ V}$		1.9	
	$V_{CC} = 2.3\text{ V}$		3.1	
	$V_{CC} = 3\text{ V}$		4	
$\Delta t/\Delta v$ Input transition rise or fall rate	$V_{CC} = 0.8\text{ V to }3.6\text{ V}$		200	ns/V
T_A Operating free-air temperature		–40	85	$^{\circ}\text{C}$

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AUP1G126								UNIT
		DRL (SOT-5X3)	DBV (SOT-23)	DCK (SC70)	DRY (SON)	DSF (SON)	DPW (X2SON)	YFP (DSBGA)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	5 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	295.1	230.5	303.6	342.1	377.1	504.3	125.4	146.2	$^{\circ}\text{C/W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	131.0	172.7	203.8	233.1	187.7	234.9	1.9	1.4	$^{\circ}\text{C/W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	143.9	62.2	100.9	206.7	236.6	370.3	37.2	39.3	$^{\circ}\text{C/W}$
Ψ_{JT}	Junction-to-top characterization parameter	14.7	49.3	76.1	63.4	29.0	44.5	0.5	0.7	$^{\circ}\text{C/W}$
Ψ_{JB}	Junction-to-board characterization parameter	144.4	61.6	99.3	206.7	236.3	369.7	37.5	39.8	$^{\circ}\text{C/W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	165.2	N/A	N/A	$^{\circ}\text{C/W}$

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = −20 μA	T _A = 25°C	0.8 V to 3.6 V	V _{CC} − 0.1		V	
		T _A = −40°C to +85°C		V _{CC} − 0.1			
	I _{OH} = −1.1 mA	T _A = 25°C	1.1 V	0.75 × V _{CC}			
		T _A = −40°C to +85°C		0.7 × V _{CC}			
	I _{OH} = −1.7 mA	T _A = 25°C	1.4 V	1.11			
		T _A = −40°C to +85°C		1.03			
	I _{OH} = −1.9 mA	T _A = 25°C	1.65 V	1.32			
		T _A = −40°C to +85°C		1.3			
	I _{OH} = −2.3 mA	T _A = 25°C	2.3 V	2.05			
		T _A = −40°C to +85°C		1.97			
	I _{OH} = −3.1 mA	T _A = 25°C		1.9			
		T _A = −40°C to +85°C		1.85			
	I _{OH} = −2.7 mA	T _A = 25°C	3 V	2.72			
		T _A = −40°C to +85°C		2.67			
	I _{OH} = −4 mA	T _A = 25°C		2.6			
		T _A = −40°C to +85°C		2.55			

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OL}	I _{OL} = 20 µA	T _A = 25°C	0.8 V to 3.6 V			0.1	V
		T _A = –40°C to +85°C				0.1	
	I _{OL} = 1.1 mA	T _A = 25°C	1.1 V			0.3 × V _{CC}	
		T _A = –40°C to +85°C				0.3 × V _{CC}	
	I _{OL} = 1.7 mA	T _A = 25°C	1.4 V			0.31	
		T _A = –40°C to +85°C				0.37	
	I _{OL} = 1.9 mA	T _A = 25°C	1.65 V			0.31	
		T _A = –40°C to +85°C				0.35	
	I _{OL} = 2.3 mA	T _A = 25°C	2.3 V			0.31	
		T _A = –40°C to +85°C				0.33	
	I _{OL} = 3.1 mA	T _A = 25°C	3 V			0.44	
		T _A = –40°C to +85°C				0.45	
I _I	A or OE input	V _I = GND to 3.6 V	0 V to 3.6 V			0.1	µA
		T _A = –40°C to +85°C				0.5	
I _{off}	V _I or V _O = 0 V to 3.6 V	T _A = 25°C	0 V			0.2	µA
		T _A = –40°C to +85°C				0.6	
ΔI _{off}	V _I or V _O = 0 V to 3.6 V	T _A = 25°C	0 V to 0.2 V			0.2	µA
		T _A = –40°C to +85°C				0.6	
I _{OZ}	V _O = V _{CC} or GND, T _A = –40°C to +85°C		3.6 V			0.5	µA
I _{CC}	V _I = GND or (V _{CC} to 3.6 V), OE = GND, I _O = 0	T _A = 25°C	0.8 V to 3.6 V			0.5	µA
		T _A = –40°C to +85°C				0.9	
ΔI _{CC}	A input	T _A = 25°C	3.3 V			40	µA
		T _A = –40°C to +85°C				50	
	OE input	T _A = 25°C				110	
		T _A = –40°C to +85°C				120	
	All inputs	V _I = GND to 3.6 V, OE = V _{CC} ⁽²⁾ , T _A = 25°C or T _A = –40°C to +85°C	0.8 V to 3.6 V			0	
C _i	V _I = V _{CC} or GND, T _A = 25°C		0 V		1.5		pF
			3.6 V		1.5		
C _O	V _O = V _{CC} or GND, T _A = 25°C		3.6 V		3		pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND

(2) To show I_{CC} is very low when the input-disable feature is enabled

6.6 Switching Characteristics: $C_L = 5 \text{ pF}$

over recommended operating free-air temperature range, $C_L = 5 \text{ pF}$ (unless otherwise noted) (see [Figure 2](#) and [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{pd}	A	Y	V _{CC} = 0.8 V	T _A = 25°C	18.1			ns
			V _{CC} = 1.2 V ± 0.1 V	T _A = 25°C	4.3	7.4	12.6	
				T _A = −40°C to +85°C	2.7	15.3		
			V _{CC} = 1.5 V ± 0.1 V	T _A = 25°C	3.3	5.2	8.5	
				T _A = −40°C to +85°C	1	10.2		
			V _{CC} = 1.8 V ± 0.15 V	T _A = 25°C	2.6	4.1	6.8	
				T _A = −40°C to +85°C	1.3	8.3		
			V _{CC} = 2.5 V ± 0.2 V	T _A = 25°C	2	2.9	4.7	
T _A = −40°C to +85°C	1.1	5.8						
t _{en}	OE	Y	V _{CC} = 0.8 V	T _A = 25°C	19.1			ns
			V _{CC} = 1.2 V ± 0.1 V	T _A = 25°C	5.1	9.3	15.9	
				T _A = −40°C to +85°C	3.6	19.2		
			V _{CC} = 1.5 V ± 0.1 V	T _A = 25°C	4.1	6.6	10.5	
				T _A = −40°C to +85°C	2.5	12.7		
			V _{CC} = 1.8 V ± 0.15 V	T _A = 25°C	3.2	5.3	8.7	
				T _A = −40°C to +85°C	2.1	10.3		
			V _{CC} = 2.5 V ± 0.2 V	T _A = 25°C	2.5	3.8	6	
T _A = −40°C to +85°C	1.6	7.2						
t _{dis}	OE	Y	V _{CC} = 0.8 V	T _A = 25°C	12.1			ns
			V _{CC} = 1.2 V ± 0.1 V	T _A = 25°C	2.4	4.1	6.9	
				T _A = −40°C to +85°C	2.2	7.7		
			V _{CC} = 1.5 V ± 0.1 V	T _A = 25°C	1.8	2.9	4.5	
				T _A = −40°C to +85°C	1.7	5.1		
			V _{CC} = 1.8 V ± 0.15 V	T _A = 25°C	1	2.9	4.3	
				T _A = −40°C to +85°C	1.5	4.7		
			V _{CC} = 2.5 V ± 0.2 V	T _A = 25°C	1	1.8	2.7	
T _A = −40°C to +85°C	1	3.3						
V _{CC} = 3.3 V ± 0.3 V	T _A = 25°C	1.2	2.2	3.2				
	T _A = −40°C to +85°C	1.1	4					

6.7 Switching Characteristics: $C_L = 10 \text{ pF}$

over recommended operating free-air temperature range, $C_L = 10 \text{ pF}$ (unless otherwise noted) (see [Figure 2](#) and [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A or B	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		20.5	13.7	ns
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	4.6	8.4	9.3	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.6		16.6	
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	3.5	5.9	7.5	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.4		11.1	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	3.9	4.7	5.3	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.3		9.1	
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$T_A = 25^\circ\text{C}$	2.3	3.4	4.3	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.6		6.4	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$T_A = 25^\circ\text{C}$	2.1	2.8		
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.4		5.2	
t_{en}	OE	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		21.8	16.8	ns
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	4.9	10.2	11.2	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	4.4		20.2	
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	3.9	7.3	9.2	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.3		13.5	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	3.4	5.8	6.4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.7		11	
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$T_A = 25^\circ\text{C}$	2.5	4.3	5.4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.1		7.8	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$T_A = 25^\circ\text{C}$	2.1	3.7		
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.9		6.4	
t_{dis}	OE	Y	$V_{CC} = 0.8 \text{ V}$	$T_A = 25^\circ\text{C}$		13		ns
			$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	3.8	6.6	11.7	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.2		14	
			$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$T_A = 25^\circ\text{C}$	2.2	4.7	7.9	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.3		9.3	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$T_A = 25^\circ\text{C}$	2.4	4.4	6.4	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	2.2		7.5	
			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$T_A = 25^\circ\text{C}$	1.3	3.1	4.9	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.2		5.4	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	$T_A = 25^\circ\text{C}$	1.9	3.4	5	
				$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.9		5.6	

6.8 Switching Characteristics: $C_L = 15 \text{ pF}$

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see [Figure 2](#) and [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{pd}	A or B	Y	V _{CC} = 0.8 V	T _A = 25°C	22.5			ns
			V _{CC} = 1.2 V ± 0.1 V	T _A = 25°C	5.8	9.3	15.1	
				T _A = −40°C to +85°C	4.3	17.9		
			V _{CC} = 1.5 V ± 0.1 V	T _A = 25°C	4.4	6.6	10.2	
				T _A = −40°C to +85°C	3	12.1		
			V _{CC} = 1.8 V ± 0.15 V	T _A = 25°C	3.5	5.3	8.3	
				T _A = −40°C to +85°C	2.3	9.9		
			V _{CC} = 2.5 V ± 0.2 V	T _A = 25°C	2.7	3.9	5.8	
T _A = −40°C to +85°C	1.9	7						
t _{en}	OE	Y	V _{CC} = 0.8 V	T _A = 25°C	25.2			ns
			V _{CC} = 1.2 V ± 0.1 V	T _A = 25°C	7	11.3	18.1	
				T _A = −40°C to +85°C	5.4	21.4		
			V _{CC} = 1.5 V ± 0.1 V	T _A = 25°C	5.5	8.1	12.2	
				T _A = −40°C to +85°C	4.1	14.5		
			V _{CC} = 1.8 V ± 0.15 V	T _A = 25°C	4.3	6.5	10.1	
				T _A = −40°C to +85°C	3.3	12		
			V _{CC} = 2.5 V ± 0.2 V	T _A = 25°C	3.4	4.8	7.1	
T _A = −40°C to +85°C	2.6	8.4						
t _{dis}	OE	Y	V _{CC} = 0.8 V	T _A = 25°C	14			ns
			V _{CC} = 1.2 V ± 0.1 V	T _A = 25°C	3.7	5.8	8.2	
				T _A = −40°C to +85°C	3.3	11		
			V _{CC} = 1.5 V ± 0.1 V	T _A = 25°C	5.5	3.9	5.9	
				T _A = −40°C to +85°C	2.1	8		
			V _{CC} = 1.8 V ± 0.15 V	T _A = 25°C	3.3	4.5	6.6	
				T _A = −40°C to +85°C	2.9	7.4		
			V _{CC} = 2.5 V ± 0.2 V	T _A = 25°C	2.3	3.2	4.3	
T _A = −40°C to +85°C	1.8	5.1						
V _{CC} = 3.3 V ± 0.3 V	T _A = 25°C	2.4	4.8	6.2				
	T _A = −40°C to +85°C	3.1	6.7					

6.9 Switching Characteristics: $C_L = 30$ pF

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 2](#) and [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	A or B	Y	$V_{CC} = 0.8$ V	$T_A = 25^\circ\text{C}$		29		ns
			$V_{CC} = 1.2$ V ± 0.1 V	$T_A = 25^\circ\text{C}$	7.4	12	18.7	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	6.6		21.4	
			$V_{CC} = 1.5$ V ± 0.1 V	$T_A = 25^\circ\text{C}$	5.7	8.6	12.5	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.9		14.7	
			$V_{CC} = 1.8$ V ± 0.15 V	$T_A = 25^\circ\text{C}$	4.8	6.9	10.1	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3.1		12	
			$V_{CC} = 2.5$ V ± 0.2 V	$T_A = 25^\circ\text{C}$	3.9	5.1	7.2	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3.3		8.7	
t_{en}	OE	Y	$V_{CC} = 0.8$ V	$T_A = 25^\circ\text{C}$		33.4		ns
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	8.8	14.1	21.8	
			$V_{CC} = 1.2$ V ± 0.1 V	$T_A = 25^\circ\text{C}$	6.9	10.1	14.6	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	5.6		17.4	
			$V_{CC} = 1.5$ V ± 0.1 V	$T_A = 25^\circ\text{C}$	5.6	8.1	12	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.7		14.1	
			$V_{CC} = 1.8$ V ± 0.15 V	$T_A = 25^\circ\text{C}$	4.3	6.1	8.5	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3.8		10	
t_{dis}	OE	Y	$V_{CC} = 0.8$ V	$T_A = 25^\circ\text{C}$		17.7		ns
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	5.8	10	16	
			$V_{CC} = 1.2$ V ± 0.1 V	$T_A = 25^\circ\text{C}$	3.7		16	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3.7		16	
			$V_{CC} = 1.5$ V ± 0.1 V	$T_A = 25^\circ\text{C}$	5.7	7.7	10.9	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1		10.7	
			$V_{CC} = 1.8$ V ± 0.15 V	$T_A = 25^\circ\text{C}$	4.5	7.7	9.8	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.4		12.5	
t_{dis}	OE	Y	$V_{CC} = 2.5$ V ± 0.2 V	$T_A = 25^\circ\text{C}$	3.9	5.6	7.4	ns
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3.2		9	
			$V_{CC} = 3.3$ V ± 0.3 V	$T_A = 25^\circ\text{C}$	3.3	8.4	10.7	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	6.6		10.8	

6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Output enabled $f = 10\text{ MHz}$	0.8 V	3.8	pF
			$1.2\text{ V} \pm 0.1\text{ V}$	3.7	
			$1.5\text{ V} \pm 0.1\text{ V}$	3.7	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.7	
			$2.5\text{ V} \pm 0.2\text{ V}$	3.9	
			$3.3\text{ V} \pm 0.3\text{ V}$	4	
	Output disabled $f = 10\text{ MHz}$		0.8 V	0	
			$1.2\text{ V} \pm 0.1\text{ V}$	0	
			$1.5\text{ V} \pm 0.1\text{ V}$	0	
			$1.8\text{ V} \pm 0.15\text{ V}$	0	
			$2.5\text{ V} \pm 0.2\text{ V}$	0	
			$2.5\text{ V} \pm 0.2\text{ V}$	0	
			$3.3\text{ V} \pm 0.3\text{ V}$	0	

6.11 Typical Characteristics

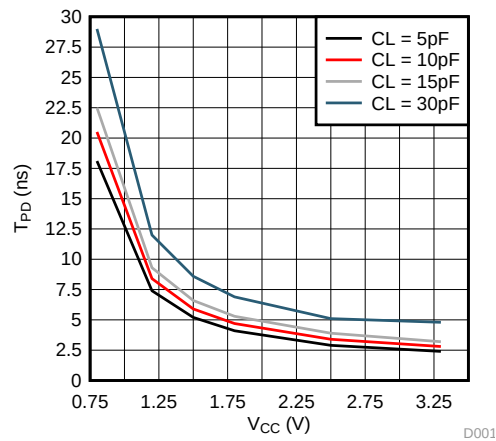
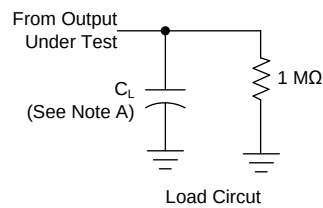


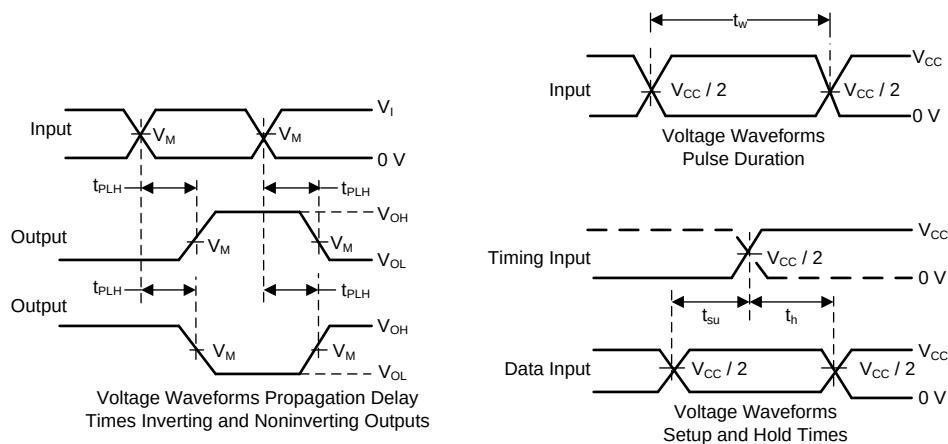
Figure 1. Propagation Delay vs. Supply Voltage and Load Capacitance

7 Parameter Measurement Information

7.1 (Propagation Delays, Setup and Hold Times, and Pulse Width)



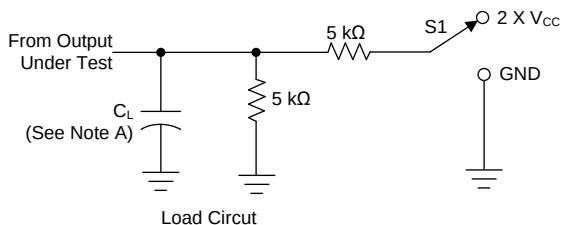
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- Notes:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r / t_f = 3 \text{ ns}$.
 - C. The outputs are measured one at a time, with one transition per measurement.
 - D. t_{PLH} And t_{PHL} Are the same as T_{pd} .
 - E. All parameters and waveforms are not applicable in all devices.

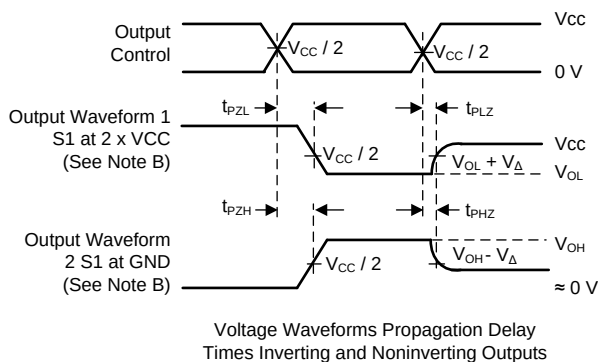
Figure 2. Load Circuit and Voltage Waveforms

7.2 (Enable and Disable Times)



Test	S1
t_{PLZ} / t_{PZL} t_{PHZ} / t_{PZH}	2 x V_{CC} GND

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$	$V_{CC} / 2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_A						



- Notes:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r / t_f = 3 \text{ ns}$
 - D. The outputs are measured one at a time, with one transmission per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family of devices is specified for low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see [Figure 7](#) and [Figure 8](#)).

The SN74AUP1G126 device contains one buffer gate device with output enable control and performs the Boolean function $Y = A$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

To assure the high-impedance state during power up or power down, OE must be tied to GND through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram

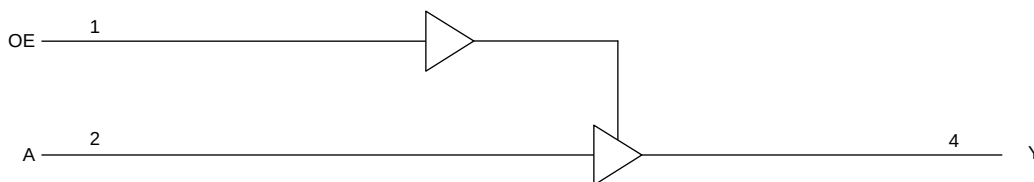


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs must have fast edge rates, as defined by $\Delta t/\Delta v$ in [Recommended Operating Conditions](#) to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

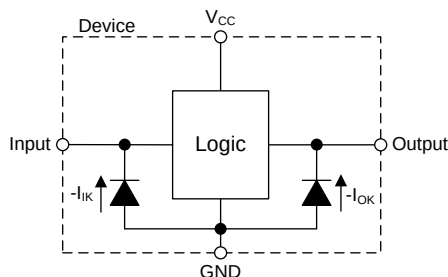


Figure 5. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Electrical Characteristics](#).

8.3.5 Overvoltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Absolute Maximum Ratings](#).

8.3.6 Output Enable

This device has an output enable (OE) pin that functions according to [Table 1](#). When the outputs of the device are disabled, they are placed into a high impedance state where it will neither source nor sink current. High-impedance outputs are also commonly referred to as three-state or tri-state outputs. The maximum leakage for the output in this state is defined by I_{OZ} in the [Electrical Characteristics](#) table.

8.4 Device Functional Modes

[Table 1](#) lists the functional modes of the SN74AUP1G126 device.

Table 1. Function Table

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AUP1G126 device is an output enabled CMOS buffer that can be used in LED indicator applications that require less than 4 mA. The device can produce up to 4 mA of drive current at 3.3 V. The inputs to the device are also overvoltage tolerant up to 3.6 V, allowing it to translate down to any valid V_{CC} .

9.2 Typical Application

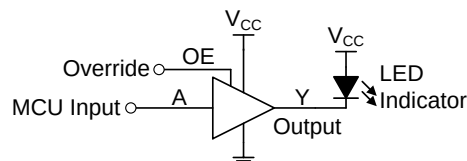


Figure 6. Application Schematic with MCU driving an LED Indicator

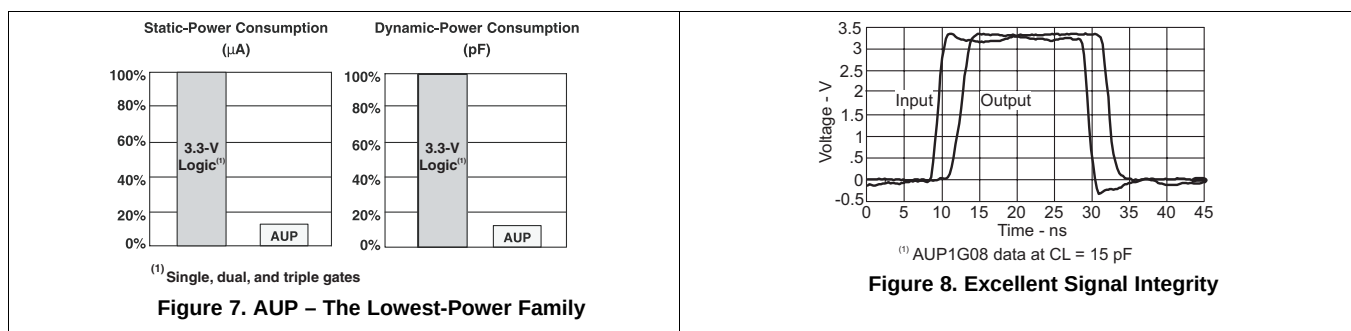
9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The output drive strength of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the [Recommended Operating Conditions](#) table at any valid V_{CC} .
2. Recommended Output Conditions
 - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
 - Outputs should not be pulled above V_{CC} .

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

The VCC pin must have a good bypass capacitor to prevent power disturbance. TI recommends to use a 0.1- μ F capacitor for this device. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. Install the bypass capacitor as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

An example layout is given in for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout.

11.2 Layout Example

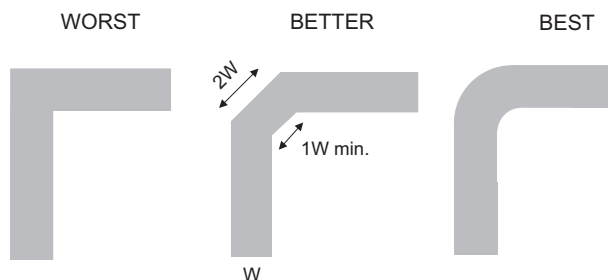


Figure 9. Trace Example

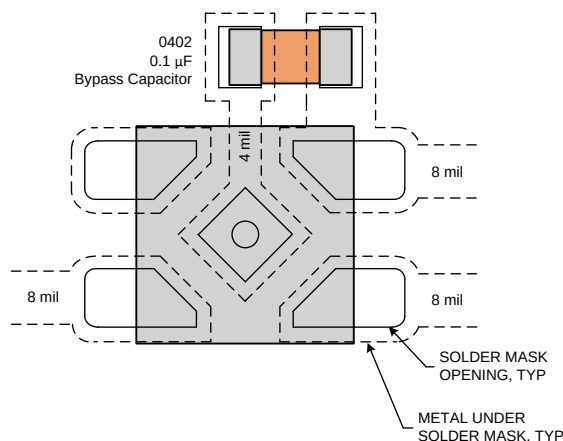


Figure 10. Example Layout With DPW (X2SON-5) Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow of Floating CMOS Inputs application report](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoStar, E2E are trademarks of Texas Instruments.
BluRay is a trademark of Blu-ray Disc Association (BDA).
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP1G126DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H26R
SN74AUP1G126DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H26R
SN74AUP1G126DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H26R
SN74AUP1G126DBVRG4.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H26R
SN74AUP1G126DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H26R
SN74AUP1G126DBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H26R
SN74AUP1G126DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(HN5, HNF, HNK, HN R)
SN74AUP1G126DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(HN5, HNF, HNK, HN R)
SN74AUP1G126DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(HN5, HNR)
SN74AUP1G126DCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(HN5, HNR)
SN74AUP1G126DPWR	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C4
SN74AUP1G126DPWR.B	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C4
SN74AUP1G126DRLR	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HN7, HNR)
SN74AUP1G126DRLR.B	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HN7, HNR)
SN74AUP1G126DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HN
SN74AUP1G126DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HN
SN74AUP1G126DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HN
SN74AUP1G126DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HN
SN74AUP1G126DSFRG4	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HN
SN74AUP1G126DSFRG4.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HN
SN74AUP1G126YFPR	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	HNN
SN74AUP1G126YFPR.B	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HNN
SN74AUP1G126YZPR	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HNN
SN74AUP1G126YZPR.B	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HNN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

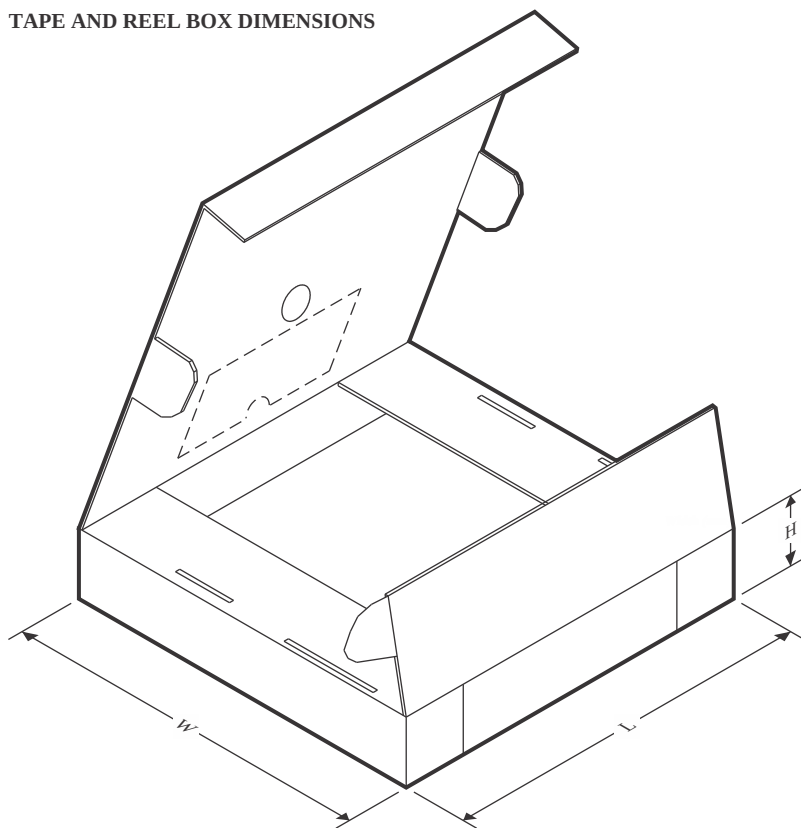


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G126DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G126DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G126DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G126DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G126DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G126DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G126DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G126DCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G126DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G126DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G126DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G126DRLR	SOT-5X3	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G126DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G126DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1G126DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74AUP1G126DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G126DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G126DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G126YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G126YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G126DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G126DBVRG4	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G126DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G126DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AUP1G126DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G126DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G126DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G126DCKT	SC70	DCK	5	250	210.0	185.0	35.0
SN74AUP1G126DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G126DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G126DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G126DRLR	SOT-5X3	DRL	5	4000	184.0	184.0	19.0
SN74AUP1G126DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G126DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1G126DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74AUP1G126DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G126DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G126DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0

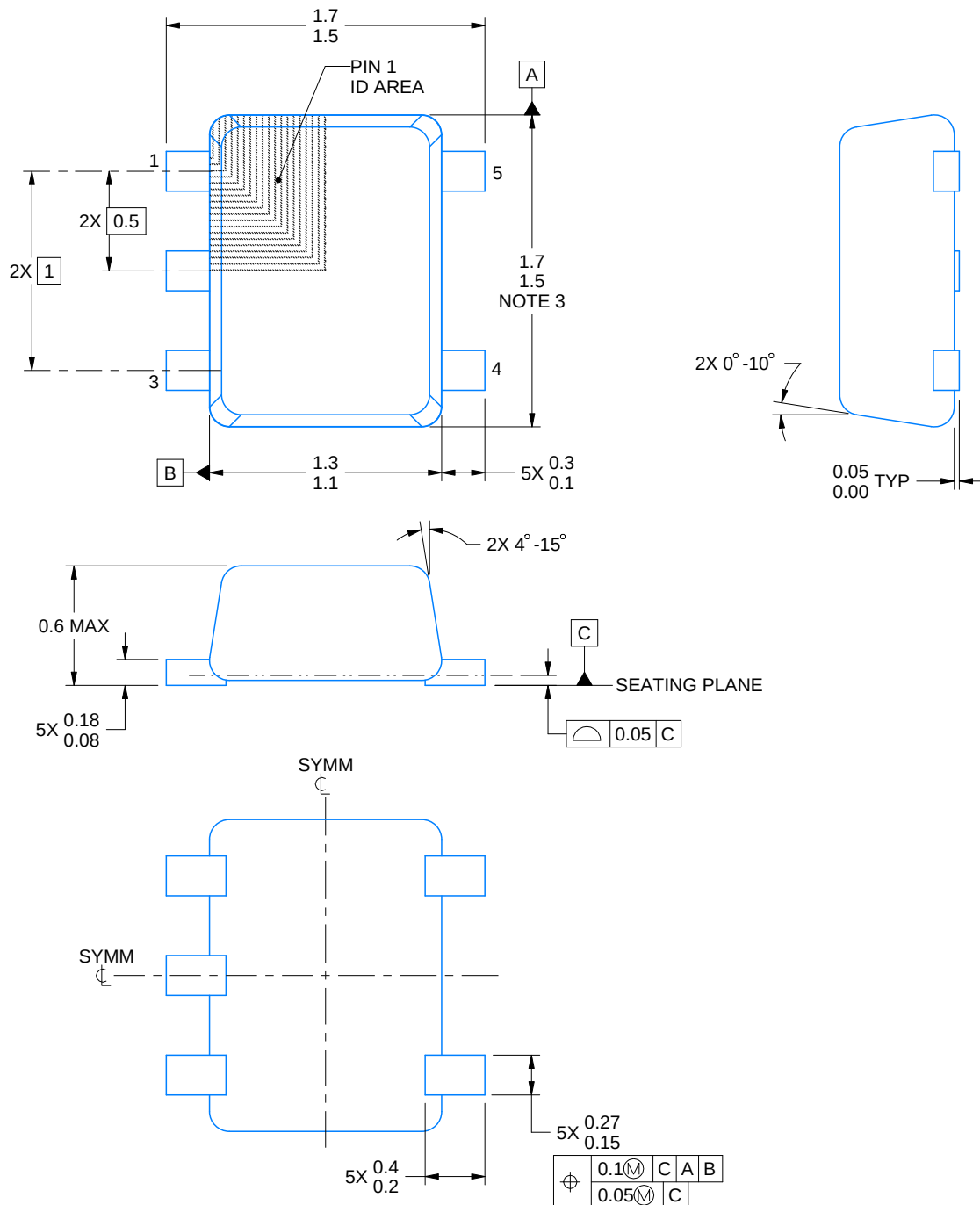
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G126YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G126YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DRL0005A

PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/E 11/2024

NOTES:

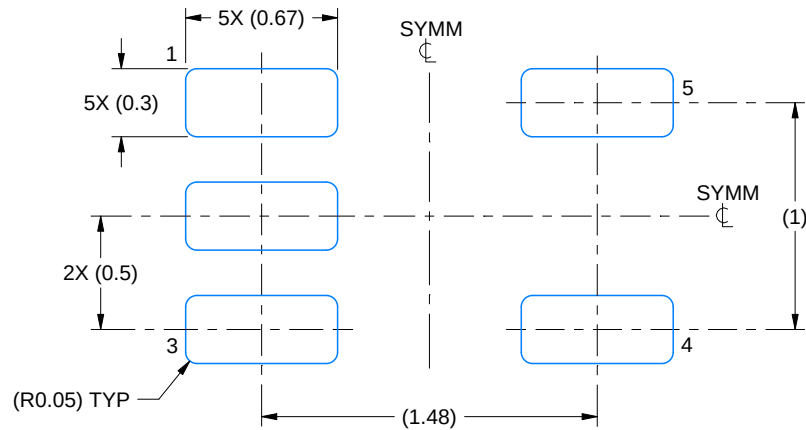
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

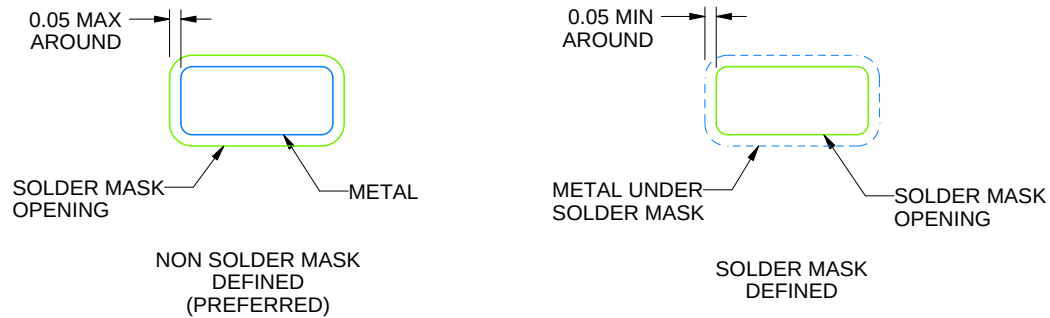
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

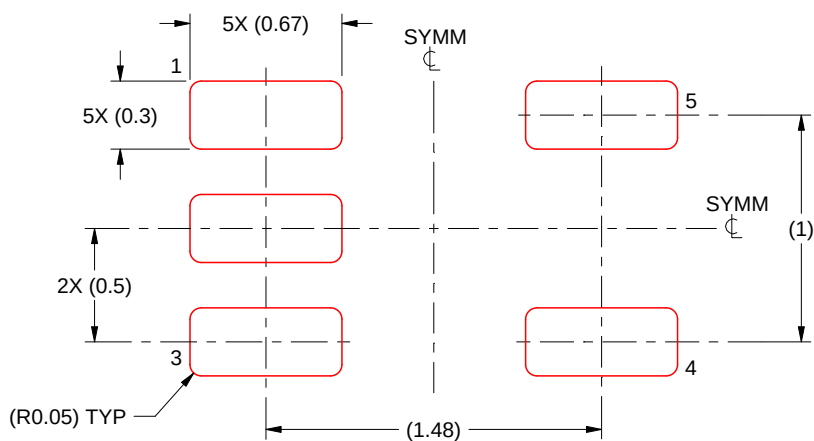
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

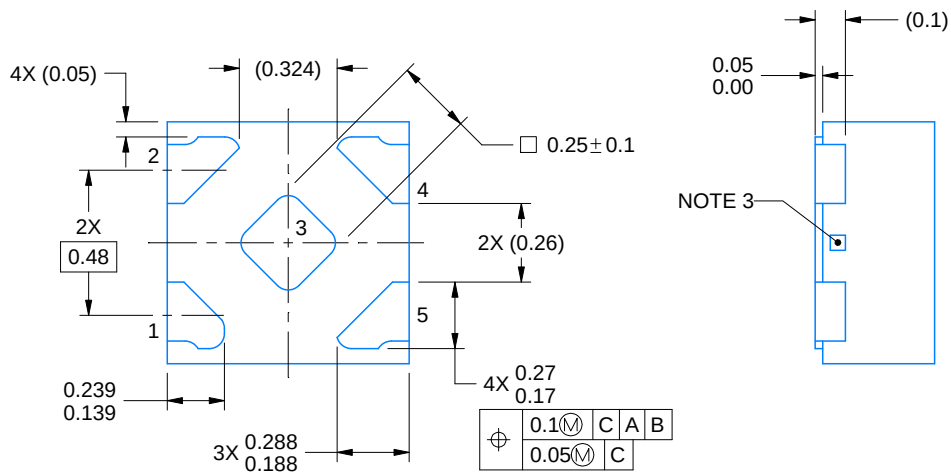
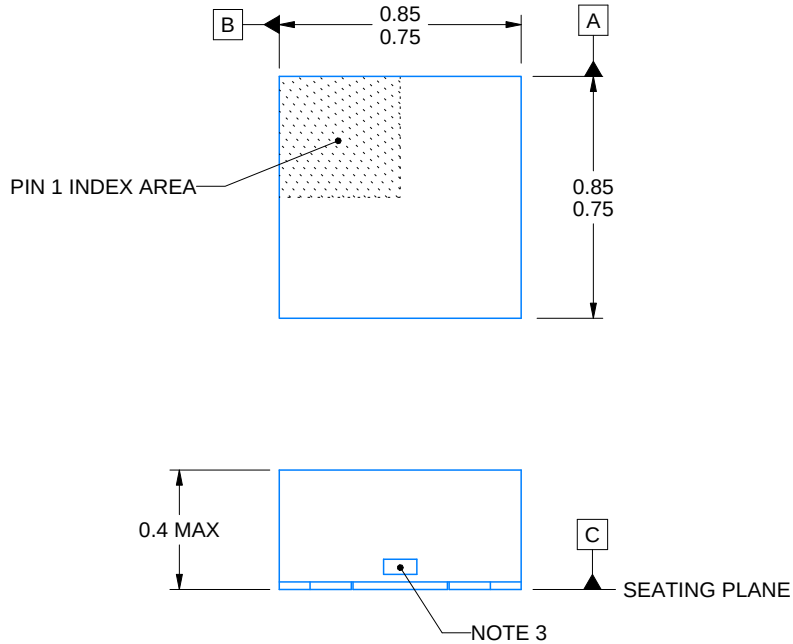
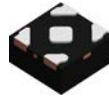
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

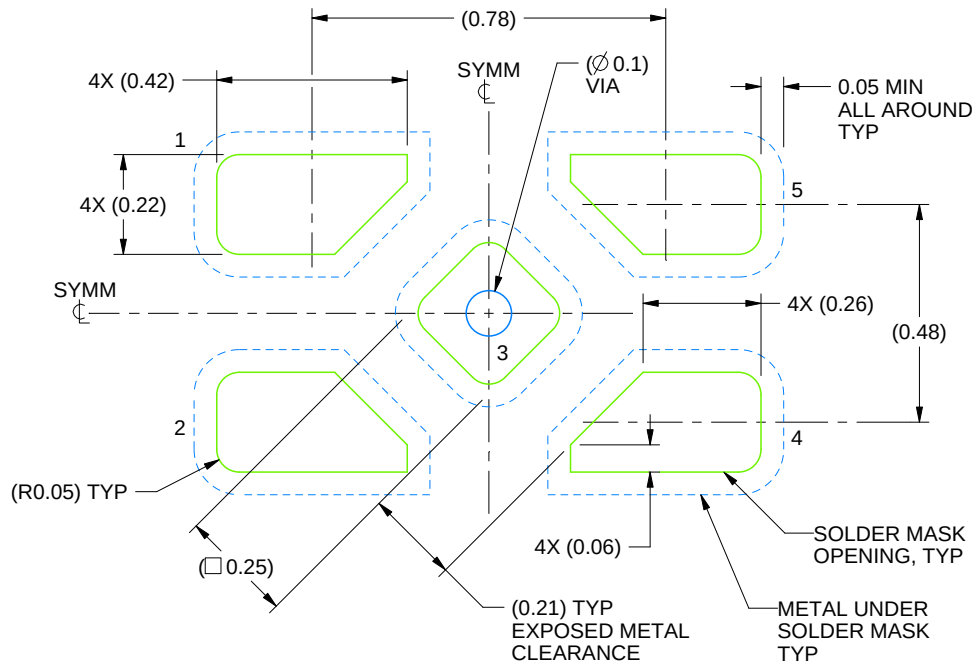
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

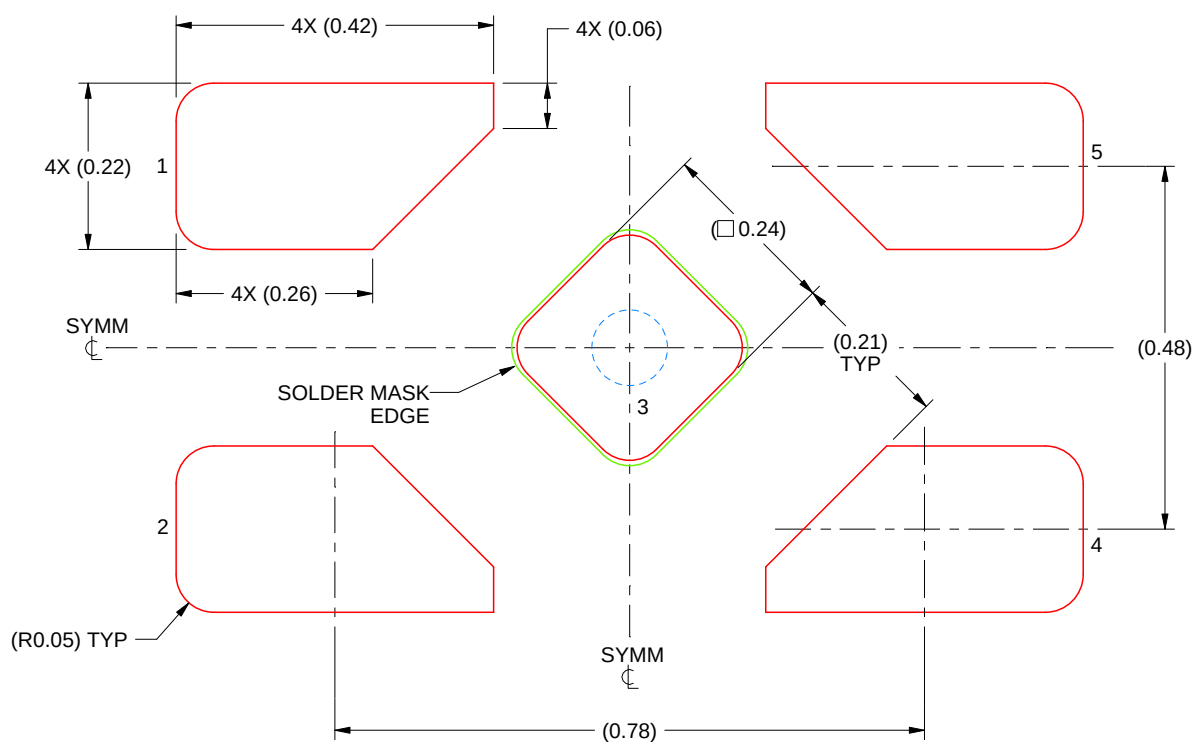
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

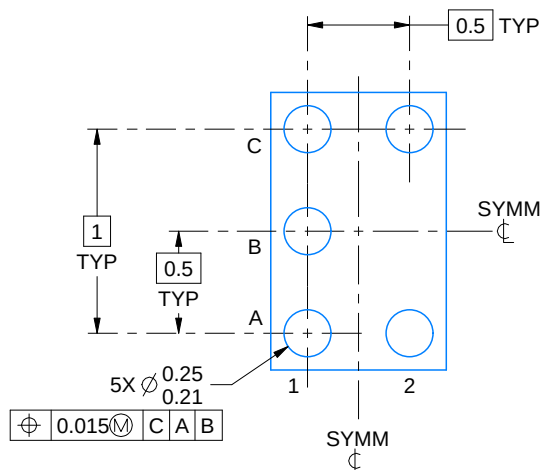
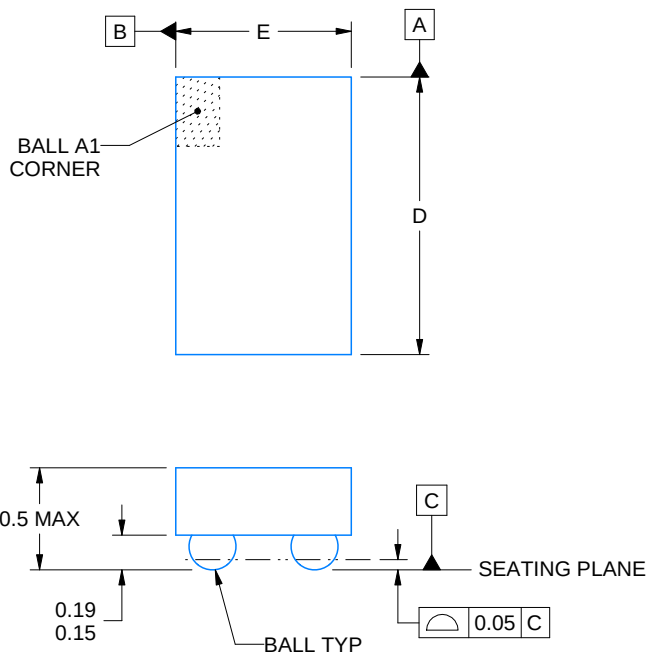
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min = 1.358 mm

E: Max = 0.918 mm, Min = 0.858 mm

4219492/A 05/2017

NOTES:

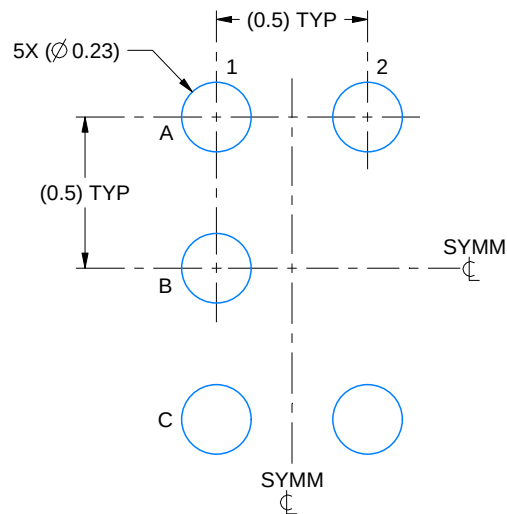
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

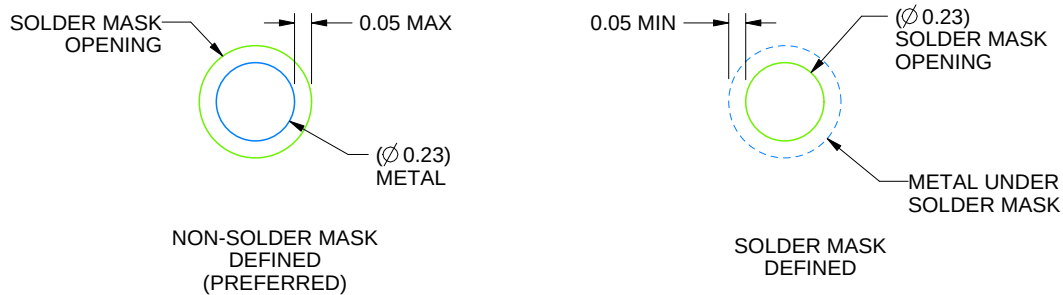
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

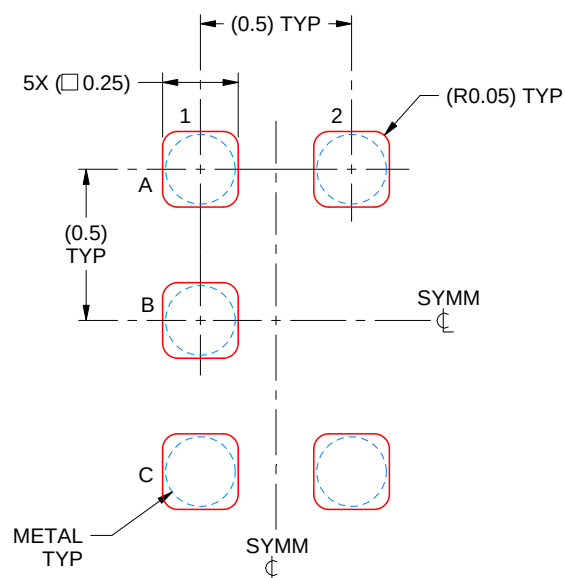
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

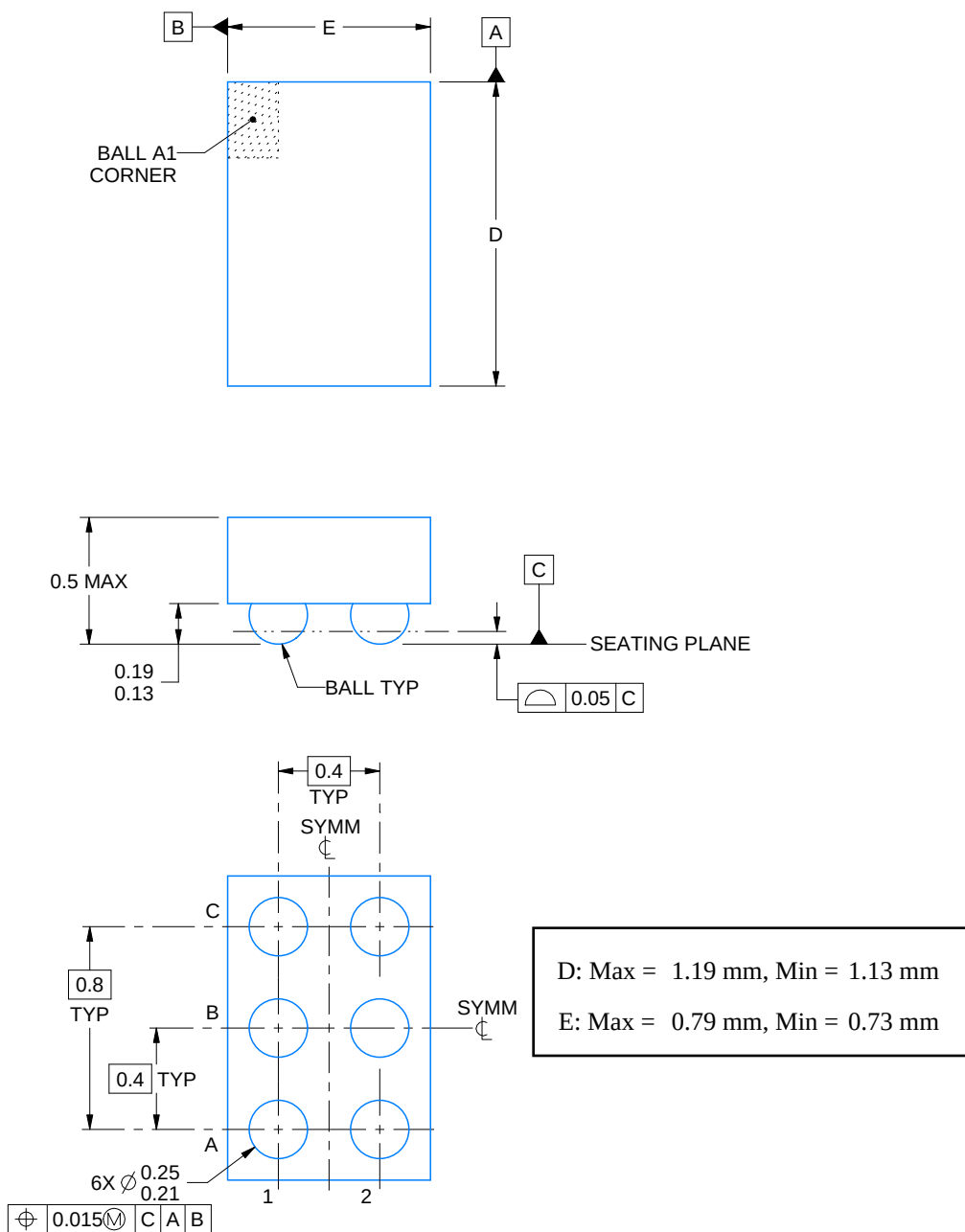
YFP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223410/A 11/2016

NOTES:

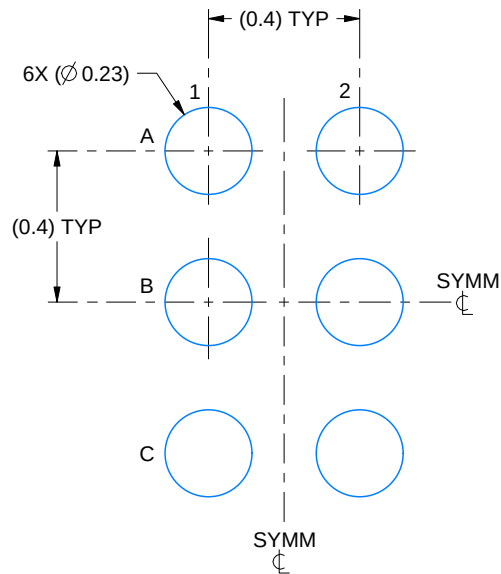
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

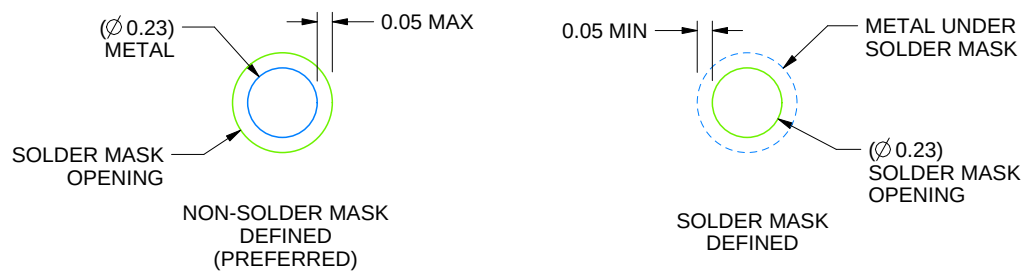
YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

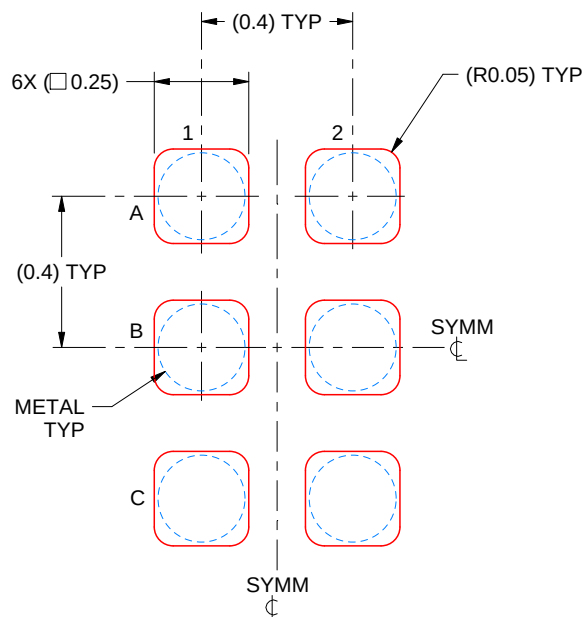
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

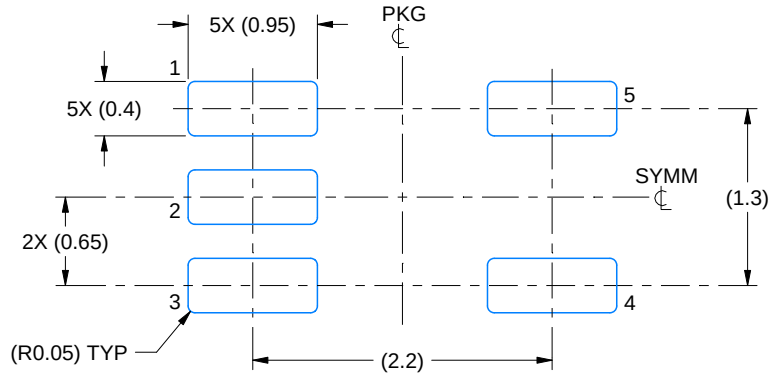


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

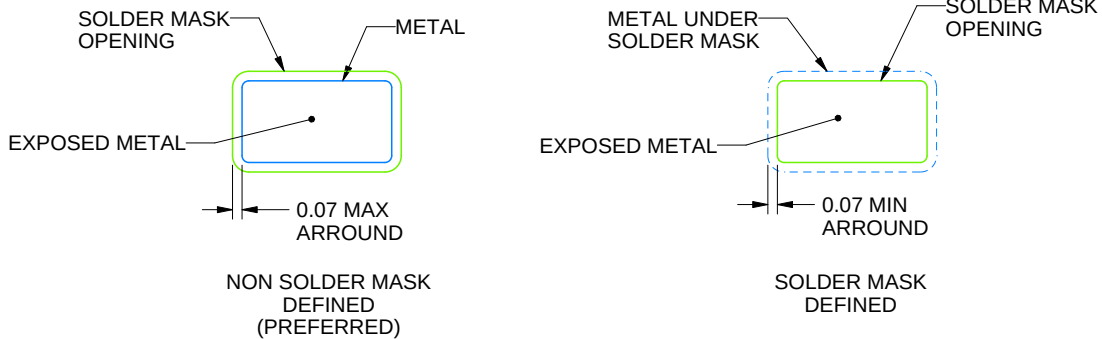
4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

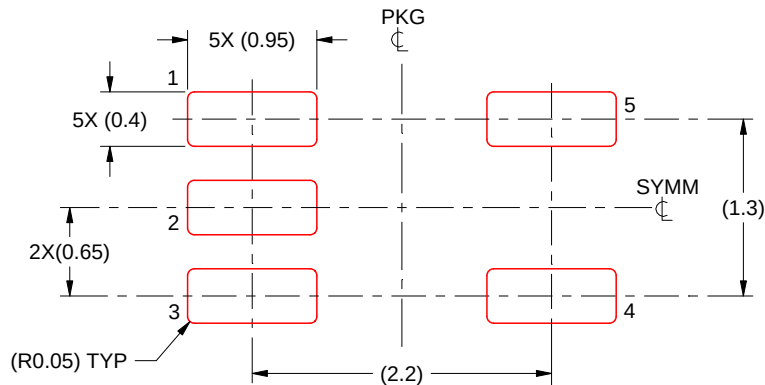


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



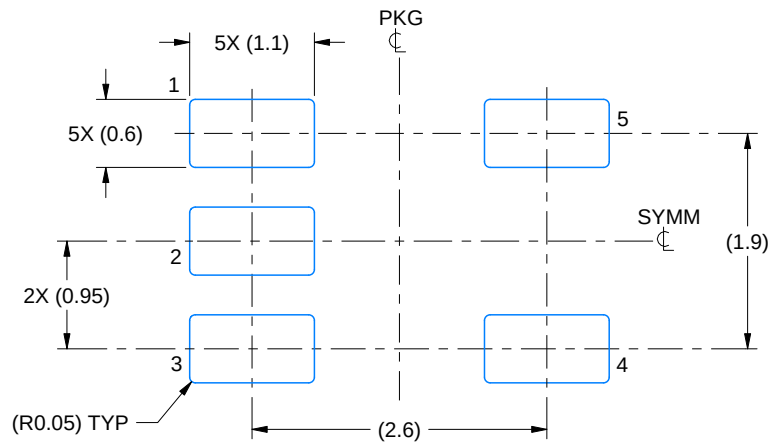
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

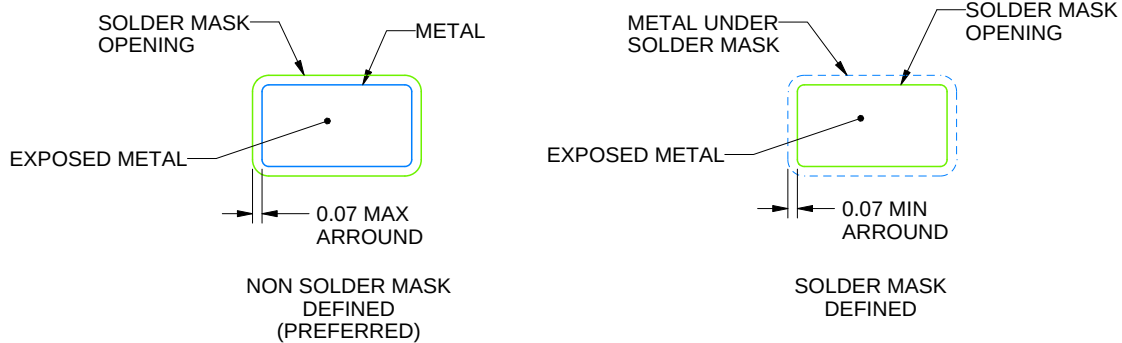
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

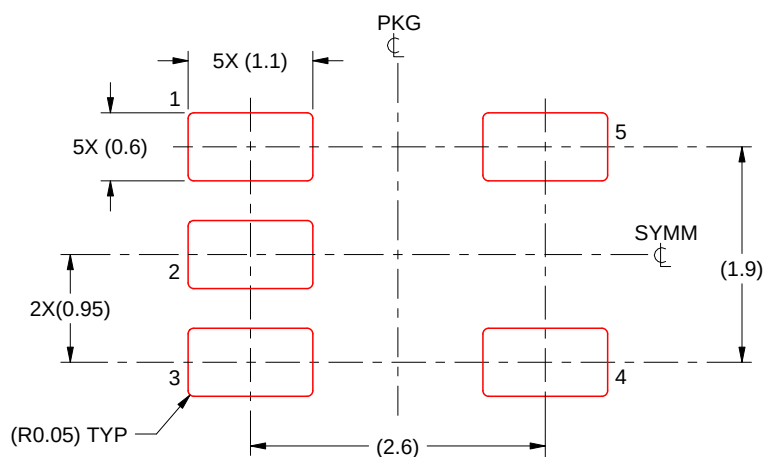
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

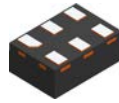
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

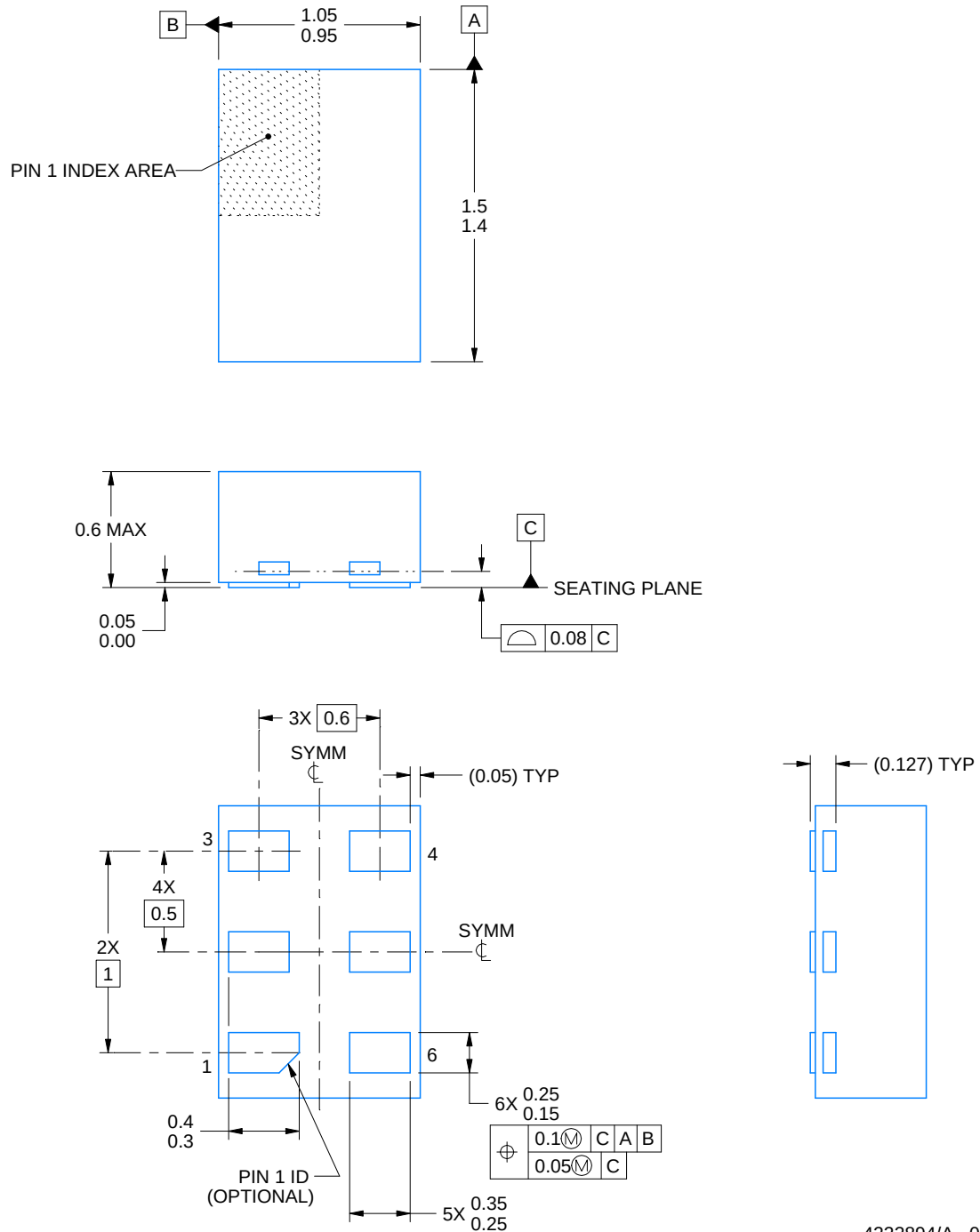
DRY0006A



PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

NOTES:

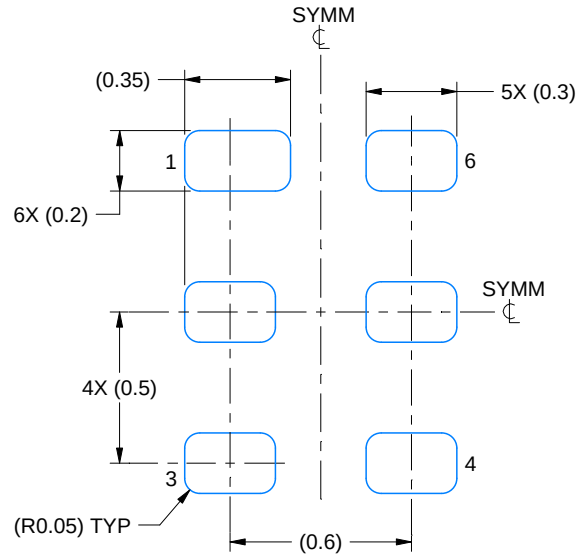
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

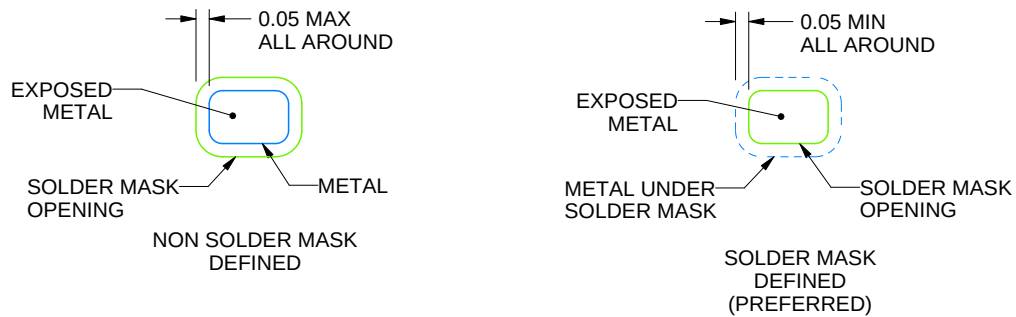
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

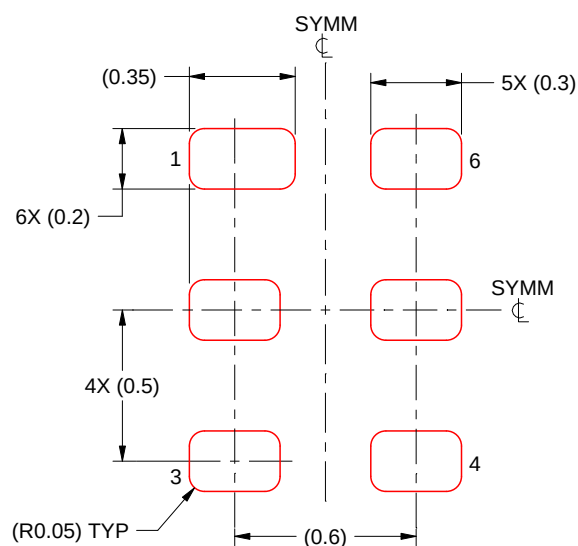
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

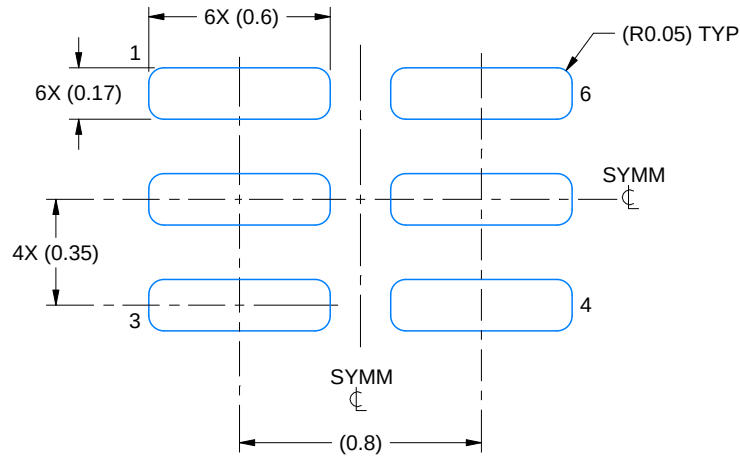
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

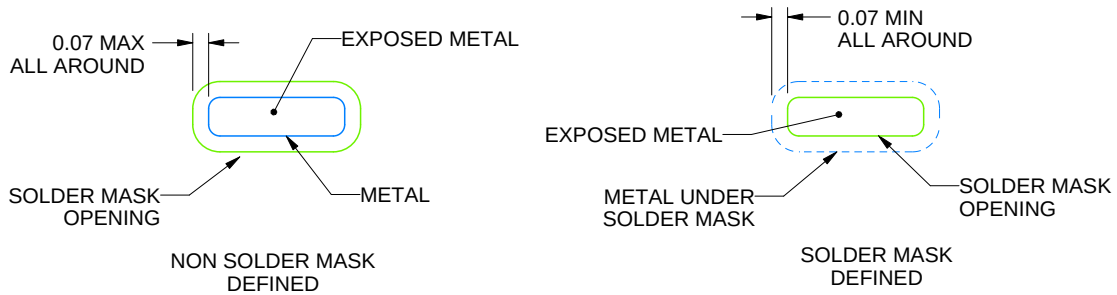
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

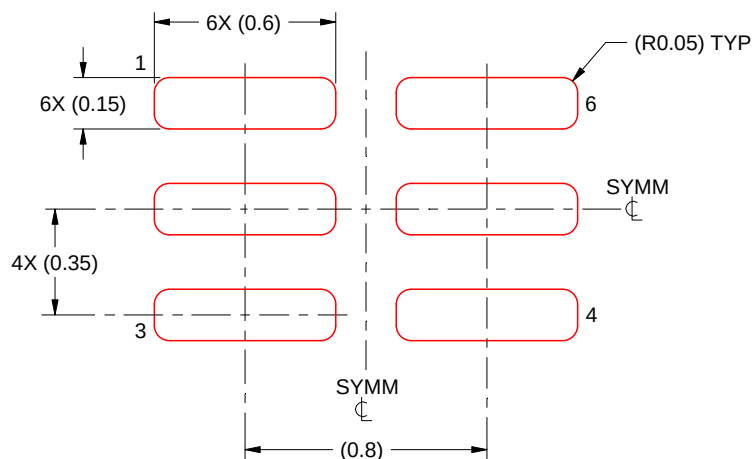
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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