

# SN54AS808B, SN74AS808B HEX 2-INPUT AND DRIVERS

SDAS018C – DECEMBER 1982 – REVISED JANUARY 1995

- High Capacitive-Drive Capability
- Typical Delay Time of 3.2 ns ( $C_L = 50$  pF) and Typical Power Dissipation of Less Than 13 mW Per Gate
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

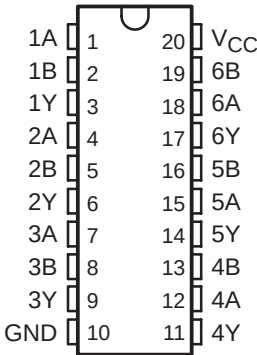
These devices contain six independent 2-input AND drivers. They perform the Boolean functions  $Y = A \bullet B$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

The SN54AS808B is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74AS808B is characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .

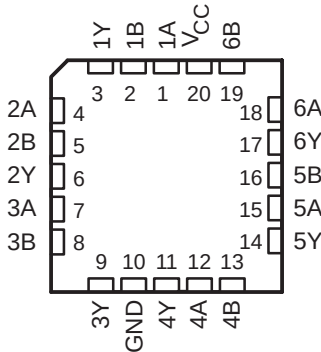
FUNCTION TABLE  
(each driver)

| INPUTS |   | OUTPUT<br>Y |
|--------|---|-------------|
| A      | B |             |
| H      | H | H           |
| L      | X | L           |
| X      | L | L           |

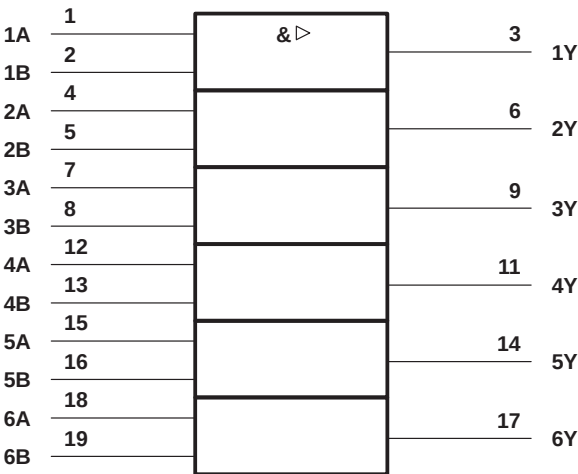
SN54AS808B . . . J PACKAGE  
SN74AS808B . . . DW OR N PACKAGE  
(TOP VIEW)



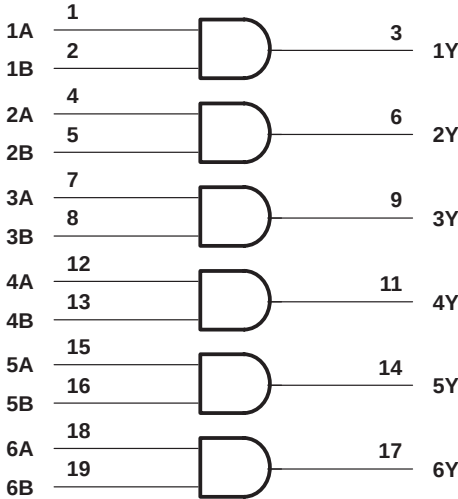
SN54AS808B . . . FK PACKAGE  
(TOP VIEW)



## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54AS808B, SN74AS808B HEX 2-INPUT AND DRIVERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                          |                |
|----------------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$                                 | 7 V            |
| Input voltage, $V_I$                                     | 7 V            |
| Operating free-air temperature range, $T_A$ : SN54AS808B | –55°C to 125°C |
| SN74AS808B                                               | 0°C to 70°C    |
| Storage temperature range                                | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

|          |                                | SN54AS808B |     |     | SN74AS808B |     |     | UNIT |
|----------|--------------------------------|------------|-----|-----|------------|-----|-----|------|
|          |                                | MIN        | NOM | MAX | MIN        | NOM | MAX |      |
| $V_{CC}$ | Supply voltage                 | 4.5        | 5   | 5.5 | 4.5        | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage       | 2          |     |     | 2          |     |     | V    |
| $V_{IL}$ | Low-level input voltage        |            |     | 0.8 |            |     | 0.8 | V    |
| $I_{OH}$ | High-level output current      |            |     | –40 |            |     | –48 | mA   |
| $I_{OL}$ | Low-level output current       |            |     | 40  |            |     | 48  | mA   |
| $T_A$    | Operating free-air temperature | –55        |     | 125 | 0          |     | 70  | °C   |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER    | TEST CONDITIONS            |                   | SN54AS808B   |                  |      | SN74AS808B   |                  |      | UNIT |
|--------------|----------------------------|-------------------|--------------|------------------|------|--------------|------------------|------|------|
|              |                            |                   | MIN          | TYP <sup>‡</sup> | MAX  | MIN          | TYP <sup>‡</sup> | MAX  |      |
| $V_{IK}$     | $V_{CC} = 4.5$ V,          | $I_I = -18$ mA    |              |                  | –1.2 |              |                  | –1.2 | V    |
| $V_{OH}$     | $V_{CC} = 4.5$ V to 5.5 V, | $I_{OH} = -2$ mA  | $V_{CC} - 2$ |                  |      | $V_{CC} - 2$ |                  |      | V    |
|              | $V_{CC} = 4.5$ V           | $I_{OH} = -3$ mA  | 2.4          | 3.2              |      | 2.4          | 3.2              |      |      |
|              |                            | $I_{OH} = -40$ mA | 2            |                  |      |              |                  |      |      |
|              |                            | $I_{OH} = -48$ mA |              |                  |      | 2            |                  |      |      |
| $V_{OL}$     | $V_{CC} = 4.5$ V           | $I_{OL} = 40$ mA  |              | 0.25             | 0.5  |              |                  |      | V    |
|              |                            | $I_{OL} = 48$ mA  |              |                  |      | 0.35         | 0.5              |      |      |
| $I_I$        | $V_{CC} = 5.5$ V,          | $V_I = 7$ V       |              |                  | 0.1  |              |                  | 0.1  | mA   |
| $I_{IH}$     | $V_{CC} = 5.5$ V,          | $V_I = 2.7$ V     |              |                  | 20   |              |                  | 20   | μA   |
| $I_{IL}$     | $V_{CC} = 5.5$ V,          | $V_I = 0.4$ V     |              |                  | –0.5 |              |                  | –0.5 | mA   |
| $I_{O}^{\S}$ | $V_{CC} = 5.5$ V,          | $V_O = 2.25$ V    | –50          |                  | –200 | –50          |                  | –200 | mA   |
| $I_{CCH}$    | $V_{CC} = 5.5$ V,          | $V_I = 4.5$ V     |              | 8                | 13   |              | 8                | 13   | mA   |
| $I_{CCL}$    | $V_{CC} = 5.5$ V,          | $V_I = 0$         |              | 20               | 33   |              | 20               | 33   | mA   |

<sup>‡</sup> All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

<sup>\S</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



# SN54AS808B, SN74AS808B HEX 2-INPUT AND DRIVERS

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## switching characteristics (see Figure 1)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R <sub>L</sub> = 500 Ω,<br>T <sub>A</sub> = MIN to MAX <sup>†</sup> |     |            |     | UNIT |
|------------------|-----------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------|-----|------------|-----|------|
|                  |                 |                | SN54AS808B                                                                                                                          |     | SN74AS808B |     |      |
|                  |                 |                | MIN                                                                                                                                 | MAX | MIN        | MAX |      |
| t <sub>PLH</sub> | A or B          | Y              | 1                                                                                                                                   | 6.5 | 1          | 6   | ns   |
| t <sub>PHL</sub> |                 |                | 1                                                                                                                                   | 6.5 | 1          | 6   |      |

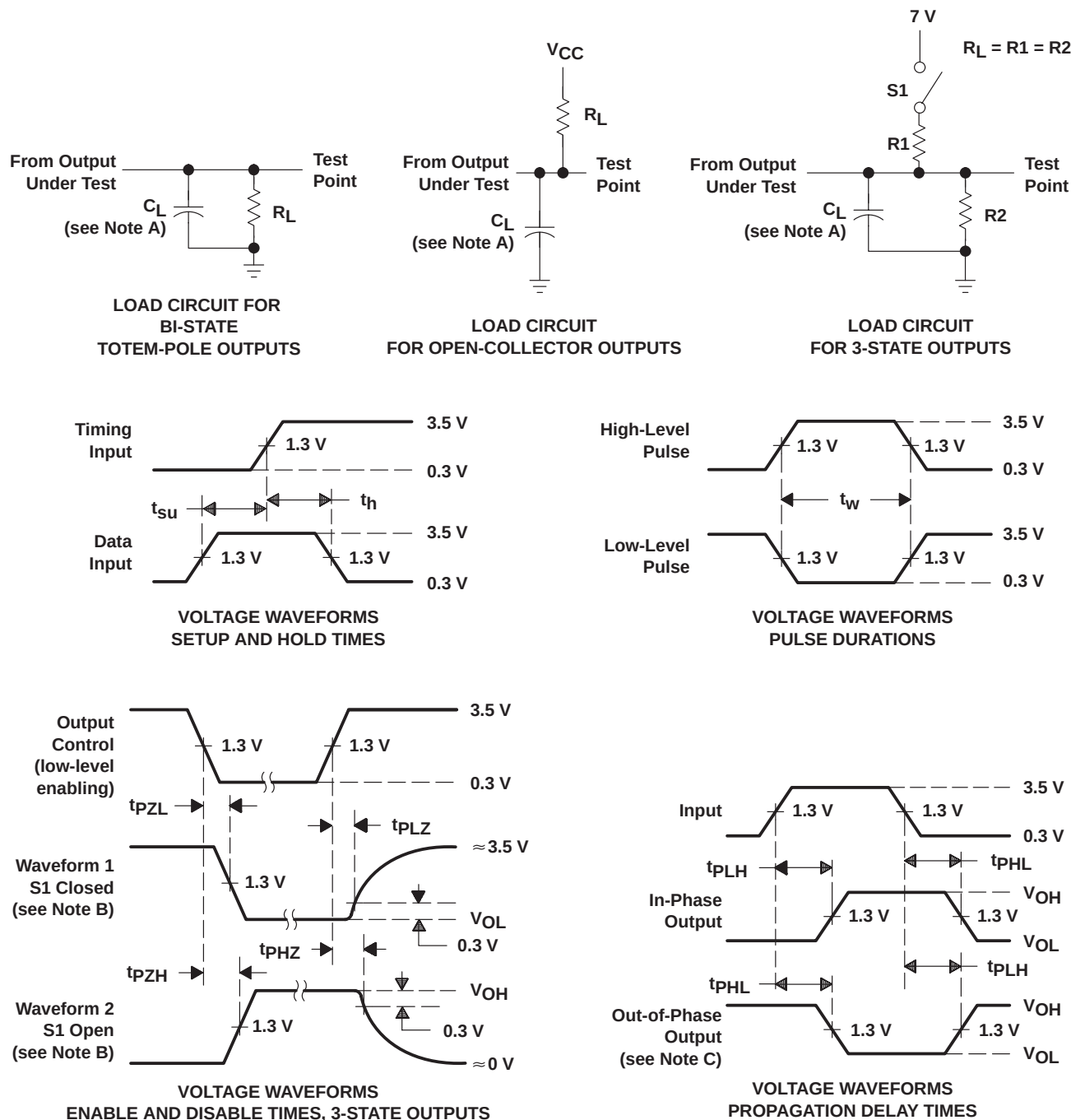
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# SN54AS808B, SN74AS808B HEX 2-INPUT AND DRIVERS

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                      |
|--------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------------------|
| <a href="#">5962-88522012A</a> | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>88522012A<br>SNJ54AS<br>808BFBK |
| <a href="#">5962-8852201RA</a> | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8852201RA<br>SNJ54AS808BJ           |
| <a href="#">SN54AS808BJ</a>    | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54AS808BJ                              |
| SN54AS808BJ.A                  | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54AS808BJ                              |
| <a href="#">SN74AS808BDW</a>   | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | AS808B                                   |
| SN74AS808BDW.A                 | Active        | Production           | SOIC (DW)   20 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | AS808B                                   |
| <a href="#">SN74AS808BN</a>    | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74AS808BN                              |
| SN74AS808BN.A                  | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74AS808BN                              |
| <a href="#">SNJ54AS808BFBK</a> | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>88522012A<br>SNJ54AS<br>808BFBK |
| SNJ54AS808BFBK.A               | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>88522012A<br>SNJ54AS<br>808BFBK |
| <a href="#">SNJ54AS808BJ</a>   | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8852201RA<br>SNJ54AS808BJ           |
| SNJ54AS808BJ.A                 | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8852201RA<br>SNJ54AS808BJ           |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54AS808B, SN74AS808B :**

- Catalog : [SN74AS808B](#)
- Military : [SN54AS808B](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TUBE



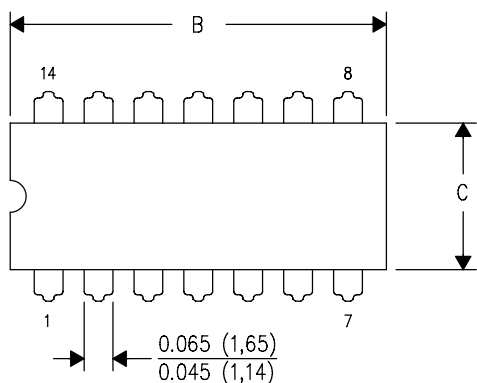
\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-88522012A  | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SN74AS808BDW    | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74AS808BDW.A  | DW           | SOIC         | 20   | 25  | 507    | 12.83  | 5080   | 6.6    |
| SN74AS808BN     | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SN74AS808BN.A   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54AS808BFK   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54AS808BFK.A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |

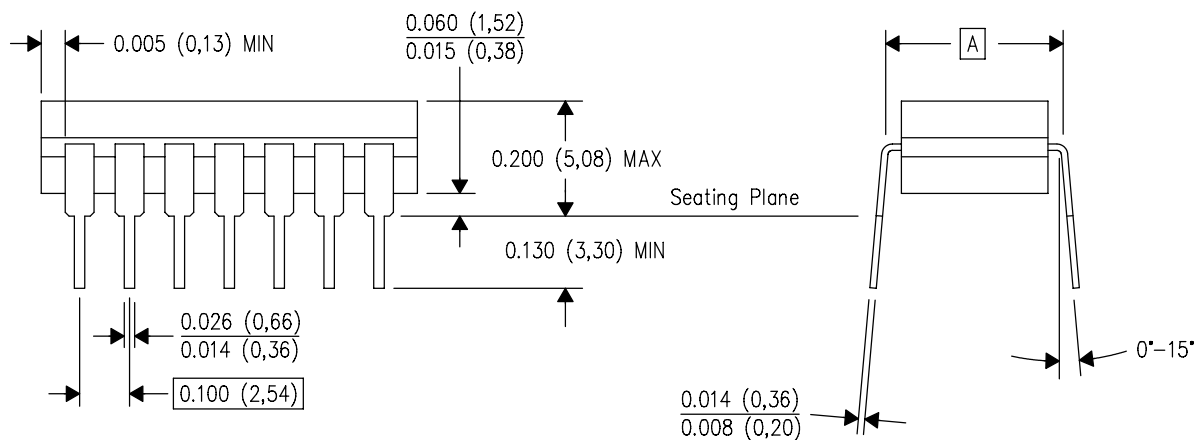
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



## GENERIC PACKAGE VIEW

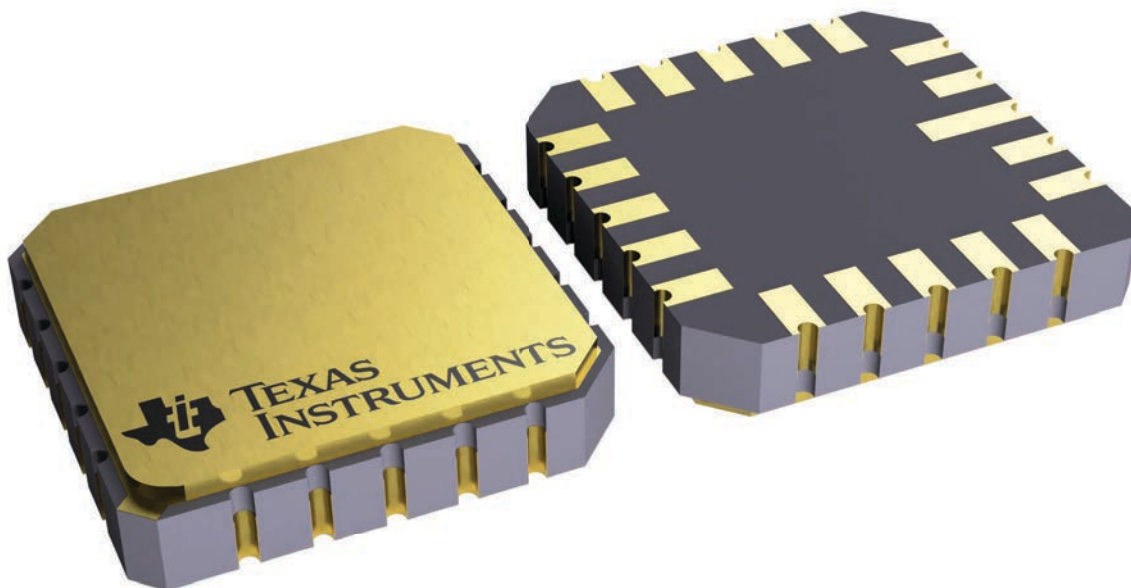
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

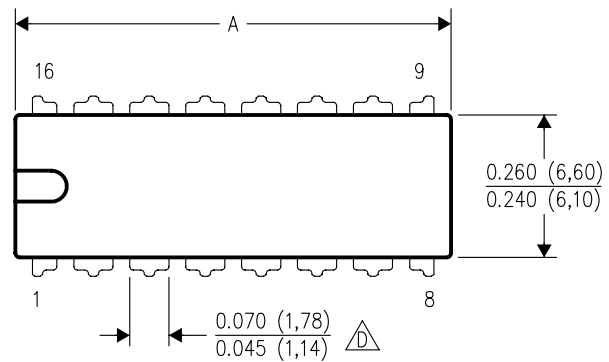


4229370VA\

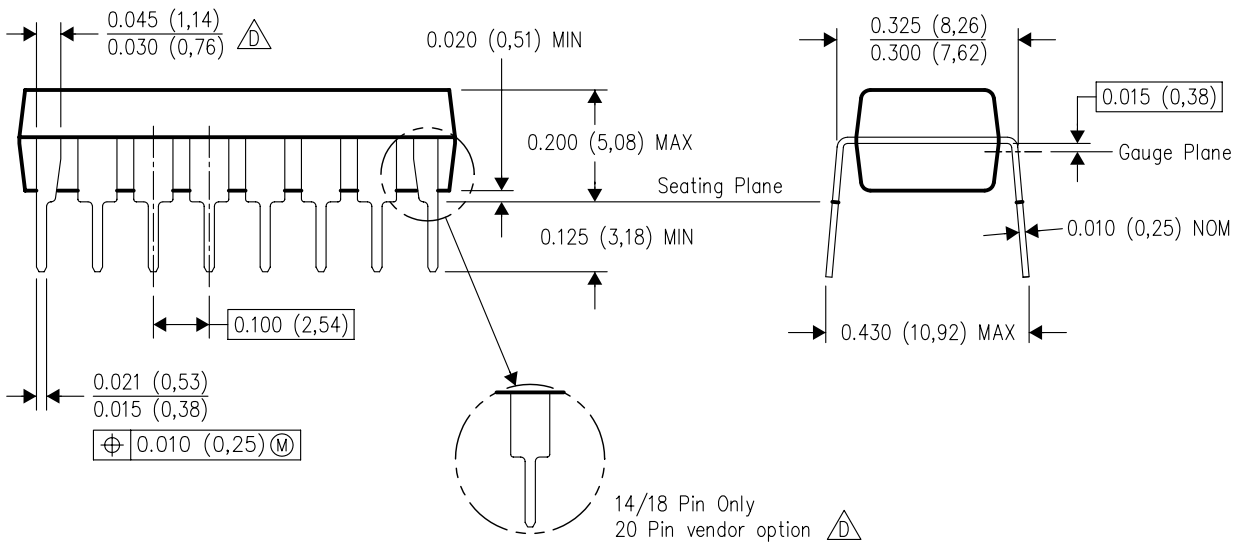
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

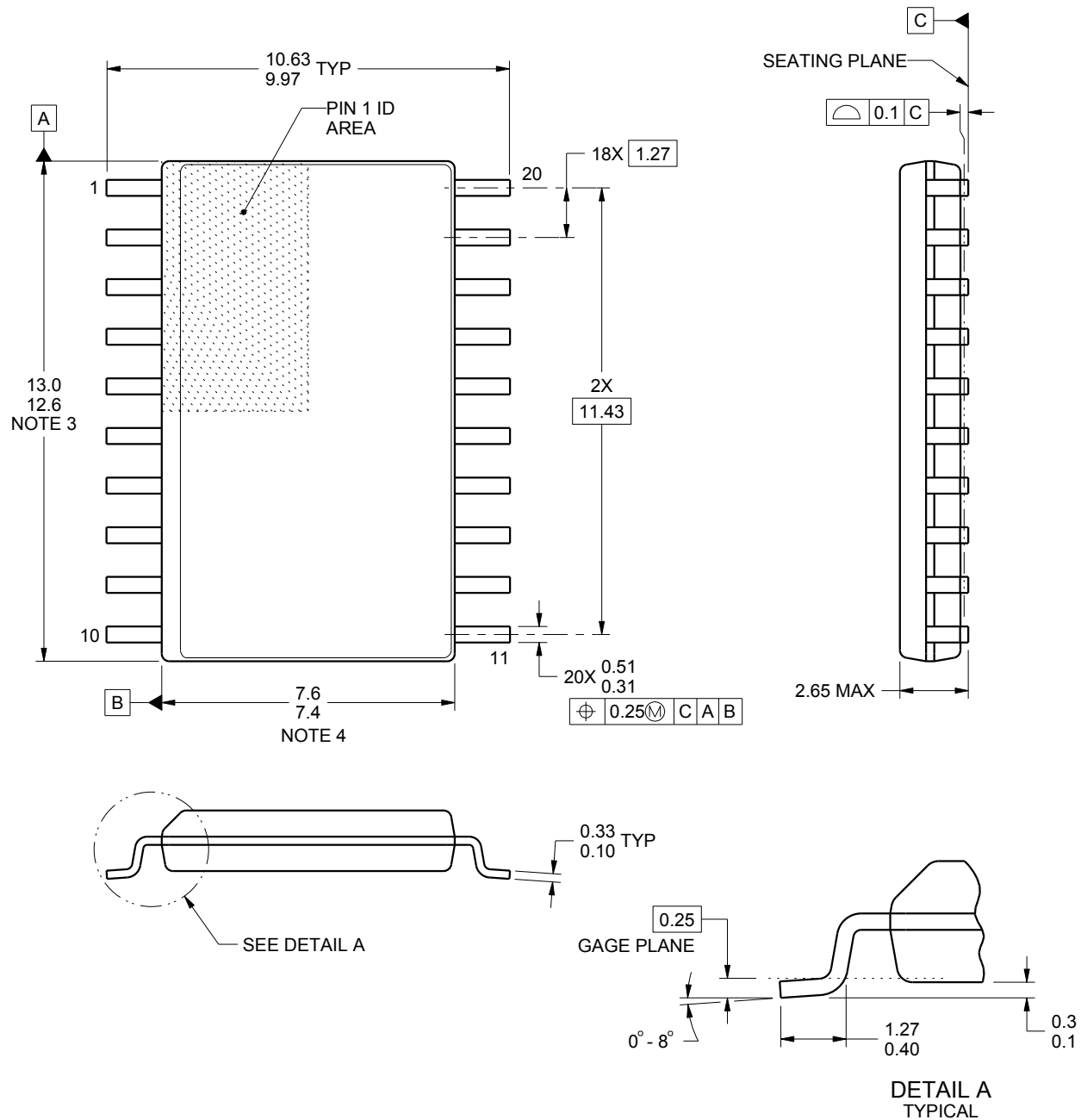
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

**DW0020A**

## PACKAGE OUTLINE

**SOIC - 2.65 mm max height**

SOIC



4220724/A 05/2016

NOTES:

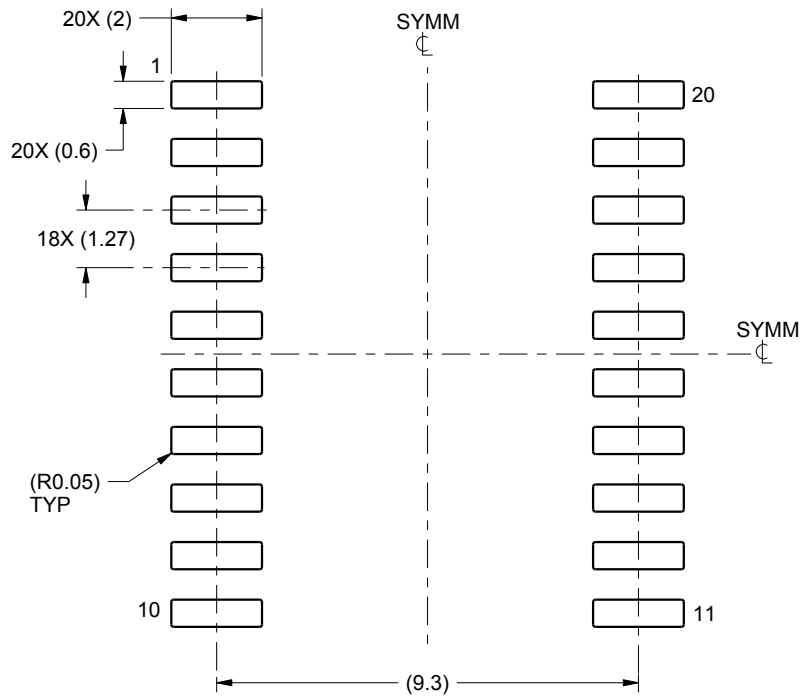
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

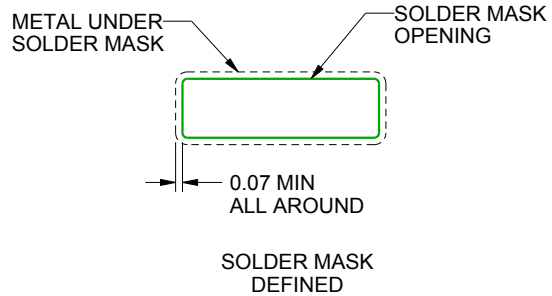
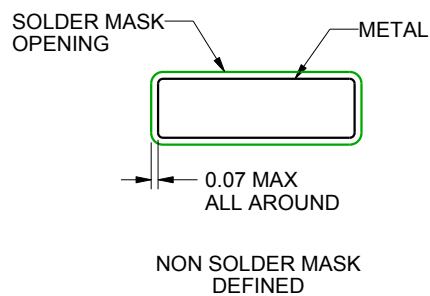
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

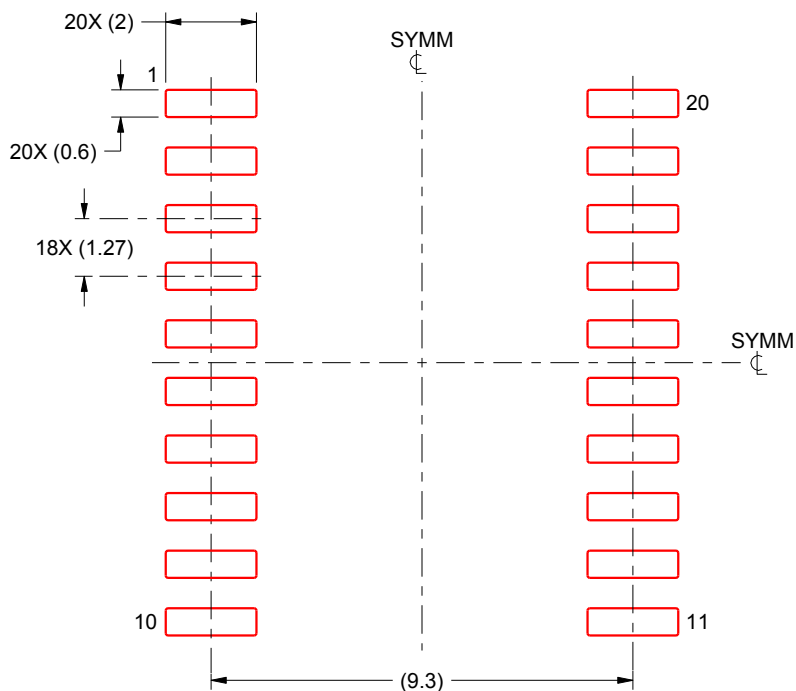
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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