

FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DESCRIPTION

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16270 is used in applications in which data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

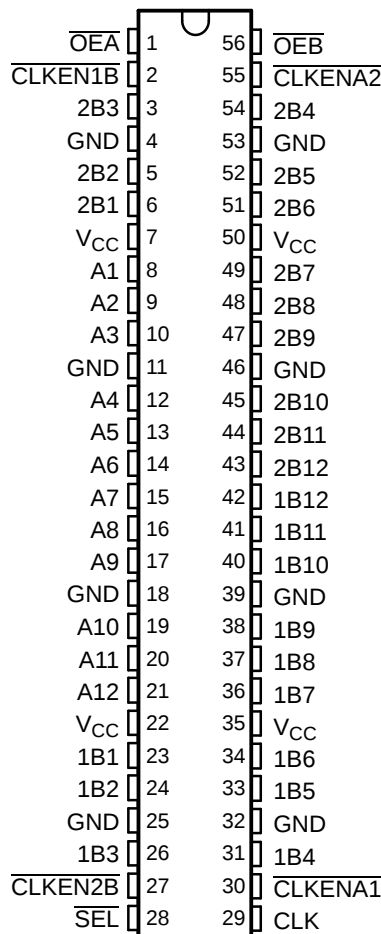
The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate $\overline{CLKEN}$ inputs are low. The select ($\overline{SEL}$) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path. Proper control of the $\overline{CLKENA}$ inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables ($\overline{OE_A}$, $\overline{OE_B}$). The control terminals are registered to synchronize the bus-direction changes with CLK.

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible, and $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to $\overline{OE}$ being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16270 is characterized for operation from -40°C to 85°C.

**DGG OR DL PACKAGE
(TOP VIEW)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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SN74ALVCH16270

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES028G--JULY 1995--REVISED AUGUST 2004

FUNCTION TABLES

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OE\overline{A}}$	$\overline{OE\overline{B}}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OE\overline{B}} = L$)

INPUTS				OUTPUTS	
$\overline{CLKEN\overline{A1}}$	$\overline{CLKEN\overline{A2}}$	CLK	A	1B	2B
L	H	X	X	1B ₀ ⁽¹⁾	2B ₀ ⁽¹⁾
L	H	X	X	1B ₀ ⁽¹⁾	2B ₀ ⁽¹⁾
L	L	↑	L	L ⁽²⁾	L
L	L	↑	H	H ⁽²⁾	H
H	L	↑	L	1B ₀ ⁽¹⁾	L
H	L	↑	H	1B ₀ ⁽¹⁾	H
H	H	X	X	1B ₀ ⁽¹⁾	2B ₀ ⁽¹⁾

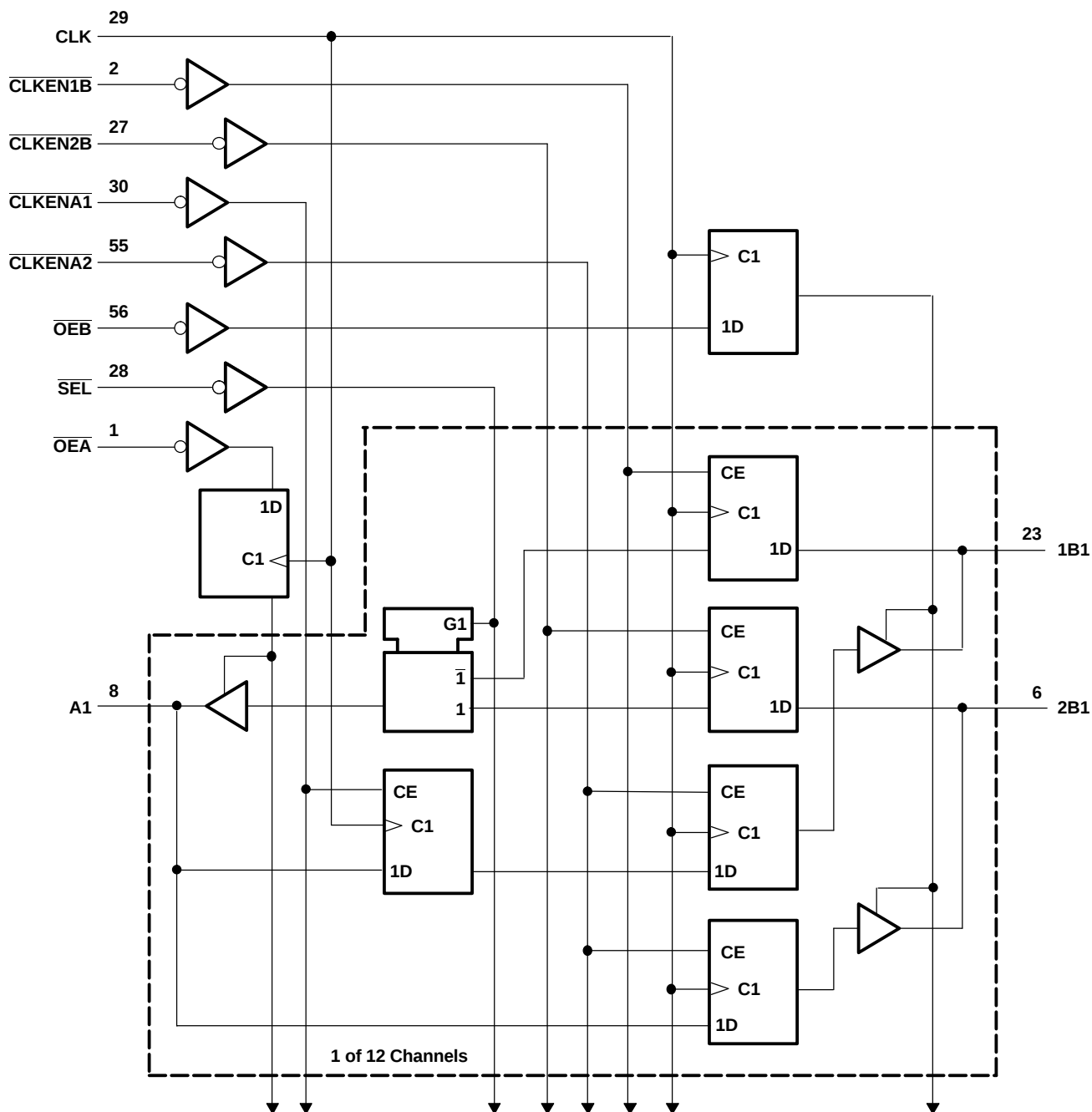
- (1) Output level before the indicated steady-state input conditions were established
(2) Two CLK edges are needed to propagate data.

B-TO-A STORAGE ($\overline{OE\overline{A}} = L$)

INPUTS						OUTPUT A
$\overline{CLKEN1\overline{B}}$	$\overline{CLKEN2\overline{B}}$	CLK	$\overline{SEL}$	1B	2B	
H	X	X	H	X	X	A ₀ ⁽¹⁾
X	H	X	L	X	X	A ₀ ⁽¹⁾
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

- (1) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



SN74ALVCH16270

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES028G–JULY 1995–REVISED AUGUST 2004

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage		-0.5	4.6	V	
V _I	Input voltage range	Except I/O ports ⁽²⁾	-0.5	4.6	V	
		I/O ports ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5		
V _O	Output voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0			-50	mA
I _{OK}	Output clamp current	V _O < 0			-50	mA
I _O	Continuous output current				±50	mA
Continuous current through each V _{CC} or GND					±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package			81	°C/W
		DL package			74	
T _{stg}	Storage temperature range		-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65		V
V_{IH}	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0.8	
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65 \text{ V}$	-4	mA
		$V_{CC} = 2.3 \text{ V}$	-12	
		$V_{CC} = 2.7 \text{ V}$	-12	
		$V_{CC} = 3 \text{ V}$	-24	
I_{OL}	Low-level output current	$V_{CC} = 1.65 \text{ V}$	4	mA
		$V_{CC} = 2.3 \text{ V}$	12	
		$V_{CC} = 2.7 \text{ V}$	12	
		$V_{CC} = 3 \text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}		I _{OH} = -100 µA	1.65 V to 3.6 V	V _{CC} - 0.2			V
		I _{OH} = -4 mA	1.65 V	1.2			
		I _{OH} = -6 mA	2.3 V	2			
		I _{OH} = -12 mA	2.3 V	1.7			
			2.7 V	2.2			
			3 V	2.4			
		I _{OH} = -24 mA	3 V	2			
V _{OL}		I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
		I _{OL} = 4 mA	1.65 V	0.45			
		I _{OL} = 6 mA	2.3 V	0.4			
		I _{OL} = 12 mA	2.3 V	0.7			
			2.7 V	0.4			
		I _{OL} = 24 mA	3 V	0.55			
I _I		V _I = V _{CC} or GND	3.6 V	±5			µA
I _{I(hold)}		V _I = 0.58 V	1.65 V	25			µA
		V _I = 1.07 V	1.65 V	-25			
		V _I = 0.7 V	2.3 V	45			
		V _I = 1.7 V	2.3 V	-45			
		V _I = 0.8 V	3 V	75			
		V _I = 2 V	3 V	-75			
		V _I = 0 to 3.6 V ⁽²⁾	3.6 V	±500			
I _{OZ} ⁽³⁾		V _O = V _{CC} or GND	3.6 V	±10			µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V	40			µA
ΔI _{CC}		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750			µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3.5			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	9			pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH16270

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES028G–JULY 1995–REVISED AUGUST 2004

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
f _{clock}	Clock frequency	(1)		150		150		150		MHz		
t _w	Pulse duration, CLK high or low	(1)		3.3		3.3		3.3		ns		
t _{su}	Setup time	A data before CLK↑		(1)		4.1		3.8		3.1		ns
		B data before CLK↑		(1)		0.9		1.2		0.9		
		CLKENA1 or CLKENA2 before CLK↑		(1)		3.5		3.2		2.7		
		CLKEN1B or CLKEN2B before CLK↑		(1)		3.4		3		2.6		
		OE data before CLK↑		(1)		4.4		3.9		3.2		
t _h	Hold time	A data after CLK↑		(1)		0		0		0.2		ns
		B data after CLK↑		(1)		1.4		1		1.7		
		CLKENA1 or CLKENA2 after CLK↑		(1)		0		0.1		0.3		
		CLKEN1B or CLKEN2B after CLK↑		(1)		0		0		0.6		
		OE after CLK↑		(1)		0		0		0.1		

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		150		150		150		MHz
t_{pd}	CLK	B	(1)		1.5	5.9	5.8		1.1	5.1	ns
		A	(1)		1.2	5.4	5.4		1	4.7	
	$\overline{\text{SEL}}$	A	(1)		1.4	6.2	6.4		1	5.5	
t_{en}	CLK	A or B	(1)		1.5	7	6.8		1	6	ns
t_{dis}	CLK	A or B	(1)		1.9	7.2	6.5		1.1	5.8	ns

(1) This information was not available at the time of publication.

OPERATING CHARACTERISTICS

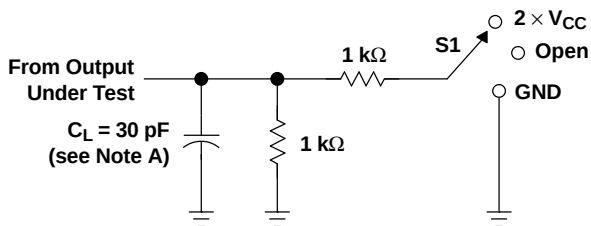
$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	(1)	87	120	pF
		Outputs disabled		(1)	80.5	118	

(1) This information was not available at the time of publication.

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8 \text{ V}$

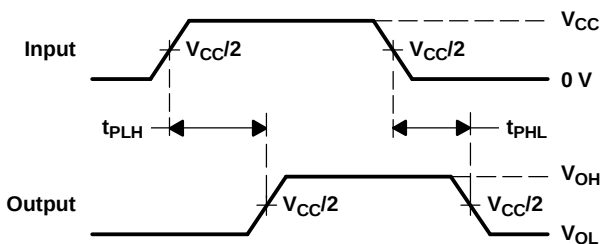


LOAD CIRCUIT

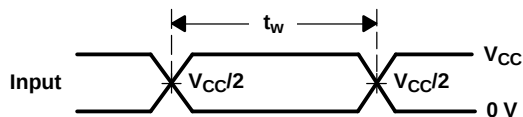
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



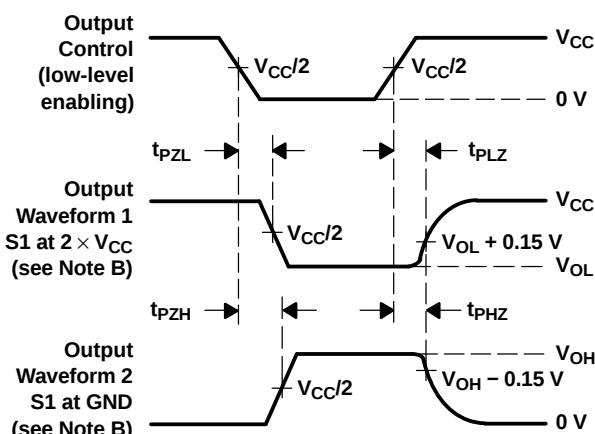
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

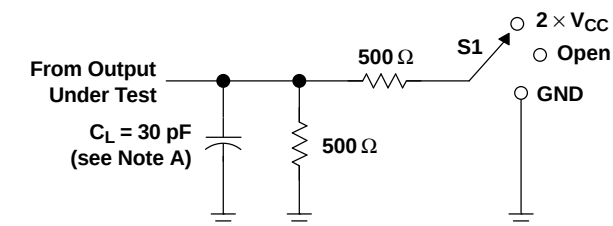
SN74ALVCH16270

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES028G–JULY 1995–REVISED AUGUST 2004

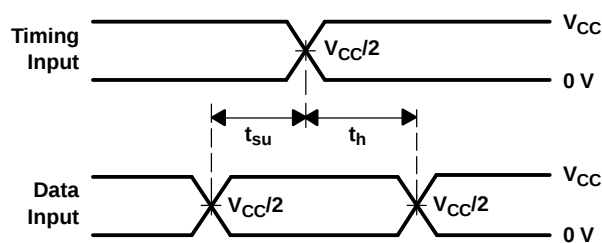
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

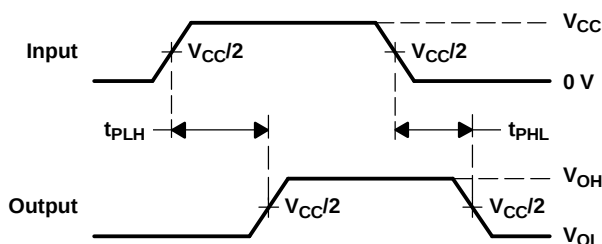


LOAD CIRCUIT

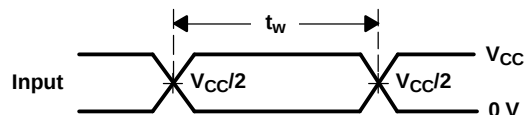
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



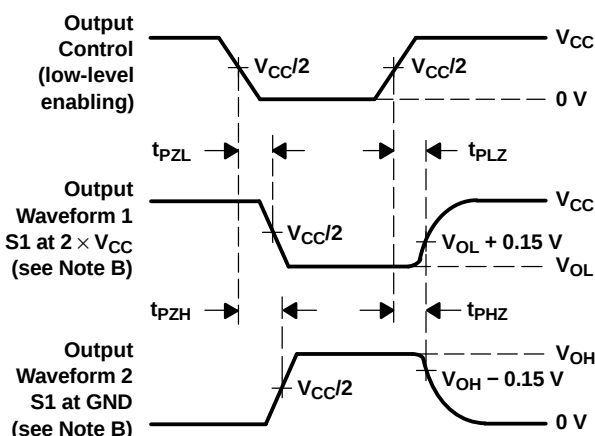
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



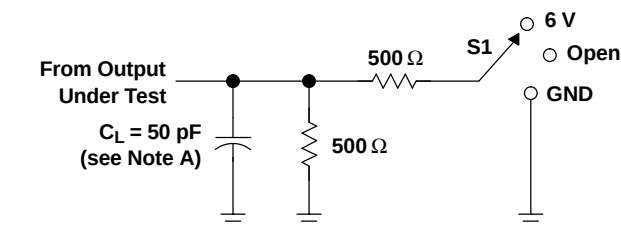
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
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 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

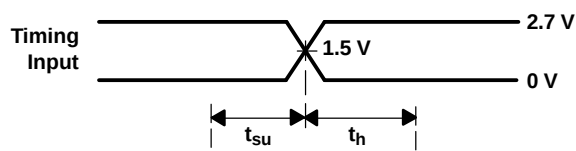
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ V}$ AND $3.3 \text{ V} \pm 0.3 \text{ V}$

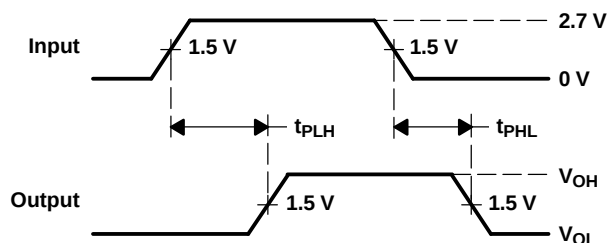


LOAD CIRCUIT

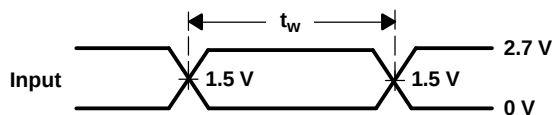
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



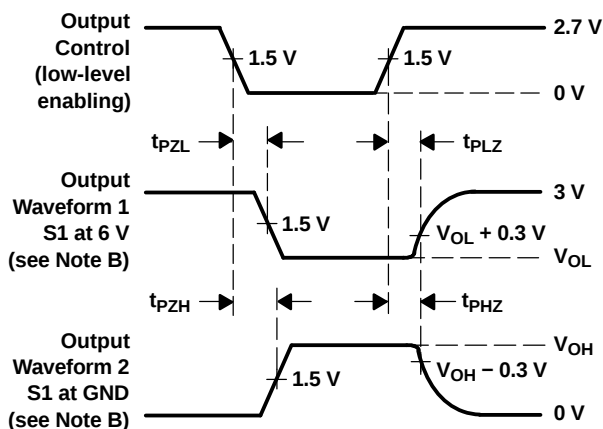
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

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 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALVCH16270DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16270
SN74ALVCH16270DL.B	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16270
SN74ALVCH16270DLR	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16270
SN74ALVCH16270DLR.B	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16270

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16270DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

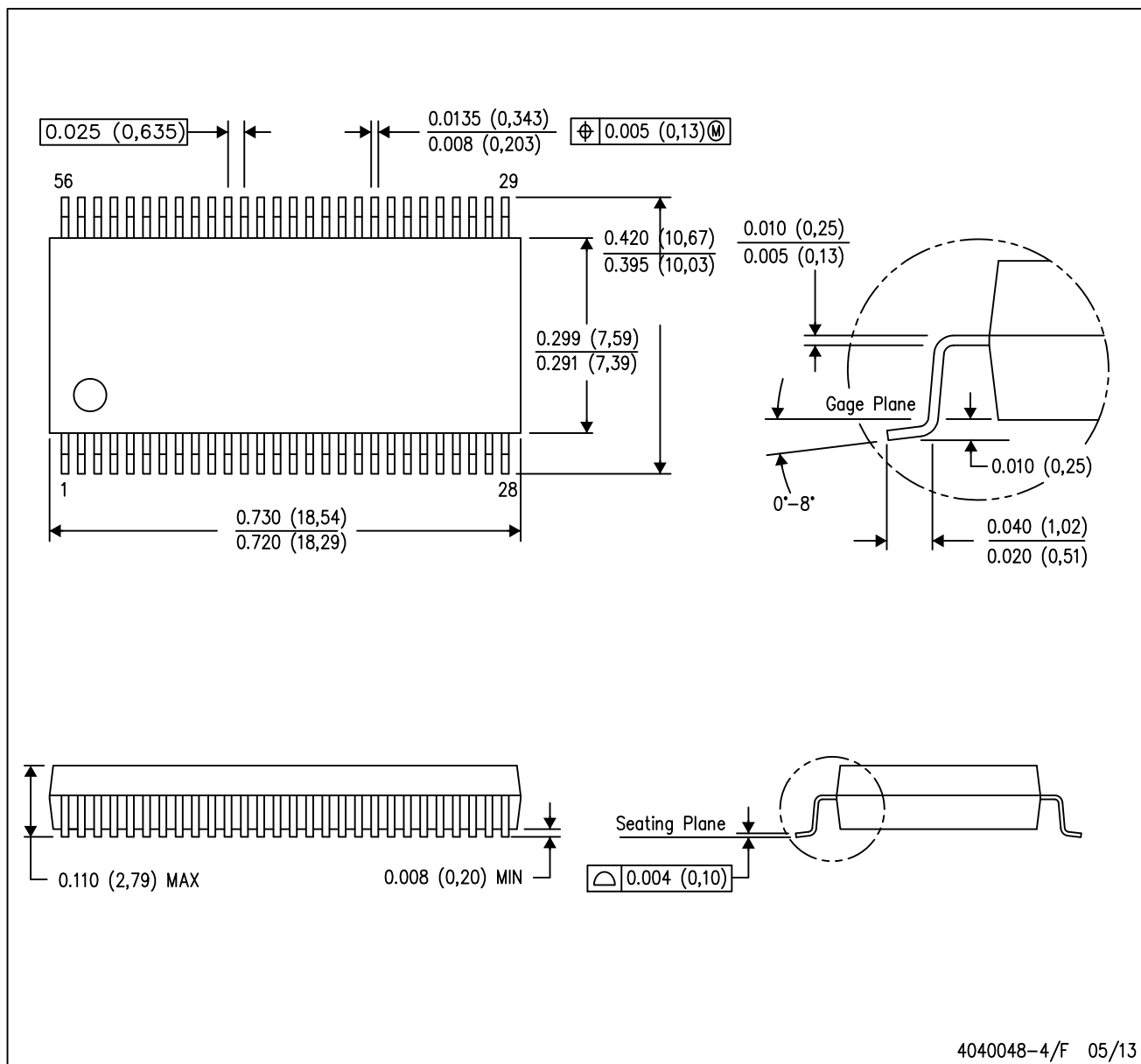


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16270DLR	SSOP	DL	56	1000	356.0	356.0	53.0

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118

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