

# SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS036D – APRIL 1982 – REVISED AUGUST 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

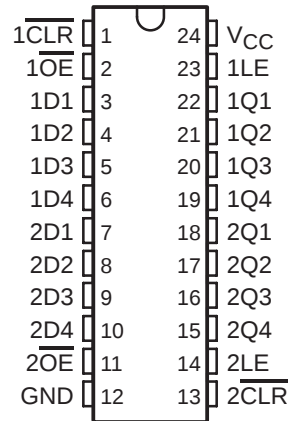
## description

These dual 4-bit D-type latches feature 3-state outputs designed specifically for bus driving. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

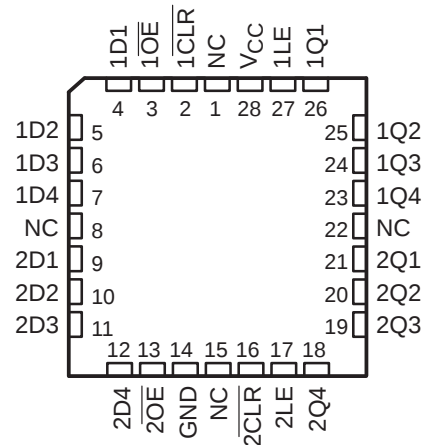
The dual 4-bit latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs in true form, according to the function table. When LE is low, the outputs are latched. When the clear (CLR) input goes low, the Q outputs go low independently of LE. The outputs are in the high-impedance state when the output-enable ( $\overline{OE}$ ) input is at a high logic level.

The SN54ALS873B and SN54AS873A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS873B and SN74AS873A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS873B, SN54AS873A . . . JT PACKAGE  
SN74ALS873B, SN74AS873A . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54ALS873B, SN54AS873A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each latch)

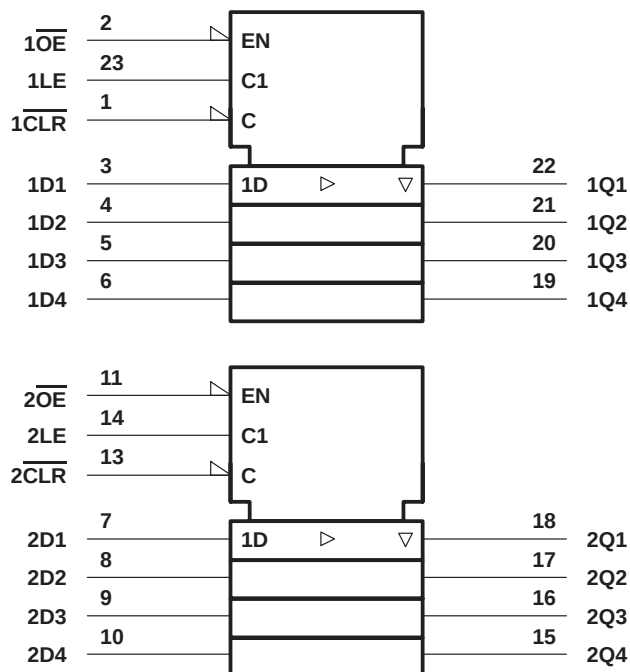
| INPUTS          |                  |    |   | OUTPUT<br>Q |
|-----------------|------------------|----|---|-------------|
| $\overline{OE}$ | $\overline{CLR}$ | LE | D |             |
| L               | L                | X  | X | L           |
| L               | H                | H  | H | H           |
| L               | H                | H  | L | L           |
| L               | H                | L  | X | $Q_0$       |
| H               | X                | X  | X | Z           |

# SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A

## DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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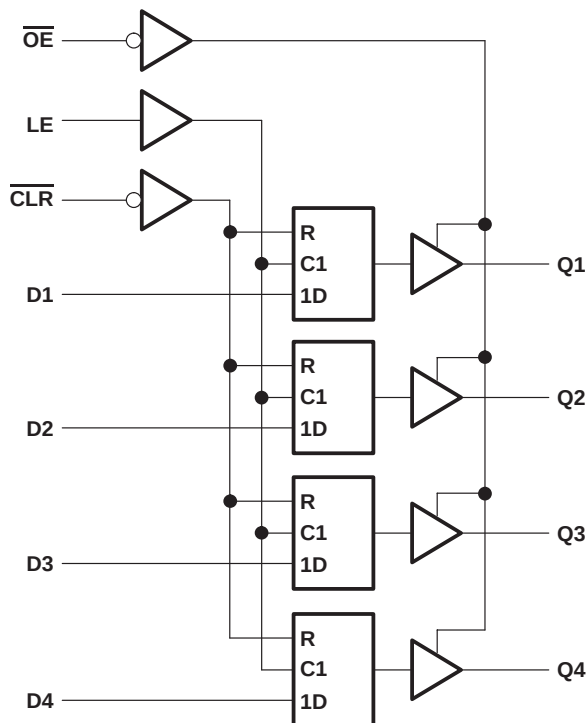
### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW, JT, and NT packages.

### logic diagram (each quad latch, positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|                                                           |                |
|-----------------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$                                  | 7 V            |
| Input voltage, $V_I$                                      | 7 V            |
| Voltage applied to a disabled 3-state output              | 5.5 V          |
| Operating free-air temperature range, $T_A$ : SN54ALS873B | –55°C to 125°C |
| SN74ALS873B                                               | 0°C to 70°C    |
| Storage temperature range                                 | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

|          |                                | SN54ALS873B |     |     | SN74ALS873B |     |      | UNIT |
|----------|--------------------------------|-------------|-----|-----|-------------|-----|------|------|
|          |                                | MIN         | NOM | MAX | MIN         | NOM | MAX  |      |
| $V_{CC}$ | Supply voltage                 | 4.5         | 5   | 5.5 | 4.5         | 5   | 5.5  | V    |
| $V_{IH}$ | High-level input voltage       | 2           |     |     | 2           |     |      | V    |
| $V_{IL}$ | Low-level input voltage        |             |     | 0.7 |             |     | 0.8  | V    |
| $I_{OH}$ | High-level output current      |             |     | –1  |             |     | –2.6 | mA   |
| $I_{OL}$ | Low-level output current       |             |     | 12  |             |     | 24   | mA   |
| $T_A$    | Operating free-air temperature | –55         |     | 125 | 0           |     | 70   | °C   |



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# SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A

## DUAL 4-BIT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                   | TEST CONDITIONS                                             |                           | SN54ALS873B         |      |          | SN74ALS873B         |      |     | UNIT |
|-----------------------------|-------------------------------------------------------------|---------------------------|---------------------|------|----------|---------------------|------|-----|------|
|                             |                                                             |                           | MIN                 | TYP† | MAX      | MIN                 | TYP† | MAX |      |
| V <sub>IK</sub>             | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA            |                           | −1.2                |      |          | −1.2                |      |     | V    |
| V <sub>OH</sub>             | V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = −0.4 mA |                           | V <sub>CC</sub> − 2 |      |          | V <sub>CC</sub> − 2 |      |     | V    |
|                             | V <sub>CC</sub> = 4.5 V                                     | I <sub>OH</sub> = −1 mA   | 2.4                 | 3.3  |          |                     |      |     |      |
|                             |                                                             | I <sub>OH</sub> = −2.6 mA |                     |      |          | 2.4                 | 3.2  |     |      |
| V <sub>OL</sub>             | V <sub>CC</sub> = 4.5 V                                     | I <sub>OL</sub> = 12 mA   | 0.25                | 0.4  | 0.25 0.4 |                     |      | V   |      |
|                             |                                                             | I <sub>OL</sub> = 24 mA   |                     |      |          | 0.35 0.5            |      |     |      |
| I <sub>OZH</sub>            | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V             |                           | 20                  |      |          | 20                  |      |     | μA   |
| I <sub>OZL</sub>            | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.4 V             |                           | −20                 |      |          | −20                 |      |     | μA   |
| I <sub>I</sub>              | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V               |                           | 0.1                 |      |          | 0.1                 |      |     | mA   |
| I <sub>IH</sub>             | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V             |                           | 20                  |      |          | 20                  |      |     | μA   |
| I <sub>IL</sub>             | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V             |                           | −0.2                |      |          | −0.2                |      |     | mA   |
| I <sub>O</sub> <sup>‡</sup> | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V            |                           | −20                 | −112 | −30      | −112                |      |     | mA   |
| I <sub>CC</sub>             | V <sub>CC</sub> = 5.5 V                                     | Outputs high              | 11                  | 21   | 11       | 21                  |      |     | mA   |
|                             |                                                             | Outputs low               | 16                  | 29   | 16       | 29                  |      |     |      |
|                             |                                                             | Outputs disabled          | 20                  | 31   | 20       | 31                  |      |     |      |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

|          |                             |         | SN54ALS873B |     | SN74ALS873B |     | UNIT |
|----------|-----------------------------|---------|-------------|-----|-------------|-----|------|
|          |                             |         | MIN         | MAX | MIN         | MAX |      |
| $t_w$    | Pulse duration              | CLR low | 15          |     | 15          |     | ns   |
|          |                             | LE high | 10          |     | 10          |     |      |
| $t_{su}$ | Setup time, data before LE↓ |         | 10          |     | 10          |     | ns   |
| $t_h$    | Hold time, data after LE↓   |         | 7           |     | 7           |     | ns   |



# SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A

## DUAL 4-BIT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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#### switching characteristics (see Figure 1)

| PARAMETER        | FROM<br>(INPUT)         | TO<br>(OUTPUT) | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R1 = 500 Ω,<br>R2 = 500 Ω,<br>T <sub>A</sub> = MIN to MAX† |     |             |     | UNIT |
|------------------|-------------------------|----------------|----------------------------------------------------------------------------------------------------------------------------|-----|-------------|-----|------|
|                  |                         |                | SN54ALS873B                                                                                                                |     | SN74ALS873B |     |      |
|                  |                         |                | MIN                                                                                                                        | MAX | MIN         | MAX |      |
| t <sub>PLH</sub> | D                       | Q              | 2                                                                                                                          | 23  | 2           | 14  | ns   |
| t <sub>PHL</sub> |                         |                | 2                                                                                                                          | 17  | 2           | 14  |      |
| t <sub>PLH</sub> | LE                      | Q              | 8                                                                                                                          | 31  | 8           | 22  | ns   |
| t <sub>PHL</sub> |                         |                | 8                                                                                                                          | 26  | 8           | 21  |      |
| t <sub>PHL</sub> | $\overline{\text{CLR}}$ | Q              | 6                                                                                                                          | 27  | 6           | 20  | ns   |
| t <sub>PZH</sub> | $\overline{\text{OE}}$  | Q              | 4                                                                                                                          | 24  | 4           | 18  | ns   |
| t <sub>PZL</sub> |                         |                | 4                                                                                                                          | 23  | 4           | 18  |      |
| t <sub>PHZ</sub> | $\overline{\text{OE}}$  | Q              | 2                                                                                                                          | 12  | 2           | 10  | ns   |
| t <sub>PLZ</sub> |                         |                | 2                                                                                                                          | 30  | 2           | 15  |      |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|                                                                   |                |
|-------------------------------------------------------------------|----------------|
| Supply voltage, V <sub>CC</sub>                                   | 7 V            |
| Input voltage, V <sub>I</sub>                                     | 7 V            |
| Voltage applied to a disabled 3-state output                      | 5.5 V          |
| Operating free-air temperature range, T <sub>A</sub> : SN54AS873A | –55°C to 125°C |
| SN74AS873A                                                        | 0°C to 70°C    |
| Storage temperature range                                         | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

|                 |                                | SN54AS873A |     |     | SN74AS873A |     |     | UNIT |
|-----------------|--------------------------------|------------|-----|-----|------------|-----|-----|------|
|                 |                                | MIN        | NOM | MAX | MIN        | NOM | MAX |      |
| V <sub>CC</sub> | Supply voltage                 | 4.5        | 5   | 5.5 | 4.5        | 5   | 5.5 | V    |
| V <sub>IH</sub> | High-level input voltage       | 2          |     |     | 2          |     |     | V    |
| V <sub>IL</sub> | Low-level input voltage        |            |     | 0.8 |            |     | 0.8 | V    |
| I <sub>OH</sub> | High-level output current      |            |     | –12 |            |     | –15 | mA   |
| I <sub>OL</sub> | Low-level output current       |            |     | 32  |            |     | 48  | mA   |
| T <sub>A</sub>  | Operating free-air temperature | –55        |     | 125 | 0          |     | 70  | °C   |



# SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A

## DUAL 4-BIT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                   | TEST CONDITIONS                                           |                          | SN54AS873A          |      |          | SN74AS873A          |      |     | UNIT |
|-----------------------------|-----------------------------------------------------------|--------------------------|---------------------|------|----------|---------------------|------|-----|------|
|                             |                                                           |                          | MIN                 | TYP† | MAX      | MIN                 | TYP† | MAX |      |
| V <sub>IK</sub>             | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA          |                          | −1.2                |      |          | −1.2                |      |     | V    |
| V <sub>OH</sub>             | V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = −2 mA |                          | V <sub>CC</sub> − 2 |      |          | V <sub>CC</sub> − 2 |      |     | V    |
|                             | V <sub>CC</sub> = 4.5 V                                   | I <sub>OH</sub> = −12 mA | 2.4                 | 3.2  |          |                     |      |     |      |
|                             |                                                           | I <sub>OH</sub> = −15 mA |                     |      | 2.4      | 3.3                 |      |     |      |
| V <sub>OL</sub>             | V <sub>CC</sub> = 4.5 V                                   | I <sub>OL</sub> = 32 mA  | 0.25 0.5            |      |          |                     |      |     | V    |
|                             |                                                           | I <sub>OL</sub> = 48 mA  |                     |      | 0.35 0.5 |                     |      |     |      |
| I <sub>OZH</sub>            | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V           |                          | 50                  |      |          | 50                  |      |     | μA   |
| I <sub>OZL</sub>            | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.4 V           |                          | −50                 |      |          | −50                 |      |     | μA   |
| I <sub>I</sub>              | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V             |                          | 0.1                 |      |          | 0.1                 |      |     | mA   |
| I <sub>IH</sub>             | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V           |                          | 20                  |      |          | 20                  |      |     | μA   |
| I <sub>IL</sub>             | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V           |                          | −0.5                |      |          | −0.5                |      |     | mA   |
| I <sub>O</sub> <sup>‡</sup> | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V          |                          | −30                 | −112 |          | −30                 | −112 |     | mA   |
| I <sub>CC</sub>             | V <sub>CC</sub> = 5.5 V                                   | Outputs high             | 68                  | 110  |          | 68                  | 110  |     | mA   |
|                             |                                                           | Outputs low              | 67                  | 109  |          | 67                  | 109  |     |      |
|                             |                                                           | Outputs disabled         | 80                  | 129  |          | 80                  | 129  |     |      |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

|            |                             |         | SN54AS873A |     | SN74AS873A |     | UNIT |
|------------|-----------------------------|---------|------------|-----|------------|-----|------|
|            |                             |         | MIN        | MAX | MIN        | MAX |      |
| $t_W^*$    | Pulse duration              | CLR low | 5          |     | 5          |     | ns   |
|            |                             | LE high | 6          |     | 5          |     |      |
| $t_{su}^*$ | Setup time, data before LE↓ |         | 2          |     | 2          |     | ns   |
| $t_h^*$    | Hold time, data after LE↓   |         | 4.5        |     | 4.5        |     | ns   |

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



# SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A

## DUAL 4-BIT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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#### switching characteristics (see Figure 1)

| PARAMETER        | FROM<br>(INPUT)         | TO<br>(OUTPUT) | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R1 = 500 Ω,<br>R2 = 500 Ω,<br>T <sub>A</sub> = MIN to MAX† |      |            |      | UNIT |
|------------------|-------------------------|----------------|----------------------------------------------------------------------------------------------------------------------------|------|------------|------|------|
|                  |                         |                | SN54AS873A                                                                                                                 |      | SN74AS873A |      |      |
|                  |                         |                | MIN                                                                                                                        | MAX  | MIN        | MAX  |      |
| t <sub>PLH</sub> | D                       | Q              | 3                                                                                                                          | 12.5 | 3          | 9.5  | ns   |
| t <sub>PHL</sub> |                         |                | 3                                                                                                                          | 8.5  | 3          | 7.5  |      |
| t <sub>PLH</sub> | LE                      | Q              | 6                                                                                                                          | 15.5 | 6          | 13   | ns   |
| t <sub>PHL</sub> |                         |                | 4                                                                                                                          | 9    | 4          | 7.5  |      |
| t <sub>PHL</sub> | $\overline{\text{CLR}}$ | Q              | 3                                                                                                                          | 10.5 | 3          | 9    | ns   |
| t <sub>PZH</sub> | $\overline{\text{OE}}$  | Q              | 2                                                                                                                          | 8    | 2          | 6.5  | ns   |
| t <sub>PZL</sub> |                         |                | 4                                                                                                                          | 11   | 4          | 10.5 |      |
| t <sub>PHZ</sub> | $\overline{\text{OE}}$  | Q              | 2                                                                                                                          | 8    | 2          | 7.5  | ns   |
| t <sub>PLZ</sub> |                         |                | 2                                                                                                                          | 8.5  | 2          | 7.5  |      |

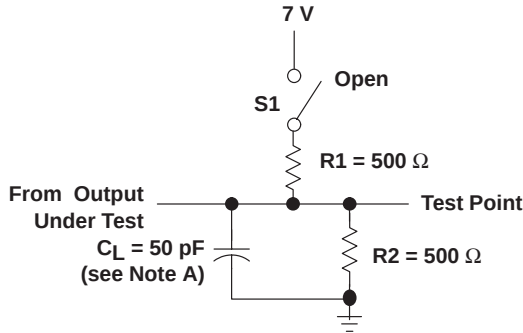
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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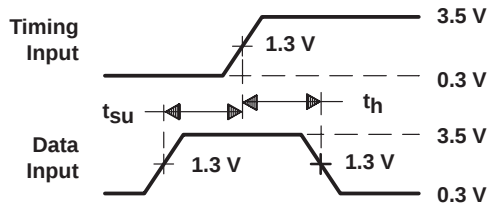
## PARAMETER MEASUREMENT INFORMATION



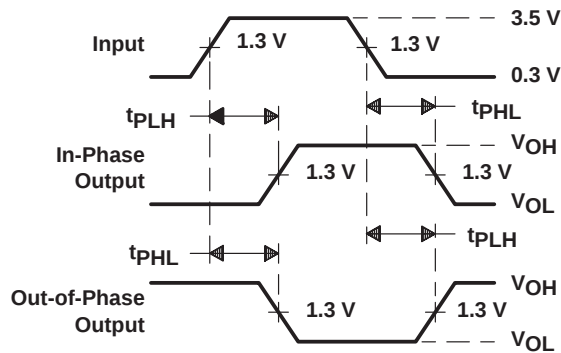
SWITCH POSITION TABLE

| TEST      | S1     |
|-----------|--------|
| $t_{PLH}$ | Open   |
| $t_{PHL}$ | Open   |
| $t_{PZH}$ | Open   |
| $t_{PZL}$ | Closed |
| $t_{PHZ}$ | Open   |
| $t_{PLZ}$ | Closed |

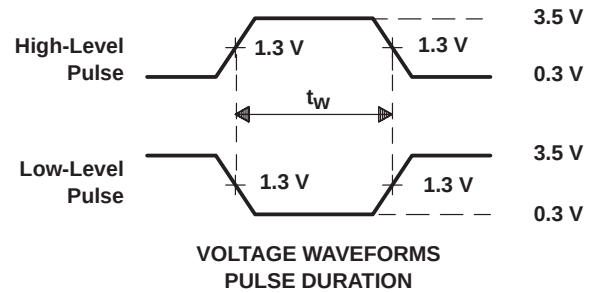
LOAD CIRCUIT FOR 3-STATE OUTPUTS



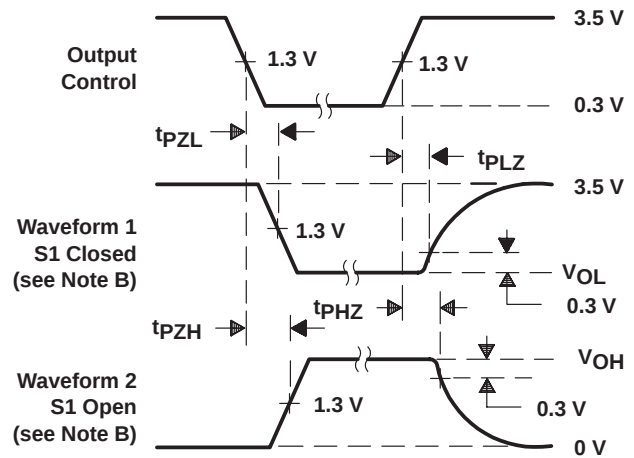
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)              |
|---------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------------|
| <a href="#">84032013A</a>       | Active        | Production           | LCCC (FK)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 84032013A<br>SNJ54ALS<br>873BFBK |
| <a href="#">8403201LA</a>       | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8403201LA<br>SNJ54ALS873BJT      |
| <a href="#">SN74ALS873BDW</a>   | Obsolete      | Production           | SOIC (DW)   24 | -                     | -           | Call TI                              | Call TI                           | 0 to 70      |                                  |
| <a href="#">SN74ALS873BDWR</a>  | Active        | Production           | SOIC (DW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | ALS873B                          |
| SN74ALS873BDWR.A                | Active        | Production           | SOIC (DW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | ALS873B                          |
| <a href="#">SNJ54ALS873BFBK</a> | Active        | Production           | LCCC (FK)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 84032013A<br>SNJ54ALS<br>873BFBK |
| SNJ54ALS873BFBK.A               | Active        | Production           | LCCC (FK)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 84032013A<br>SNJ54ALS<br>873BFBK |
| <a href="#">SNJ54ALS873BJT</a>  | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8403201LA<br>SNJ54ALS873BJT      |
| SNJ54ALS873BJT.A                | Active        | Production           | CDIP (JT)   24 | 15   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8403201LA<br>SNJ54ALS873BJT      |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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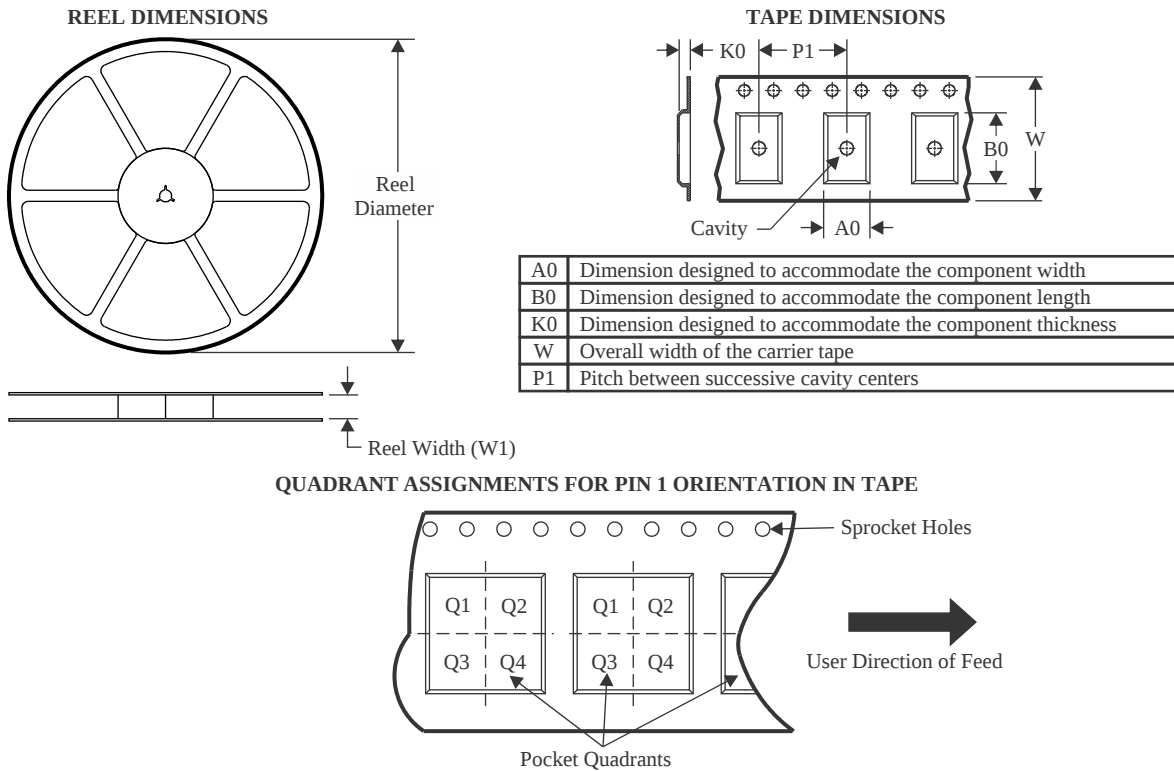
**OTHER QUALIFIED VERSIONS OF SN54ALS873B, SN74ALS873B :**

- Catalog : [SN74ALS873B](#)
- Military : [SN54ALS873B](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

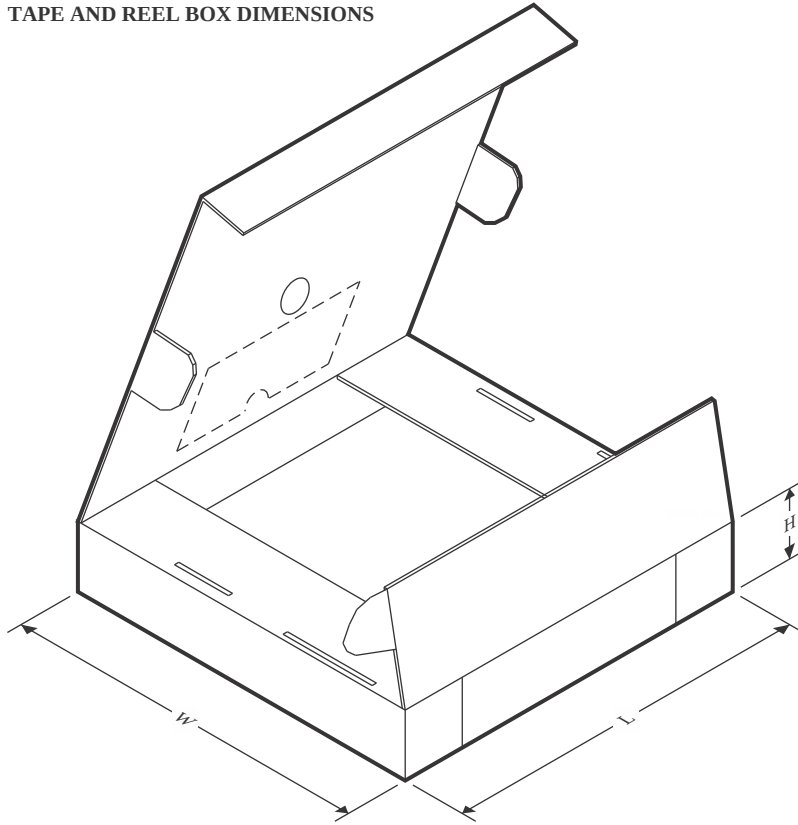
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS873BDWR | SOIC         | DW              | 24   | 2000 | 330.0              | 24.4               | 10.75   | 15.7    | 2.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

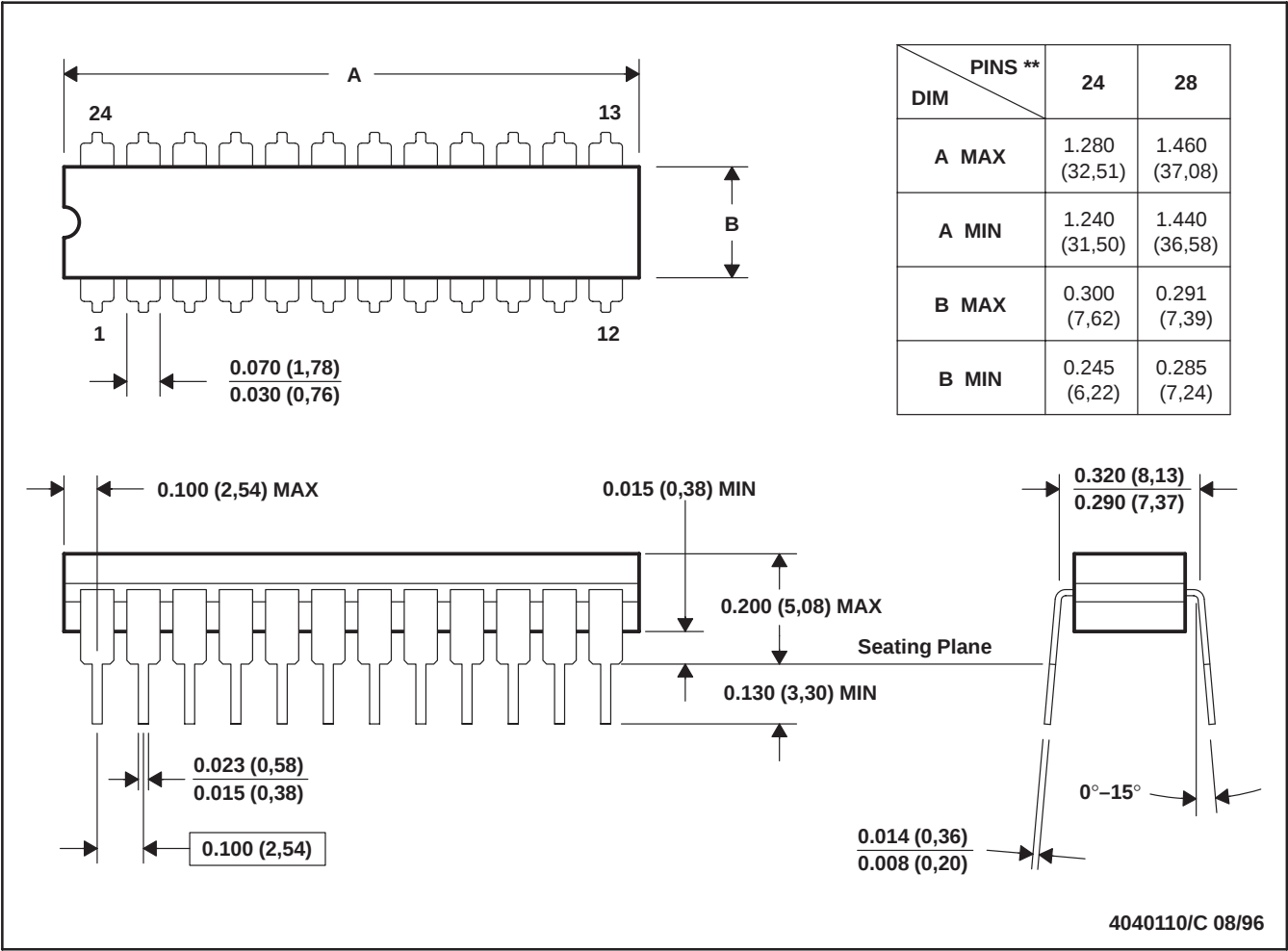


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS873BDWR | SOIC         | DW              | 24   | 2000 | 350.0       | 350.0      | 43.0        |

JT (R-GDIP-T\*\*) 24 LEADS SHOWN

CERAMIC DUAL-IN-LINE

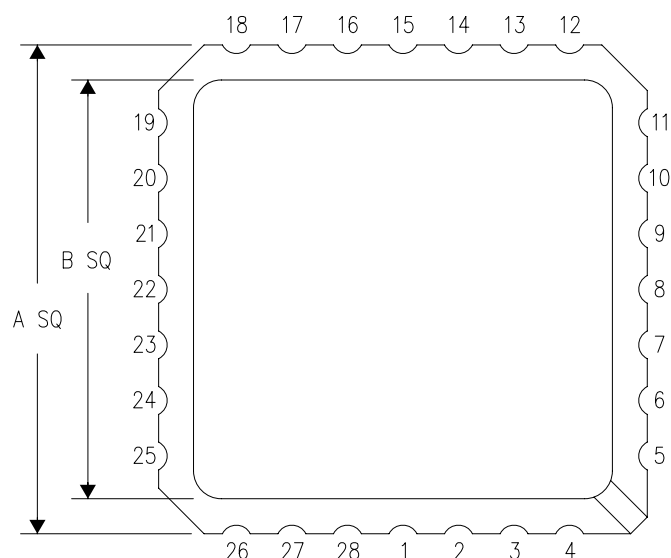


- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package can be hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification.  
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

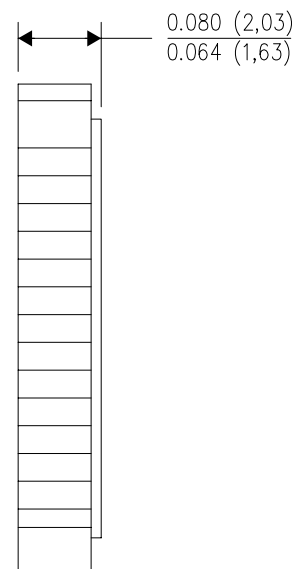
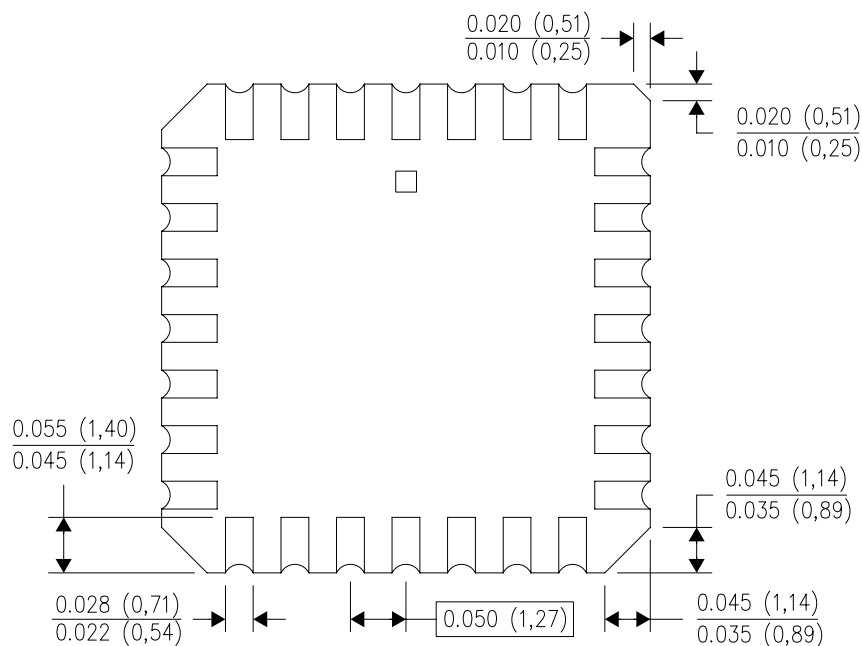
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |

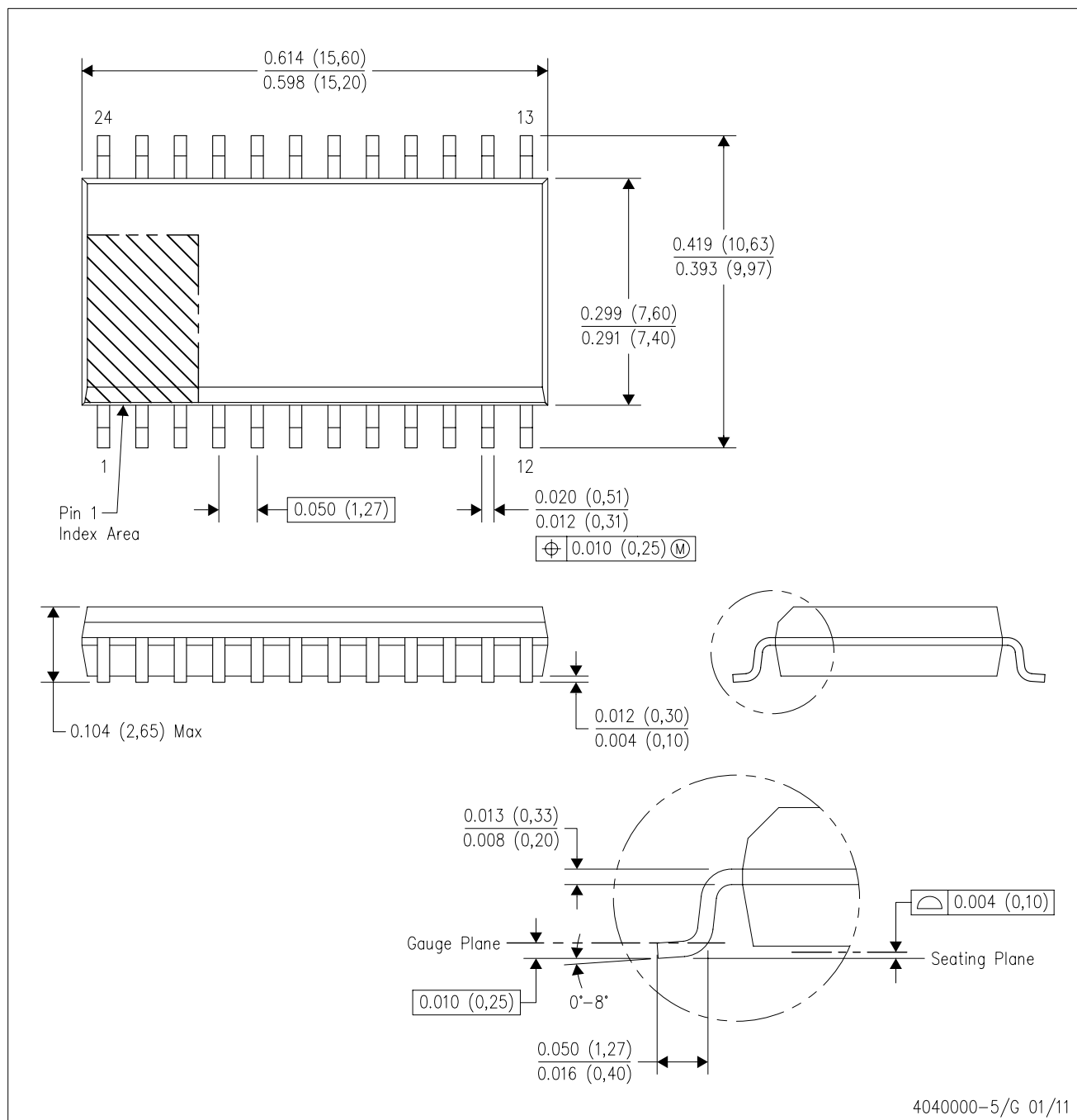


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

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Last updated 10/2025