# SN74ACT07-Q1 Automotive Hex Buffers with TTL-Compatible Inputs and Open-Drain Outputs

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Available in wettable flank QFN package
- Operating voltage range of 4.5V to 5.5V
- TTL-compatible inputs
- Continuous 24mA output drive at 5V
- Supports up to 75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Fast operation with delay of 8.3ns max

## 2 Applications

- Drive an indicator LED
- Level-shift using open-drain outputs
- Control a relay

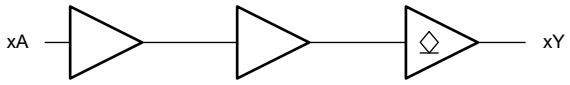
## 3 Description

The SN74ACT07-Q1 device contains six independent CMOS logic buffers with TTL-compatible inputs and open-drain outputs.

**Device Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SN74ACT07-Q1 | BQA (WQFN, 14) | 3mm × 2.5mm | 3mm × 2.5mm |
| | PW (TSSOP, 14) | 5mm × 6.4mm | 5mm × 4.4mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Functional Diagram**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Pin Configuration and Functions

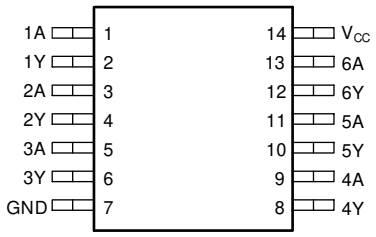


**Figure 4-1. PW Package, 14-Pin TSSOP (Top View)**

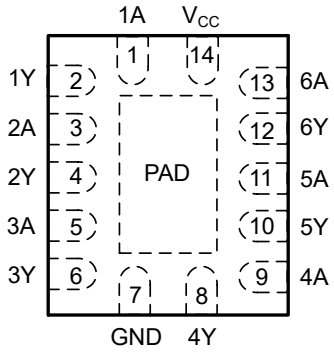


**Figure 4-2. BQA Package, 14-Pin WQFN (Top View)**

**Table 4-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A | 1 | Input | Channel 1, Input A |
| 1Y | 2 | Output | Channel 1, Output Y |
| 2A | 3 | Input | Channel 2, Input A |
| 2Y | 4 | Output | Channel 2, Output Y |
| 3A | 5 | Input | Channel 3, Input A |
| 3Y | 6 | Output | Channel 3, Output Y |
| GND | 7 | — | Ground |
| 4Y | 8 | Output | Channel 4, Output Y |
| 4A | 9 | Input | Channel 4, Input A |
| 5Y | 10 | Output | Channel 5, Output Y |
| 5A | 11 | Input | Channel 5, Input A |
| 6Y | 12 | Output | Channel 6, Output Y |
| 6A | 13 | Input | Channel 6, Input A |
| $V_{CC}$ | 14 | — | Positive Supply |
| Thermal Pad(1) | | — | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply |

(1) BQA package only.

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | -0.5 | $V_{CC}$ + 0.5V | V |
| $V_O$ | Output voltage range(2) | | -0.5 | 7 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V | | ±20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < -0.5V | | -50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to 5.5V | | 50 | mA |
| | Continuous output current through $V_{CC}$ or GND | | | ±200 | mA |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |
| $T_J$ | Junction temperature | | | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B | ±1000 | |

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| Spec | Description | Condition | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | V |
| $V_{IL}$ | Low-Level input voltage | | | 0.8 | V |
| $V_I$ | Input Voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output Voltage | | 0 | 5.5 | V |
| $I_{OL}$ | Low-level output current | | | 24 | mA |
| Δt/Δv | Input transition rise or fall rate | | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | | -40 | 125 | °C |

## 5.4 Thermal Information

| PACKAGE | PINS | THERMAL METRIC(1) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | $R_{θJA}$ | $R_{θJC(top)}$ | $R_{θJB}$ | $Ψ_{JT}$ | $Ψ_{JB}$ | $R_{θJC(bot)}$ | |
| PW (TSSOP) | 14 | 132.2 | 64.8 | 88.4 | 11.9 | 87.4 | N/A | °C/W |
| BQA (WQFN) | 14 | 85.4 | 89.0 | 54.8 | 9.1 | 54.7 | 31.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.


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## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{OL}$ | $I_{OL}$ = 50µA | 4.5V | | 0.001 | 0.1 | V |
| | | 5.5V | | 0.001 | 0.1 | |
| | $I_{OL}$ = 24mA | 4.5V | | | 0.5 | |
| | $I_{OL}$ = 24mA | 5.5V | | | 0.5 | |
| | $I_{OL}$ = 75mA(1) | 5.5V | | | 1.65 | |
| $I_I$ | $V_I$ = 5.5V or GND | 0 to 5.5V | | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5V | | | 2 | µA |
| $\Delta I_{CC}$ | $V_I$ = $V_{CC}$ – 2.1; Any Input | 4.5 to 5.5V | | | 1.5 | mA |
| $C_I$ | $V_I$ = $V_{CC}$ or GND | 5V | | 2 | | pF |
| $C_O$ | $V_O$ = $V_{CC}$ or GND | 5V | | 3 | | pF |
| $C_{PD}$ | $C_L$ = 50pF, F = 1MHz | 5V | | 12 | | pF |

(1) Duration not to exceed 2ms

## 5.6 Switching Characteristics

$C_L$ = 50 pF; over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*.

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $t_{PLZ}$ | A | Y | 5V | | 1.9 | 2.9 | ns |
| $t_{PZL}$ | A | Y | 5V | | 6.1 | 8.3 | ns |

## 5.7 Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

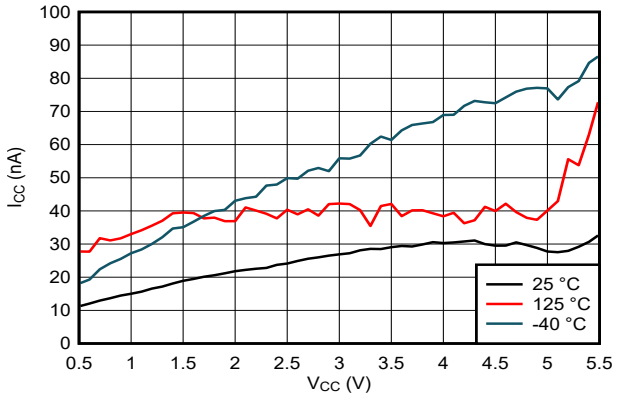


**Figure 5-1. Supply Current Across Supply Voltage**

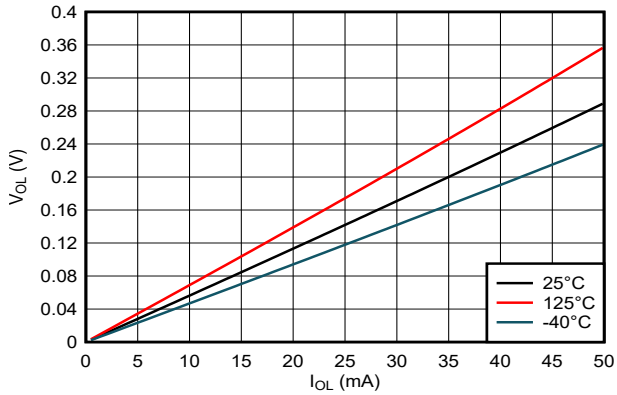


**Figure 5-2. Output Voltage vs Current in LOW State; 5V Supply**

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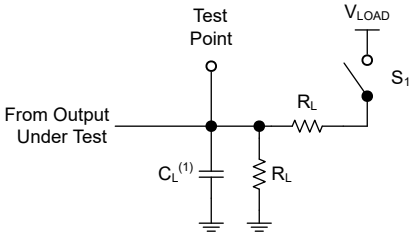
## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_O$ = 50Ω, $t_t$ < 2.5ns, $V_t$ = 1.5V.

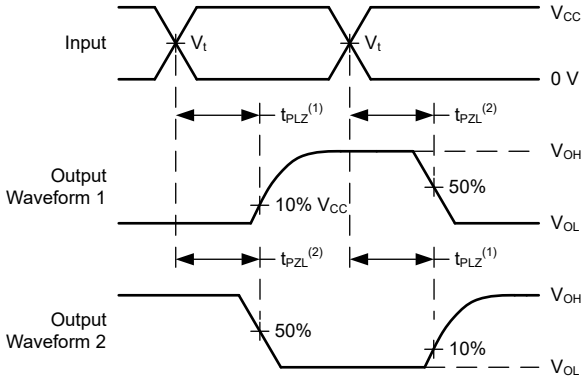
The outputs are measured individually with one input transition per measurement.

| TEST | S1 | $R_L$ | $C_L$ | ΔV | $V_{LOAD}$ |
|---|---|---|---|---|---|
| $t_{PLZ}$, $t_{PZL}$ | CLOSED | 500Ω | 50pF | 0.3V | 2×$V_{CC}$ |




(1) $C_L$ includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for Open-Drain Outputs**




(1) $t_{PLZ}$ is the same as $t_{dis}$.

(2) $t_{PZL}$ is the same as $t_{en}$.

**Figure 6-2. Voltage Waveforms Propagation Delays**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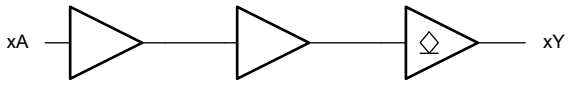
# 7 Detailed Description

## 7.1 Description

This device contains six independent buffers with open-drain outputs. Each gate performs the Boolean function Y = A in positive logic.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### *7.3.1 Open-Drain CMOS Outputs*

This device includes open-drain CMOS outputs. Open-drain outputs can only drive the output low. When in the high logical state, open-drain outputs will be in a high-impedance state. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused open-drain CMOS outputs should be left disconnected.

### *7.3.2 TTL-Compatible CMOS Inputs*

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at $V_{CC}$ or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and typically will meet all requirements.

### *7.3.3 Wettable Flanks*

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet where packages include this feature.

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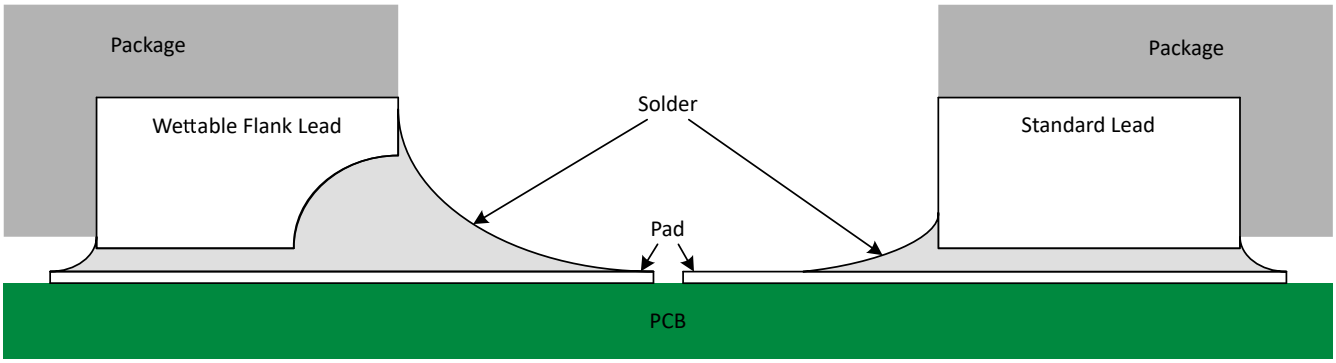


**Figure 7-1. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering**

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-1, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

### *7.3.4 Clamp Diode Structure*

The inputs to this device have both positive and negative clamping diodes, and the outputs to this device have negative clamping diodes only as depicted in Figure 7-2.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

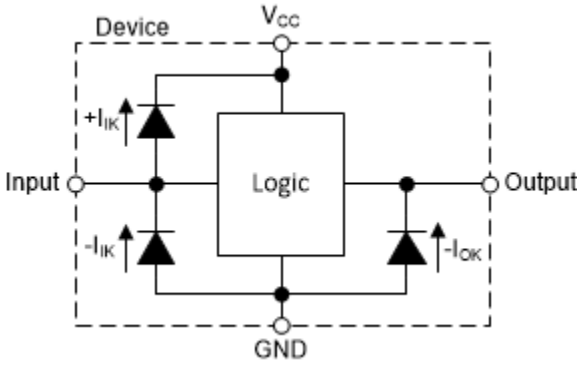


**Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output**


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## 7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74ACT07-Q1.

**Table 7-1. Function Table**

| INPUTS(1) | OUTPUT(2) |
|---|---|
| A | Y |
| L | L |
| H | Z |

(1) H = High voltage level, L = Low voltage level
(2) L = Driving low, Z = High-impedance state

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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

Open-drain outputs like those available in the SN74ACT07-Q1 provide the ability to discharge a voltage node to ground without otherwise loading the node significantly. It is recommended to add a series resistor between the output and any capacitance larger than 50pF as shown in the *Typical Application Block Diagram* to prevent damage to the device.

The required resistor value can be determined using the maximum capacitor voltage and the maximum continuous current for the output from the equation: $R \geq V_C/I_{O(max)}$.

For any given RC combination, the discharge time can be determined using the discharge plot provided in the *Application Timing Diagram* and the equation $\tau = R \times C$. For example, to discharge a capacitor to 10% of the starting value, it takes approximately $2.303 \times \tau = 2.303 \times R \times C$ seconds.

## 8.2 Typical Application

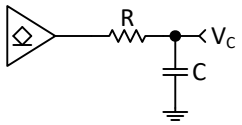


**Figure 8-1. Typical Application Block Diagram**


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### 8.2.1 Design Requirements

#### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74ACT07-Q1 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74ACT07-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74ACT07-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

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#### 8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74ACT07-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74ACT07-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### 8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.


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### 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74ACT07-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

### 8.2.3 Application Curves

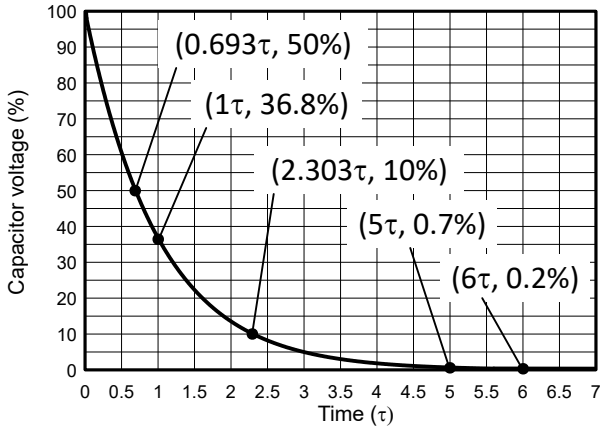


**Figure 8-2. Application Timing Diagram**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces
  - For traces longer than 12cm
    - Use impedance controlled traces

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- Source-terminate using a series damping resistor near the output
- Avoid branches; buffer signals that must branch separately

### *8.4.2 Layout Example*

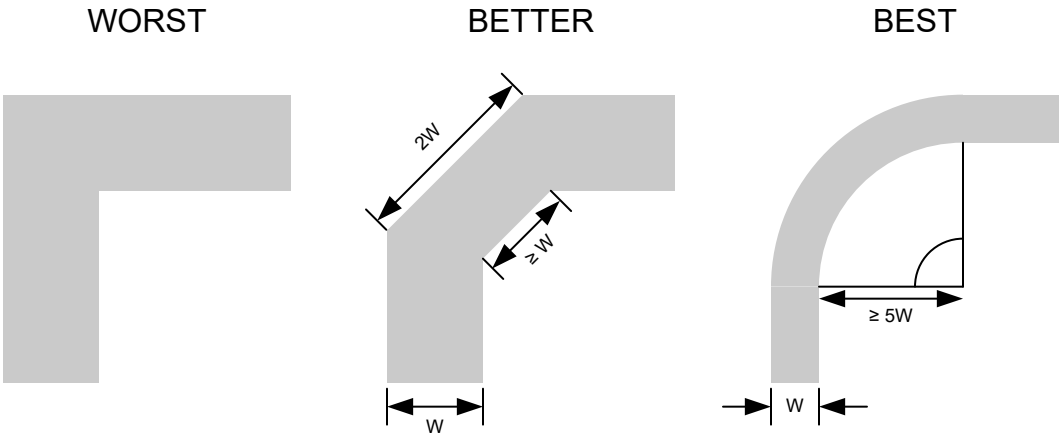


**Figure 8-3. Example Trace Corners for Improved Signal Integrity**

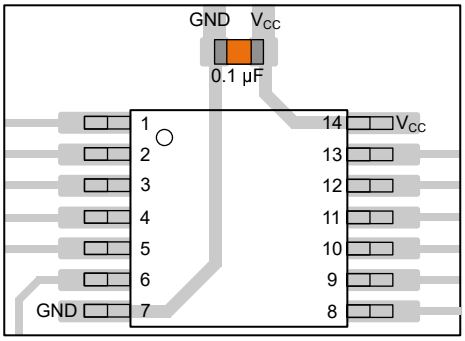


**Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages**

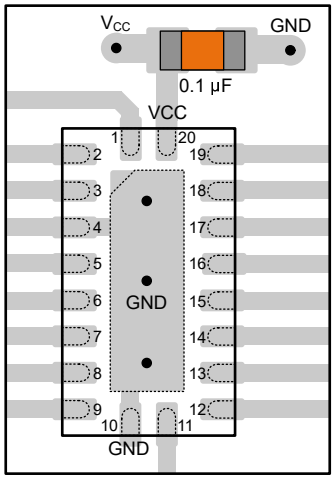


**Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages**

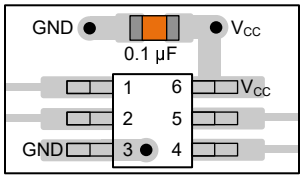


**Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**

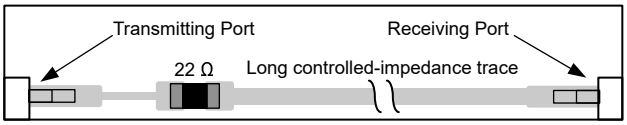


**Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity**


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# 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| November 2024 | * | Initial release |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74ACT07PWRQ1 | Active | Production | TSSOP (PW) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ACT07Q |
| SN74ACT07PWRQ1.A | Active | Production | TSSOP (PW) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ACT07Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74ACT07-Q1 :**

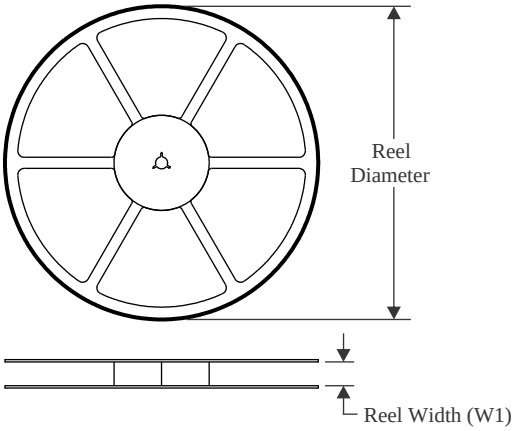
- Catalog : SN74ACT07

NOTE: Qualified Version Definitions:

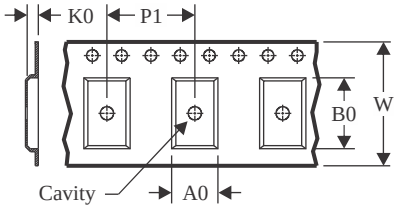
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

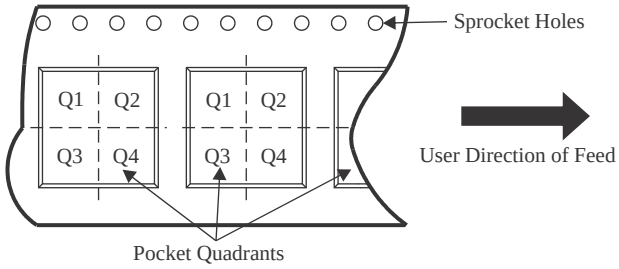



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

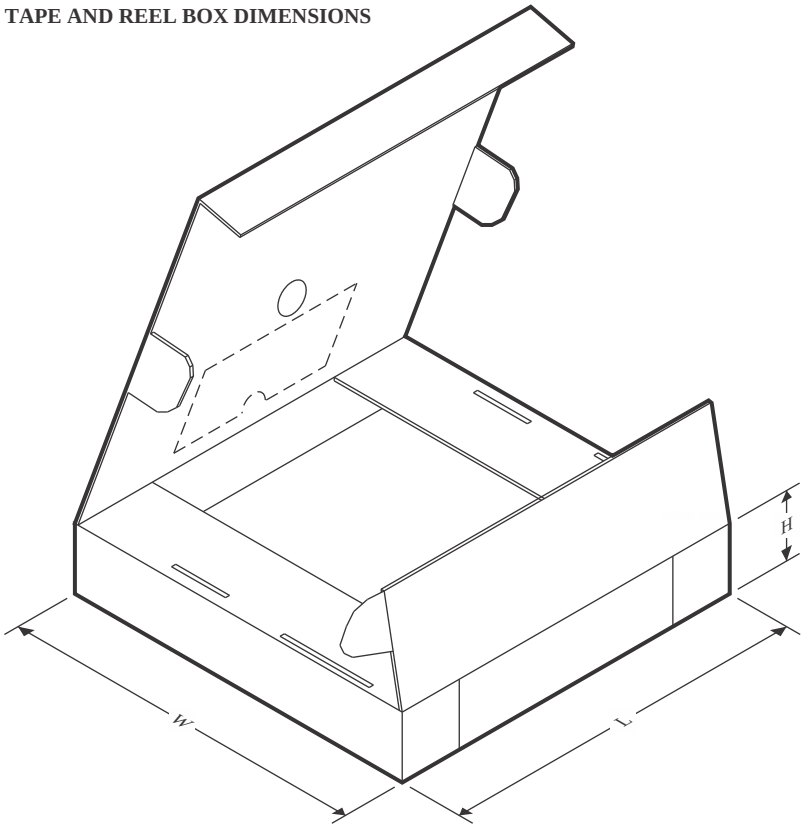
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ACT07PWRQ1 | TSSOP | PW | 14 | 3000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

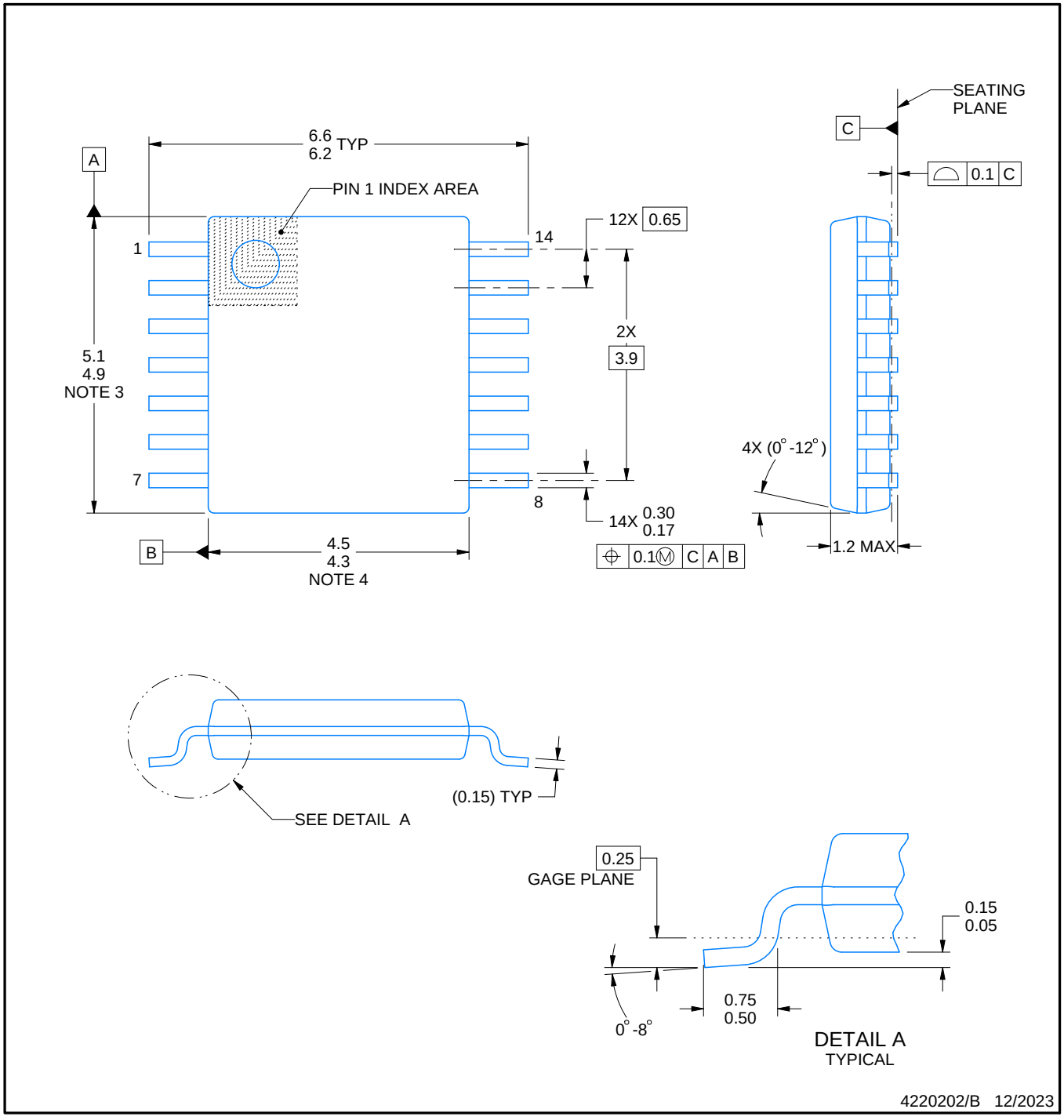
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ACT07PWRQ1 | TSSOP | PW | 14 | 3000 | 353.0 | 353.0 | 32.0 |

# PACKAGE OUTLINE

## PW0014A

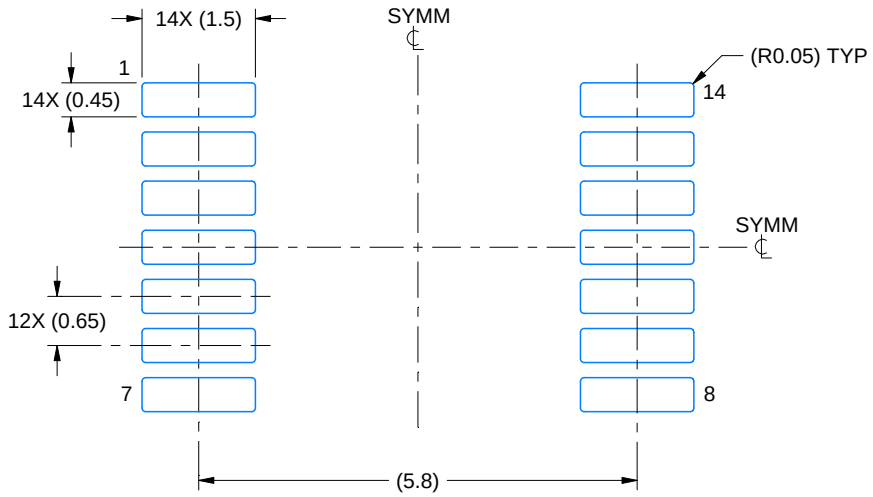
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

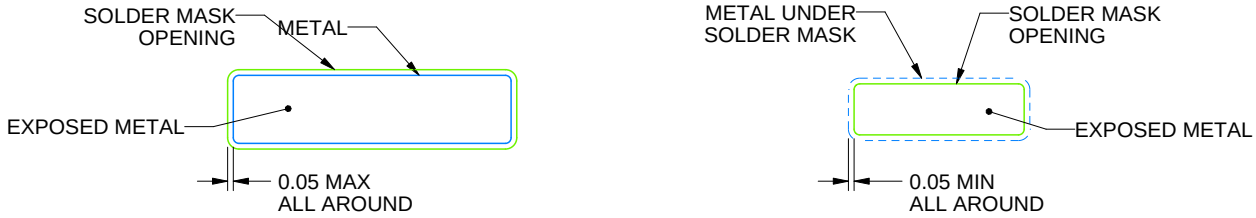



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

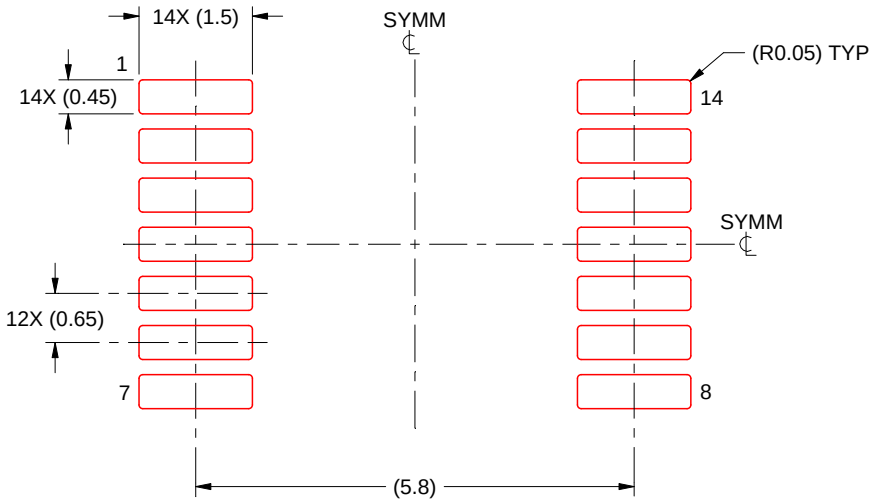



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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