

SN5497, SN7497

SDLS130 - DECEMBER 1972 - REVISED MARCH 1988

- **Perform Fixed-Rate or Variable-Rate Frequency Division**
- **For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations**
- **Typical Maximum Clock Frequency . . . 32 Megahertz**

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. These six-bit serial binary counters feature buffered clock, clear, and enable inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe, and enable inputs are low. With the counter enabled, the output frequency is equal to the input frequency multiplied by the rate input M and divided by 64, ie.:

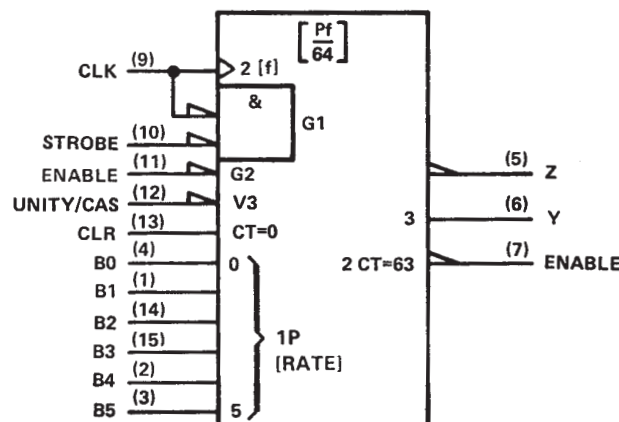
$$f_{out} = \frac{M \cdot f_{in}}{64}$$

where: $M = F \cdot 2^5 + E \cdot 2^4 + D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform 12-bit rate multiplication, the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output.

The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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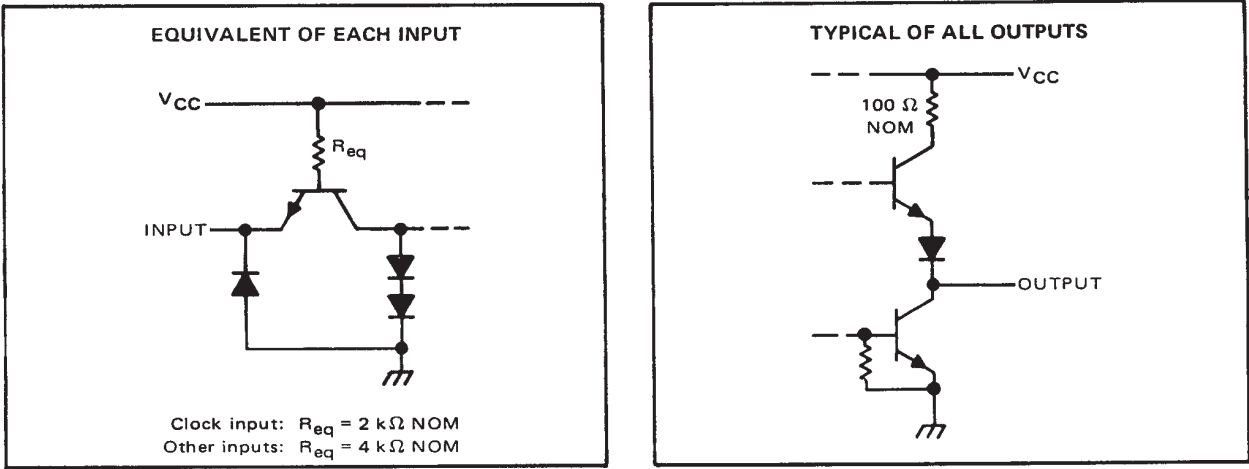


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SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

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schematics of inputs and outputs



STATE AND/OR RATE FUNCTION TABLE (See Note A)

			INPUTS								OUTPUTS			
CLEAR	ENABLE	STROBE	BINARY RATE B5 B4 B3 B2 B1 B0					NUMBER OF CLOCK PULSES	UNITY/ CASCADE	LOGIC LEVEL OR NUMBER OF PULSES				
										Y	Z	ENABLE		
H	X	H	X	X	X	X	X	X	H	L	H	H	B	
L	L	L	L	L	L	L	L	L	H	L	H	1	C	
L	L	L	L	L	L	L	L	H	H	1	1	1	C	
L	L	L	L	L	L	L	H	L	H	2	2	1	C	
L	L	L	L	L	L	H	L	L	H	4	4	1	C	
L	L	L	L	L	H	L	L	L	H	8	8	1	C	
L	L	L	L	H	L	L	L	L	H	16	16	1	C	
L	L	L	H	L	L	L	L	L	H	32	32	1	C	
L	L	L	H	H	H	H	H	H	H	63	63	1	C	
L	L	L	H	H	H	H	H	H	L	H	63	1	D	
L	L	L	H	L	H	L	L	L	H	40	40	1	E	

- NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.
B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low unity/cascade will cause output Y to remain high.
C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.
D. Unity/cascade is used to inhibit output Y.
E. $f_{out} = \frac{M \cdot f_{in}}{64} = \frac{(8 + 32) f_{in}}{64} = \frac{40 f_{in}}{64} = 0.625 f_{in}$

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The diagram illustrates a 5-bit parallel counter circuit. It features five D-type flip-flops labeled QA, QB, QC, QD, and QE. Each flip-flop has a data input (G), a clock input (T), and a clear input (CLEAR). The outputs of the flip-flops are connected to five 3-to-8 decoders labeled A, B, C, D, and E. The decoders have inputs RATE INPUT B5, RATE INPUT B4, RATE INPUT B3, RATE INPUT B2, RATE INPUT B1, and RATE INPUT B0. The outputs of the decoders are connected to a 5-input OR gate, which produces the Z OUTPUT. The Z OUTPUT is also connected to a 6-input AND gate, which produces the Y OUTPUT. The Y OUTPUT is connected to a 7-input AND gate, which produces the ENABLE OUTPUT. The ENABLE INPUT (11) is connected to the 7-input AND gate. The CLEAR (13) and CLOCK (9) inputs are connected to the clear and clock inputs of the flip-flops. The STROBE (10) input is connected to the RATE INPUT B5 input of the decoders.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN5497 (see Note 2)	–55°C to 125°C
SN7497	0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

	SN5497			SN7497			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	20			20			ns
Width of clear pulse, $t_{w(clear)}$	15			15			ns
Enable setup time, t_{SU} : (See Figure 1)							
Before positive-going transition of clock pulse	25			25			ns
Before negative-going transition of previous clock pulse	0	$t_{w(clock)} - 10$		0	$t_{w(clock)} - 10$		
Enable hold time, t_H : (See Figure 1)							
After positive-going transition of clock pulse	0	$t_{w(clock)} - 10$		0	$t_{w(clock)} - 10$		ns
After negative-going transition of previous clock pulse	20	$t_{cp} - 10$		20	$t_{cp} - 10$		
Operating free-air temperature, T_A (See Note 2)	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			–1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			80	μ A
					40	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–3.2	mA
					–1.6	
I_{OS}	Short circuit output current§	$V_{CC} = \text{MAX}$	–18		–55	mA
I_{CCH}	Supply current, outputs high	$V_{CC} = \text{MAX},$ See Note 3		58		mA
I_{CCL}	Supply current, outputs low	$V_{CC} = \text{MAX},$ See Note 4		80	120	mA

† For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

- NOTES:
1. Voltage values are with respect to network ground terminal.
 2. An SN5497 in the W package operating at free-air temperatures above 118°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 55°C/W.
 3. I_{CCH} is measured with outputs open and all inputs grounded.
 4. I_{CCL} is measured with outputs open and all inputs at 4.5 V.



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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$

PARAMETER†	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			C _L = 15 pF, R _L = 400 Ω, See Figure 1	25	32		MHz
t _{PLH}	Enable	Enable			13	20	ns
t _{PHL}					14	21	
t _{PLH}	Strobe	Z			12	18	ns
t _{PHL}					15	23	
t _{PLH}	Clock	Y			26	39	ns
t _{PHL}					20	30	
t _{PLH}	Clock	Z			12	18	ns
t _{PHL}					17	26	
t _{PLH}	Rate	Z			6	10	ns
t _{PHL}					9	14	
t _{PLH}	Unity/Cascade	Y			9	14	ns
t _{PHL}					6	10	
t _{PLH}	Strobe	Y			19	30	ns
t _{PHL}					22	33	
t _{PLH}	Clock	Enable			19	30	ns
t _{PHL}					22	33	
t _{PLH}	Clear	Y			24	36	ns
t _{PHL}		Z			15	23	
t _{PLH}	Any Rate Input	Y			15	23	ns
t _{PHL}						15	

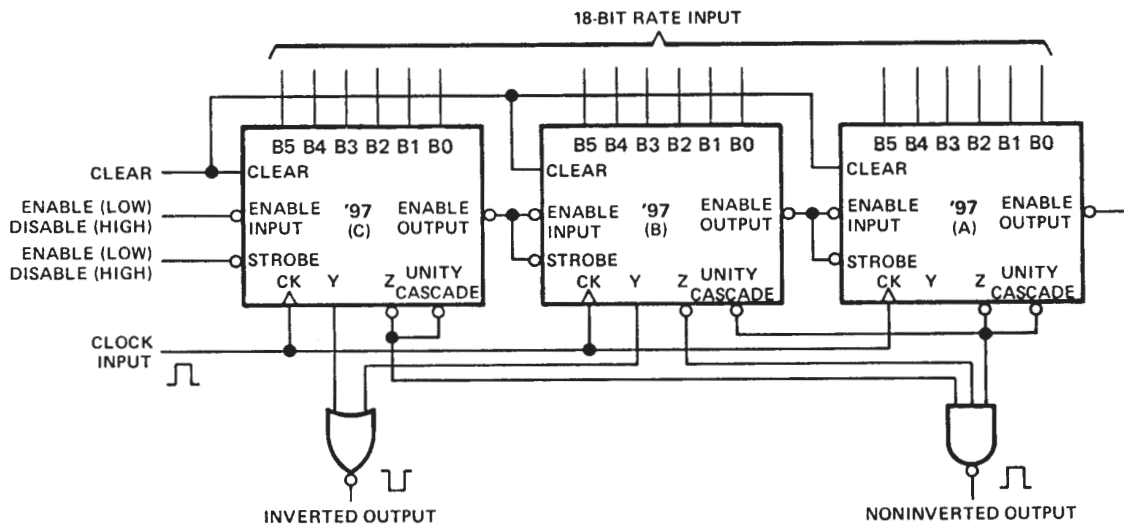
† $f_{\max}$ $\equiv$ maximum clock frequency.

t_{PLH} $\equiv$ propagation delay time, low-to-high-level output.

t_{PHL} $\equiv$ propagation delay time, high-to-low-level output.

TYPICAL APPLICATION DATA

This application demonstrates how the '97 can be cascaded to perform 18-bit rate multiplication. This scheme is expandable to n-bits by extending the pattern illustrated.

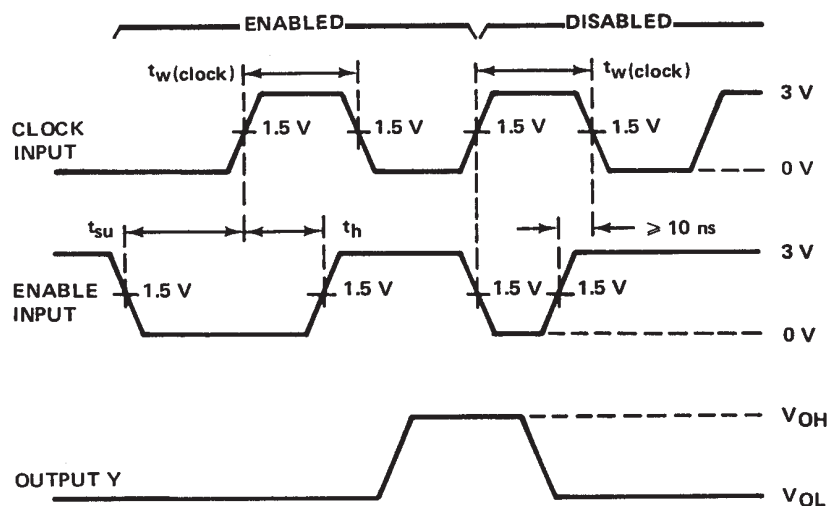


As illustrated, two of the 6-bit multipliers can be cascaded by connecting the Z output of unit A to the unity cascade input of unit B, in which case, a two-input NOR gate is used to cascade the remaining multipliers. Alternatively, all three Y outputs can be cascaded with a 3-input NOR gate. The three unused unity cascade inputs can be conveniently terminated by connecting each to its Z output.

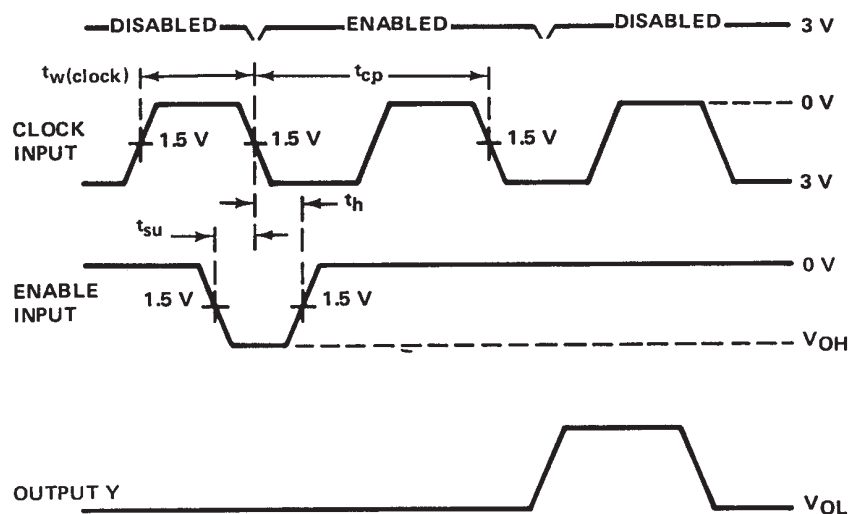
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PARAMETER MEASUREMENT INFORMATION



ENABLING FROM POSITIVE-GOING
TRANSITION OF CLOCK PULSE



ENABLING FROM NEGATIVE-GOING
TRANSITION OF PREVIOUS CLOCK PULSE

1. Unity/Cascade and pin 2 (rate input), other inputs are low. Clear the counter and apply clock and enable pulse as illustrated.
2. Setup and hold times are illustrated for enabling a single clock pulse (count). Continued application of the enable function will enable subsequent clock pulse (counts) until disabling occurs (enable goes high). The total number of counts will be determined by the total number of positive-going clock transition enabled.

NOTES: A. The input pulse generator has the following characteristics: $t_w(\text{clock}) = 20 \text{ ns}$, $t_{TLH} \leq 10 \text{ ns}$, $t_{THL} \leq 10 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$, $Z_{out} \approx 50 \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 1—SWITCHING TIMES

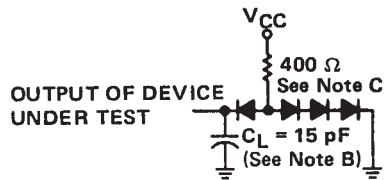


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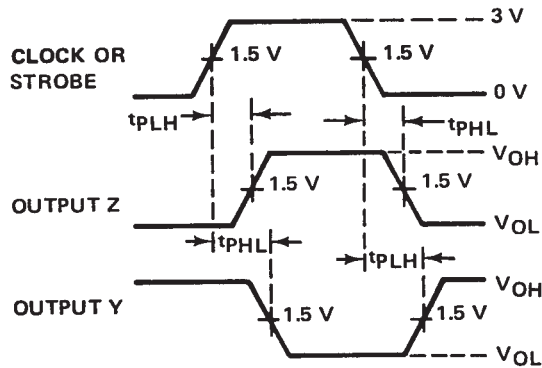
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PARAMETER MEASUREMENT INFORMATION



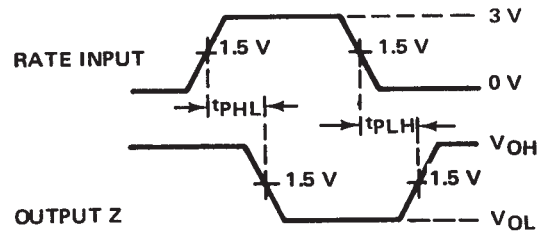
All three outputs are loaded during testing.

LOAD CIRCUIT



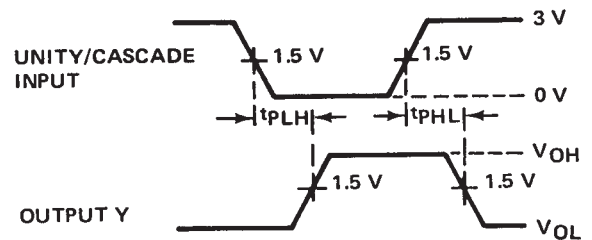
Unity/cascade and rate inputs are high, other inputs are low, and flip-flops are at any count other than maximum.

PROPAGATION DELAY TIMES, CLOCK TO Z AND Y, AND STROBE INPUT TO Z AND Y



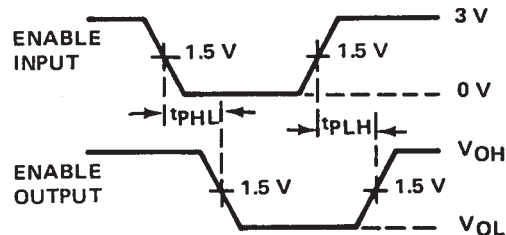
Flip-flops are at a count so that all other inputs to the gate under test are high and all other inputs, including other rate inputs, are low.

PROPAGATION DELAY TIMES, RATE INPUT TO Z



Output Z is high.

PROPAGATION DELAY TIMES, UNITY/CASCADE INPUT TO Y



Flip-flops are at the maximum count. Other inputs are low.

PROPAGATION DELAY TIMES, ENABLE INPUT TO ENABLE OUTPUT

- NOTES: A. The input pulse generator has the following characteristics: $t_{w(\text{clock})} = 20 \text{ ns}$, $t_{TLH} \leq 10 \text{ ns}$, $t_{THL} \leq 10 \text{ ns}$, $\text{PRR} = 1 \text{ MHz}$, $Z_{\text{out}} \approx 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

FIGURE 1—SWITCHING TIMES (CONTINUED)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN5497J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN5497J
SN5497J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN5497J
SN5497J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN5497J
SN7497N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN7497N
SN7497N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN7497N
SN7497N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN7497N
SN7497N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN7497N
SNJ5497J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ5497J
SNJ5497J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ5497J
SNJ5497J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ5497J
SNJ5497J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ5497J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN5497, SN7497 :

- Catalog : [SN7497](#)
- Military : [SN5497](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



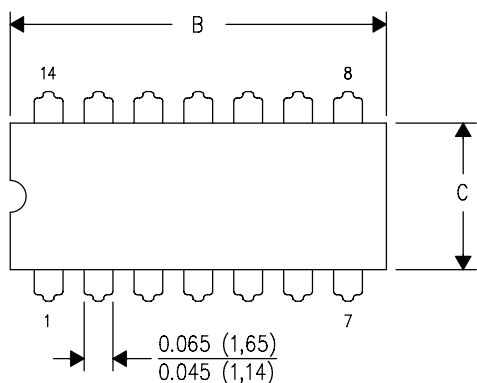
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN7497N	N	PDIP	16	25	506	13.97	11230	4.32
SN7497N	N	PDIP	16	25	506	13.97	11230	4.32
SN7497N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN7497N.A	N	PDIP	16	25	506	13.97	11230	4.32

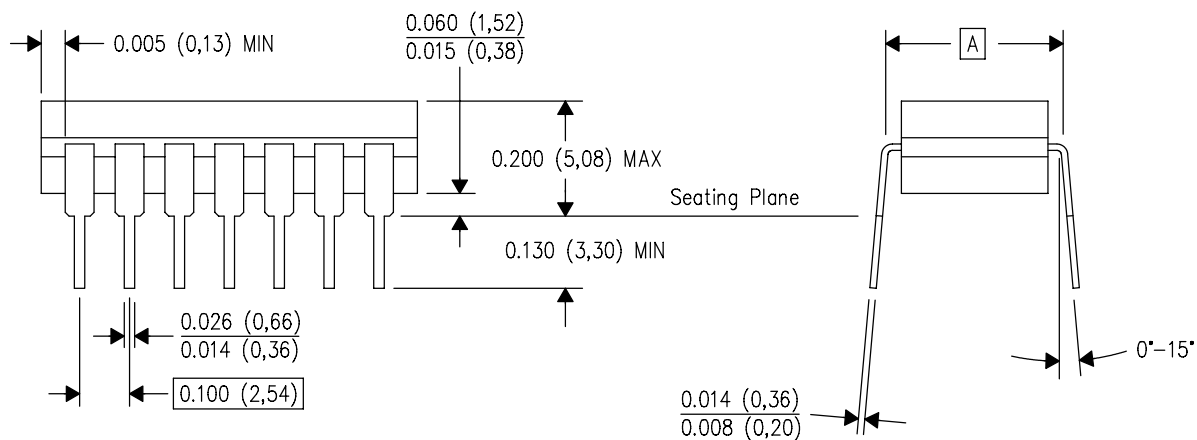
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



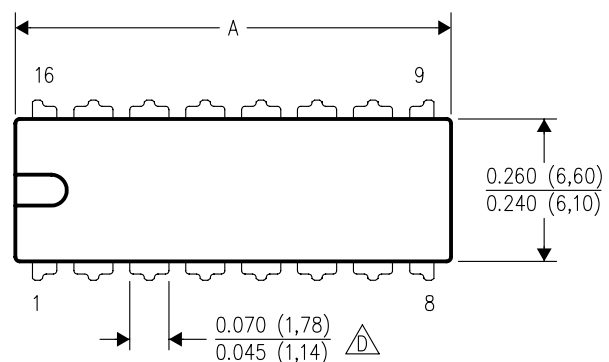
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

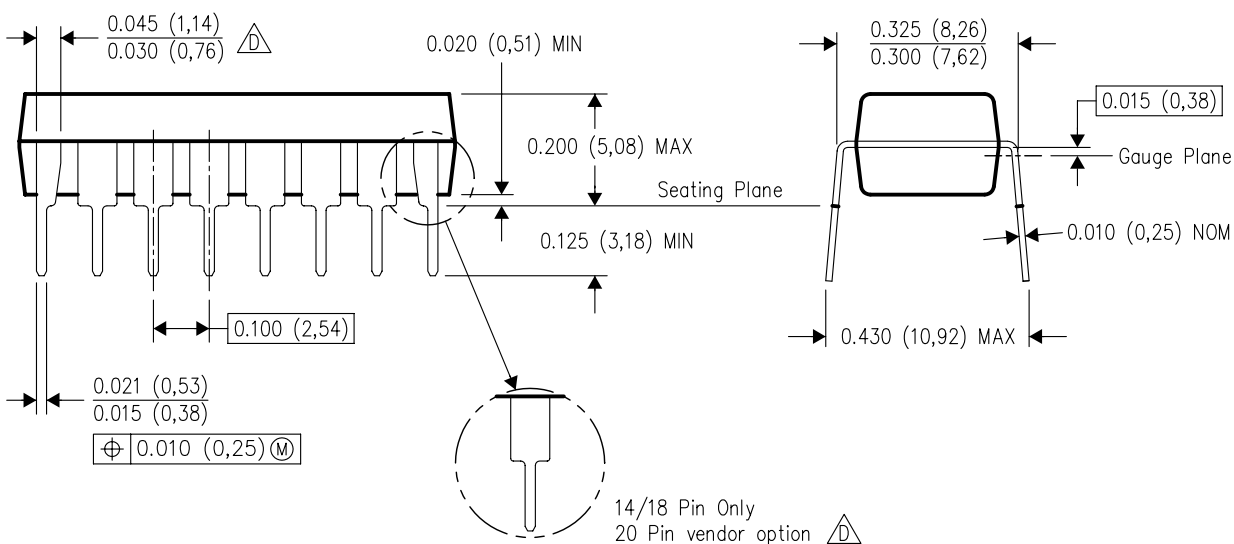
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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