

HIGH-SPEED DIFFERENTIAL LINE DRIVER

FEATURES

- Designed for Signaling Rates

NOTE: The signaling rate is the number of voltage transitions that can be made per second.

Up to 150 Mbps

- Low-Voltage Differential Signaling With Typical Output Voltage of 700 mV and a 100-Ω Load**
- Propagation Delay Time of 2.3 ns, Typical**
- Single 3.3-V Supply Operation**
- One Driver's Power Dissipation at 75 MHz, 50 mW, Typical**
- High-Impedance Outputs When Disabled or With $V_{CC} < 1.5$ V**
- Bus-Pin ESD Protection Exceeds 12 kV**
- Low-Voltage CMOS (LVCMOS) Logic Input Levels Are 5-V Tolerant**

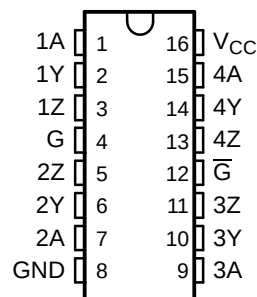
DESCRIPTION

The SN65LVDM31 incorporates four differential line drivers that implement the electrical characteristics of low-voltage differential signaling. This product offers a low-power alternative to 5-V PECL drivers with similar signal levels. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 540 mV into a 100-Ω load when enabled by either an active-low or active-high enable input.

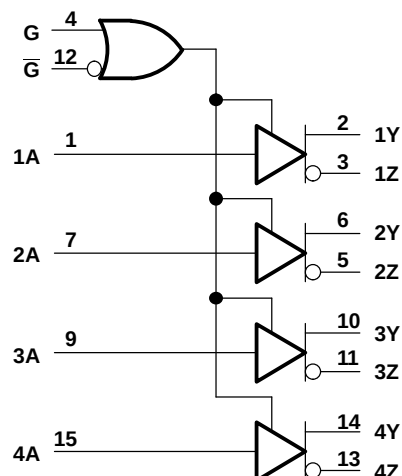
The intended application of this device and signaling technique is for both point-to-point and multiplexed baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDM31 is characterized for operation from –40°C to 85°C.

SN65LVDM31D (Marked as LVDM31)
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

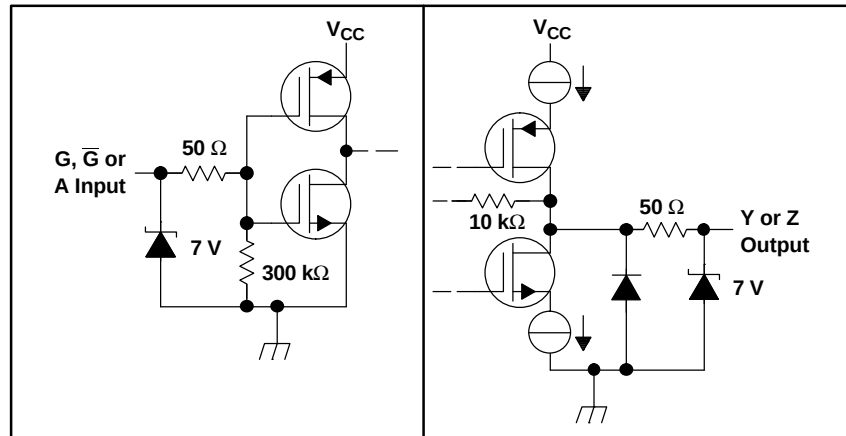


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		UNIT
Supply voltage range V_{CC} ⁽²⁾		–0.5 V to 4 V
Input voltage range	Inputs	–0.5 V to 6 V
	Y or Z	–0.5 V to 4 V
Electrostatic discharge ⁽³⁾ : Y, Z, and GND		Class 3, A:12 kV, B:600 V
Continuous power dissipation		See Dissipation Rating Table
Storage temperature range		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	OPERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	3	3.3	3.6	V
V_{IH} High-level input voltage	2.0			V
V_{IL} Low-level input voltage			0.8	V
T_A Operating free-air temperature	40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OD}	Differential output voltage magnitude	R _L = 100 Ω,	See Figure 2	540	700	860	mV
		R _L = 50 Ω,	See Figure 2	270	350	430	
Δ V _{OD}	Change in differential output voltage magnitude between logic states	See Figure 2		–25	0	25	mV
V _{OC(SS)}	Steady-state common-mode output voltage	See Figure 3		1.14	1.2	1.3	V
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states			–30	0	30	mV
V _{OC(PP)}	Peak-to-peak common-mode output voltage				70	100	
I _{CC}	Supply current	Enabled, No load	V _{IN} = 0 or V _{CC}		6	10	mA
		Enabled, R _L = 100 Ω			35	40	
		Disabled			0.5	0.7	
I _{IH}	High-level input current	V _{IH} = 3 V		–10	3	10	μA
I _{IL}	Low-level input current	V _{IL} = 0 V		–10	0	10	μA
I _{OS}	Short-circuit output current	V _{OY} or V _{OZ} = 0 V			7	10	mA
		V _{OD} = 0 V			7	10	
I _{OZ}	High-impedance state output current	V _O = 0 V or V _{CC}				±1	μA
I _{O(OFF)}	Power-off output current	V _{CC} = 1.5 V,	V _O = 3.6 V			±1	μA

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	See Figure 4	1.8	2.3	2.9	ns
t _{PHL}	Propagation delay time, high-to-low-level output		1.8	2.3	2.9	ns
t _r	Differential output signal rise time		0.4	0.6	1.0	ns
t _f	Differential output signal fall time		0.4	0.6	1.0	ns
t _{sk(p)}	Pulse skew (t _{PHL} – t _{PLH})			50	350	ps
t _{sk(o)}	Channel-to-channel output skew ⁽¹⁾				200	ps
t _{sk(pp)}	Part-to-part skew ⁽²⁾	See Figure 5			1	ns
t _{PZH}	Propagation delay time, high-impedance-to-high-level output			6	15	ns
t _{PZL}	Propagation delay time, high-impedance-to-low level output			6	15	ns
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output			6	15	ns
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output			6	15	ns

(1) t_{sk(o)} is the maximum delay time difference between drivers on the same device.

(2) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

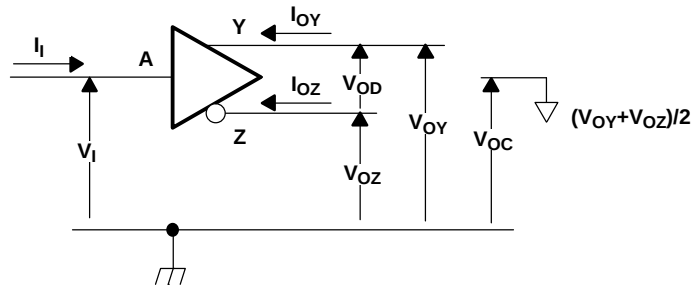
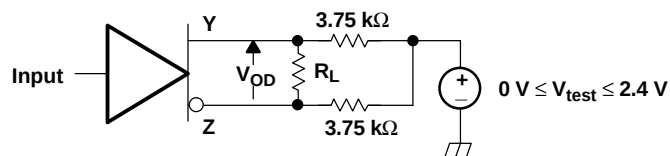
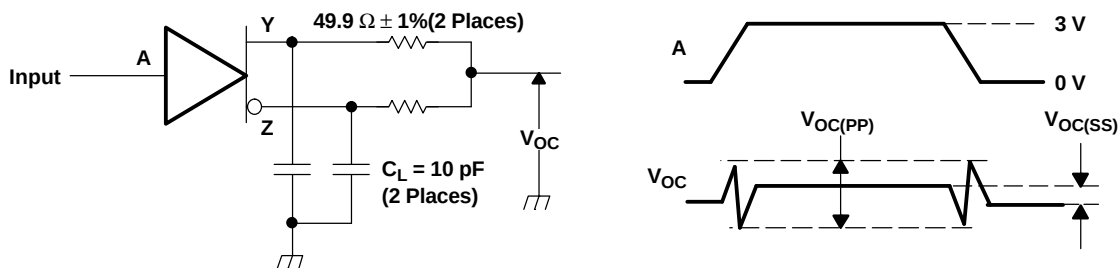
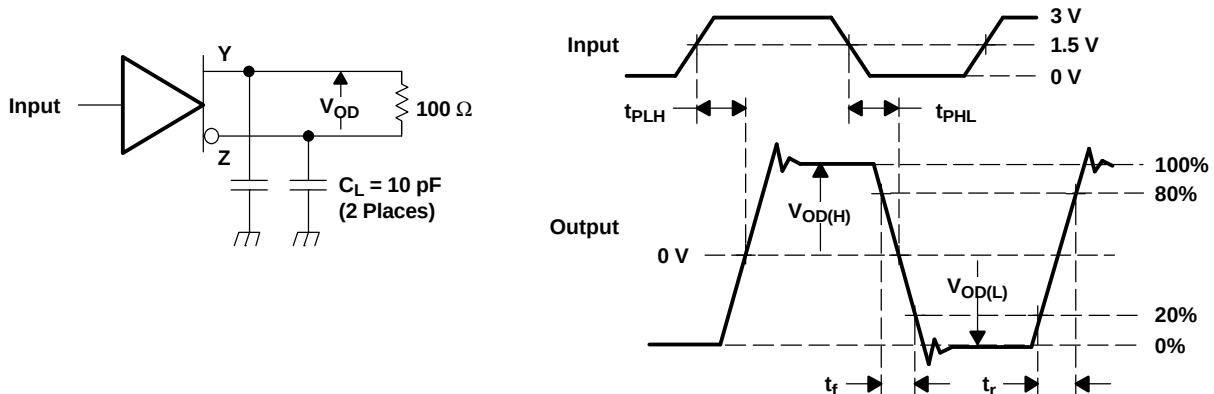


Figure 1. Driver Voltage and Current Definitions

Figure 2. V_{OD} Test Circuit

NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the DUT. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

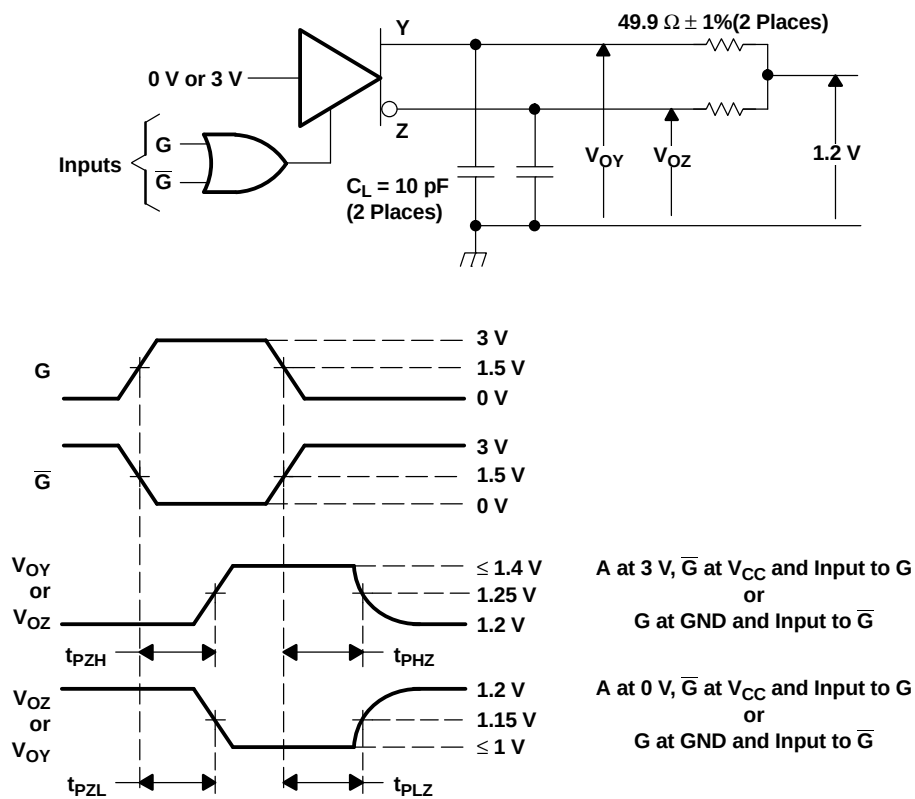
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the DUT.

Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the DUT.

Figure 5. Enable and Disable Time Circuit and Definitions

TYPICAL CHARACTERISTICS

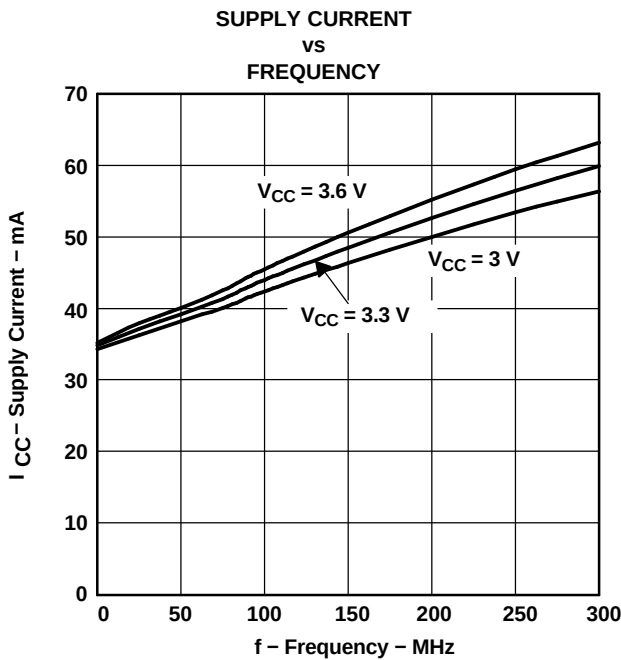


Figure 6.

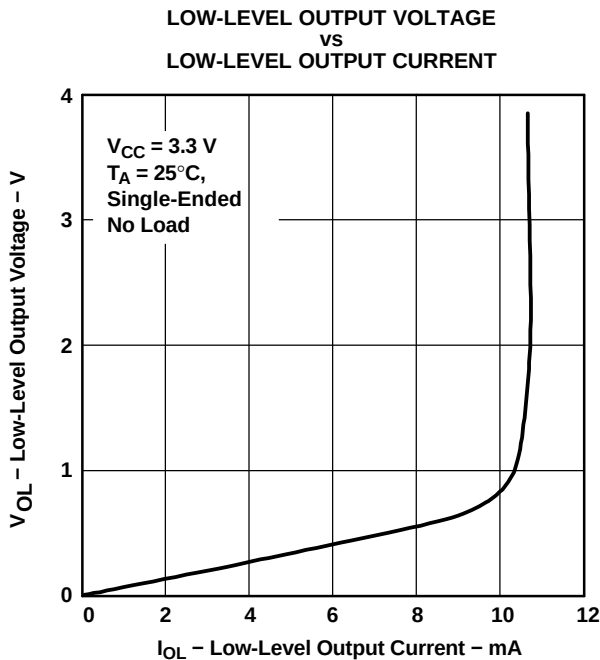


Figure 7.

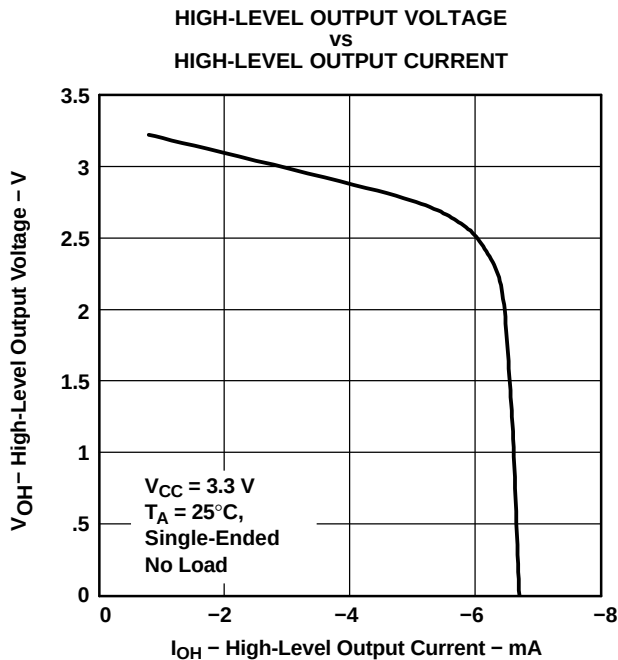


Figure 8.

TYPICAL CHARACTERISTICS (continued)

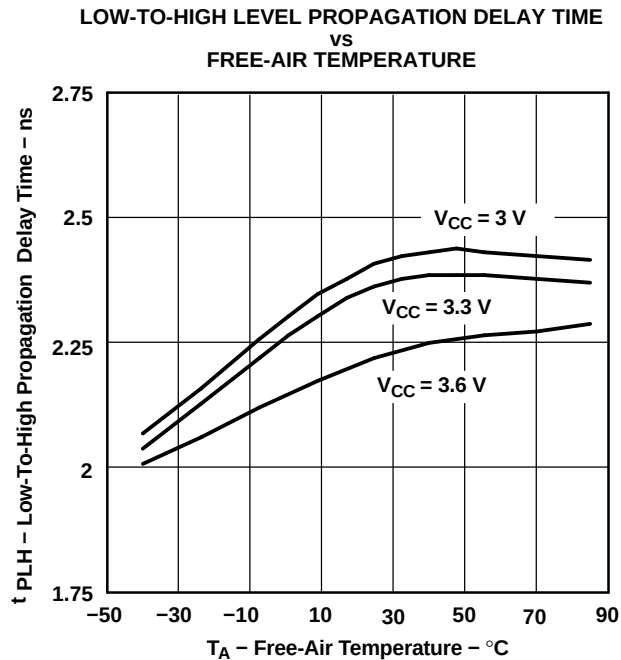


Figure 9.

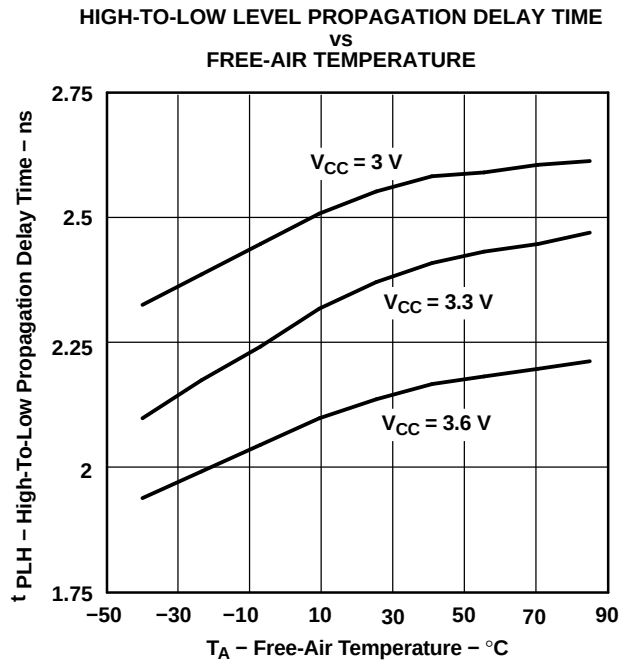


Figure 10.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDM31D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM31
SN65LVDM31D.B	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM31
SN65LVDM31DG4	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM31
SN65LVDM31DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM31
SN65LVDM31DR.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM31
SN65LVDM31DRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM31
SN65LVDM31DRG4.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDM31

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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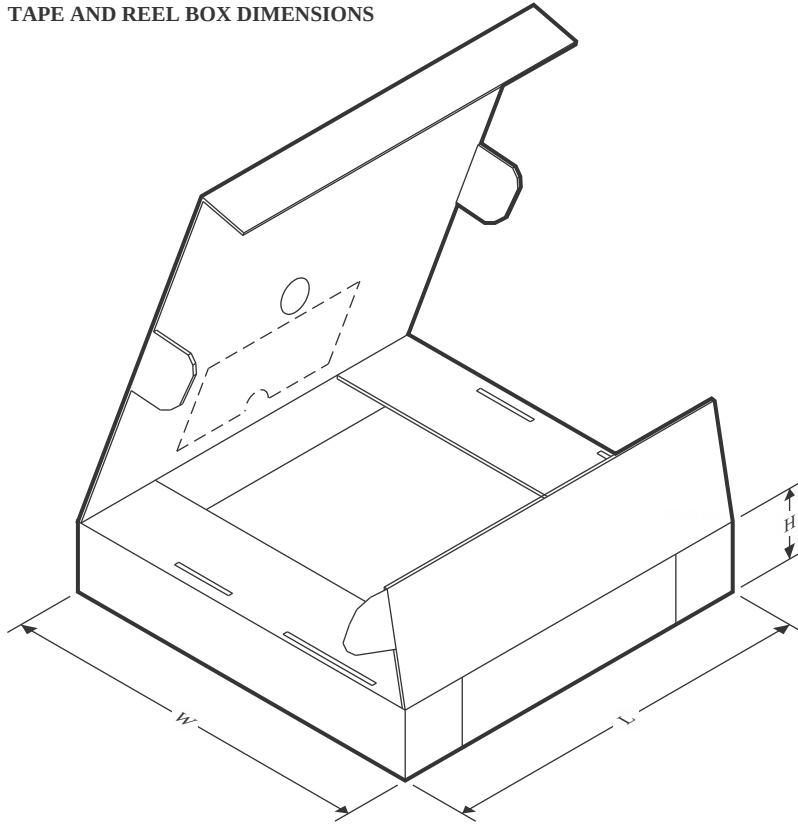
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDM31DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDM31DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

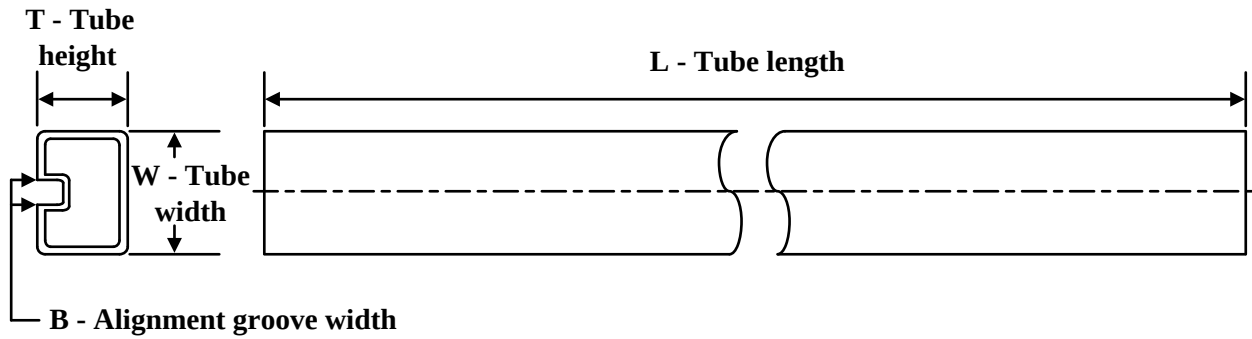
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDM31DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDM31DRG4	SOIC	D	16	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LVDM31D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDM31D.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDM31DG4	D	SOIC	16	40	505.46	6.76	3810	4

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Last updated 10/2025