SN54SC245-SEP Radiation-Tolerant, 1.2-V to 5.5-V, Octal Bus Transceivers With 3-State Outputs

1 Features

- Vendor item drawing available, VID V62/23616
- Total ionizing dose characterized at 30 krad(Si)
  - Total ionizing dose characterized radiation lot acceptance testing (TID RLAT) for every wafer lot to 30 krad(Si)
- Single-event effects (SEE) characterized:
  - Single event latch-up (SEL) immune to linear energy transfer (LET) = 43 MeV-cm2 /mg
  - Single event transient (SET) characterized to 43 MeV-cm2 /mg
- Wide operating range of 1.2 V to 5.5 V
- 5.5 V tolerant input pins
- Output drive up to 25 mA at 5-V
- Latch-up performance exceeds 250 mA per JESD 17
- Space enhanced plastic (SEP)
  - Controlled baseline
  - Gold bondwire
  - NiPdAu lead finish
  - One assembly and test site
  - One fabrication site
  - Military (–55°C to 125°C) temperature range
  - Extended product life cycle
  - Product traceability
  - Meets NASAs ASTM E595 outgassing specification

2 Applications

- Enable or Disable a Digital Signal
- Eliminate Slow or Noisy Input Signals
- Hold a Signal During Controller Reset
- Debounce a Switch

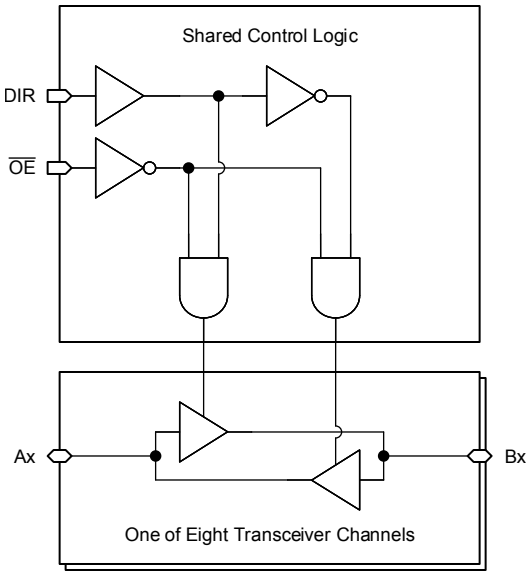
3 Description

SN54SC245-SEP is an octal bus transceiver with 3-state outputs. All eight channels are controlled by the direction (DIR) pin and output enable ($\overline{OE}$) pin. The output enable ($\overline{OE}$) controls all outputs in the device. When the $\overline{OE}$ pin is in the low state, the appropriate outputs as determined by the direction (DIR) pin are enabled. When the $\overline{OE}$ pin is in the high state, all outputs of the device are disabled. All disabled outputs are placed into the high-impedance state.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)(3)
SN54SC245-SEP	PW (TSSOP, 20)	6.5 mm × 6.4 mm	6.5 mm × 4.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Simplified Logic Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial Release

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5 Pin Configuration and Functions

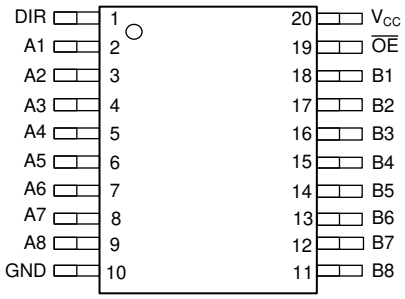

Figure 5-1. PW Package, 20-Pin TSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DIR	1	I	Direction control input (L = B → A, H = A → B)
A1	2	I/O	Channel 1 output/input A
A2	3	I/O	Channel 2 output/input A
A3	4	I/O	Channel 3 output/input A
A4	5	I/O	Channel 4 output/input A
A5	6	I/O	Channel 5 output/input A
A6	7	I/O	Channel 6 output/input A
A7	8	I/O	Channel 7 output/input A
A8	9	I/O	Channel 8 output/input A
GND	10	G	Ground
B8	11	I/O	Channel 8 input/output B
B7	12	I/O	Channel 7 input/output B
B6	13	I/O	Channel 6 input/output B
B5	14	I/O	Channel 5 input/output B
B4	15	I/O	Channel 4 input/output B
B3	16	I/O	Channel 3 input/output B
B2	17	I/O	Channel 2 input/output B
B1	18	I/O	Channel 1 input/output B
$\overline{OE}$	19	I	Output enable, active low
V_{CC}	20	P	Positive supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range(2)		-0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		-0.5	7	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5 V	-20		mA
I_{OK}	Output clamp current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	-20	20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}	-25	25	mA
	Continuous output current through V_{CC} or GND		-75	75	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 1.2 V to 1.3 V	0.78		V
		V_{CC} = 1.65 V to 2 V	1.1		
		V_{CC} = 2.25 V to 2.75 V	1.28		
		V_{CC} = 3 V to 3.6 V	1.45		
		V_{CC} = 4.5 V to 5.5 V	2		
V_{IL}	Low-Level input voltage	V_{CC} = 1.2 V to 1.3 V		0.36	V
		V_{CC} = 1.65 V to 2 V		0.51	
		V_{CC} = 2.25 V to 2.75 V		0.65	
		V_{CC} = 3 V to 3.6 V		0.75	
		V_{CC} = 4.5 V to 5.5 V		0.80	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	3-state	0	V_{CC}	V
		High or low state	0	V_{CC}	
I_O	Output Current	V_{CC} = 1.65 V to 2.0 V		±3	mA
		V_{CC} = 2.25 V to 2.75 V		±7	
		V_{CC} = 3.3 V to 5.0 V		±15	
		V_{CC} = 4.5 V to 5.5 V		±25	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.6 V to 5.5 V		20	ns/V
T_A	Operating free-air temperature		–55	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74SC245-SEP PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.8	°C/W
Y_{JB}	Junction-to-board characterization parameter	69.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = -55°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH} = -50 µA	1.2 V to 5.5 V	V_{CC}-0.1			V
	I_{OH} = -1 mA	1.2 V	0.8			
	I_{OH} = -2 mA	1.65 V	1.21			
	I_{OH} = -3 mA	2.25 V	1.93			
	I_{OH} = -5.5 mA	3.0 V	2.49			
	I_{OH} = -8 mA	4.5 V	3.95			
V_{OL}	I_{OL} = 50 µA	1.2 V to 5.5 V			0.1	V
	I_{OL} = 1 mA	1.2 V			0.2	
	I_{OL} = 2 mA	1.65 V			0.25	
	I_{OL} = 3 mA	2.25 V			0.2	
	I_{OL} = 5.5 mA	3.0 V			0.25	
	I_{OH} = 8 mA	4.5 V			0.35	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	1.2 V to 1.3 V		2	750	µA
		1.65 V to 2.0 V		10	850	µA
		4.5 V to 5.5 V		20	1,100	µA
Δ_{ICC}	One input at 0.3 V or 3.4 V, other inputs at V_{CC} or GND	5.5 V			1.5	mA
	One input at 0.3 V or 1.1 V, other inputs at V_{CC} or GND	1.8 V			10	µA
I_I	V_I = 0 V to V_{CC}	V_I = 0 V to V_{CC}			±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±2.5	µA
C_i	V_I = V_{CC} or GND	3.3 V		2	10	pF
C_O	Vo = V_{CC} or GND	3.3 V		5		pF
C_{PD} (1) (2)	C_L = 50 pF, F = 10 MHz	1.65 V to 5.5 V		15		pF

(1) C_{PD} is used to determine the dynamic power consumption, per channel.
(2) $P_D = V_{CC}^2 \times F_I \times (C_{PD} + C_L)$ where F_I= input frequency, C_L= output load capacitance, V_{CC}= supply voltage.

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6.6 Switching Characteristics 1.2-V V_{CC}

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			-55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	A or B	B or A	C_L = 15 pF		32.7	62.5	1	32.2	68.4	ns
t_{en}	$\overline{OE}$	A or B			44.6	85	1	44	90.5	ns
t_{dis}	$\overline{OE}$	A or B			35.2	63.6	1	34.7	67	ns
t_{pd}	A or B	B or A	C_L = 50 pF		40.9	77.7	1	40.2	86.7	ns
t_{en}	$\overline{OE}$	A or B			53.4	98.3	1	52.7	109.7	ns
t_{dis}	$\overline{OE}$	A or B			43.4	71.5	1	42.9	76.5	ns
$t_{sk(o)}$			C_L = 50 pF		3.4	8.6		3.3	9.3	ns

6.7 Switching Characteristics 1.8-V V_{CC}

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			-55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	A or B	B or A	C_L = 15 pF		11.5	19.3	1	11.9	22.4	ns
t_{en}	$\overline{OE}$	A or B			15.7	25.6	1	16.3	38.8	ns
t_{dis}	$\overline{OE}$	A or B			13.6	22	1	13.9	30.7	ns
t_{pd}	A or B	B or A	C_L = 50 pF		15	24.6	1	15.3	27.9	ns
t_{en}	$\overline{OE}$	A or B			19.4	30.6	1	19.9	44.3	ns
t_{dis}	$\overline{OE}$	A or B			18.6	30.2	1	18.9	33.4	ns
$t_{sk(o)}$			C_L = 50 pF			2.1			2.2	ns

6.8 Switching Characteristics 2.5-V V_{CC}

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			-55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	A or B	B or A	C_L = 15 pF		7.2	11.2	1	7.5	13.7	ns
t_{en}	$\overline{OE}$	A or B			10	15.2	1	10.7	23	ns
t_{dis}	$\overline{OE}$	A or B			8.1	13.6	1	8.4	17	ns
t_{pd}	A or B	B or A	C_L = 50 pF		9.7	14.9	1	10.1	17.7	ns
t_{en}	$\overline{OE}$	A or B			12.9	18.7	1	13.6	26.9	ns
t_{dis}	$\overline{OE}$	A or B			11.7	19.9	1	12	22.4	ns
$t_{sk(o)}$			C_L = 50 pF			1.1			1.2	ns

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6.9 Switching Characteristics 3.3-V V_{CC}

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			-55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	A or B	B or A	C_L = 15 pF		5.5	8	1	5.7	10	ns
t_{en}	$\overline{OE}$	A or B			7.5	11	1	8.2	16.5	ns
t_{dis}	$\overline{OE}$	A or B			5.9	9.9	1	6	12.4	ns
t_{pd}	A or B	B or A	C_L = 50 pF		7.6	11	1	7.8	13.1	ns
t_{en}	$\overline{OE}$	A or B			10.1	14.9	1	10.6	20	ns
t_{dis}	$\overline{OE}$	A or B			8.5	14.7	1	8.5	15.9	ns
$t_{sk(o)}$			C_L = 50 pF			0.7			0.9	ns

6.10 Switching Characteristics 5-V V_{CC}

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			-55°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	A or B	B or A	C_L = 15 pF		4.1	5.5	1	4.4	6.8	ns
t_{en}	$\overline{OE}$	A or B			5.4	8.5	1	6	11	ns
t_{dis}	$\overline{OE}$	A or B			4.5	7.3	1	4.4	8.4	ns
t_{pd}	A or B	B or A	C_L = 50 pF		5.8	7.8	1	6	9.3	ns
t_{en}	$\overline{OE}$	A or B			7.5	12.6	1	8	14.1	ns
t_{dis}	$\overline{OE}$	A or B			5.7	10.6	1	5.7	11.4	ns
$t_{sk(o)}$			C_L = 50 pF			0.6			0.6	ns

6.11 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.6		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

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6.12 Typical Characteristics

T_A = 25°C (unless otherwise noted)

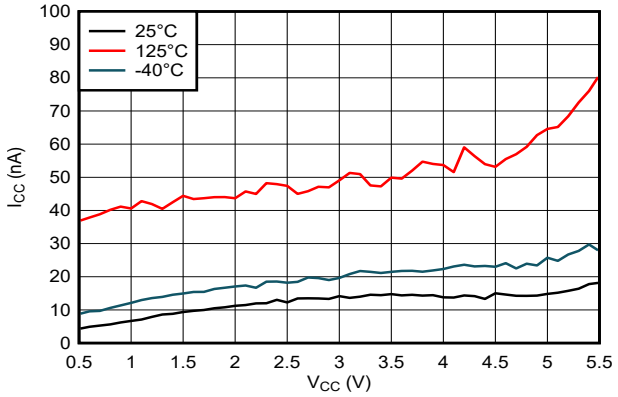

Figure 6-1. Supply Current Across Operating Voltage

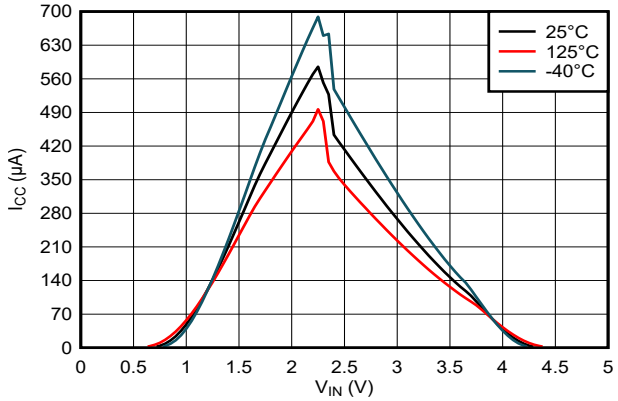

Figure 6-2. Supply Current Across Input Voltage, 5-V Supply

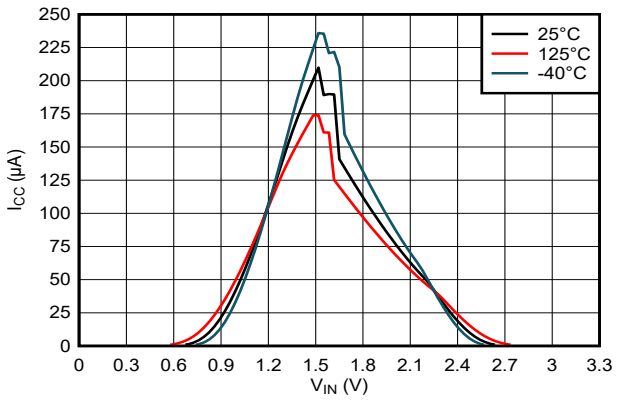

Figure 6-3. Supply Current Across Input Voltage, 3.3-V Supply

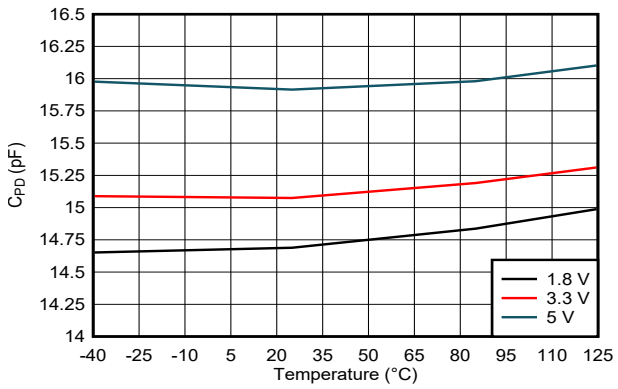

Figure 6-4. Power Dissipation Capacitance per Gate Across Temperature, 1.8-V, 3.3-V, and 5-V Supply

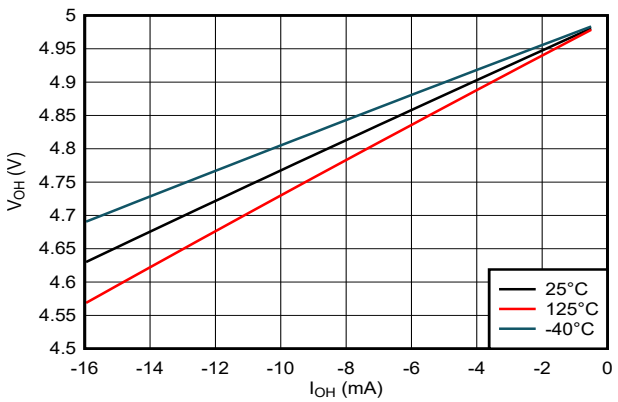

Figure 6-5. Output Voltage vs Current in HIGH State; 5-V Supply

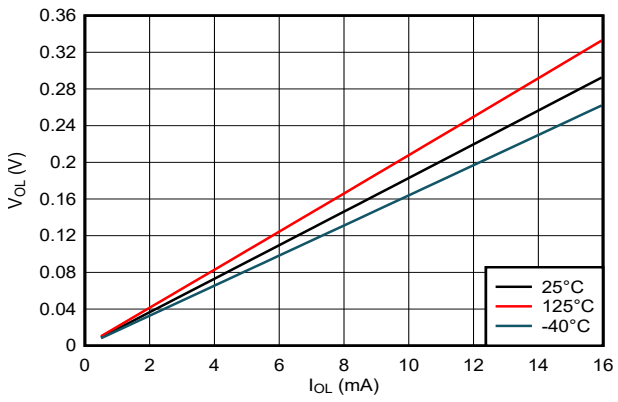

Figure 6-6. Output Voltage vs Current in LOW State; 5-V Supply

6.12 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

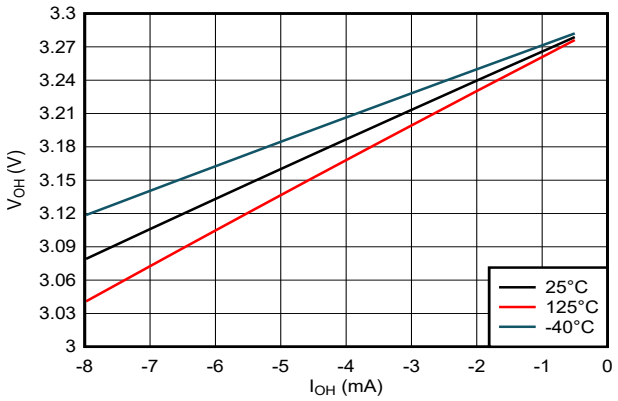

Figure 6-7. Output Voltage vs Current in HIGH State; 3.3-V Supply

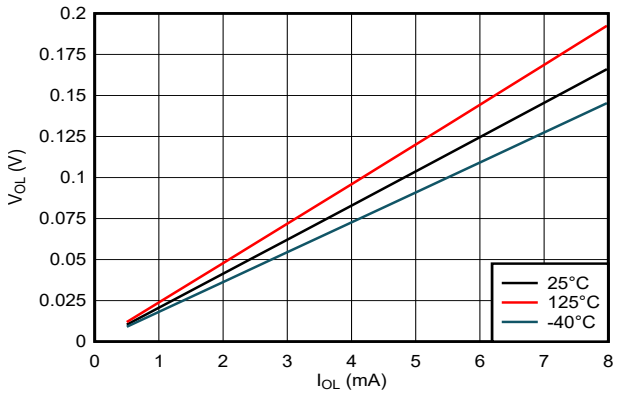

Figure 6-8. Output Voltage vs Current in LOW State; 3.3-V Supply

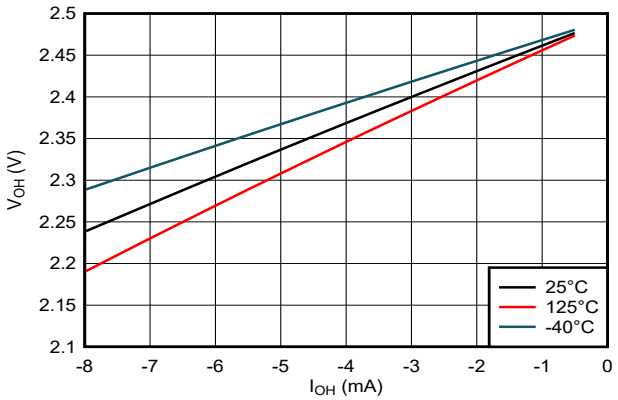

Figure 6-9. Output Voltage vs Current in HIGH State; 2.5-V Supply

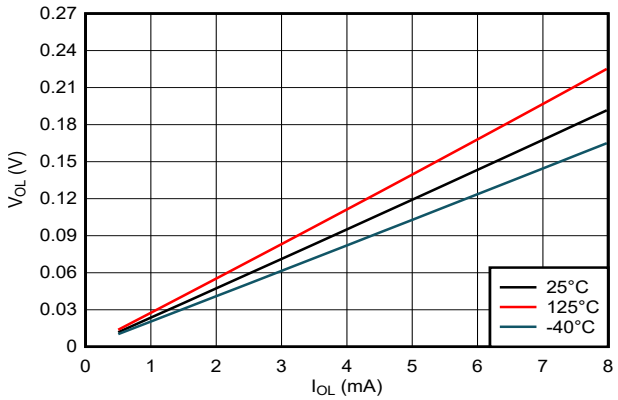

Figure 6-10. Output Voltage vs Current in LOW State; 2.5-V Supply

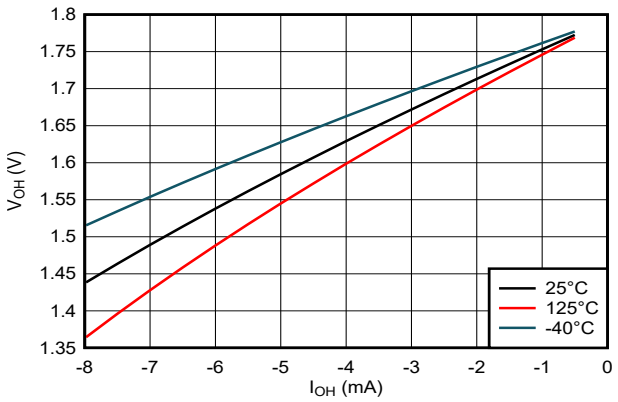

Figure 6-11. Output Voltage vs Current in HIGH State; 1.8-V Supply

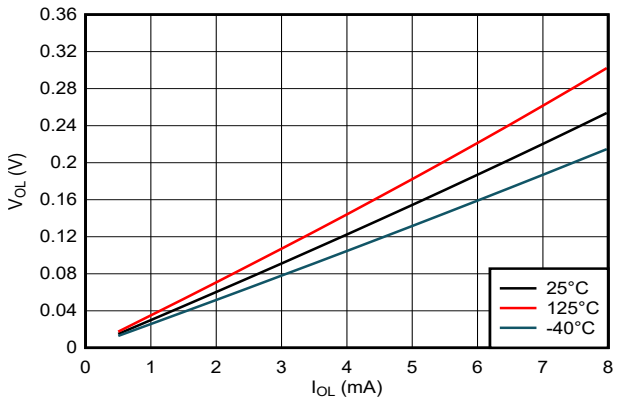

Figure 6-12. Output Voltage vs Current in LOW State; 1.8-V Supply

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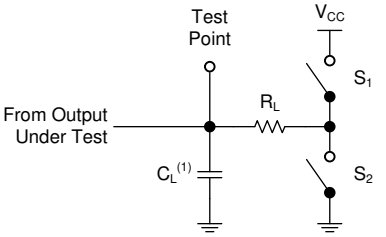
7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t< 2.5 ns.

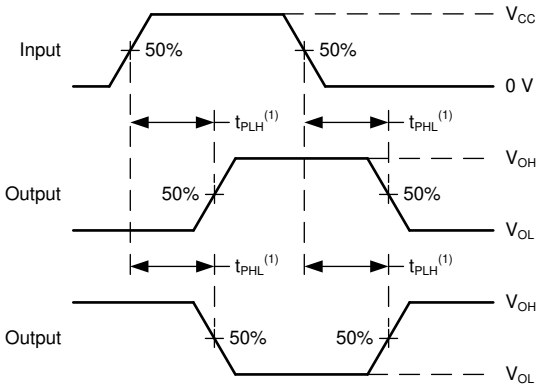
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



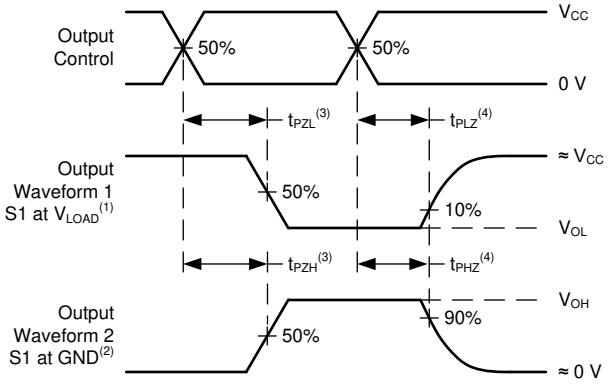
(1) C_L includes probe and test-fixture capacitance.

Figure 7-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 7-2. Voltage Waveforms Propagation Delays



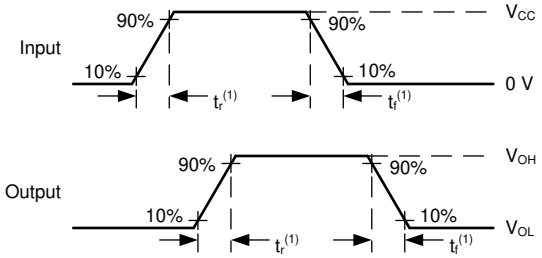
(1) S1 = CLOSED, S2 = OPEN.

(2) S1 = OPEN, S2 = CLOSED.

(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 7-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 7-4. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

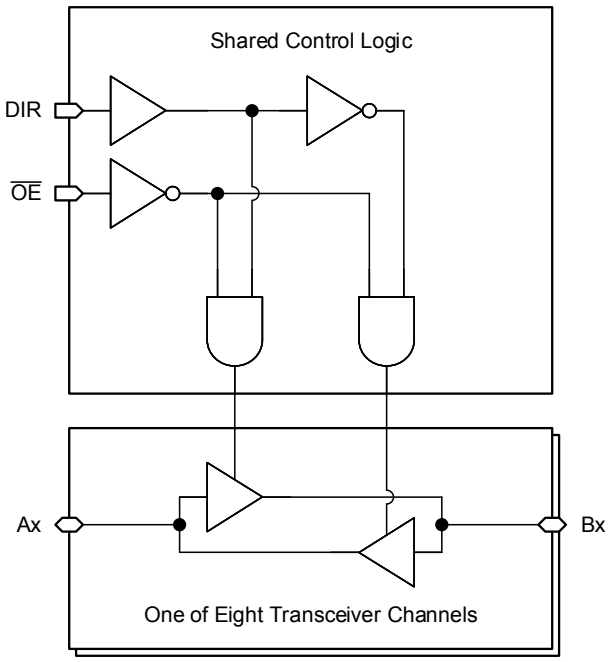
8.1 Overview

The SN54SC245-SEP is an octal bus transceiver with 3-state outputs. All eight channels are controlled by the direction (DIR) pin and output enable ($\overline{OE}$) pin. Each transceiver includes one buffer oriented from Ax to Bx and one from Bx to Ax, with at least one output disabled at all times. The direction (DIR) pin controls which buffer is active. The buffer that is not active has the output placed into the high-impedance state.

The output enable ($\overline{OE}$) controls all outputs in the device. When the $\overline{OE}$ pin is in the low state, the appropriate outputs as determined by the direction (DIR) pin are enabled. When the $\overline{OE}$ pin is in the high state, all outputs of the device are disabled. All disabled outputs are placed into the high-impedance state.

To enable the high-impedance state during power up or power down, the $\overline{OE}$ pin should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table. Typically a 10-kΩ resistor will be sufficient.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-kΩ resistor is recommended and will typically meet all requirements.

8.3.2 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

8.3.3 Clamp Diode Structure

As Figure 8-1 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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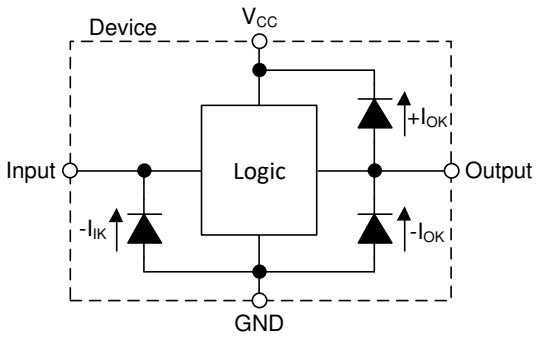

Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN54SC245-SEP.

Table 8-1. Function Table

INPUTS(1)		OUTPUTS(2)	
$\overline{OE}$	DIR	A	B
L	L	B	Z
L	H	Z	A
H	X	Z	Z

(1) H = High voltage level, L = Low voltage level, X = Do not care
(2) A = Logic value at 'A' input, B = Logic value at 'B' input, Z = High impedance

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN54SC245-SEP can be used to drive signals over relatively long traces or transmission lines. To reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver, a series damping resistor placed in series with the transmitter's output can be used. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

9.2 Typical Application

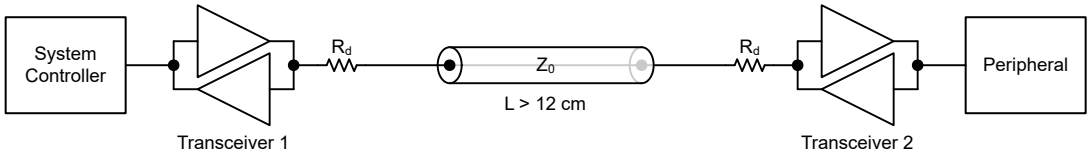

Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN54SC245-SEP plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN54SC245-SEP plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN54SC245-SEP can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN54SC245-SEP can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

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CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN54SC245-SEP (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN54SC245-SEP has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, the limit will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN54SC245-SEP to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω, which will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

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9.2.3 Application Curve

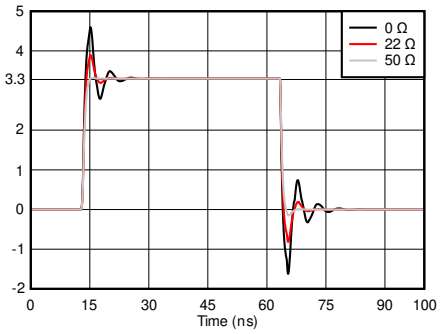

Figure 9-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor (R_d) Values

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

9.4.2 Layout Example

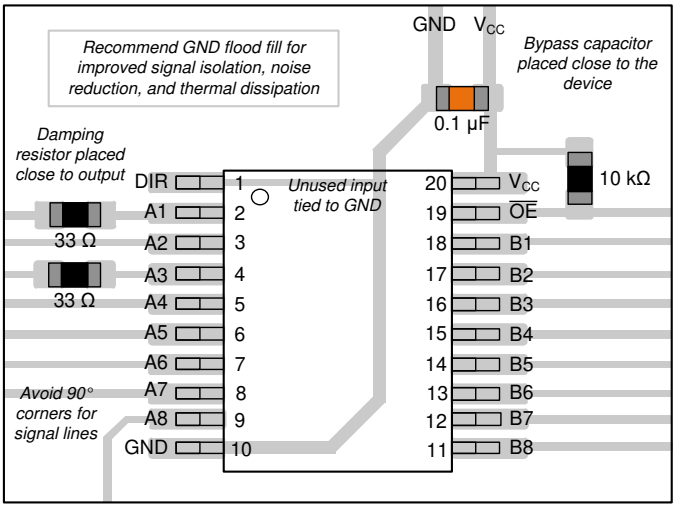

Figure 9-3. Example Layout for the SN54SC245-SEP

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation*
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*

10.2 Receiving Notification of Documentation Updates

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10.3 Support Resources

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN54SC245MPWTSEP	Active	Production	TSSOP (PW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SC245SEP
SN54SC245MPWTSEP.A	Active	Production	TSSOP (PW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	SC245SEP
V62/23616-01XE	Active	Production	TSSOP (PW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See SN54SC245MPWTSEP	SC245SEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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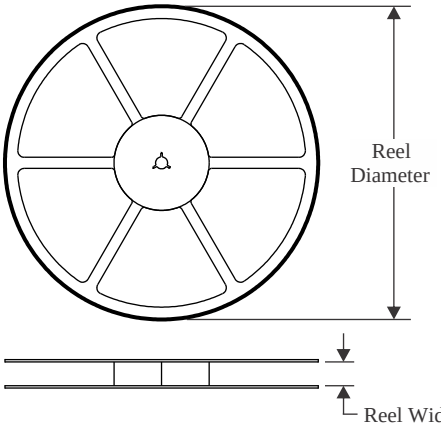
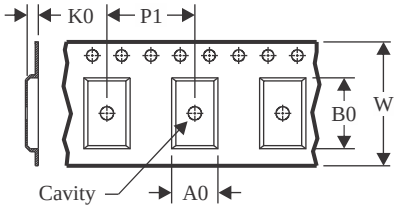
TAPE AND REEL INFORMATION

REEL DIMENSIONS

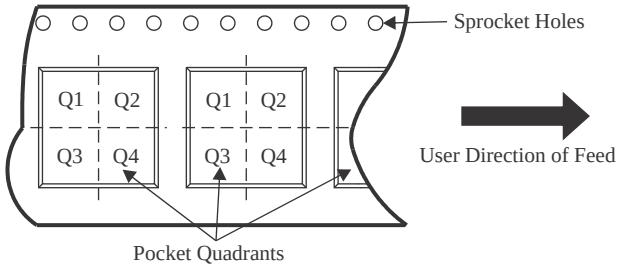


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

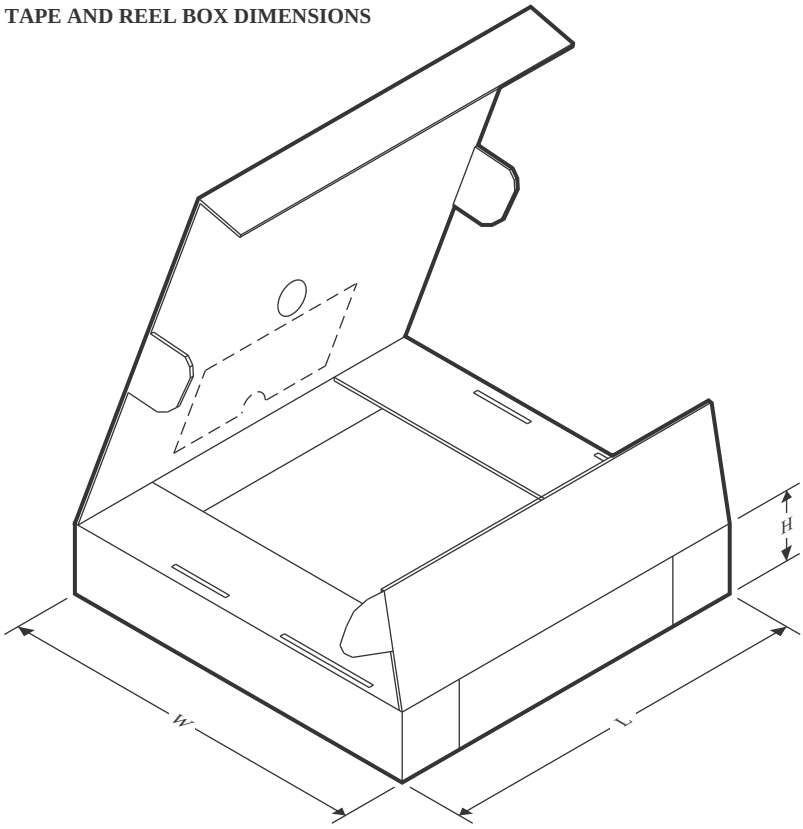
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN54SC245MPWTSEP	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

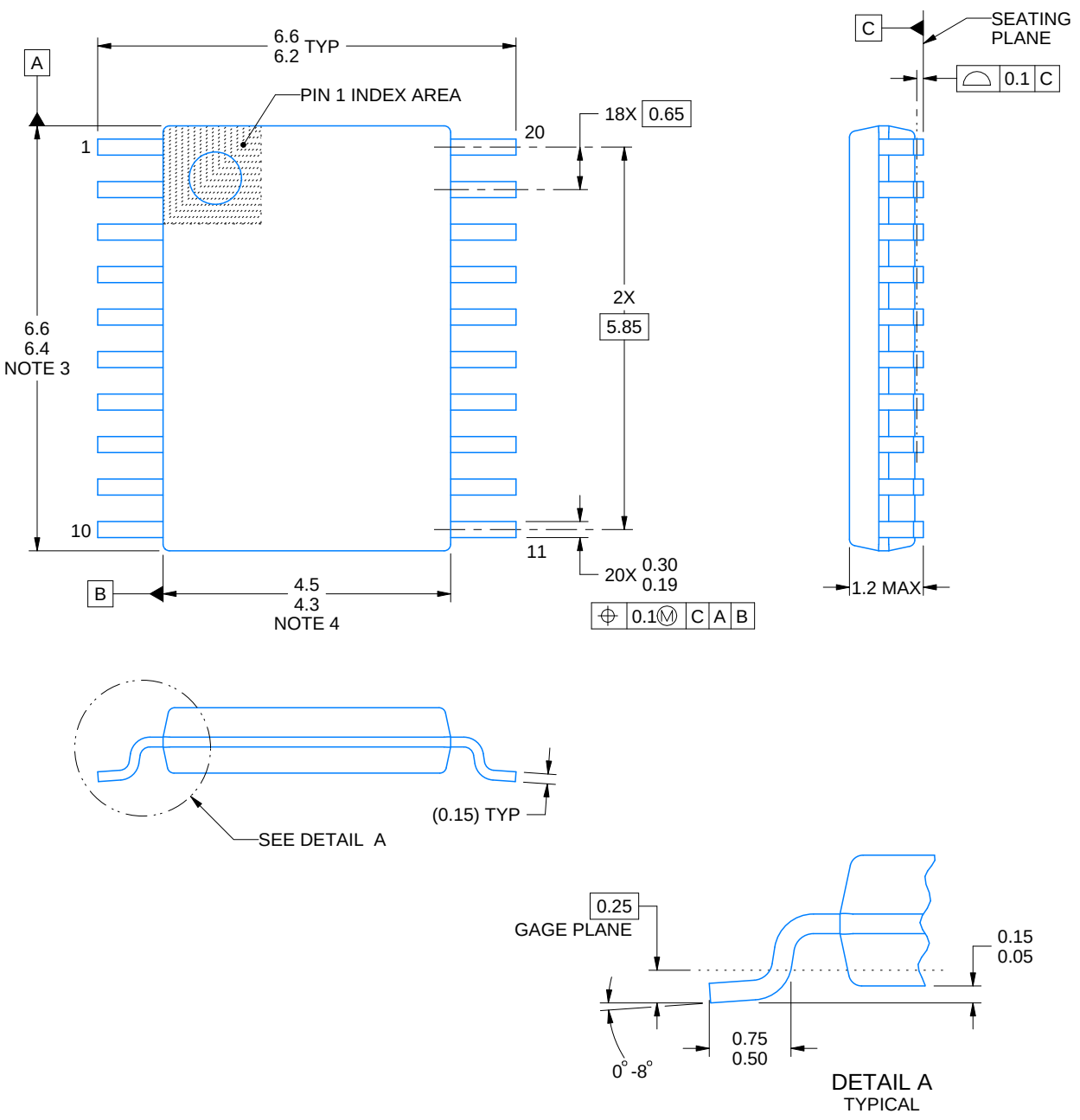
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN54SC245MPWTSEP	TSSOP	PW	20	250	353.0	353.0	32.0

PACKAGE OUTLINE

PW0020A

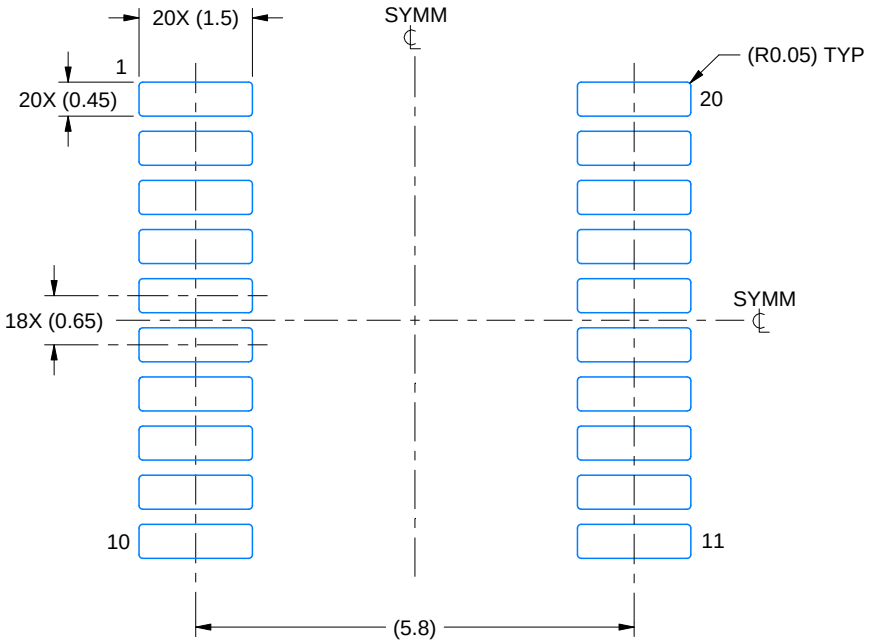
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

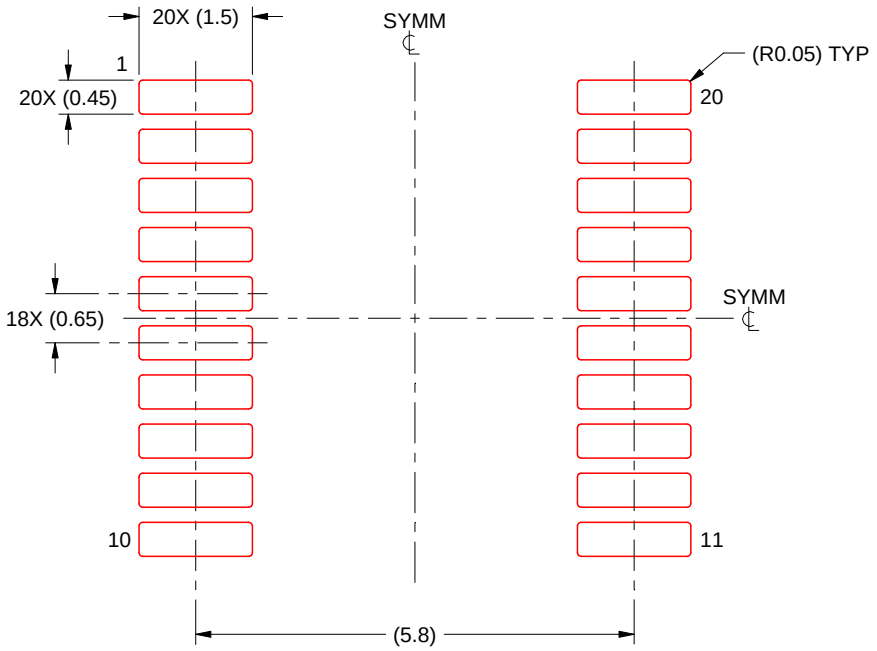


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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