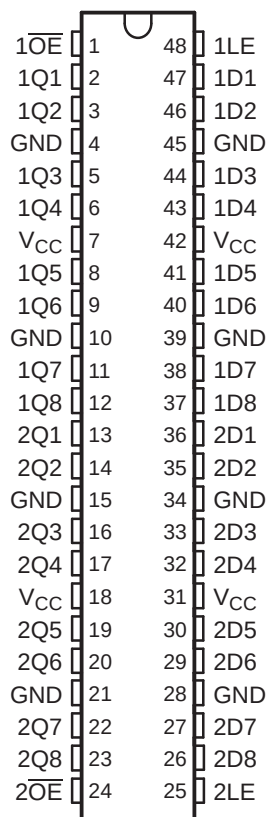


FEATURES

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54LVTH16373... WD PACKAGE
SN74LVTH16373... DGG OR DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The 'LVTH16373 devices are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	FBGA – GRD	Reel of 1000	SN74LVTH16373GRDR	LL373
	FBGA – ZRD (Pb-free)		SN74LVTH16373ZRDR	
	SSOP – DL	Tube of 25	SN74LVTH16373DL	LVTH16373
			SN74LVTH16373DLG4	
		Reel of 1000	SN74LVTH16373DLR	
			SN74LVTH16373DLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVTH16373DGGR	LVTH16373
	VFBGA – GQL	Reel of 1000	SN74LVTH16373GQLR	LL373
	VFBGA – ZQL (Pb-free)		SN74LVTH16373ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN54LVTH16373, SN74LVTH16373

3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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ORDERING INFORMATION (continued)

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CFP – WD	Tube	SNJ54LVTH16373WD	SNJ54LVTH16373WD
			5962-9681001QXA	

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

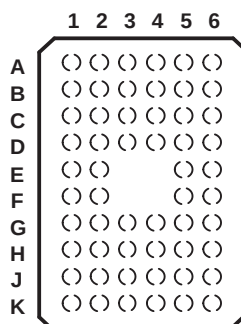
$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

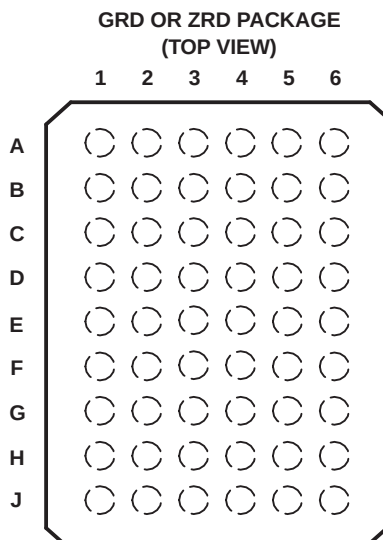
GQL OR ZQL PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL/ZQL Package)

	1	2	3	4	5	6
A	1 $\overline{OE}$	NC	NC	NC	NC	1CLK
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	V _{CC}	V _{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	V _{CC}	V _{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2 $\overline{OE}$	NC	NC	NC	NC	2CLK

(1) NC – No internal connection



TERMINAL ASSIGNMENTS⁽¹⁾
(54-Ball GRD/ZRD Package)

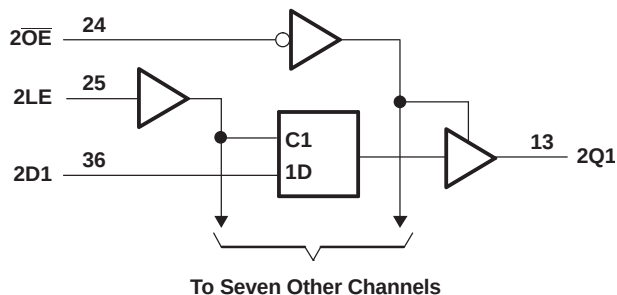
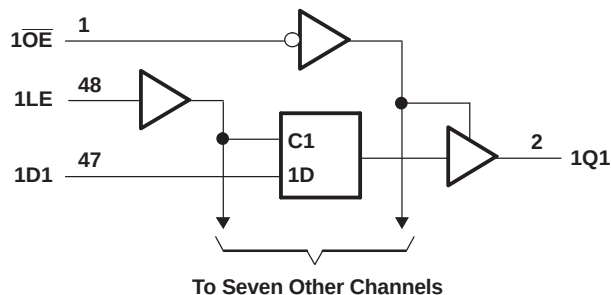
	1	2	3	4	5	6
A	1Q1	NC	1 $\overline{OE}$	1LE	NC	1D1
B	1Q3	1Q2	NC	NC	1D2	1D3
C	1Q5	1Q4	V _{CC}	V _{CC}	1D4	1D5
D	1Q7	1Q6	GND	GND	1D6	1D7
E	2Q1	1Q8	GND	GND	1D8	2D1
F	2Q3	2Q2	GND	GND	2D2	2D3
G	2Q5	2Q4	V _{CC}	V _{CC}	2D4	2D5
H	2Q7	2Q6	NC	NC	2D6	2D7
J	2Q8	NC	2 $\overline{OE}$	2LE	NC	2D8

(1) NC – No internal connection

FUNCTION TABLE
(8-BIT SECTION)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DL, and WD packages.

SN54LVTH16373, SN74LVTH16373

3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	4.6	V
V _I	Input voltage range ⁽²⁾	–0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	7	V
V _O	Voltage range applied to any output in the high state ⁽²⁾	–0.5	V _{CC} + 0.5	V
I _O	Current into any output in the low state	SN54LVTH16373	96	mA
		SN74LVTH16373	128	
I _O	Current into any output in the high state ⁽³⁾	SN54LVTH16373	48	mA
		SN74LVTH16373	64	
I _{IK}	Input clamp current	V _I < 0	–50	mA
I _{OK}	Output clamp current	V _O < 0	–50	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package	70	°C
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
T _{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This current flows only when the output is in the high state and V_O > V_{CC}.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		SN54LVTH16373		SN74LVTH16373		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		–24		–32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outpts enabled			10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16373		SN74LVTH16373		UNIT
				MIN	TYP ⁽¹⁾	MAX	MIN	
V _{IK}		V _{CC} = 2.7 V, I _I = −18 mA		−1.2		−1.2		V
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = −100 μA		V _{CC} − 0.2		V _{CC} − 0.2		V
		V _{CC} = 2.7 V, I _{OH} = −8 mA		2.4		2.4		
		V _{CC} = 3 V		I _{OH} = −24 mA				
				I _{OH} = −32 mA		2		
V _{OL}		V _{CC} = 2.7 V		I _{OL} = 100 μA		0.2		V
				I _{OL} = 24 mA		0.5		
		V _{CC} = 3 V		I _{OL} = 16 mA		0.4		
				I _{OL} = 32 mA		0.5		
				I _{OL} = 48 mA		0.55		
				I _{OL} = 64 mA		0.55		
I _I		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10		10		μA
	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1		±1		
	Data inputs	V _{CC} = 3.6 V		V _I = V _{CC}		1		
				V _I = 0		−5		
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100		μA
I _{I(hold)}	Data inputs	V _{CC} = 3 V		V _I = 0.8 V		75		μA
				V _I = 2 V		−75		
		V _{CC} = 3.6 V, ⁽²⁾ V _I = 0 to 3.6 V				±500		
I _{OZH}		V _{CC} = 3.6 V, V _O = 3 V		5		5		μA
I _{OZL}		V _{CC} = 3.6 V, V _O = 0.5 V		−5		−5		μA
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care		±100 ⁽³⁾		±100		μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care		±100 ⁽³⁾		±100		μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.19		mA
				Outputs low		5		
				Outputs disabled		0.19		
ΔI _{CC} ⁽⁴⁾		V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2		mA
C _i		V _I = 3 V or 0		3		3		pF
C _o		V _O = 3 V or 0		9		9		pF

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

SN54LVTH16373, SN74LVTH16373

3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCBS144P – MAY 1992 – REVISED NOVEMBER 2006

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		SN54LVTH16373				SN74LVTH16373				UNIT
		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE high	3		3		3		3		ns
t _{su}	Setup time, data before LE↓	2		2		1		0.6		ns
t _h	Hold time, data after LE↓	3		3.3		1		1.1		ns

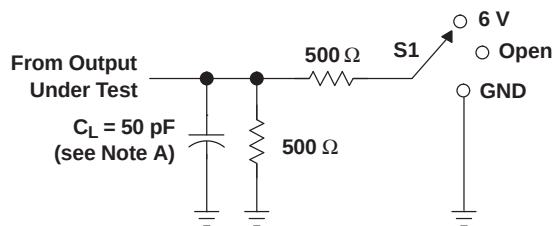
Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see [Figure 1](#))

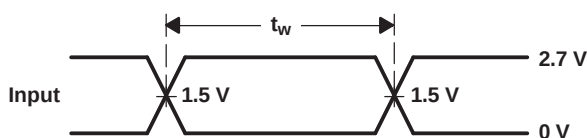
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16373				SN74LVTH16373				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP ⁽¹⁾	MAX	MIN		MAX
t _{PLH}	D	Q	1.4	4.5	5.2		1.5	2.7	3.8	4.2		ns
t _{PHL}			1.4	4.4	4.8		1.5	2.5	3.6	4		
t _{PLH}	LE	Q	1.8	5.5	5.8		2.1	3	4.3	4.8		ns
t _{PHL}			1.8	5.2	5.6		2.1	2.9	4	4		
t _{PZH}	OE	Q	1.4	5.7	6.7		1.5	2.8	4.3	5.1		ns
t _{PZL}			1.4	5.5	6		1.5	2.8	4.3	4.7		
t _{PHZ}	OE	Q	2	6	6.2		2.4	3.5	5	5.4		ns
t _{PLZ}			1.4	5.2	5.6		2	3.2	4.7	4.8		
t _{sk(LH)}									0.5			ns
t _{sk(HL)}									0.5			

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

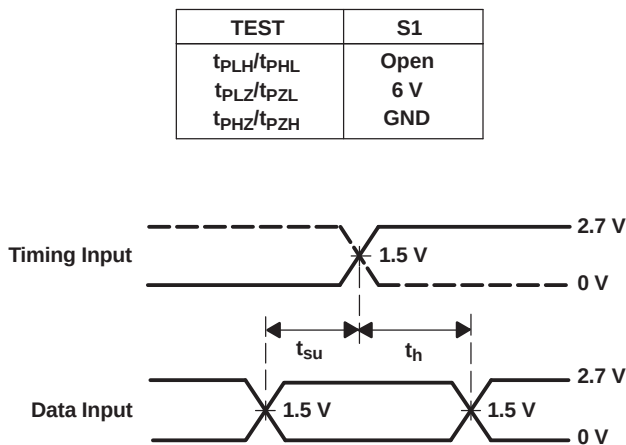
PARAMETER MEASUREMENT INFORMATION



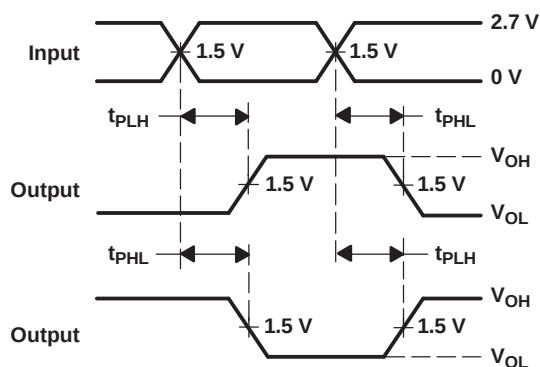
LOAD CIRCUIT



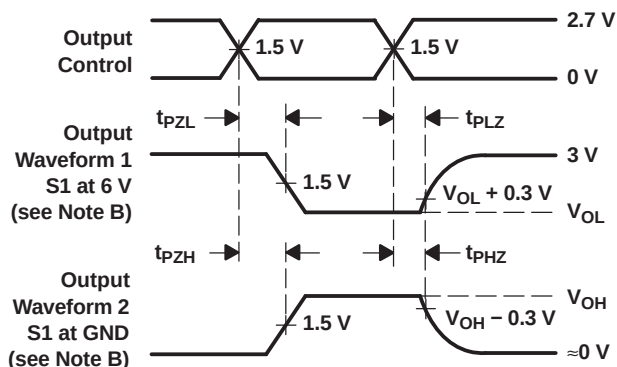
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9681001QXA	Active	Production	CFP (WD) 48	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681001QX A SNJ54LVTH16373 WD
74LVTH16373DGGR1G4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16373
74LVTH16373DGGR1G4.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16373
SN74LVTH16373DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16373
SN74LVTH16373DGGR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16373
SN74LVTH16373DL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16373
SN74LVTH16373DL.B	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16373
SN74LVTH16373DLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16373
SN74LVTH16373DLR.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16373
SN74LVTH16373DLRG4	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16373
SN74LVTH16373DLRG4.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16373
SNJ54LVTH16373WD	Active	Production	CFP (WD) 48	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681001QX A SNJ54LVTH16373 WD

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVTH16373, SN74LVTH16373 :

- Catalog : [SN74LVTH16373](#)
- Enhanced Product : [SN74LVTH16373-EP](#), [SN74LVTH16373-EP](#)
- Military : [SN54LVTH16373](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

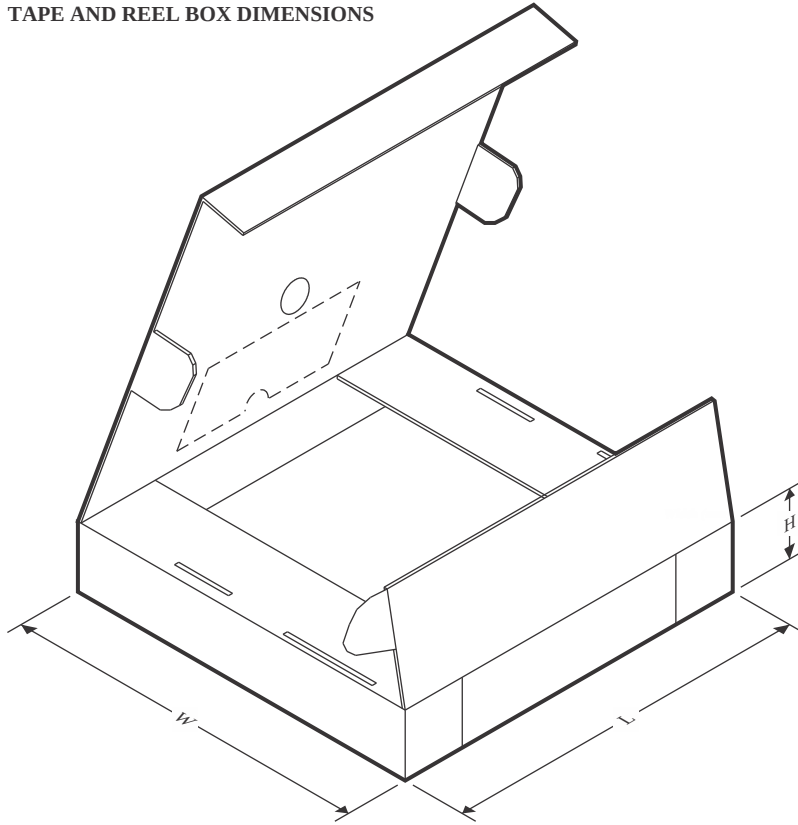
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVTH16373DGGR1G4	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH16373DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH16373DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVTH16373DLRG4	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

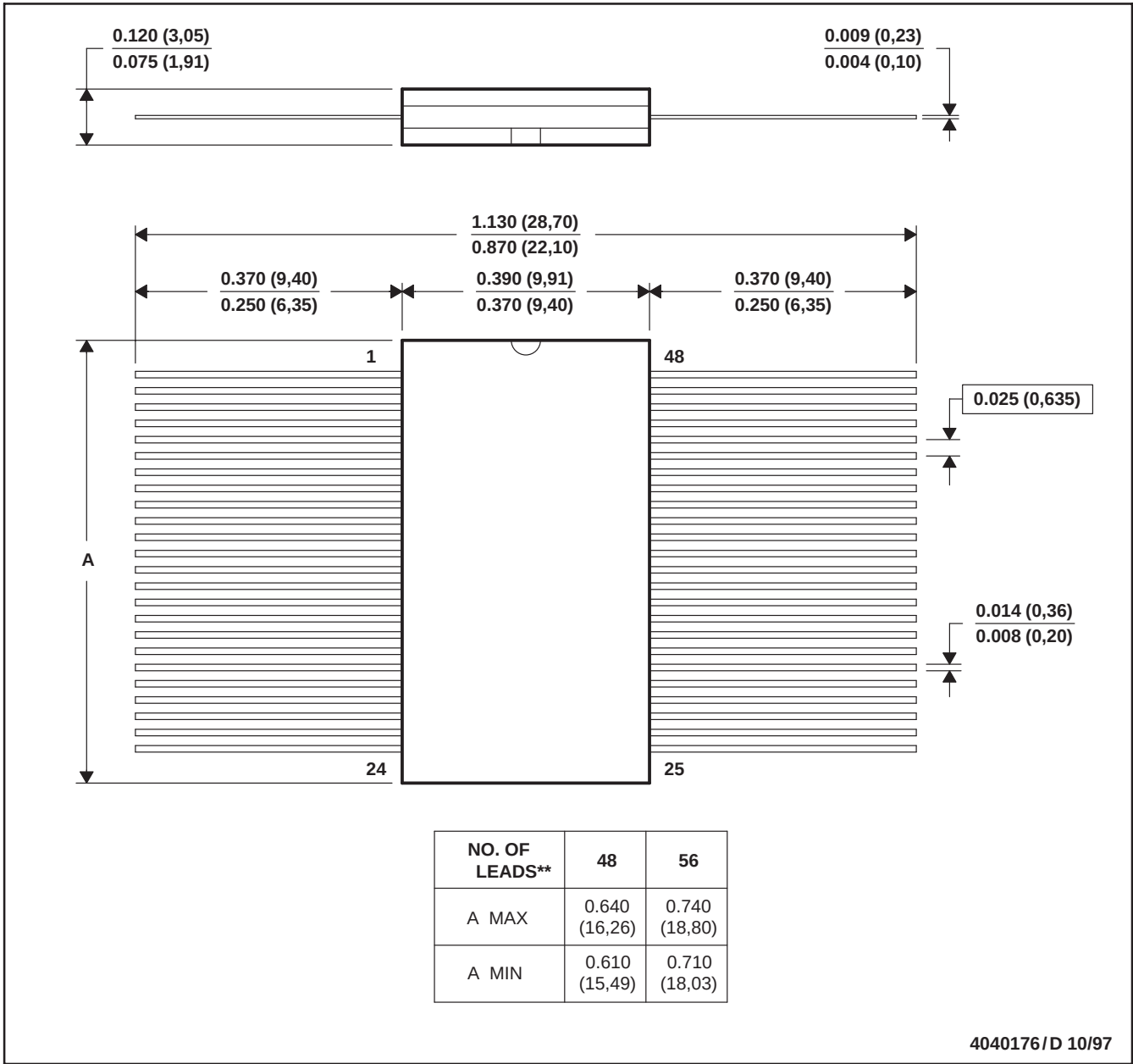


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVTH16373DGGR1G4	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74LVTH16373DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74LVTH16373DLR	SSOP	DL	48	1000	356.0	356.0	53.0
SN74LVTH16373DLRG4	SSOP	DL	48	1000	356.0	356.0	53.0

WD (R-GDFP-F**)
48 LEADS SHOWN

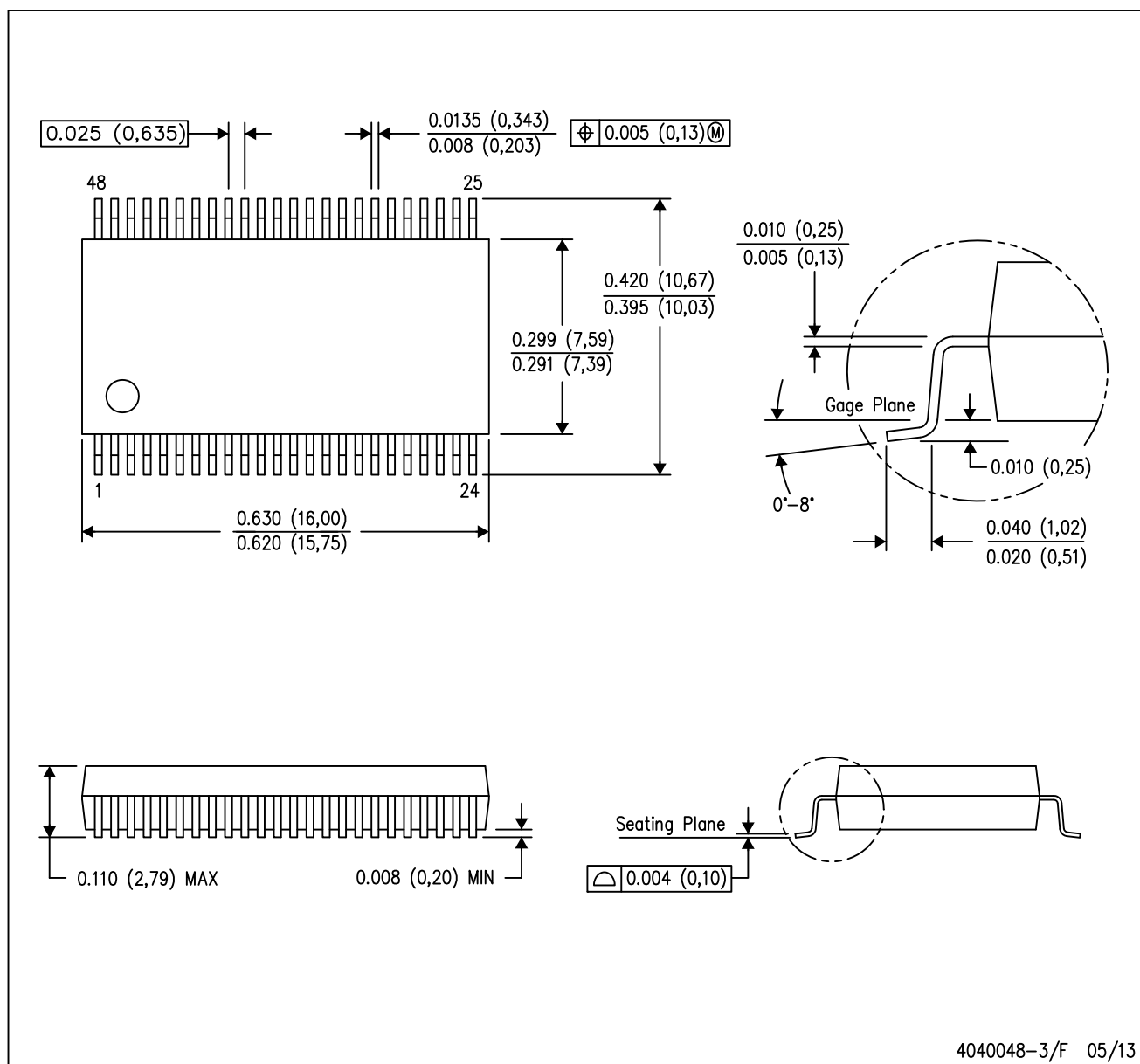
CERAMIC DUAL FLATPACK



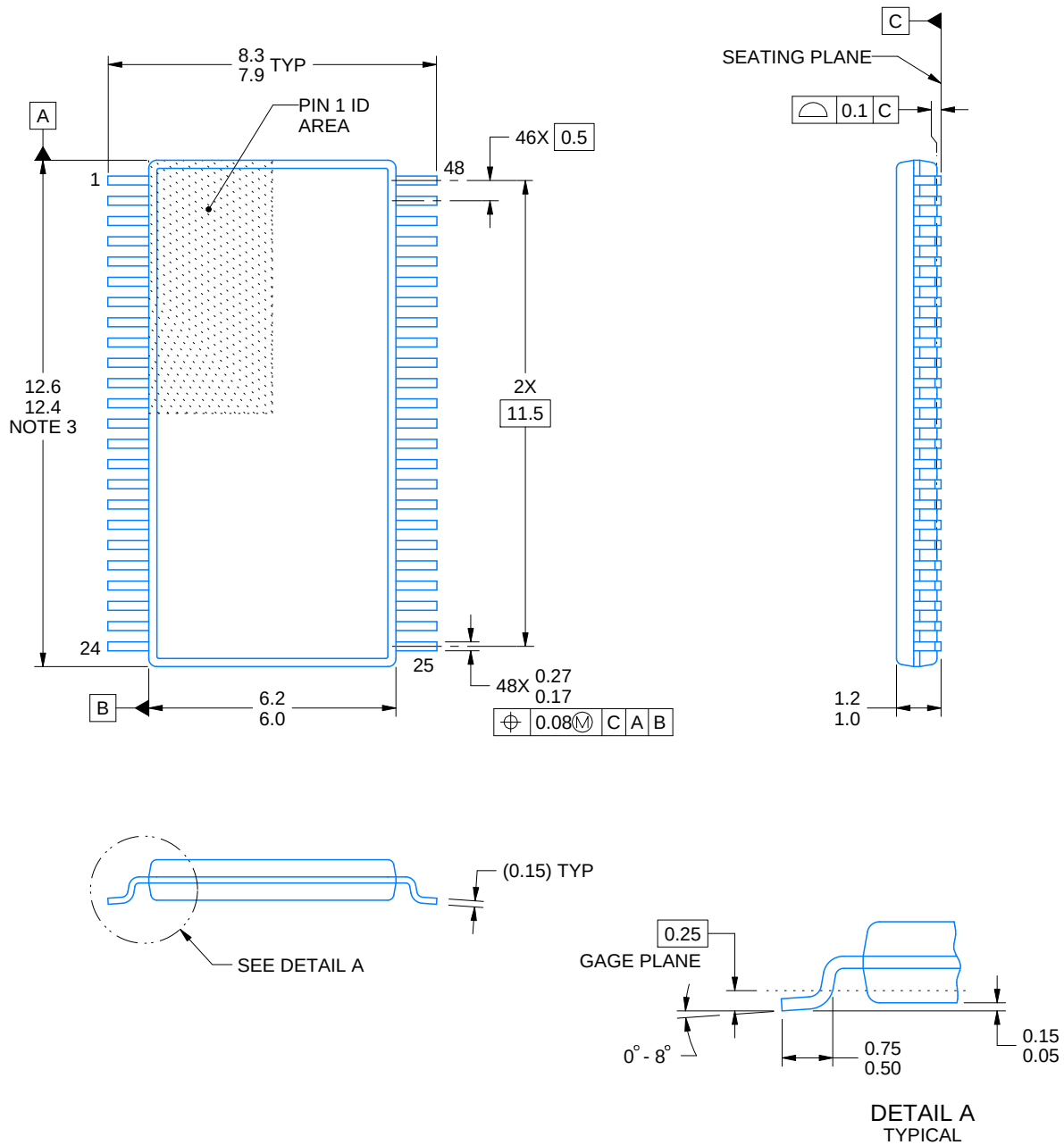
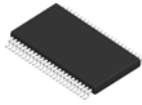
- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only
E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



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NOTES:

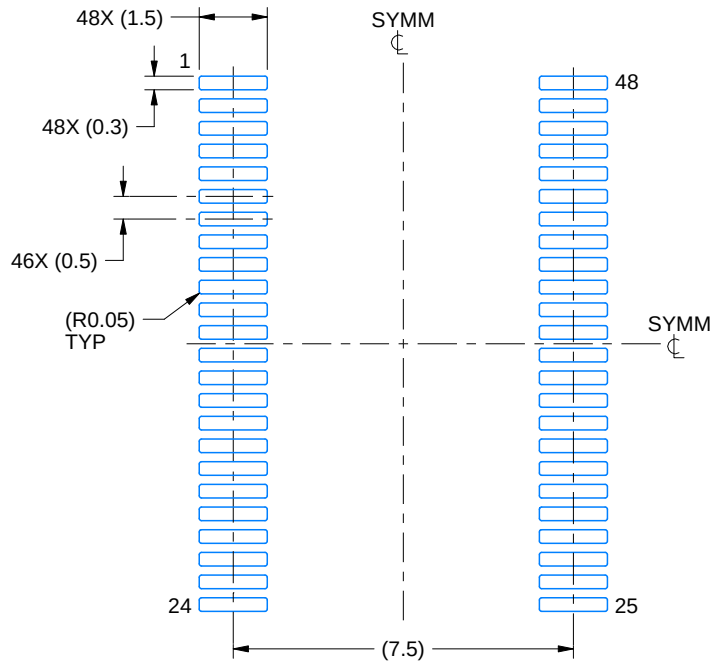
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

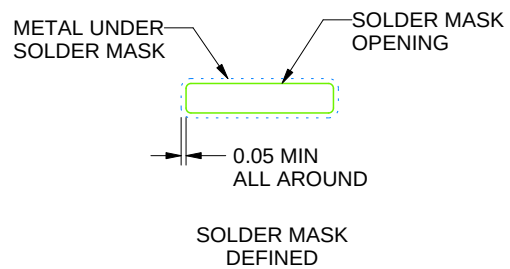
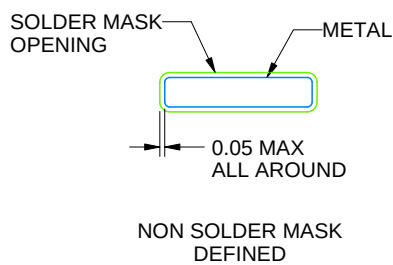
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

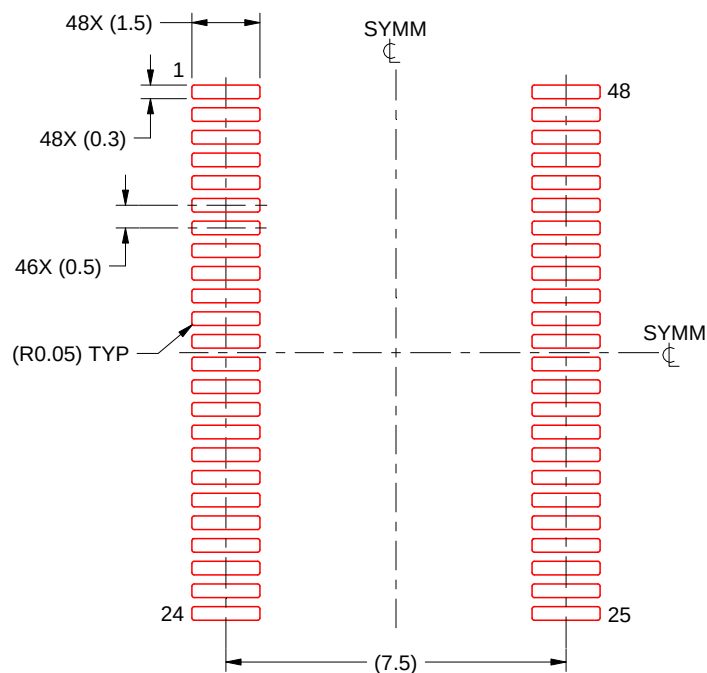
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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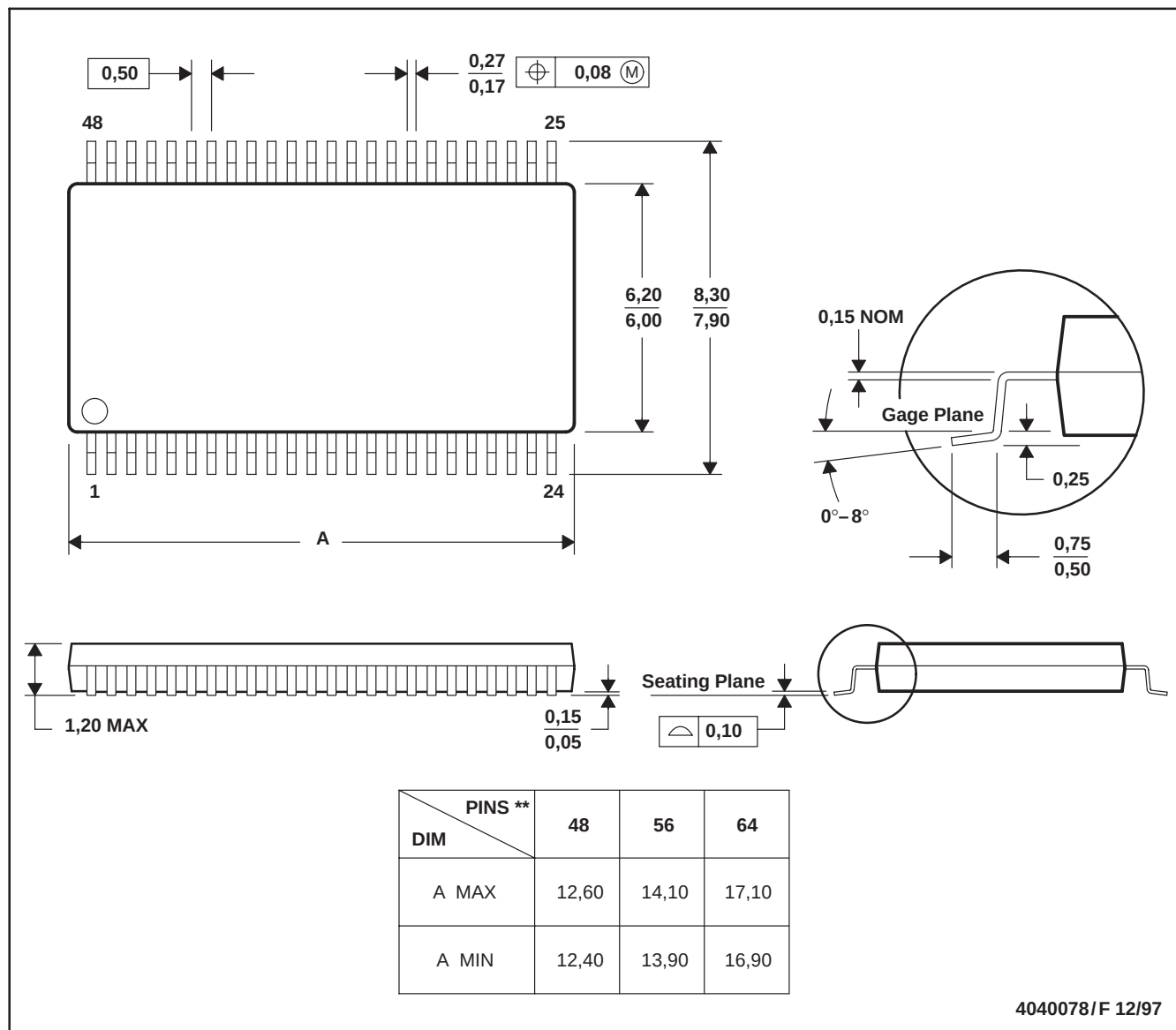
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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