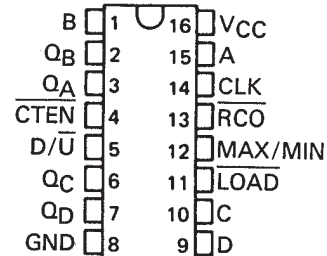


# SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SDLS072 – DECEMBER 1972 – REVISED MARCH 1988

- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presetable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications

SN54190, SN54191, SN54LS190,  
SN54LS191 . . . J PACKAGE  
SN74190, SN74191 . . . N PACKAGE  
SN74LS190, SN74LS191 . . . D OR N PACKAGE  
(TOP VIEW)



| TYPE           | AVERAGE<br>PROPAGATION<br>DELAY | TYPICAL<br>MAXIMUM<br>CLOCK<br>FREQUENCY | TYPICAL<br>POWER<br>DISSIPATION |
|----------------|---------------------------------|------------------------------------------|---------------------------------|
| '190, '191     | 20ns                            | 25MHz                                    | 325mW                           |
| 'LS190, 'LS191 | 20ns                            | 25MHz                                    | 100mW                           |

## description

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter count up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

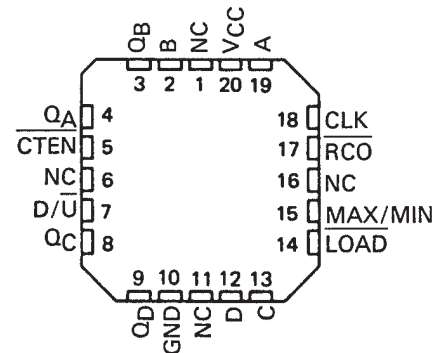
These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Series 54' and 54LS' are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; Series 74' and 74LS' are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54LS190, SN54LS191 . . . FK PACKAGE  
(TOP VIEW)

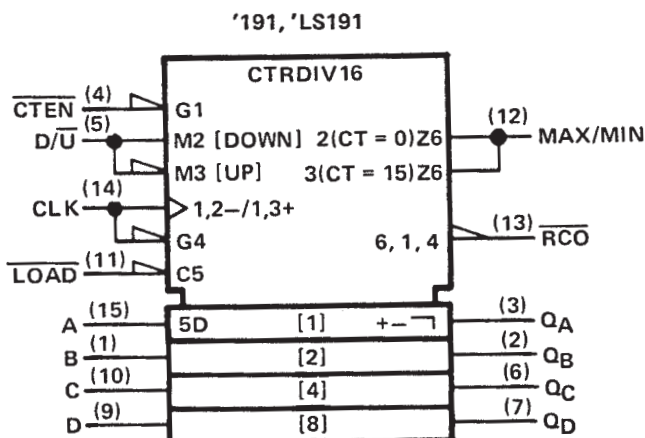
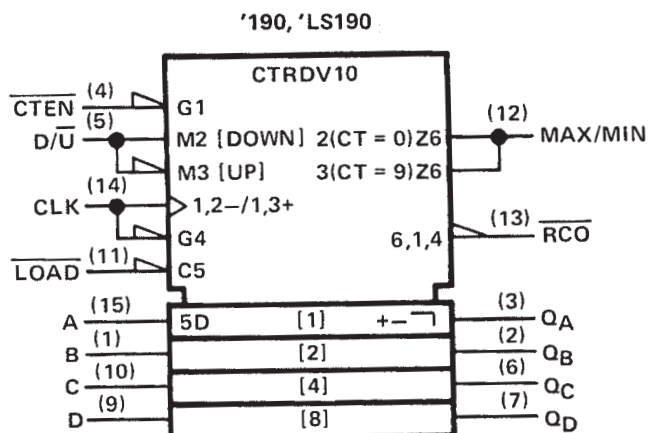


NC - No internal connection

SN54190, SN54191, SN54LS190, SN54LS191,  
 SN74190, SN74191, SN74LS190, SN74LS191  
 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

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logic symbols†



† These symbols are accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for D, J, and N packages.

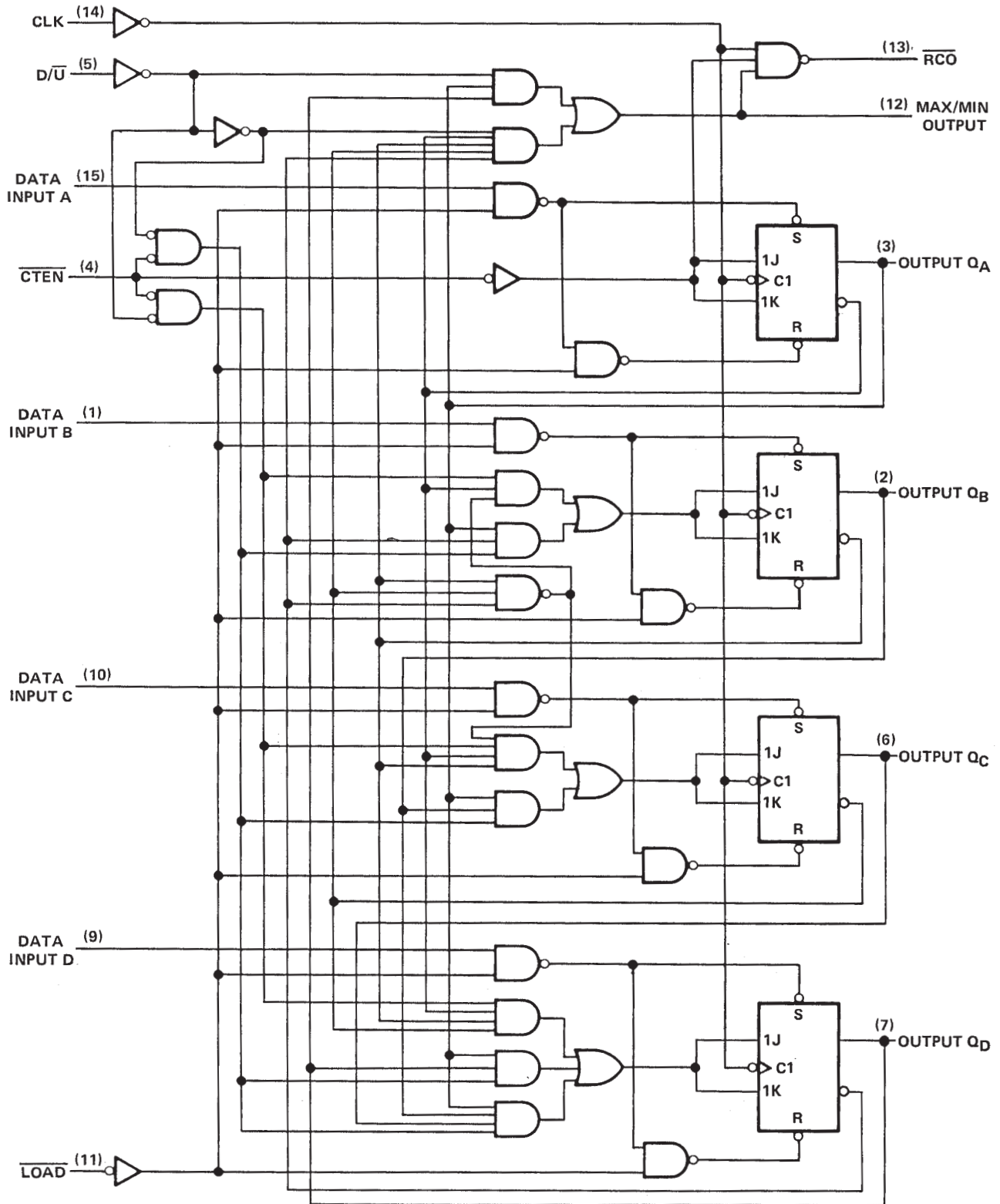
# SN54190, SN54LS190, SN74190, SN74LS190

## SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

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logic diagram (positive logic)

'190, 'LS190 DECADE COUNTERS



Pin numbers shown are for D, J, and N packages.



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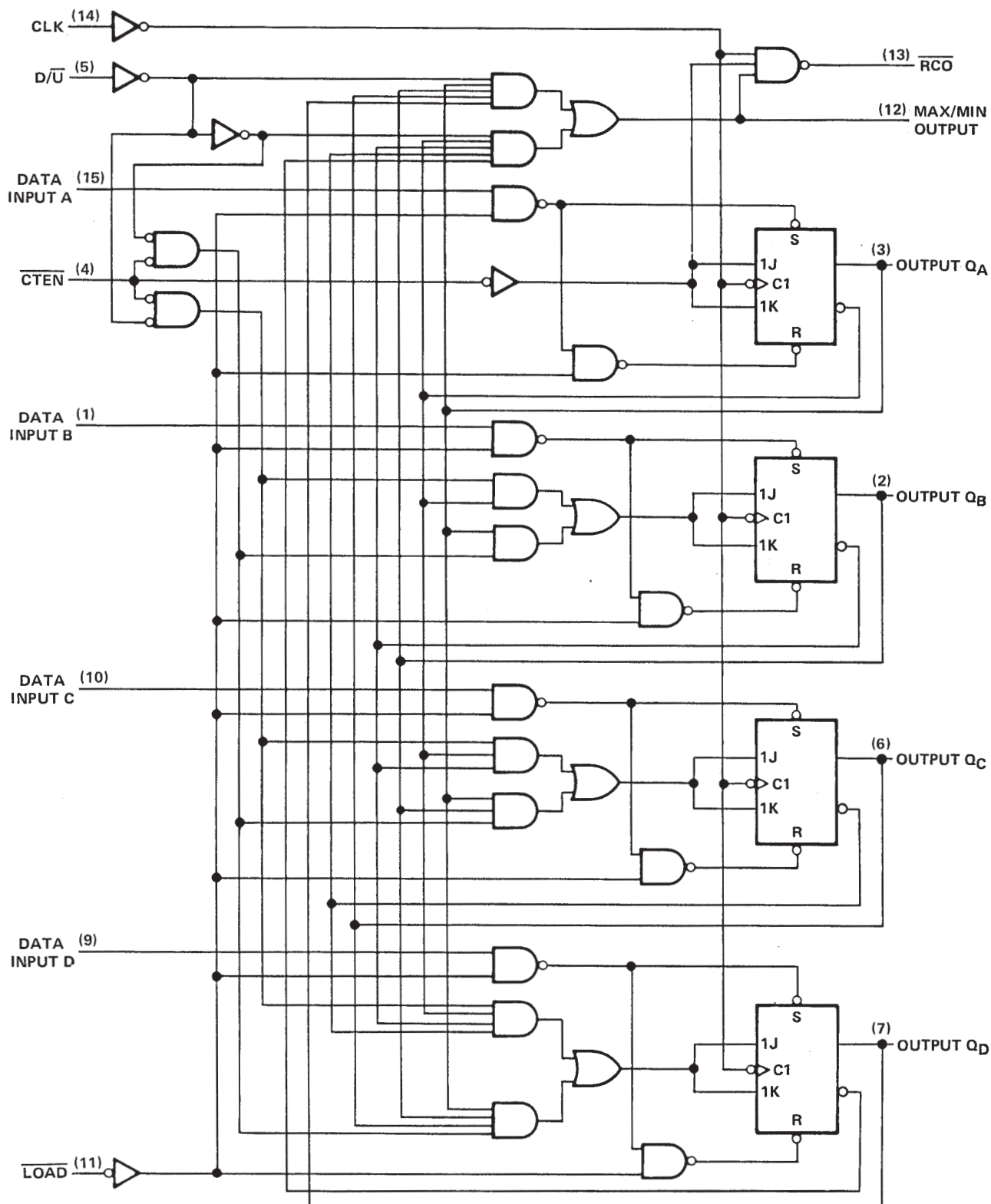
# SN54191, SN54LS191, SN74191, SN74LS191

## SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

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### logic diagram (positive logic)

'191, 'LS191 BINARY COUNTERS



Pin numbers shown are for D, J, and N packages.



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# SN54190, SN54LS190, SN74190, SN74LS190 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

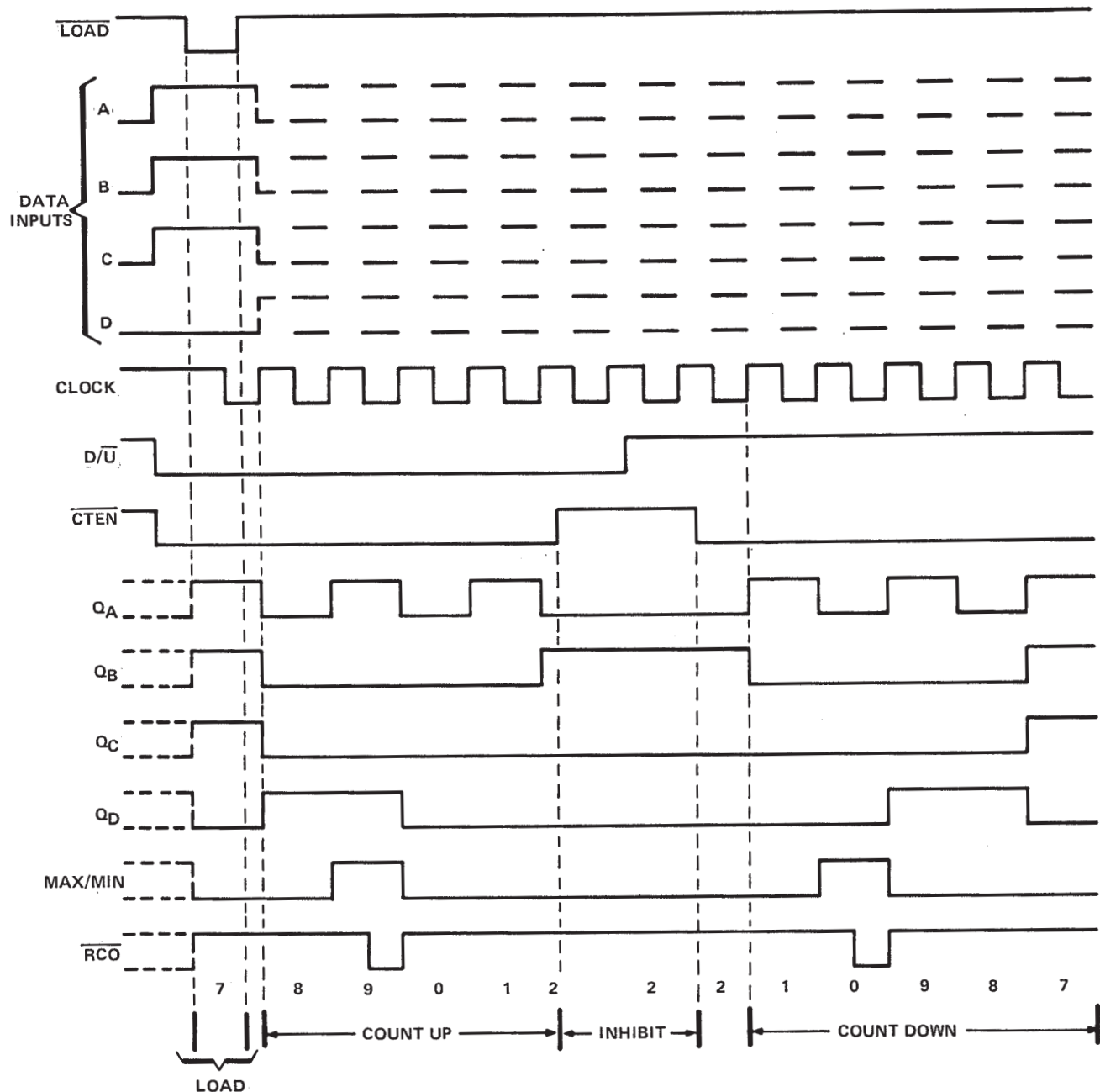
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## '190, 'LS190 DECADE COUNTERS

### typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



# SN54191, SN54LS191, SN74191, SN74LS191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

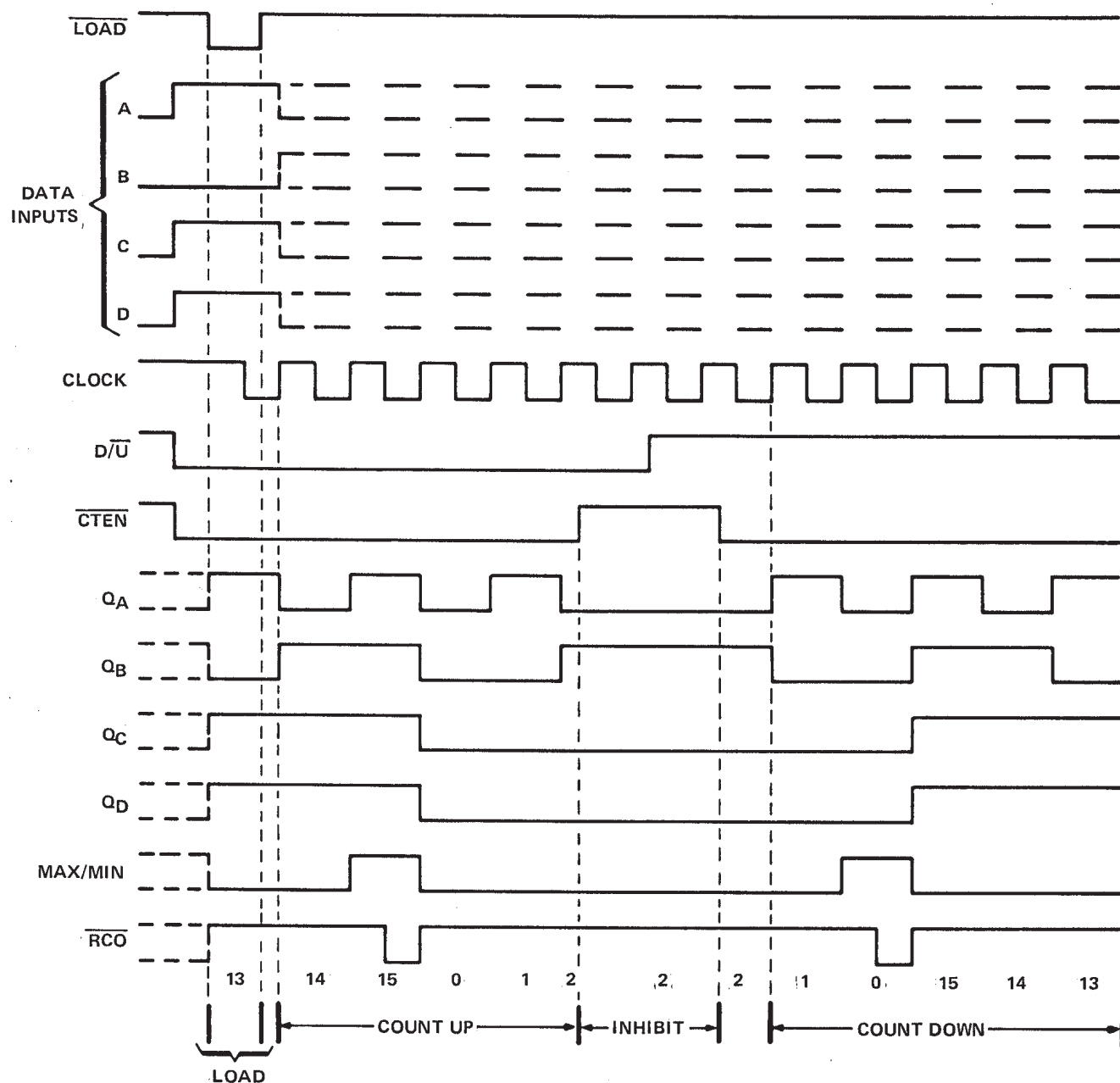
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## '191, 'LS191 BINARY COUNTERS

### typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



**SN54190, SN54191, SN54LS190, SN54LS191,  
SN74190, SN74191, SN74LS190, SN74LS191**  
**SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

|                                                               |                |
|---------------------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)                         | 7 V            |
| Input voltage: SN54', SN74' Circuits                          | 5.5 V          |
| SN54LS', SN74LS' Circuits                                     | 7 V            |
| Operating free-air temperature range: SN54', SN54LS' Circuits | –55°C to 125°C |
| SN74', SN74LS' Circuits                                       | 0°C to 70°C    |
| Storage temperature range                                     | –65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

**recommended operating conditions**

|                       |                                |                                        | SN54190, SN54191 |     |     | SN74190, SN74191 |     |      | UNIT |
|-----------------------|--------------------------------|----------------------------------------|------------------|-----|-----|------------------|-----|------|------|
|                       |                                |                                        | MIN              | NOM | MAX | MIN              | NOM | MAX  |      |
| V <sub>CC</sub>       | Supply voltage                 |                                        | 4.5              | 5   | 5.5 | 4.75             | 5   | 5.25 | V    |
| I <sub>OH</sub>       | High-level output current      |                                        | – 0.8            |     |     | – 0.8            |     |      | mA   |
| I <sub>OL</sub>       | Low-level output current       |                                        | 16               |     |     | 16               |     |      | mA   |
| f <sub>clock</sub>    | Input clock frequency          |                                        | 0                | 20  |     | 0                | 20  |      | MHz  |
| t <sub>w(clock)</sub> | Width of clock input pulse     |                                        | 25               |     |     | 25               |     |      | ns   |
| t <sub>w(load)</sub>  | Width of load input pulse      |                                        | 35               |     |     | 35               |     |      | ns   |
| t <sub>su</sub>       | Setup time                     | Data, high or low (See Figure 1 and 2) | 20               |     |     | 20               |     |      | ns   |
|                       |                                | Load inactive state                    | 20               |     |     | 20               |     |      |      |
| t <sub>hold</sub>     | Data hold time                 |                                        | 0                |     |     | 0                |     |      | ns   |
| T <sub>A</sub>        | Operating free-air temperature |                                        | – 55      125    |     |     | 0      70        |     |      | °C   |

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER |                                                     | TEST CONDITIONS†                                                                              |  | SN54190, SN54191 |      |      | SN74190, SN74191 |      |      | UNIT |
|-----------|-----------------------------------------------------|-----------------------------------------------------------------------------------------------|--|------------------|------|------|------------------|------|------|------|
|           |                                                     |                                                                                               |  | MIN              | TYP‡ | MAX  | MIN              | TYP‡ | MAX  |      |
| $V_{IH}$  | High-level input voltage                            | $V_{CC} = \text{MIN}$                                                                         |  | 2                |      |      | 2                |      |      | V    |
| $V_{IL}$  | Low-level input voltage                             | $V_{CC} = \text{MIN}$                                                                         |  |                  |      | 0.8  |                  |      | 0.8  | V    |
| $V_{IK}$  | Input clamp voltage                                 | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$                                                   |  |                  |      | –1.5 |                  |      | –1.5 | V    |
| $V_{OH}$  | High-level output voltage                           | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.8 \text{ mA}$ |  | 2.4              | 3.4  |      | 2.4              | 3.4  |      | V    |
| $V_{OL}$  | Low-level output voltage                            | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$   |  |                  | 0.2  | 0.4  |                  | 0.2  | 0.4  | V    |
| $I_I$     | High-level input current at maximum input voltage   | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$                                                    |  |                  |      | 1    |                  |      | 1    | mA   |
| $I_{IH}$  | High-level input current at any input except enable | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$                                                    |  |                  |      | 40   |                  |      | 40   | µA   |
| $I_{IH}$  | High-level input current at enable input            |                                                                                               |  |                  |      | 120  |                  |      | 120  | µA   |
| $I_{IL}$  | Low-level input current at any input except enable  | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$                                                    |  |                  |      | –1.6 |                  |      | –1.6 | mA   |
| $I_{IL}$  | Low-level input current at enable input             |                                                                                               |  |                  |      | –4.8 |                  |      | –4.8 | mA   |
| $I_{OS}$  | Short-circuit output current§                       | $V_{CC} = \text{MAX}$                                                                         |  | –20              |      | –65  | –18              |      | –65  | mA   |
| $I_{CC}$  | Supply current                                      | $V_{CC} = \text{MAX}, \text{ See Note 2}$                                                     |  |                  | 65   | 99   |                  | 65   | 105  | mA   |

† For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

NOTE 2:  $I_{CC}$  is measured with all inputs grounded and all outputs open.



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# SN54190, SN54191, SN74190, SN74191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

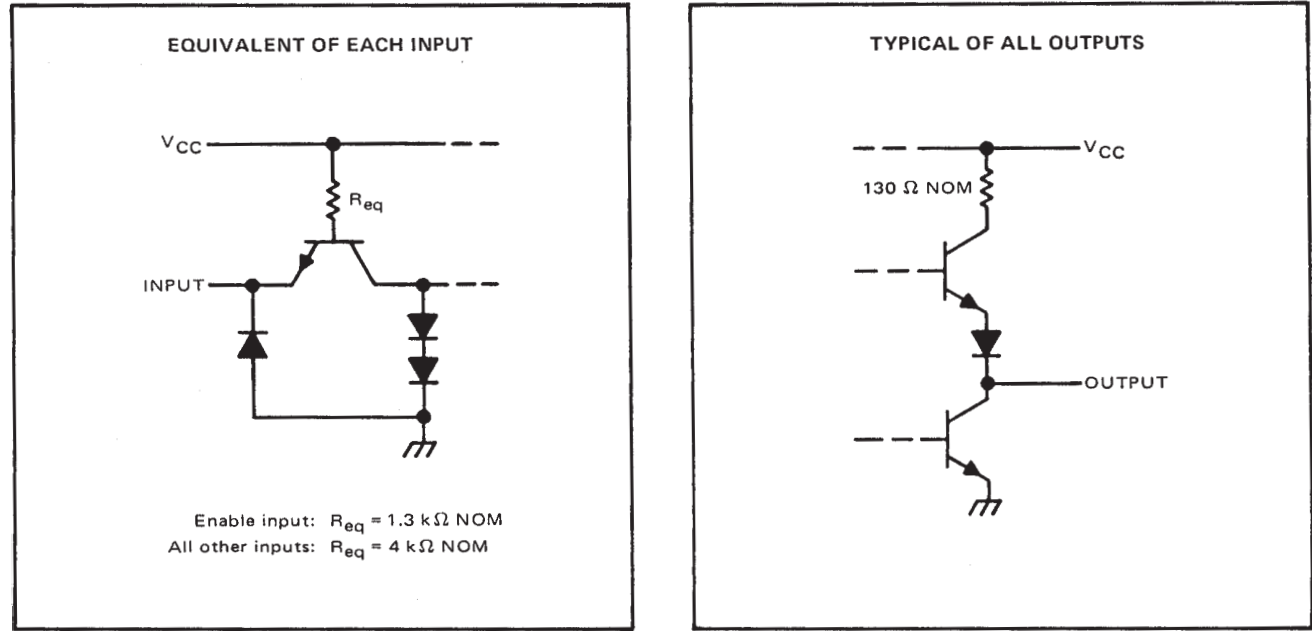
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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$

| PARAMETER†       | FROM<br>(INPUT)          | TO<br>(OUTPUT)                                                    | TEST CONDITIONS                                                               | '190, '191 |     |     | UNIT |
|------------------|--------------------------|-------------------------------------------------------------------|-------------------------------------------------------------------------------|------------|-----|-----|------|
|                  |                          |                                                                   |                                                                               | MIN        | TYP | MAX |      |
| f <sub>max</sub> |                          |                                                                   | C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω,<br>See Figures 1 and 3 thru 7 | 20         | 25  |     | MHz  |
| t <sub>PLH</sub> | $\overline{\text{Load}}$ | Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub> |                                                                               |            | 22  | 33  | ns   |
| t <sub>PHL</sub> |                          |                                                                   |                                                                               |            | 33  | 50  |      |
| t <sub>PLH</sub> | Data A, B, C, D          | Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub> |                                                                               |            | 14  | 22  | ns   |
| t <sub>PHL</sub> |                          |                                                                   |                                                                               |            | 35  | 50  |      |
| t <sub>PLH</sub> | CLK                      | $\overline{\text{RCO}}$                                           |                                                                               |            | 13  | 20  | ns   |
| t <sub>PHL</sub> |                          |                                                                   |                                                                               |            | 16  | 24  |      |
| t <sub>PLH</sub> | CLK                      | Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub> |                                                                               |            | 16  | 24  | ns   |
| t <sub>PHL</sub> |                          |                                                                   |                                                                               |            | 24  | 36  |      |
| t <sub>PLH</sub> | CLK                      | Max/Min                                                           |                                                                               |            | 28  | 42  | ns   |
| t <sub>PHL</sub> |                          |                                                                   |                                                                               |            | 37  | 52  |      |
| t <sub>PLH</sub> | D/ $\overline{\text{U}}$ | $\overline{\text{RCO}}$                                           |                                                                               |            | 30  | 45  | ns   |
| t <sub>PHL</sub> |                          |                                                                   |                                                                               |            | 30  | 45  |      |
| t <sub>PLH</sub> | D/ $\overline{\text{U}}$ | Max/Min                                                           |                                                                               |            | 21  | 33  | ns   |
| t <sub>PHL</sub> |                          |                                                                   |                                                                               |            | 22  | 33  |      |

†  $f_{\text{max}}$  = maximum clock frequency  
 $t_{\text{PLH}}$  = propagation delay time, low-to-high-level output  
 $t_{\text{PHL}}$  = propagation delay time, high-to-low-level output

## schematics of inputs and outputs



# SN54LS190, SN54LS191, SN74LS190, SN74LS191

## SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

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### recommended operating conditions

|                       |                                       | SN54LS190<br>SN54LS191 |     |       | SN74LS190<br>SN74LS191 |     |       | UNIT |
|-----------------------|---------------------------------------|------------------------|-----|-------|------------------------|-----|-------|------|
|                       |                                       | MIN                    | NOM | MAX   | MIN                    | NOM | MAX   |      |
| V <sub>CC</sub>       | Supply voltage                        | 4.5                    | 5   | 5.5   | 4.75                   | 5   | 5.25  | V    |
| I <sub>OH</sub>       | High-level output current             |                        |     | – 0.4 |                        |     | – 0.4 | mA   |
| I <sub>OL</sub>       | Low-level output current              |                        |     | 4     |                        |     | 8     | mA   |
| f <sub>clock</sub>    | Clock frequency                       | 0                      |     | 20    | 0                      |     | 20    | MHz  |
| t <sub>w(clock)</sub> | Width of clock input pulse            | 25                     |     |       | 25                     |     |       | ns   |
| t <sub>w(load)</sub>  | Width of load input pulse             | 35                     |     |       | 35                     |     |       | ns   |
| t <sub>su</sub>       | Data setup time (See Figures 1 and 2) | 20                     |     |       | 20                     |     |       | ns   |
| t <sub>su</sub>       | Load inactive state setup time        | 30                     |     |       | 30                     |     |       | ns   |
| t <sub>h</sub>        | Data hold time                        | 5                      |     |       | 5                      |     |       | ns   |
| t <sub>h</sub>        | Enable hold time                      | 0                      |     |       | 0                      |     |       | ns   |
| t <sub>enable</sub>   | Count enable time (see Note 3)        | 40                     |     |       | 40                     |     |       | ns   |
| T <sub>A</sub>        | Operating free-air temperature        | – 55                   |     | 125   | 0                      |     | 70    | °C   |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       |                                                   | TEST CONDITIONS†                                                                                                  |                        | SN54LS190<br>SN54LS191 |      |      | SN74LS190<br>SN74LS191 |      |      | UNIT |
|-----------------|---------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|------------------------|------------------------|------|------|------------------------|------|------|------|
|                 |                                                   |                                                                                                                   |                        | MIN                    | TYP‡ | MAX  | MIN                    | TYP‡ | MAX  |      |
| V <sub>IH</sub> | High-level input voltage                          |                                                                                                                   |                        | 2                      |      |      | 2                      |      |      | V    |
| V <sub>IL</sub> | Low-level input voltage                           |                                                                                                                   |                        |                        |      | 0.7  |                        |      | 0.8  | V    |
| V <sub>IK</sub> | Input clamp voltage                               | V <sub>CC</sub> = MIN, I <sub>I</sub> = –18 mA                                                                    |                        |                        |      | –1.5 |                        |      | –1.5 | V    |
| V <sub>OH</sub> | High-level output voltage                         | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = –400 µA |                        | 2.5                    | 3.4  |      | 2.7                    | 3.4  |      | V    |
| V <sub>OL</sub> | Low-level output voltage                          | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>IL</sub> max                            | I <sub>OL</sub> = 4 mA |                        | 0.25 | 0.4  |                        | 0.25 | 0.4  | V    |
|                 |                                                   |                                                                                                                   | I <sub>OL</sub> = 8 mA |                        |      |      |                        | 0.35 | 0.5  |      |
| I <sub>I</sub>  | High-level input current at maximum input voltage | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V                                                                       | Enable                 |                        |      | 0.3  |                        |      | 0.3  | mA   |
|                 |                                                   |                                                                                                                   | Others                 |                        |      | 0.1  |                        |      | 0.1  |      |
| I <sub>IH</sub> | High-level input current                          | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V                                                                     | Enable                 |                        |      | 60   |                        |      | 60   | µA   |
|                 |                                                   |                                                                                                                   | Others                 |                        |      | 20   |                        |      | 20   |      |
| I <sub>IL</sub> | Low-level input current                           | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V                                                                     | Enable                 |                        |      | –1.2 |                        |      | –1.2 | mA   |
|                 |                                                   |                                                                                                                   | Others                 |                        |      | –0.4 |                        |      | –0.4 |      |
| I <sub>OS</sub> | Short-circuit output current§                     | V <sub>CC</sub> = MAX,                                                                                            |                        | –20                    |      | –100 | –20                    |      | –100 | mA   |
| I <sub>CC</sub> | Supply current                                    | V <sub>CC</sub> = MAX, See Note 2                                                                                 |                        | 20                     |      | 35   | 20                     |      | 35   | mA   |

† For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 2. I<sub>CC</sub> is measured with all inputs grounded and all outputs open.

3. Minimum count enable time is the interval immediately preceeding the rising edge of the clock pulse during which interval the count enable input must be low to ensure counting.

SN54LS190, SN54LS191, SN74LS190, SN74LS191  
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

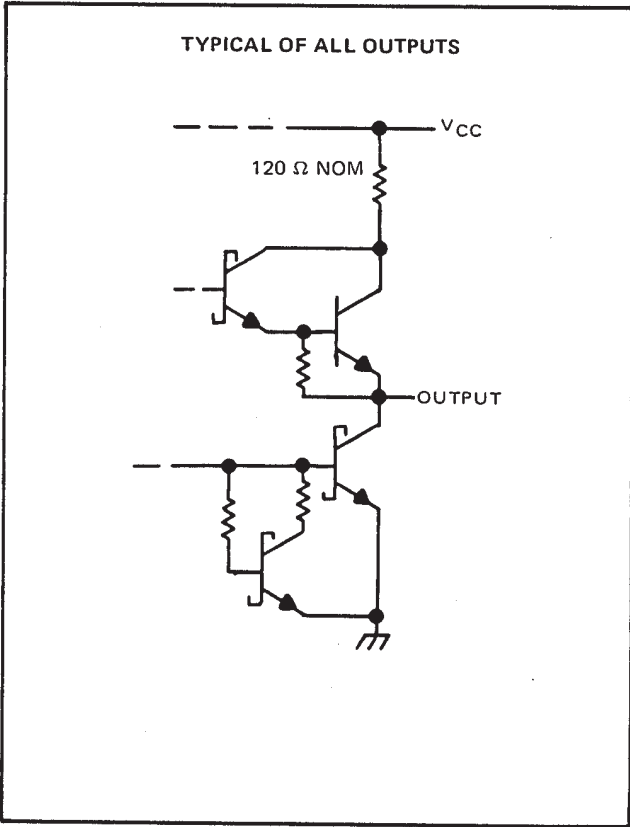
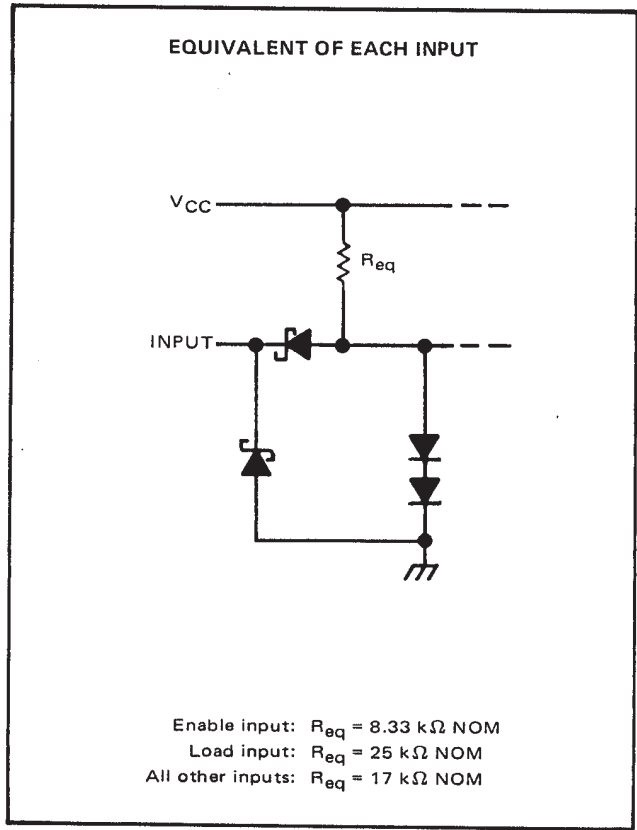
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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER†       | FROM<br>(INPUT)          | TO<br>(OUTPUT)          | TEST CONDITIONS                                                              | 'LS190, 'LS191 |     |     | UNIT |
|------------------|--------------------------|-------------------------|------------------------------------------------------------------------------|----------------|-----|-----|------|
|                  |                          |                         |                                                                              | MIN            | TYP | MAX |      |
| $f_{\max}$       |                          |                         | $C_L = 15\text{ pF}, R_L = 2\text{ k}\Omega$ ,<br>See Figures 1 and 3 thru 7 | 20             | 25  |     | MHz  |
| $t_{\text{PLH}}$ | $\overline{\text{Load}}$ | $Q_A, Q_B, Q_C, Q_D$    |                                                                              |                | 22  | 33  | ns   |
| $t_{\text{PHL}}$ |                          |                         |                                                                              |                | 33  | 50  |      |
| $t_{\text{PLH}}$ | Data A, B, C, D          | $Q_A, Q_B, Q_C, Q_D$    |                                                                              |                | 20  | 32  | ns   |
| $t_{\text{PHL}}$ |                          |                         |                                                                              |                | 27  | 40  |      |
| $t_{\text{PLH}}$ | CLK                      | $\overline{\text{RCO}}$ |                                                                              |                | 13  | 20  | ns   |
| $t_{\text{PHL}}$ |                          |                         |                                                                              |                | 16  | 24  |      |
| $t_{\text{PLH}}$ | CLK                      | $Q_A, Q_B, Q_C, Q_D$    |                                                                              |                | 16  | 24  | ns   |
| $t_{\text{PHL}}$ |                          |                         |                                                                              |                | 24  | 36  |      |
| $t_{\text{PLH}}$ | CLK                      | Max/Min                 |                                                                              |                | 28  | 42  | ns   |
| $t_{\text{PHL}}$ |                          |                         |                                                                              |                | 37  | 52  |      |
| $t_{\text{PLH}}$ | $D/\overline{U}$         | $\overline{\text{RCO}}$ |                                                                              |                | 30  | 45  | ns   |
| $t_{\text{PHL}}$ |                          |                         |                                                                              |                | 30  | 45  |      |
| $t_{\text{PLH}}$ | $D/\overline{U}$         | Max/Min                 |                                                                              |                | 21  | 33  | ns   |
| $t_{\text{PHL}}$ |                          |                         |                                                                              |                | 22  | 33  |      |
| $t_{\text{PLH}}$ | $\overline{\text{CTEN}}$ | $\overline{\text{RCO}}$ |                                                                              |                | 21  | 33  | ns   |
| $t_{\text{PHL}}$ |                          |                         |                                                                              |                | 22  | 33  |      |

†  $f_{\max}$  = maximum clock frequency  
   $t_{PLH}$  = propagation delay time, low-to-high-level output  
   $t_{PHL}$  = propagation delay time, high-to-low-level output

schematics of inputs and outputs



SN54190, SN54191, SN54LS190, SN54LS191,  
SN74190, SN74191, SN74LS190, SN74LS191  
**SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL**

SDLS072 – DECEMBER 1972 – REVISED MARCH 1988

**PARAMETER MEASUREMENT INFORMATION**

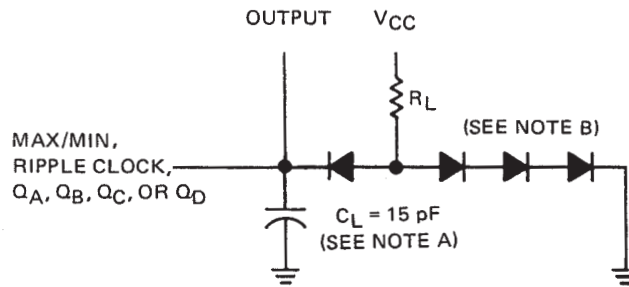


**FIGURE 1—LOAD CIRCUIT  
FOR SWITCHING TIME MEASUREMENT**

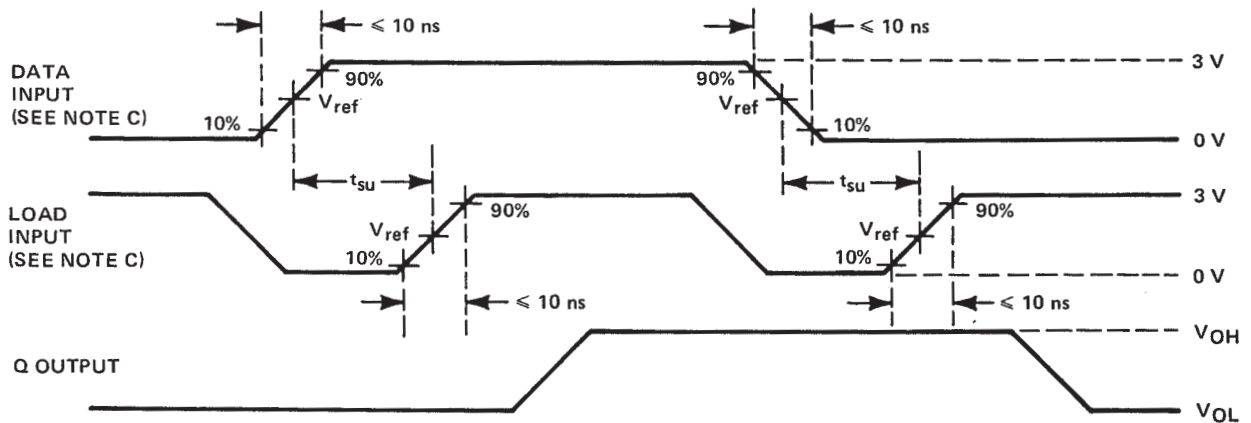
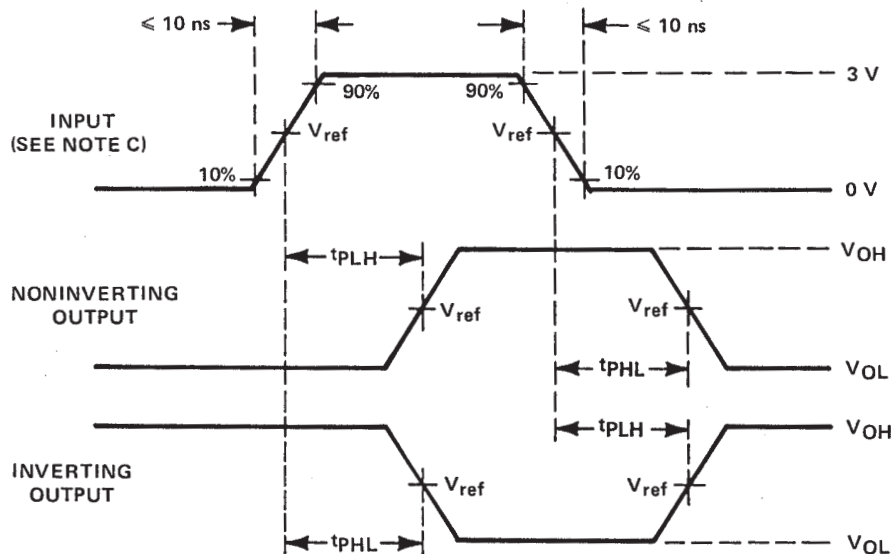


**FIGURE 2—DATA SETUP TIME VOLTAGE WAVEFORMS**



See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

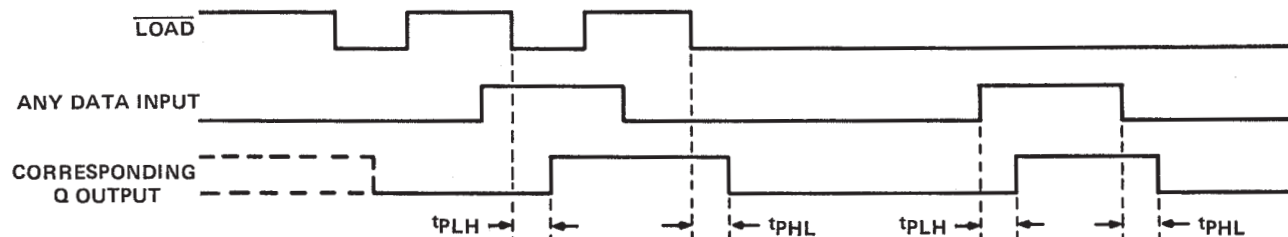
**FIGURE 3—GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All diodes are 1N3064 or equivalent.  
C. The input pulses are supplied by generators having the following characteristics:  $Z_{out} = 50 \Omega$ , duty cycle  $\leq 50\%$ , PRR  $\leq 1$  MHz.  
D.  $V_{ref} = 1.5$  V for '190 and '191; 1.3 V for 'LS190 and 'LS191.

SN54190, SN54191, SN54LS190, SN54LS191,  
 SN74190, SN74191, SN74LS190, SN74LS191  
 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

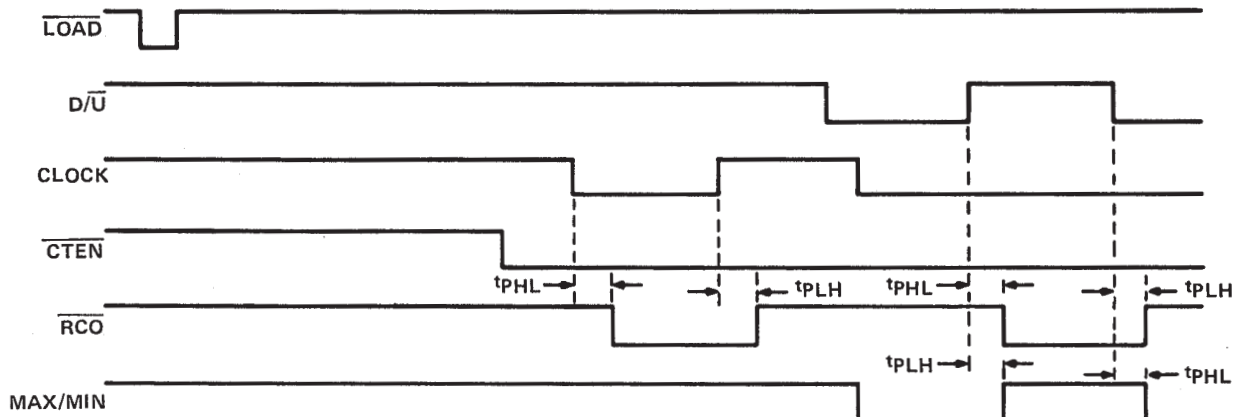
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PARAMETER MEASUREMENT INFORMATION (continued)



NOTE E: Conditions on other inputs are irrelevant.

FIGURE 4—LOAD TO OUTPUT AND DATA TO OUTPUT

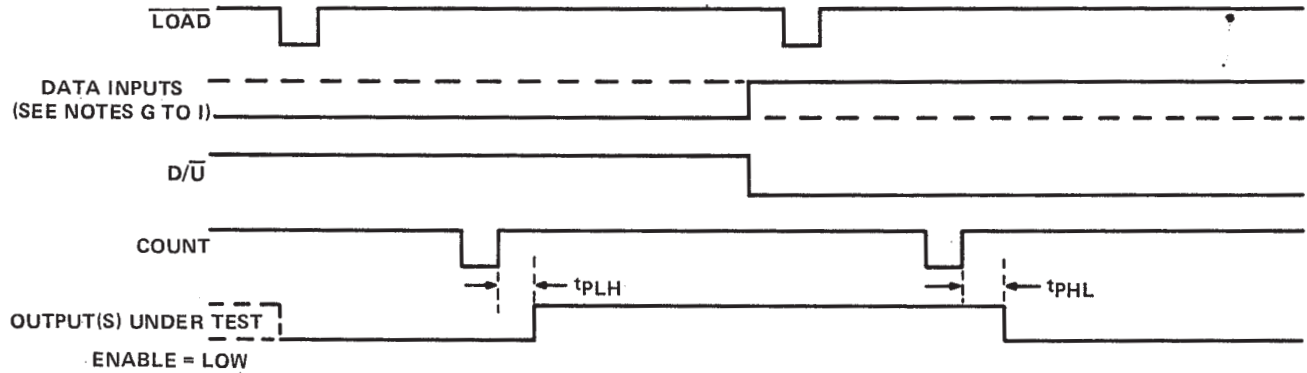


NOTE F: All data inputs are low.

FIGURE 5—ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN

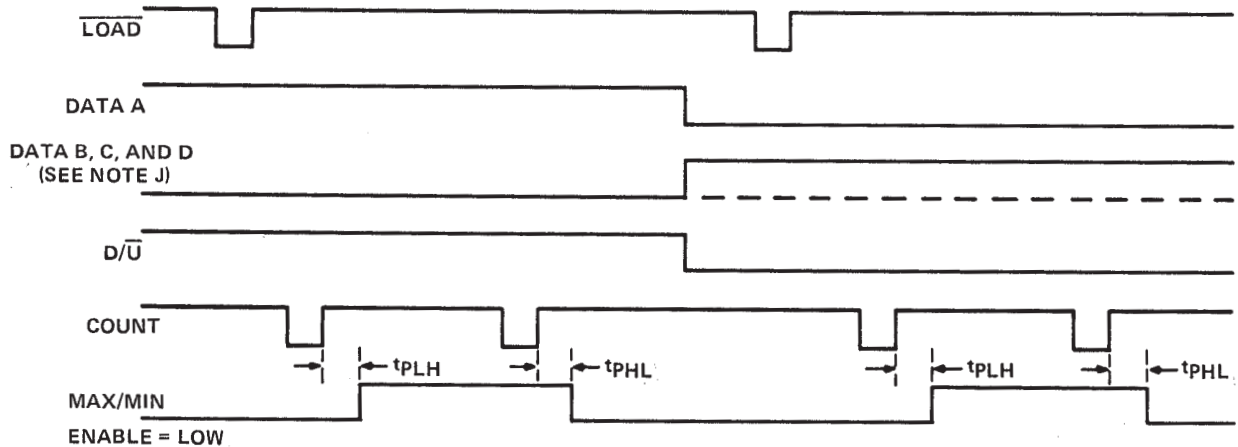
PARAMETER MEASUREMENT INFORMATION (continued)

switching characteristics (continued)



- NOTES: G. To test  $Q_A$ ,  $Q_B$ , and  $Q_C$  outputs of '190 and 'LS190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
- H. To test  $Q_D$  output of '190 and 'LS190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.
- I. To test  $Q_A$ ,  $Q_B$ ,  $Q_C$ , and  $Q_D$  outputs of '191 and 'LS191: All four data inputs are shown by the solid line.

FIGURE 6-CLOCK TO OUTPUT



NOTE J: Data inputs B and C are shown by the dashed line for the '190 and 'LS190 and the solid line for the '191 and 'LS191: Data input D is shown by the solid line for both devices.

FIGURE 7-CLOCK TO MAX/MIN

**PACKAGING INFORMATION**

| Orderable part number            | Status<br>(1)    | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|----------------------------------|------------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| <a href="#">7600901EA</a>        | Active           | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7600901EA<br>SNJ54LS191J      |
| <a href="#">7600901FA</a>        | Active           | Production           | CFP (W)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7600901FA<br>SNJ54LS191W      |
| <a href="#">JM38510/31509BEA</a> | Active           | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>31509BEA          |
| JM38510/31509BEA.A               | Active           | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>31509BEA          |
| <a href="#">JM38510/31509BFA</a> | Active           | Production           | CFP (W)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>31509BFA          |
| JM38510/31509BFA.A               | Active           | Production           | CFP (W)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>31509BFA          |
| <a href="#">M38510/31509BEA</a>  | Active           | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>31509BEA          |
| <a href="#">M38510/31509BFA</a>  | Active           | Production           | CFP (W)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>31509BFA          |
| <a href="#">SN54LS191J</a>       | Active           | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54LS191J                    |
| SN54LS191J.A                     | Active           | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54LS191J                    |
| <a href="#">SN74LS191D</a>       | Obsolete         | Production           | SOIC (D)   16  | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | LS191                         |
| <a href="#">SN74LS191DR</a>      | Active           | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | LS191                         |
| SN74LS191DR.A                    | Active           | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | LS191                         |
| <a href="#">SN74LS191N</a>       | Active           | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74LS191N                    |
| SN74LS191N.A                     | Active           | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | SN74LS191N                    |
| <a href="#">SN74LS191NSR</a>     | Last<br>Time Buy | Production           | SOP (NS)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 74LS191                       |
| SN74LS191NSR.A                   | Last<br>Time Buy | Production           | SOP (NS)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | 0 to 70      | 74LS191                       |
| <a href="#">SNJ54LS191FK</a>     | Active           | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 76009012A<br>SNJ54LS<br>191FK |
| SNJ54LS191FK.A                   | Active           | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 76009012A<br>SNJ54LS<br>191FK |

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)      |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--------------------------|
| <a href="#">SNJ54LS191J</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7600901EA<br>SNJ54LS191J |
| SNJ54LS191J.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7600901EA<br>SNJ54LS191J |
| <a href="#">SNJ54LS191W</a> | Active        | Production           | CFP (W)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7600901FA<br>SNJ54LS191W |
| SNJ54LS191W.A               | Active        | Production           | CFP (W)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 7600901FA<br>SNJ54LS191W |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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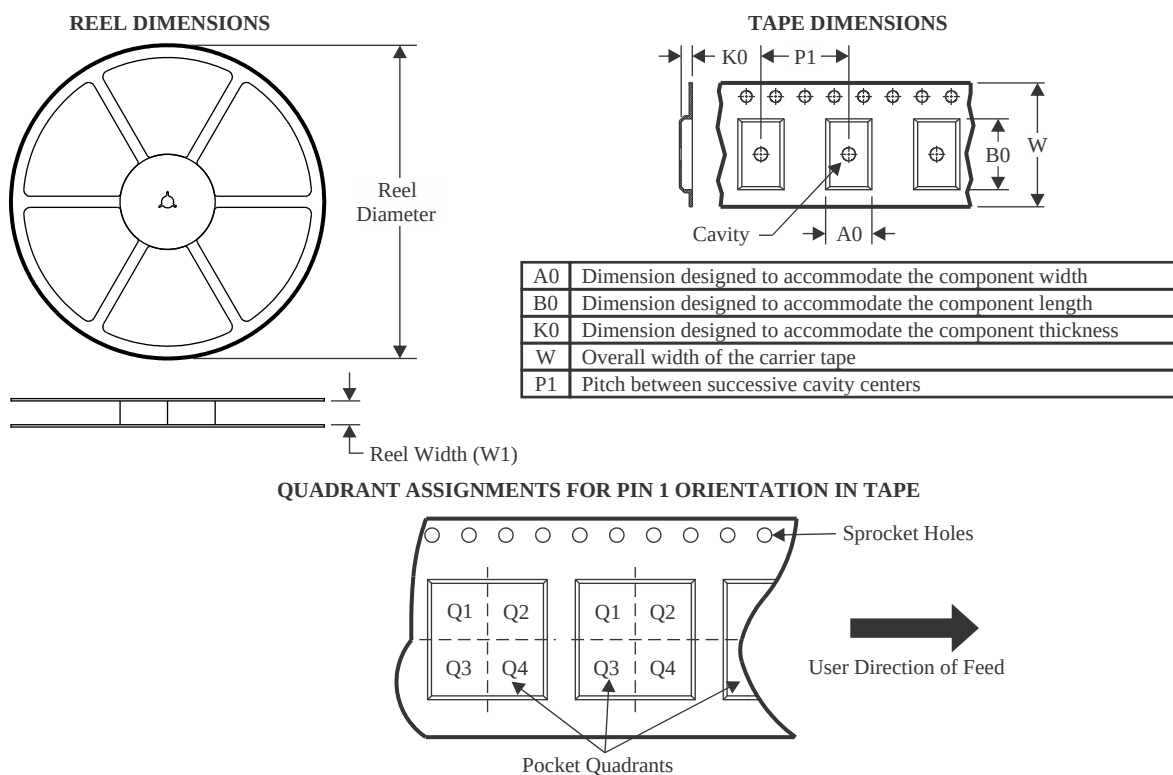
**OTHER QUALIFIED VERSIONS OF SN54LS191, SN74LS191 :**

- Catalog : [SN74LS191](#)
- Military : [SN54LS191](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

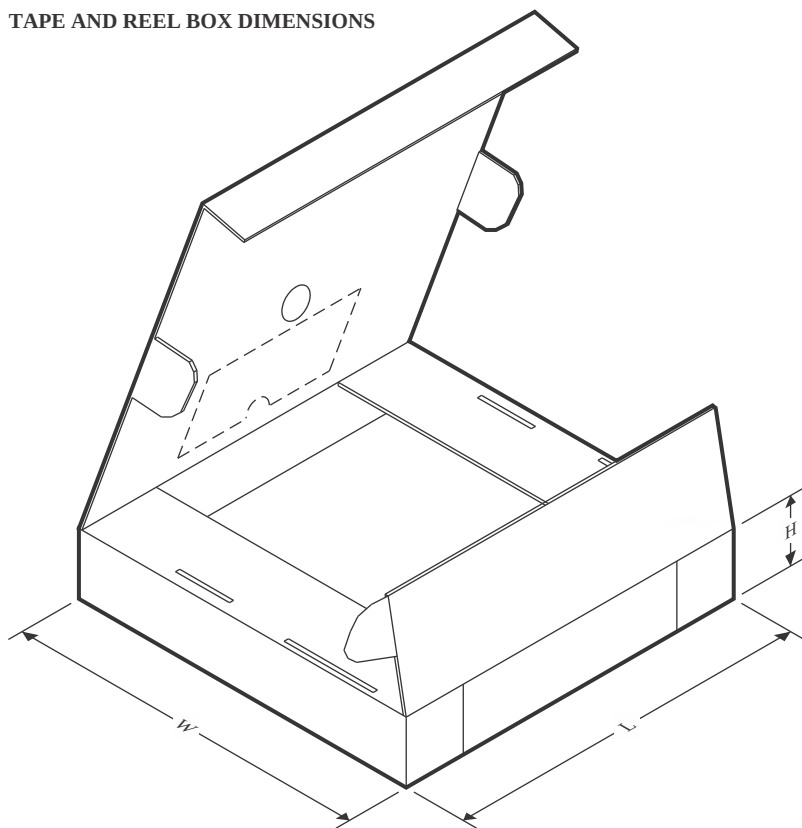
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS191DR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LS191NSR | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |

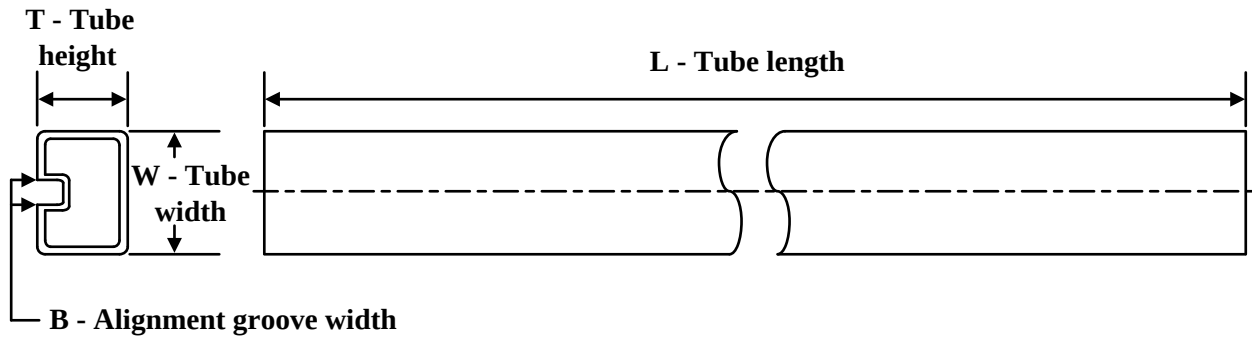
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

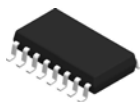
| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS191DR  | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| SN74LS191NSR | SOP          | NS              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

## TUBE



\*All dimensions are nominal

| Device             | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 7600901FA          | W            | CFP          | 16   | 25  | 506.98 | 26.16  | 6220   | NA     |
| JM38510/31509BFA   | W            | CFP          | 16   | 25  | 506.98 | 26.16  | 6220   | NA     |
| JM38510/31509BFA.A | W            | CFP          | 16   | 25  | 506.98 | 26.16  | 6220   | NA     |
| M38510/31509BFA    | W            | CFP          | 16   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74LS191N         | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74LS191N         | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74LS191N.A       | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74LS191N.A       | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54LS191FK       | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54LS191FK.A     | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54LS191W        | W            | CFP          | 16   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SNJ54LS191W.A      | W            | CFP          | 16   | 25  | 506.98 | 26.16  | 6220   | NA     |

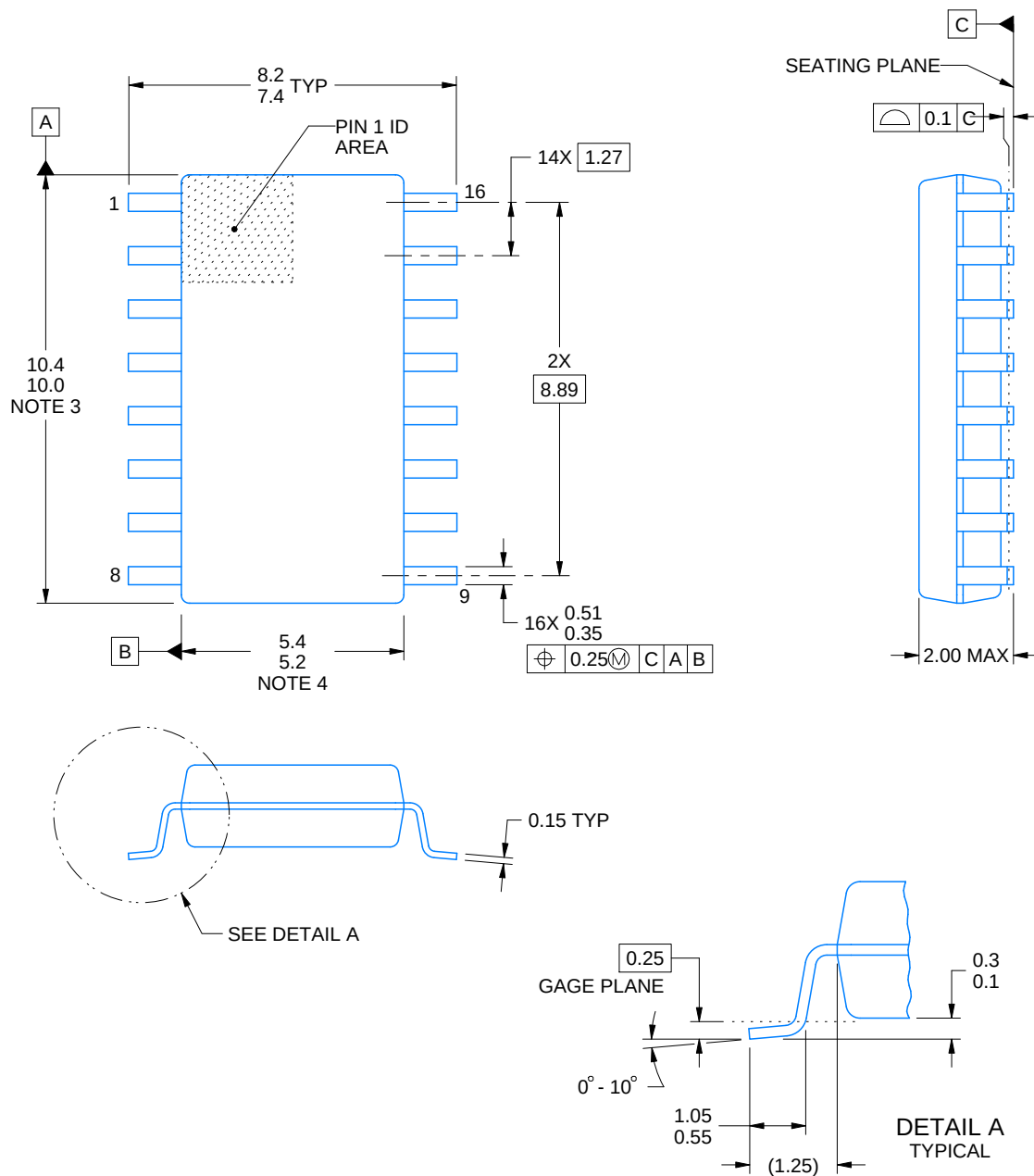


# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP

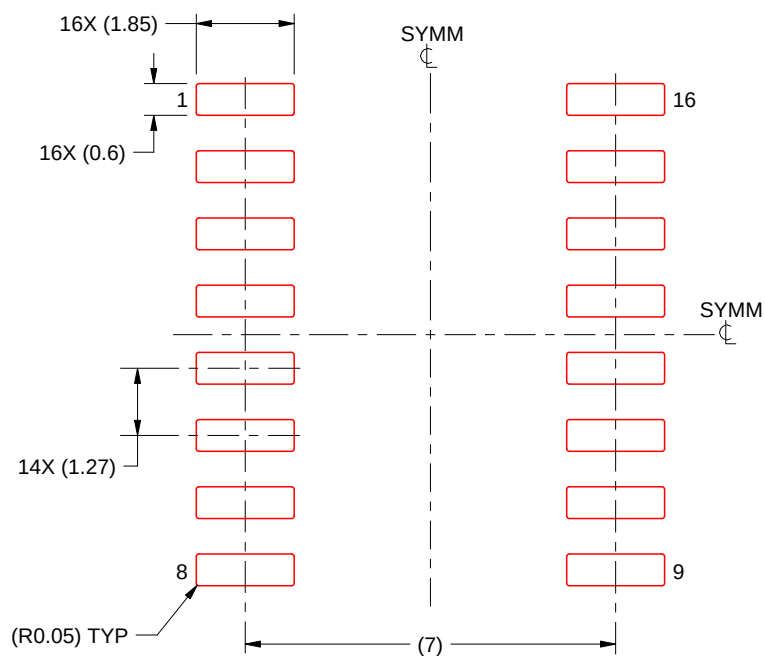


4220735/A 12/2021

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.





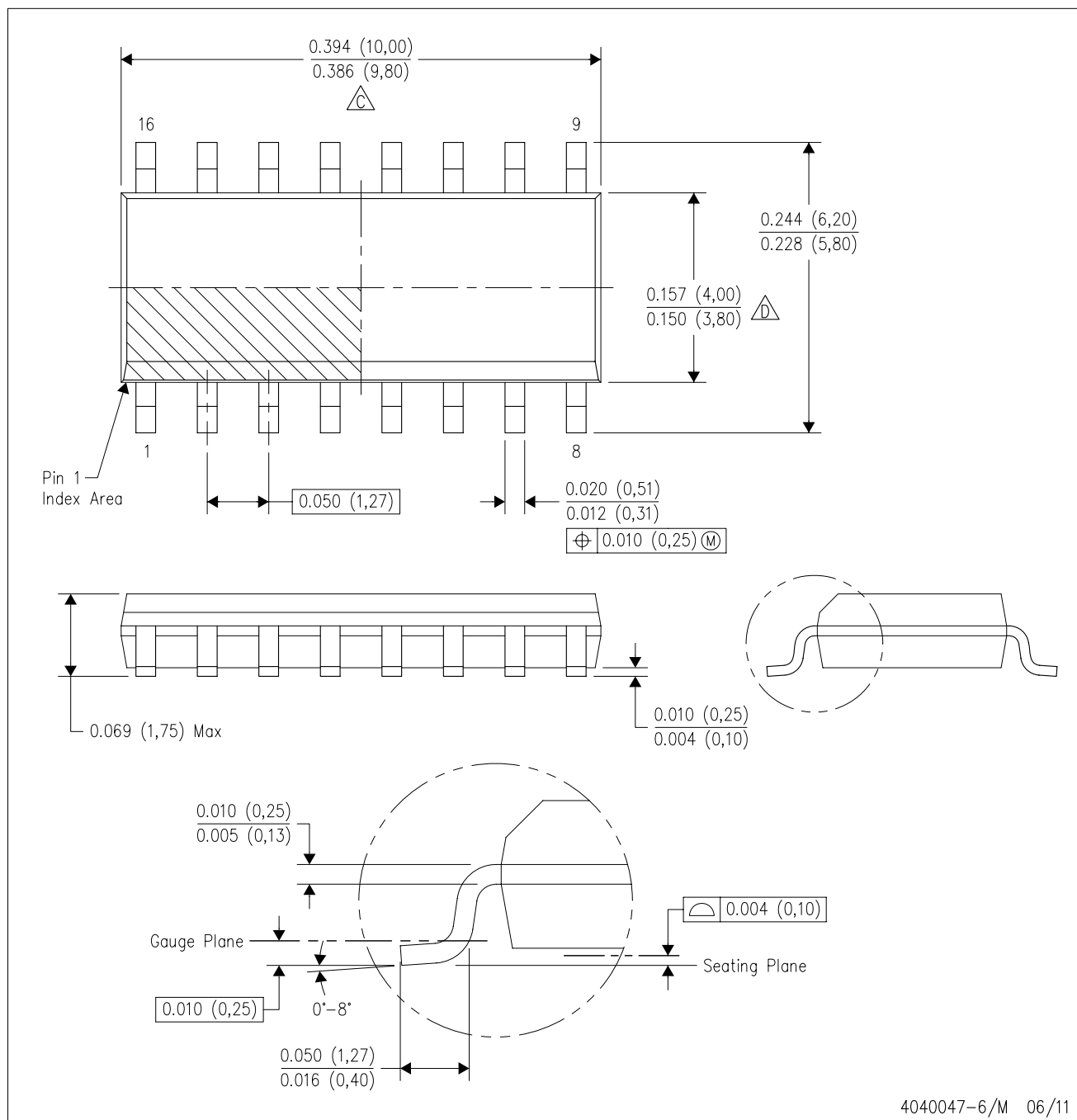
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

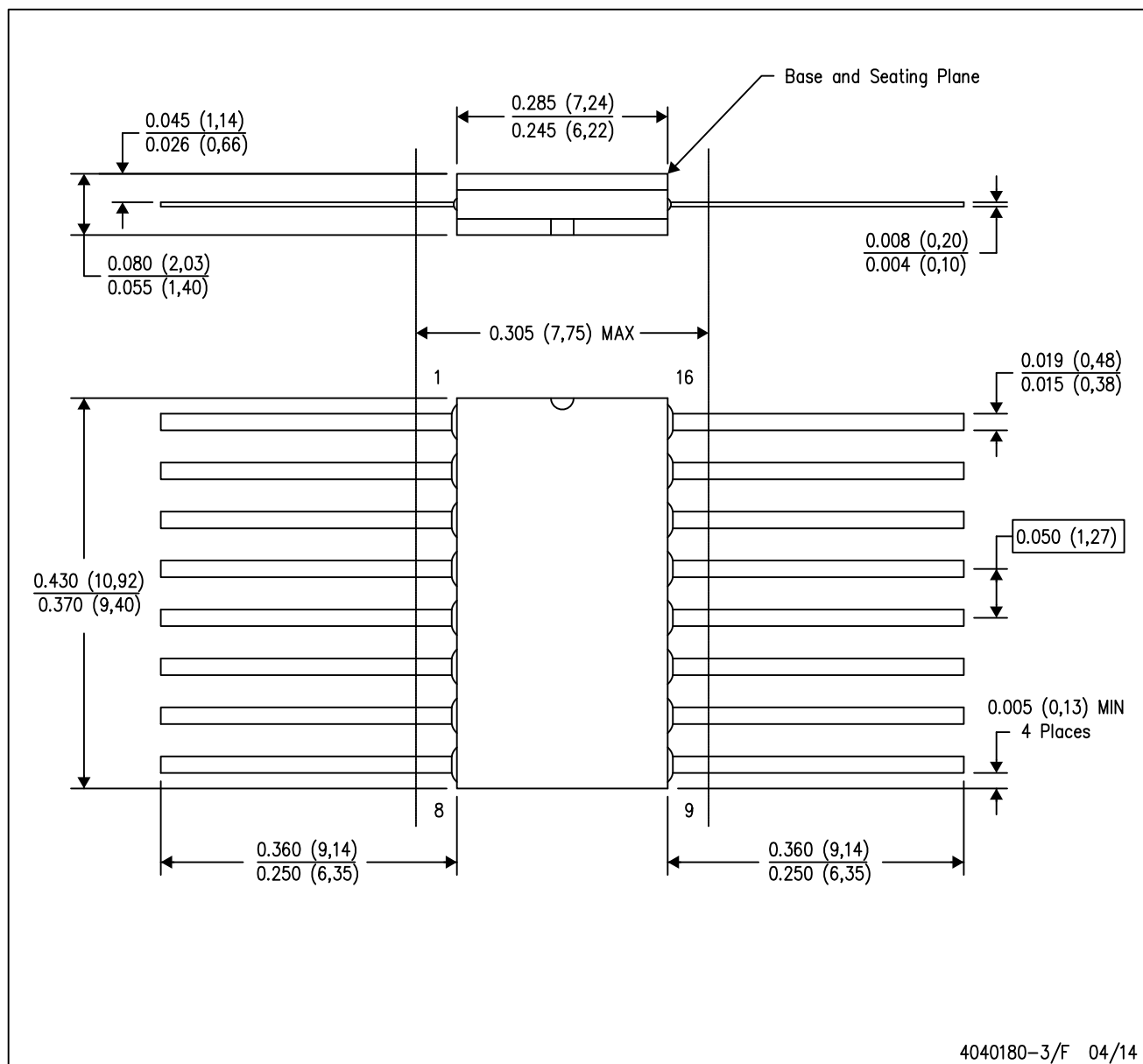


4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

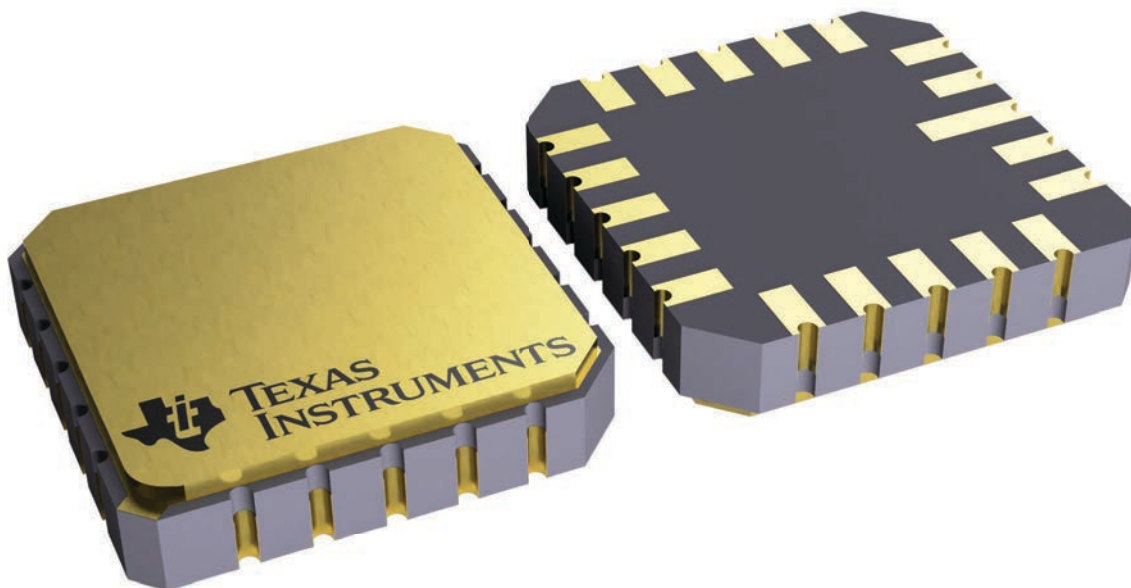
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

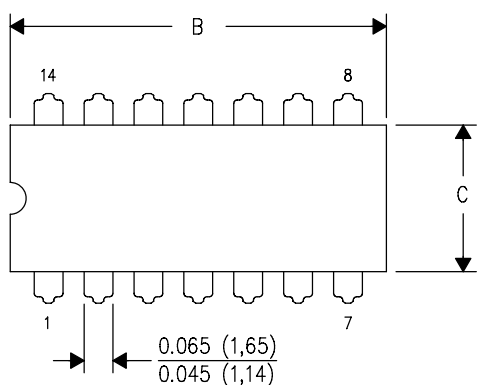


4229370VA\

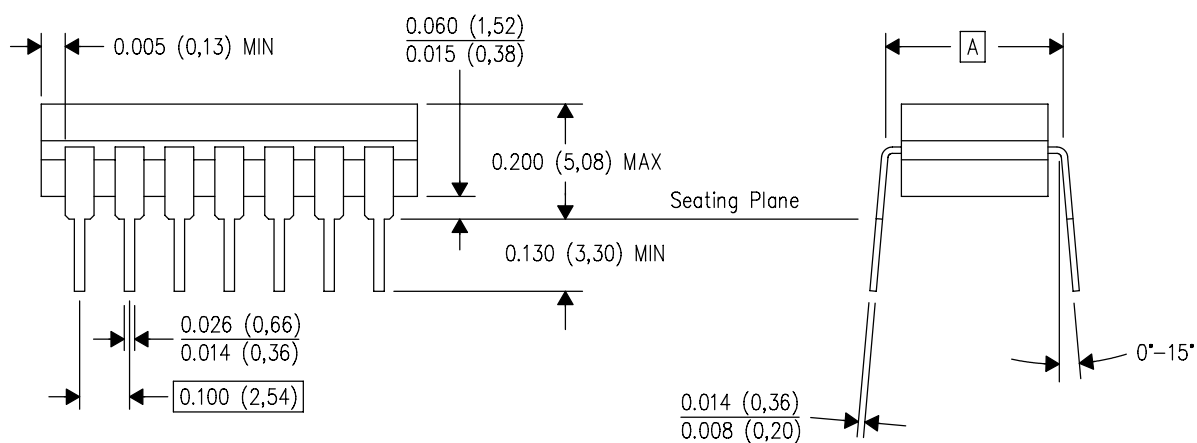
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



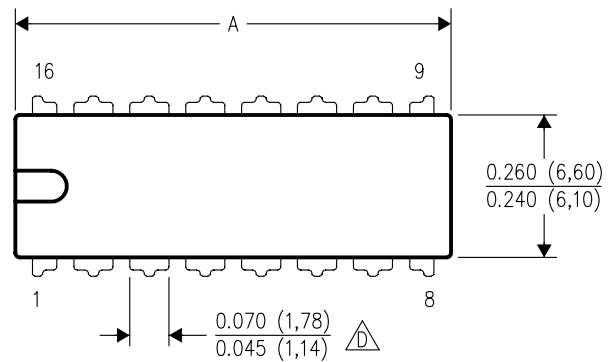
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

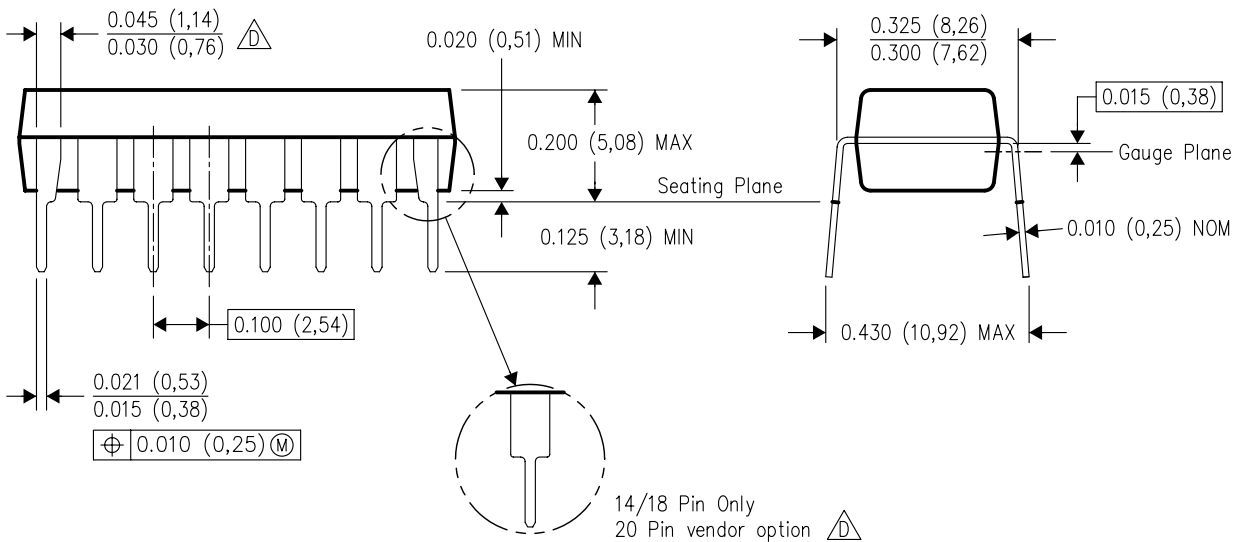
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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