SNx4AHCT123A Dual Retriggerable Monostable Multivibrators

1 Features

- Inputs are TTL-voltage compatible
- Schmitt-trigger circuitry on $\overline{A}$, B, and $\overline{CLR}$ inputs for slow input transition rates
- Edge triggered from active-high or active-low gated logic inputs
- Retriggerable for very long output pulses
- Overriding clear terminates output pulse
- Latch-up performance exceeds 100mA per JESD 78, class II

2 Description

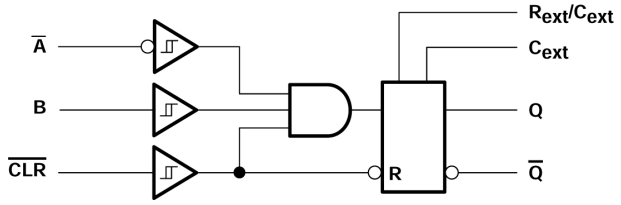
These edge-triggered multivibrators feature output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low, and the B input goes high. In the second method, the B input is high, and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

The output pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC}. To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC}. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SNx4AHCT123A	D (SOIC, 16)	9.90 mm × 6mm	9.90mm × 3.90mm
	DB (SSOP, 16)	6.20mm × 7.8mm	6.20mm × 5.30mm
	DGV (TVSOP, 16)	3.6mm × 6.4mm	3.6mm × 4.4mm
	N (PDIP, 16)	19.31mm × 9.4mm	19.31mm × 6.35mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00 mm × 4.40 mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram, Each Multivibrator (Positive Logic)

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3 Pin Configuration and Functions

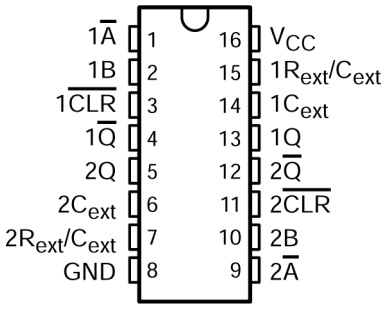
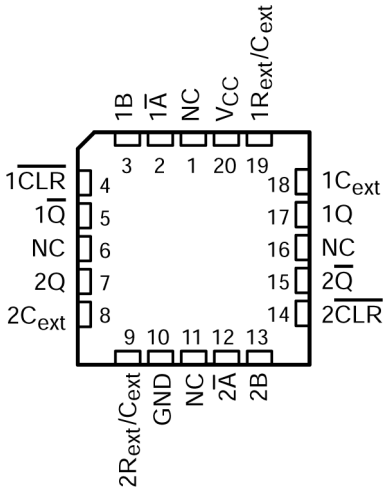


Figure 3-1. SN54AHCT123A J or W Package; SN74AHCT123A D, DB, DGV, N, or PW Package (Top View)



NC – No internal connection

Figure 3-2. SN54AHCT123A FK Package (Top View)

Table 3-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
1 $\overline{A}$	1	I	Channel 1 falling edge trigger input when 1B = H; Hold low for other input methods
1B	2	I	Channel 1 rising edge trigger input when 1 $\overline{A}$ = L; Hold high for other input methods
1 $\overline{CLR}$	3	I	Channel 1 rising edge trigger when 1 $\overline{A}$ = L and 1B = H; Hold high for other input methods; Can cut pulse length short by driving low during output
1 $\overline{Q}$	4	O	Channel 1 inverted output
2Q	5	O	Channel 2 output
2C_{ext}	6	—	Channel 2 external capacitor negative connection
2R_{ext}/C_{ext}	7	—	Channel 2 external capacitor and resistor junction connection
GND	8	—	Ground
2 $\overline{A}$	9	I	Channel 2 falling edge trigger input when 2B = H; Hold low for other input methods
2B	10	I	Channel 2 rising edge trigger input when 2 $\overline{A}$ = L; Hold high for other input methods
2 $\overline{CLR}$	11	I	Channel 2 rising edge trigger when 2 $\overline{A}$ = L and 2B = H; Hold high for other input methods; Can cut pulse length short by driving low during output
2 $\overline{Q}$	12	O	Channel 2 inverted output
1Q	13	O	Channel 1 output
1C_{ext}	14	—	Channel 1 external capacitor negative connection
1R_{ext}/C_{ext}	15	—	Channel 1 external capacitor and resistor junction connection
V_{CC}	16	—	Power supply

1. I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC} (2)	Supply voltage range		–0.5	7	V
V_I (3)	Input voltage range		–0.5	7	V
V_O (2)	Output voltage range		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0)		–20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the network ground terminal.
(3) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)(1)

		SN54AHCT123A		SN74AHCT123A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
R_{ext}	External timing resistance	1k		1k		Ω
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	1		1		ms/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

(1) Unused R_{ext}/C_{ext} terminals should be left unconnected. All remaining unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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4.4 Thermal Information

THERMAL METRIC[1]		SN74AHCT123A					UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	82	120	67	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25 °C			SN54AHCT123A		SN74AHCT123A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = -50 µA		4.5 V	4.4	4.5		4.4		4.4		V
		I_{OH} = -8 mA			3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 µA		4.5 V			0.1		0.1		0.1	V
		I_{OL} = 8 mA					0.36		0.5		0.44	
I_I	R_{ext}/C_{ext} [2]	V_I = V_{CC} or GND		5.5 V			±0.25		±2.5		±2.5	µA
	$\overline{A}$, B, and $\overline{CLR}$	V_I = V_{CC} or GND		0 V to 5.5 V			±0.1		±1[1]		±1	
I_{CC}	Quiescent	V_I = V_{CC} or GND,	I_O = 0	5.5 V			4		40		40	µA
I_{CC}	Active state (per circuit)	V_I = V_{CC} or GND, R_{ext}/C_{ext} = 0.5 V_{CC}		5.5 V		560	750		975		975	µA
ΔI_{CC} [3]		One input at 3.4 V, Other inputs at V_{CC} or GND		5.5 V			1.35		1.5		1.5	mA
C_i		V_I = V_{CC} or GND		5 V		1.9	10				10	pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
(2) This test is performed with the terminal in the off-state condition.
(3) This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or VCC.

4.6 Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

			TEST CONDITIONS	T_A = 25 °C			SN54AHCT123A		SN74AHCT123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLR}$		5			5		5		ns
		$\overline{A}$ or B trigger		5			5		5		
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ C_{ext} = 100 pF	(1)	60		(1)		(1)		ns
			R_{ext} = 1 kΩ, C_{ext} = 0.01 µF	(1)	1.5		(1)		(1)		µs

(1) See retriggering data in the *application information* section.

4.7 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54AHCT123A		SN74AHCT123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 15 pF		5.3[1]	10[1]	1[1]	13[1]	1	11	ns
t_{PHL}					5.3[1]	10[1]	1[1]	13[1]	1	11	

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over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54AHCT123A		SN74AHCT123A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{CLR}$	Q or $\overline{Q}$	C_L = 15 pF		7.7(1)	12(1)	1(1)	15(1)	1	13	ns
t_{PHL}					7.7(1)	12(1)	1(1)	15(1)	1	13	
t_{PLH}	$\overline{CLR}$ trigger	Q or $\overline{Q}$	C_L = 15 pF		8(1)	13(1)	1(1)	16(1)	1	14	ns
t_{PHL}					8(1)	13(1)	1(1)	16(1)	1	14	
t_{PLH}	$\overline{A}$ or B	Q or $\overline{Q}$	C_L = 50 pF		6.8	11	1	14	1	12	ns
t_{PHL}					6.8	11	1	14	1	12	
t_{PLH}	$\overline{CLR}$	Q or $\overline{Q}$	C_L = 50 pF		9.2	13	1	16	1	14	ns
t_{PHL}					9.2	13	1	16	1	14	
t_{PLH}	$\overline{CLR}$ trigger	Q or $\overline{Q}$	C_L = 50 pF		9.5	14	1	17	1	15	ns
t_{PHL}					9.5	14	1	17	1	15	
t_w (2)		Q or $\overline{Q}$	C_L = 50 pF, C_{ext} = 28 pF, R_{ext} = 2 kΩ		133	200		240		240	ns
			C_L = 50 pF, C_{ext} = 0.01 µF R_{ext} = 10 kΩ	90	100	110	90	110	90	110	µs
			C_L = 50 pF, C_{ext} = 0.1 µF, R_{ext} = 10 kΩ	0.9	1	1.1	0.9	1.1	0.9	1.1	ms
Δ_{tw} (3)					±1						%

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) t_w = Pulse duration at Q and $\overline{Q}$ outputs
(3) Δ_{tw} = Output pulse-duration variation (Q and $\overline{Q}$) between circuits in same package

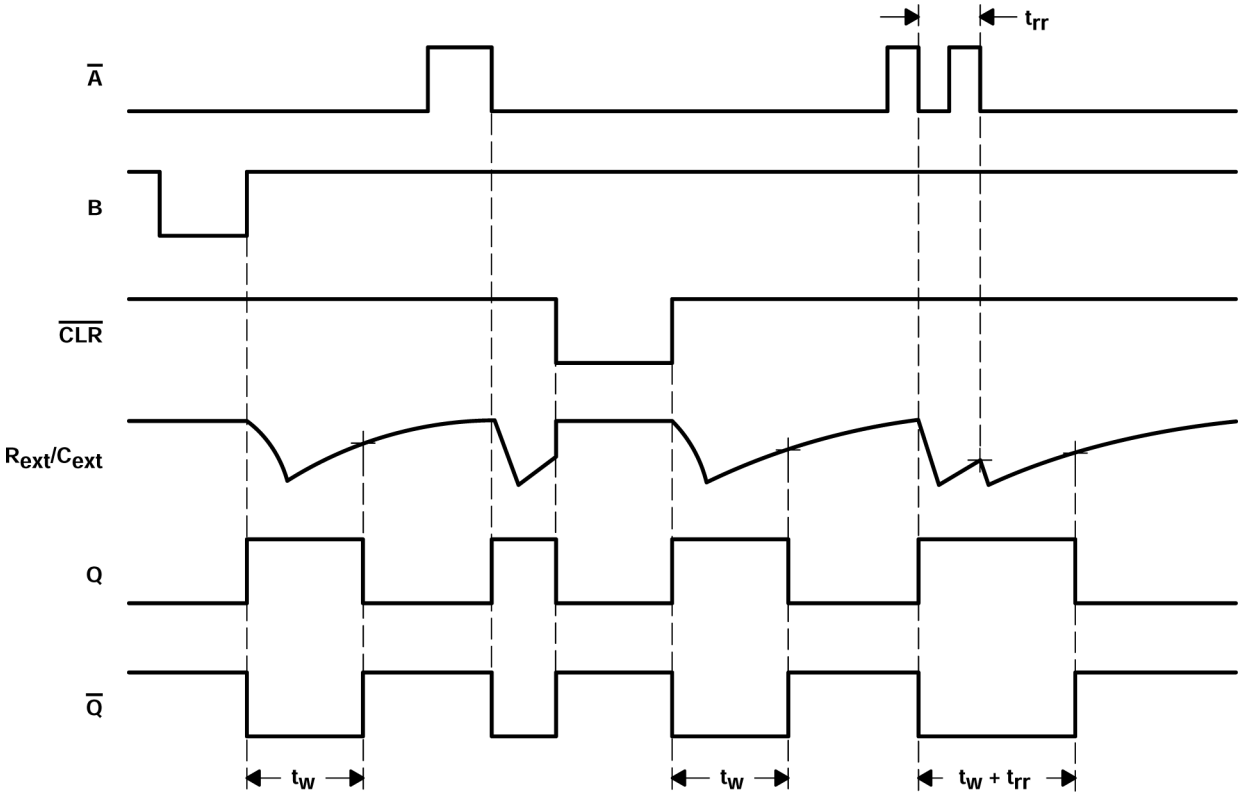
4.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

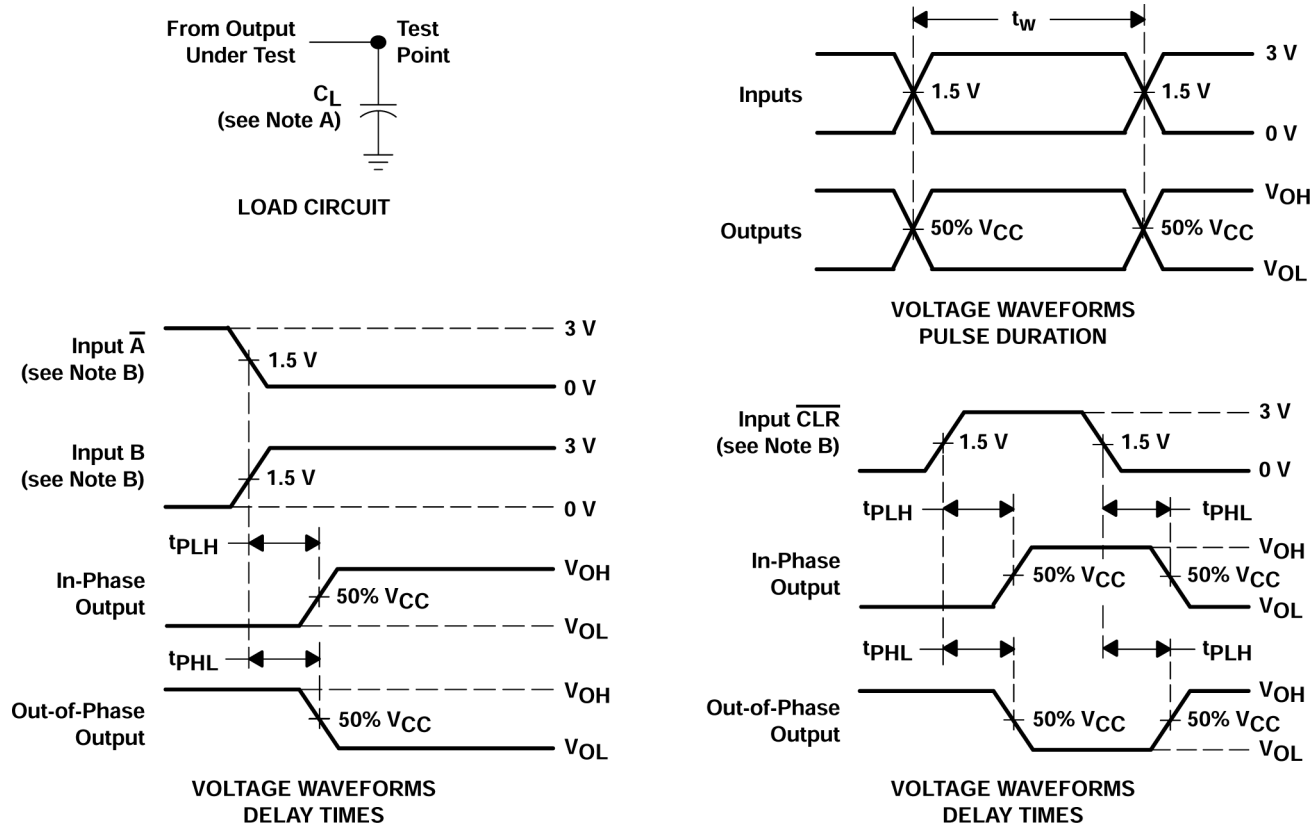
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	29	pF

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4.9 Input/Output Timing Diagram



5 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: Z_O = 50 Ω, t_r 3 ns. 3 ns, t_f

C. The outputs are measured one at a time with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms

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6 Detailed Description

6.1 Overview

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The $\overline{A}$, B, and $\overline{CLR}$ inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\overline{A}$) or high-level-active (B) input. Pulse duration can be reduced by taking $\overline{CLR}$ low. $\overline{CLR}$ input can be used to override $\overline{A}$ or B inputs. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

The variance in output pulse duration from device to device typically is less than ±0.5% for given external timing components. An example of this distribution for the ’AHCT123A is shown in Figure 7-9. Variations in output pulse duration versus supply voltage and temperature are shown in Figure 7-5.

During power up, Q outputs are in the low state, and $\overline{Q}$ outputs are in the high state. The outputs are glitch free, without applying a reset pulse.

For additional application information on multivibrators, see the application report, *Designing With the SN74AHC123A and SN74AHCT123A*, literature number SCLA014.

6.2 Functional Block Diagram

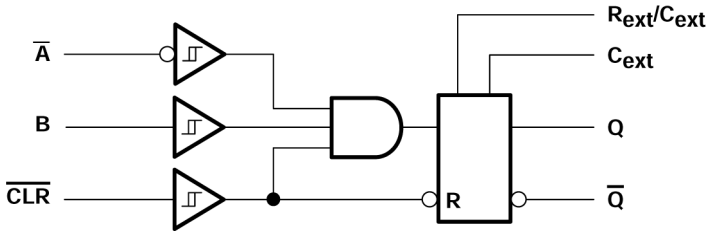


Figure 6-1. Logic Diagram, Each Multivibrator (Positive Logic)

6.3 Feature Description

6.3.1 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

6.3.2 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

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TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and typically will meet all requirements.

6.4 Device Functional Modes

Table 6-1. Function Table (Each Multivibrator)

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L(1)	H(1)
X	X	L	L(1)	H(1)
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

(1) These outputs are based on the assumption that the indicated steady-state conditions at the $\overline{A}$ and B inputs have been set up long enough to complete any pulse started before the setup.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

7.1.1 Caution in Use

To prevent malfunctions due to noise, connect a high-frequency capacitor between V_{CC} and GND, and keep the wiring between the external components and C_{ext} and R_{ext}/C_{ext} terminals as short as possible.

7.1.2 Power-down Considerations

Large values of C_{ext} may cause problems when powering down the 'AHCT123A devices because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{CC} through the protection diodes at pin 2 or pin 14. Current through the input protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \times C_{ext}/30$ mA. For example, if V_{CC} = 5 V and C_{ext} = 15 pF, the V_{CC} supply must turn off no faster than $t = (5\ V) \times (15\ pF)/30mA = 2.5$ ns. Usually, this is not a problem because power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of V_{CC} to zero occurs, the 'AHCT123A devices may sustain damage. To avoid this possibility, use external clamping diodes.

7.1.3 Output Pulse Duration

The output pulse duration, t_w, is determined primarily by the values of the external capacitance (C_T) and timing resistance (R_T). The timing components are connected as shown in Figure 7-1.

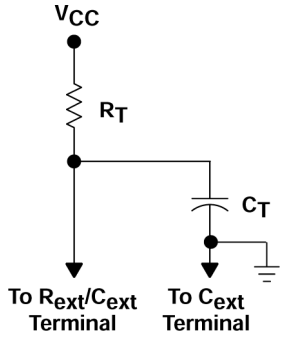


Figure 7-1. Timing-Component Connections

The pulse duration is given by:

$t_w = K \times R_T \times C_T$ (1)

if C_T is ≥ 1000 pF, K = 1.0 or

if C_T is < 1000 pF, K can be determined from Figure 7-4

where:

t_w = pulse duration in ns

R_T = external timing resistance in kΩ

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C_T = external capacitance in pF

K = multiplier factor

Equation 1 and Figure 7-2 can be used to determine values for pulse duration, external resistance, and external capacitance.

7.1.4 Retriggering Data

The minimum input retriggering time (t_{MIR}) is the minimum time required after the initial signal before retriggering the input. After t_{MIR}, the device retriggers the output. Experimentally, it also can be shown that to retrigger the output pulse, the two adjacent input signals should be t_{MIR} apart, where t_{MIR} = 0.30 × t_w. The retrigger pulse duration is calculated as shown in Figure 7-2.

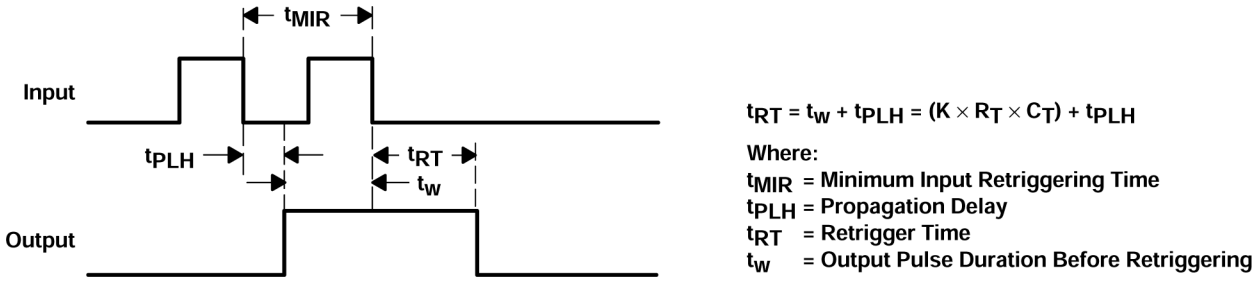


Figure 7-2. Retrigger Pulse Duration

The minimum value from the end of the input pulse to the beginning of the retriggered output should be approximately 15 ns to ensure a retriggered output (see Figure 7-3).

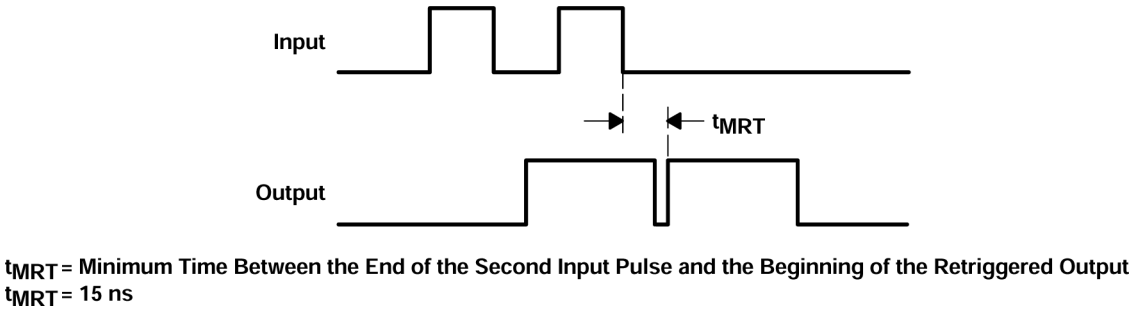


Figure 7-3. Input/Output Requirements

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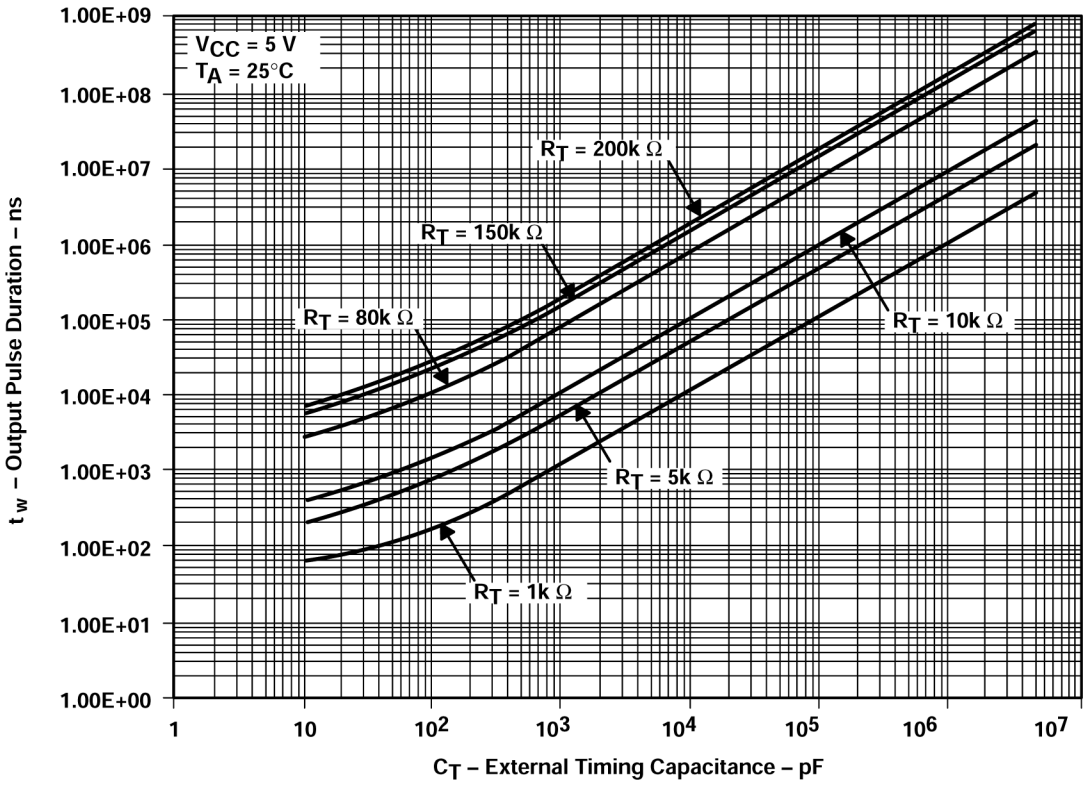


Figure 7-4. Output Pulse Duration vs External Timing Capacitance

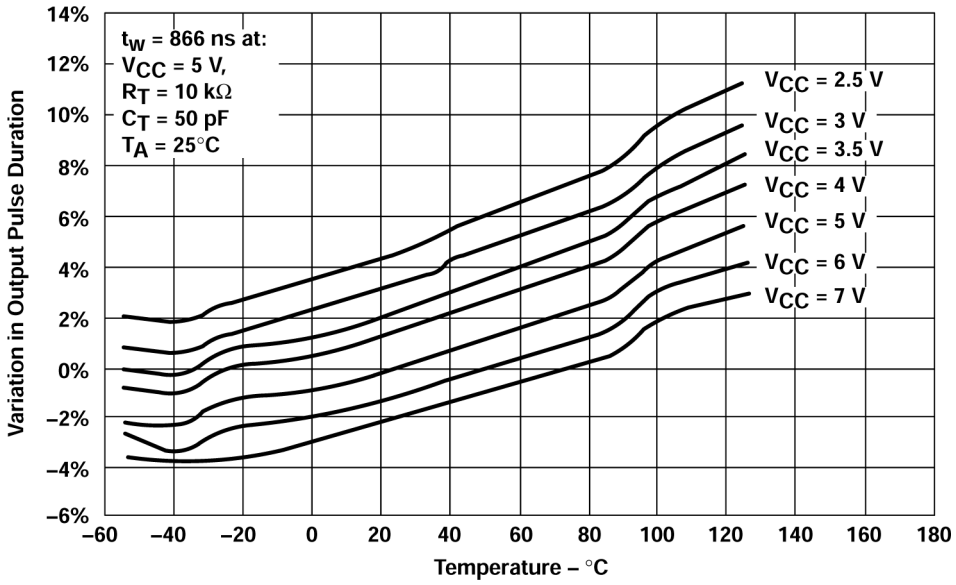


Figure 7-5. Variations in Output Pulse Duration vs Temperature

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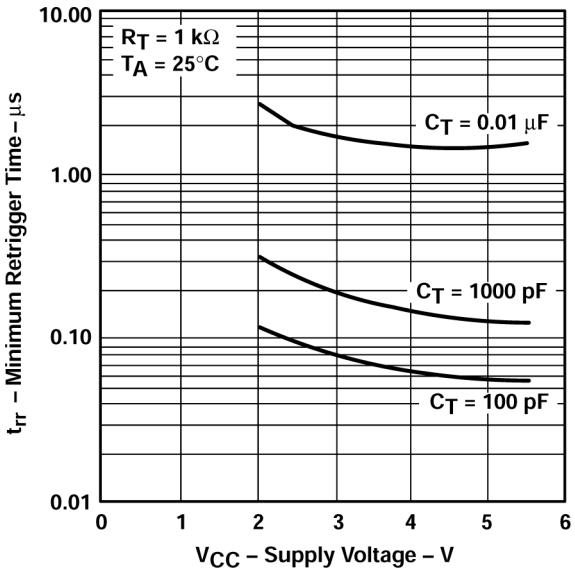


Figure 7-6. Minimum Trigger Time vs v_{CC} Characteristics

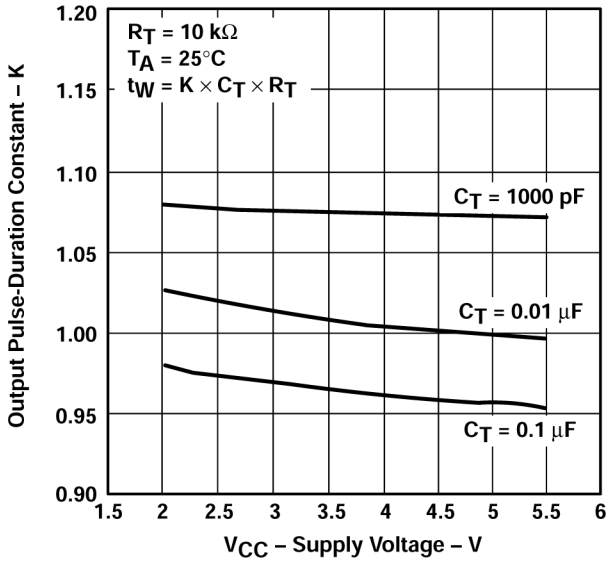


Figure 7-7. Output Pulse-duration Constant vs Supply Voltage

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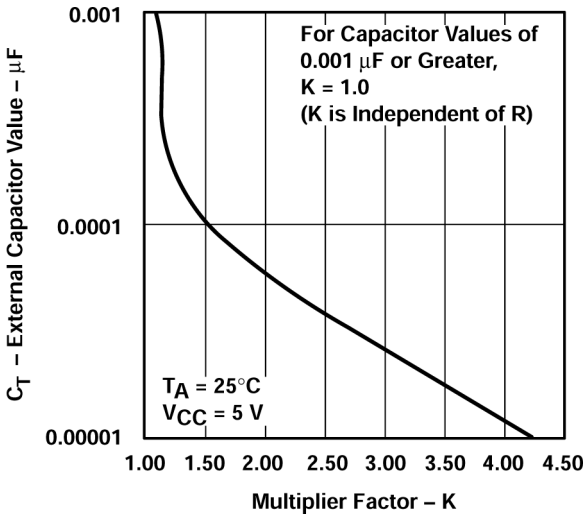


Figure 7-8. External Capacitance vs Multiplier Factor

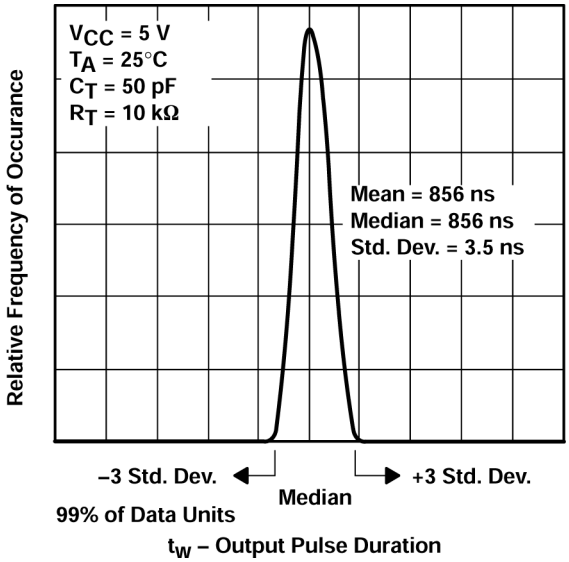


Figure 7-9. Distribution of Units vs Output Pulse Duration

7.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For the SNx4AHCT123A, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

7.3 Layout

7.3.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry

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- 8mil to 12mil trace width
- Lengths less than 12cm to minimize transmission line effects
- Avoid 90° corners for signal traces
- Use an unbroken ground plane below signal traces
- Flood fill areas around signal traces with ground
- For traces longer than 12cm
  - Use impedance controlled traces
  - Source-terminate using a series damping resistor near the output
  - Avoid branches; buffer signals that must branch separately

7.3.2 Layout Example

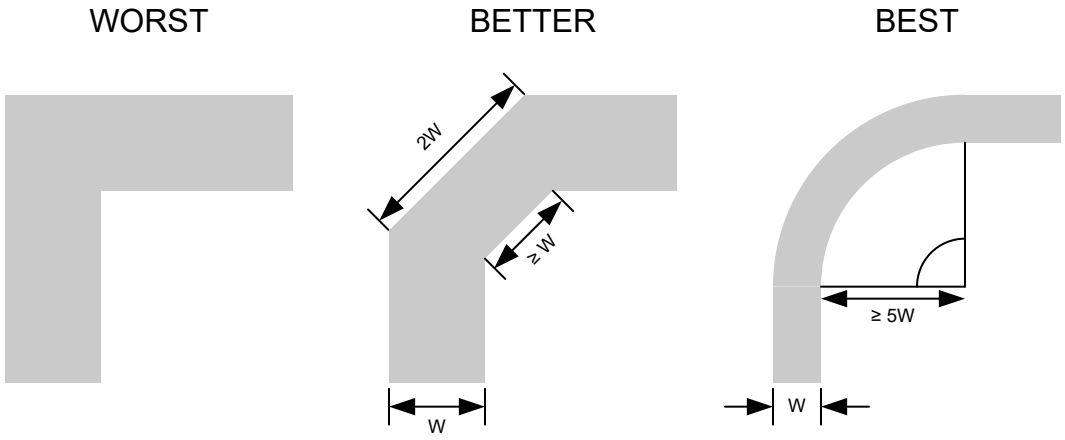


Figure 7-10. Example Trace Corners for Improved Signal Integrity

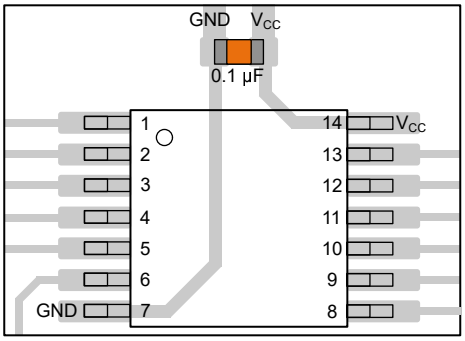


Figure 7-11. Example Bypass Capacitor Placement for TSSOP and Similar Packages

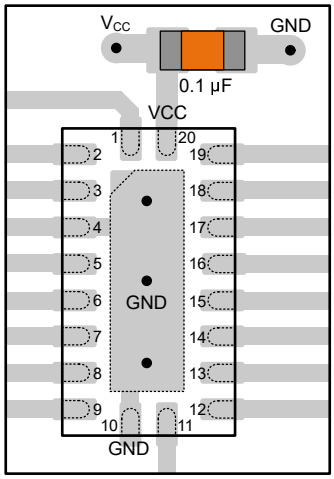


Figure 7-12. Example Bypass Capacitor Placement for WQFN and Similar Packages

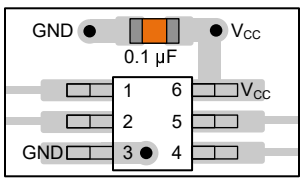


Figure 7-13. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

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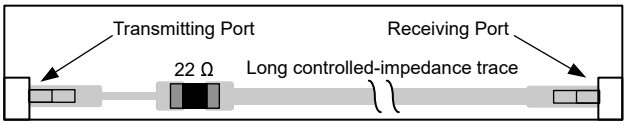


Figure 7-14. Example Damping Resistor Placement for Improved Signal Integrity

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2003) to Revision H (January 2025)	Page
• Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,*Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted references to machine model throughout data sheet	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9861601Q2A	Last Time Buy	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9861601Q2A SNJ54AHCT123AFK
5962-9861601QEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9861601QEA SNJ54AHCT123AJ
5962-9861601QFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9861601QFA SNJ54AHCT123AW
SN74AHCT123AD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	AHCT123A
SN74AHCT123ADBR	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB123A
SN74AHCT123ADBR.A	Active	Production	SSOP (DB) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB123A
SN74AHCT123ADGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB123A
SN74AHCT123ADGVR.A	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB123A
SN74AHCT123ADR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT123A
SN74AHCT123ADR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT123A
SN74AHCT123AN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHCT123AN
SN74AHCT123AN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AHCT123AN
SN74AHCT123APWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB123A
SN74AHCT123APWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB123A
SNJ54AHCT123AFK	Last Time Buy	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9861601Q2A SNJ54AHCT123AFK
SNJ54AHCT123AFK.A	Last Time Buy	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9861601Q2A SNJ54AHCT123AFK
SNJ54AHCT123AJ	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9861601QEA SNJ54AHCT123AJ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AHCT123AJ.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9861601QE A SNJ54AHCT123AJ
SNJ54AHCT123AW	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9861601QF A SNJ54AHCT123AW
SNJ54AHCT123AW.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9861601QF A SNJ54AHCT123AW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHCT123A, SN74AHCT123A :

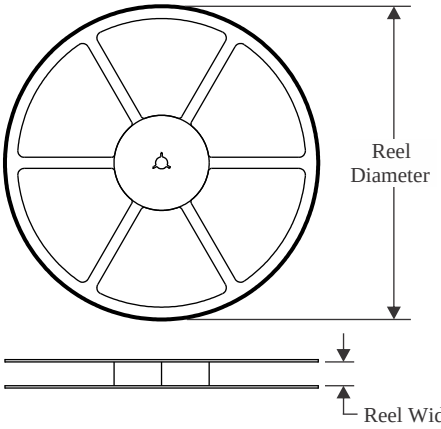
- Catalog : SN74AHCT123A
- Military : SN54AHCT123A

NOTE: Qualified Version Definitions:

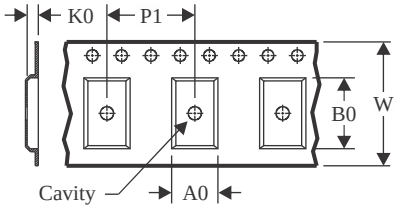
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

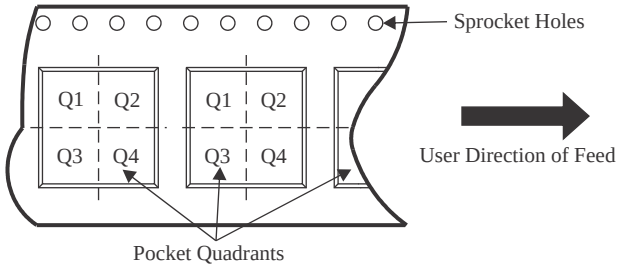


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

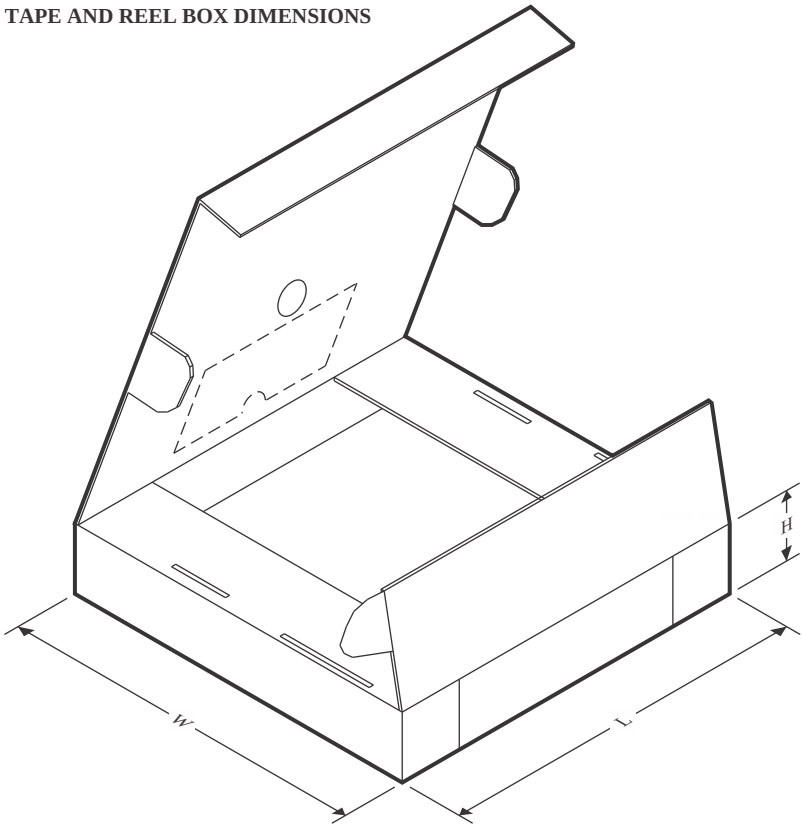
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT123ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT123ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT123ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT123APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

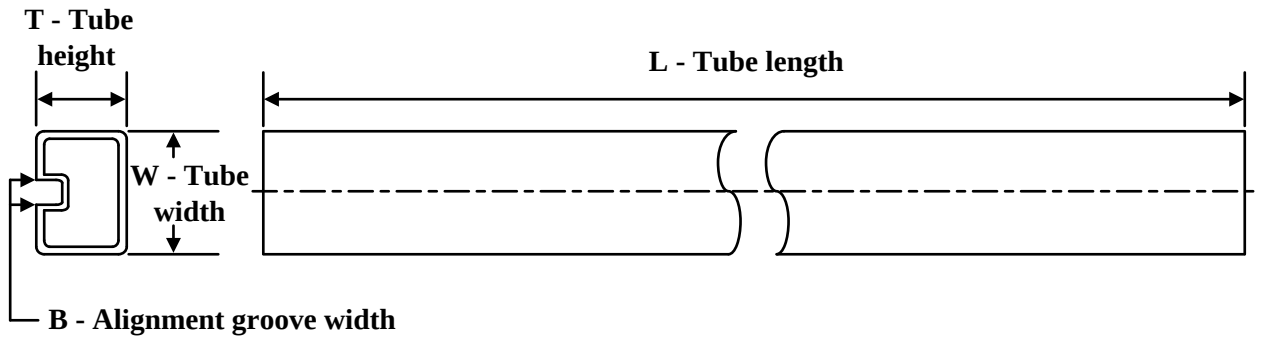
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT123ADBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74AHCT123ADGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74AHCT123ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHCT123APWR	TSSOP	PW	16	2000	353.0	353.0	32.0

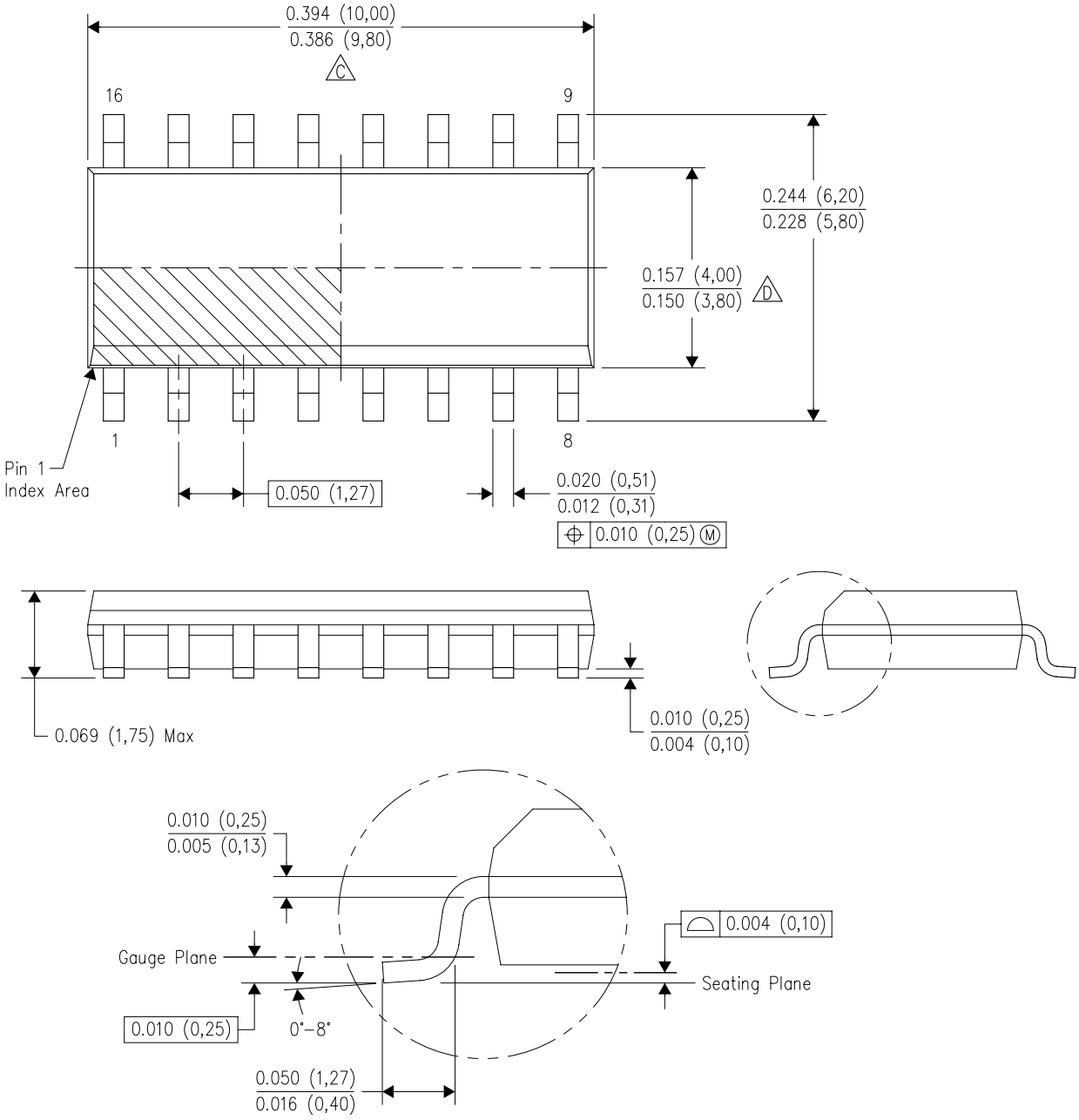
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9861601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9861601QFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74AHCT123AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHCT123AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54AHCT123AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT123AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT123AW	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54AHCT123AW.A	W	CFP	16	25	506.98	26.16	6220	NA

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



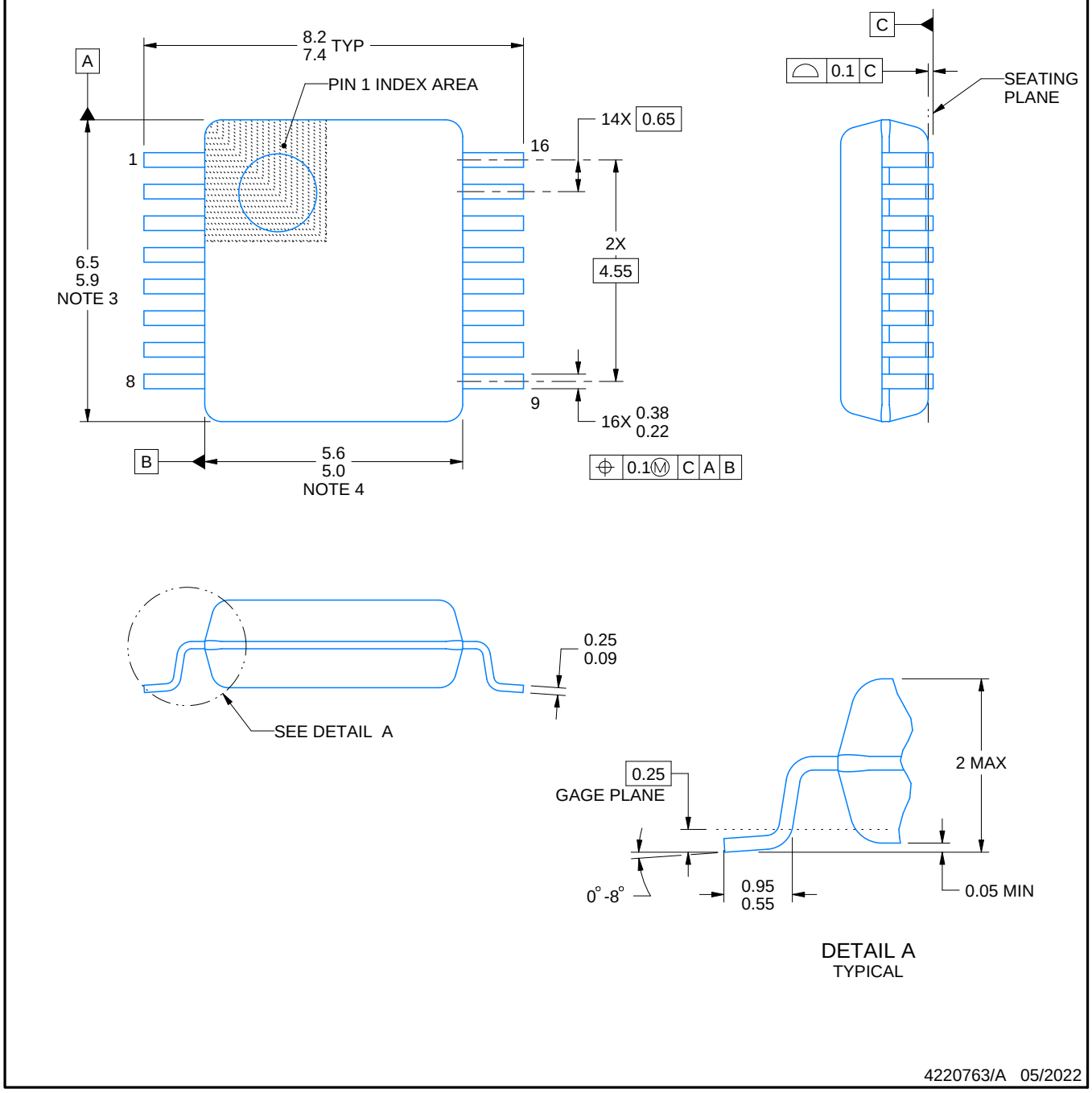
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

DB0016A

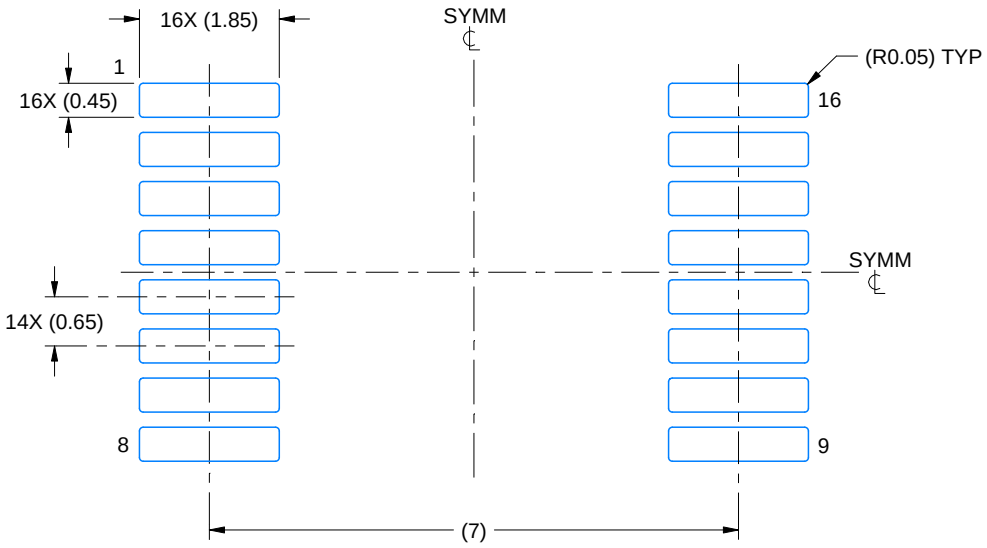
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

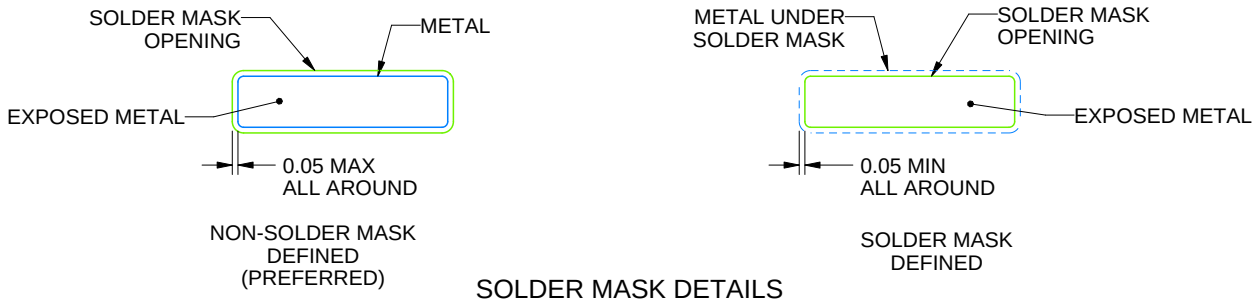


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

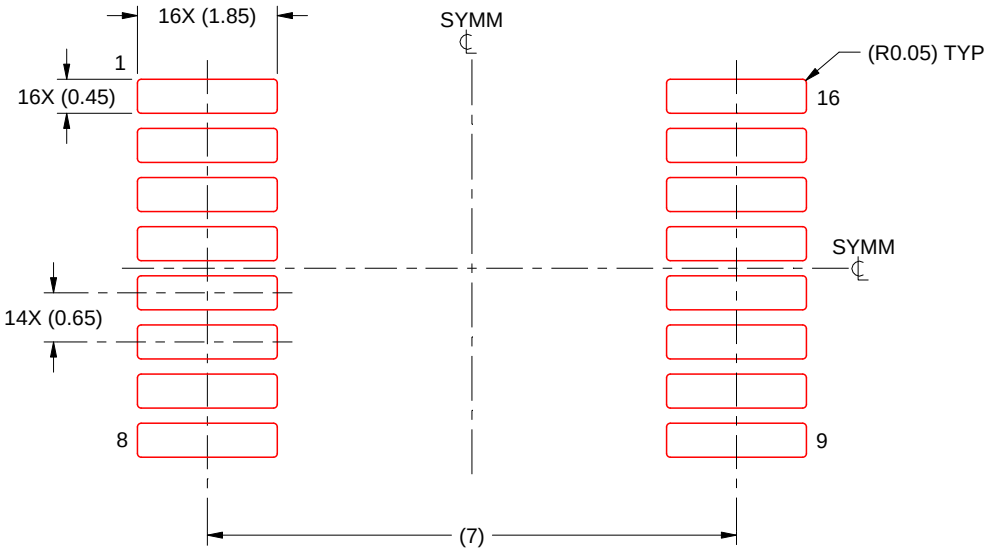


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

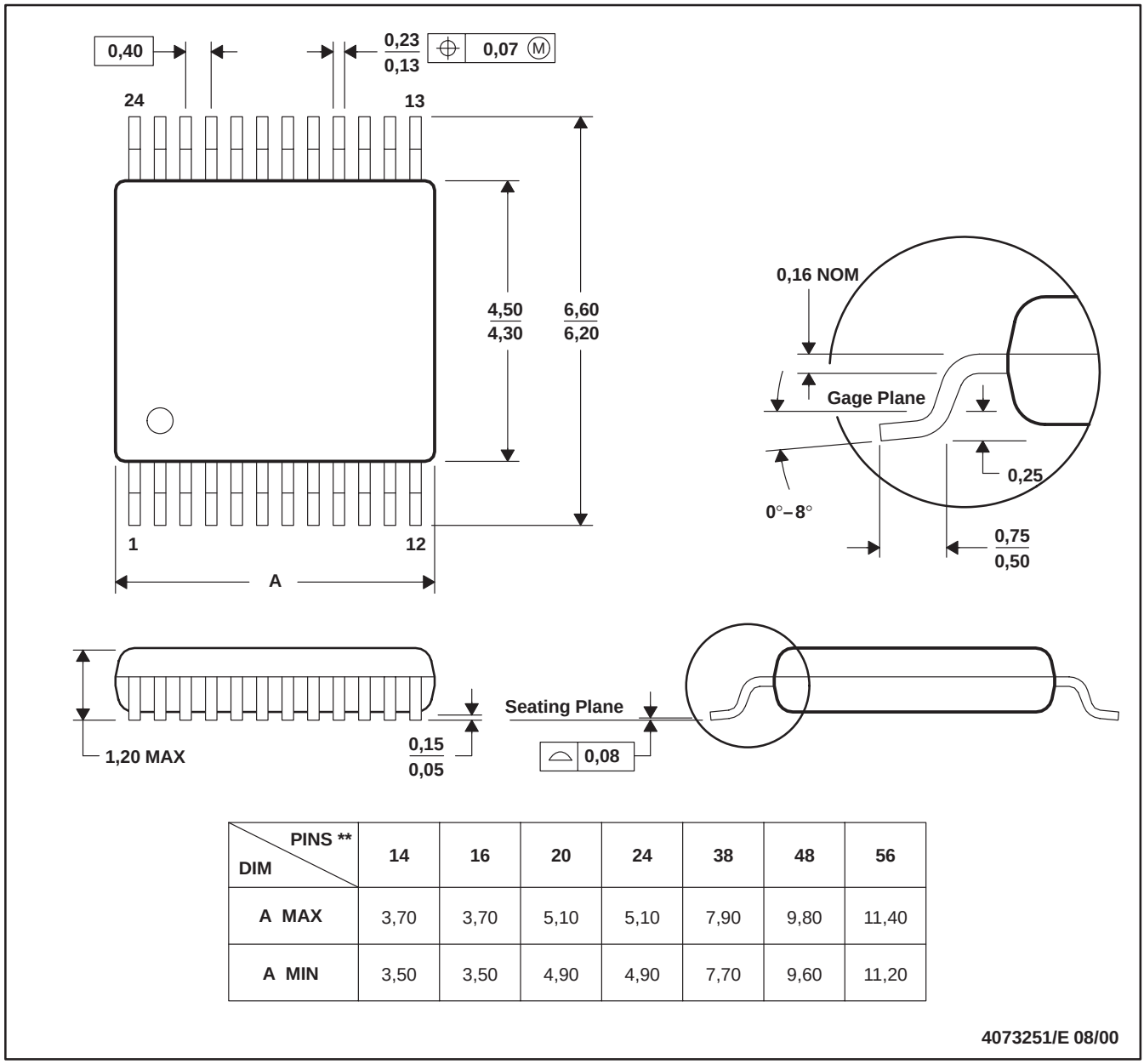
4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

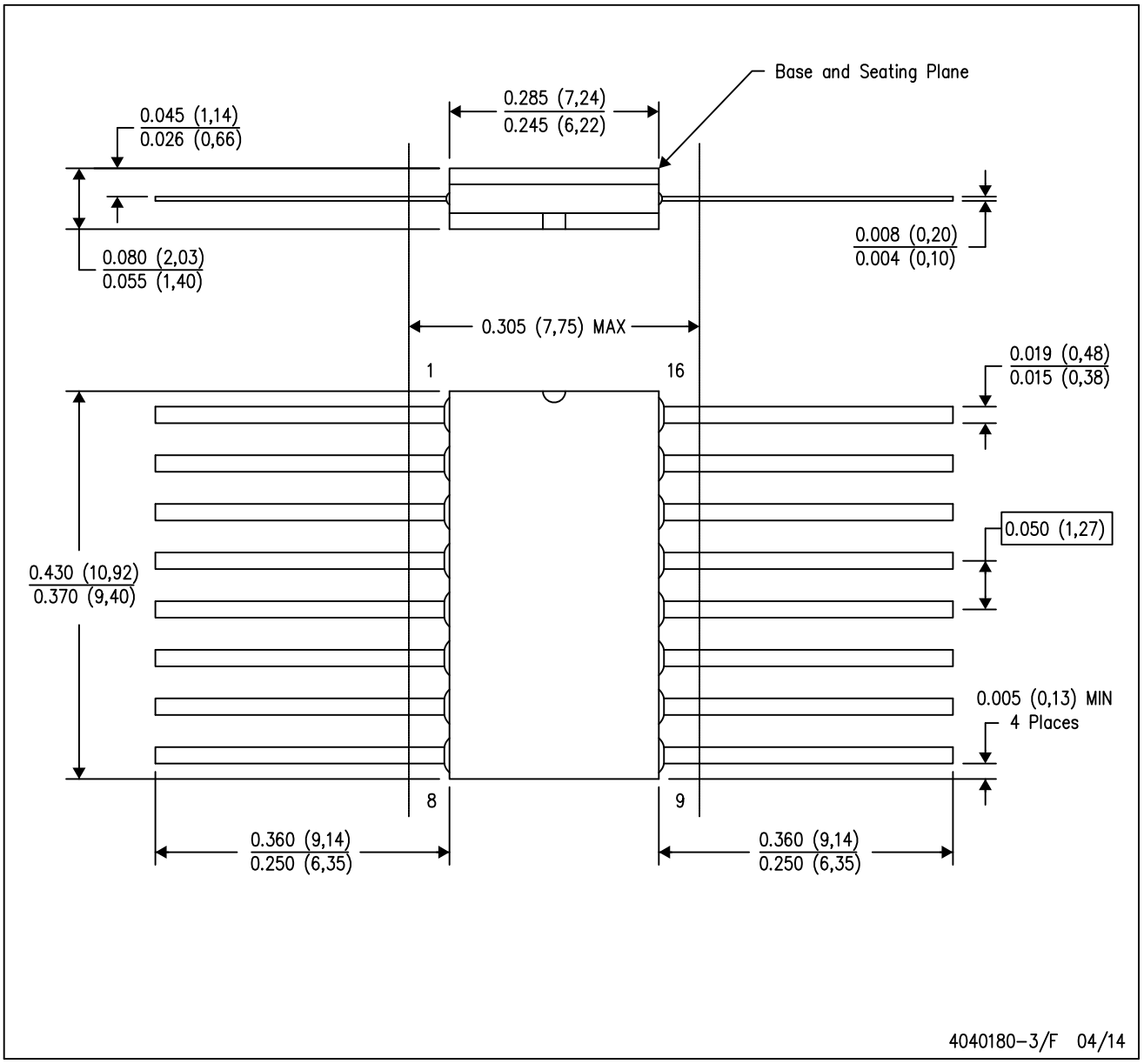


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

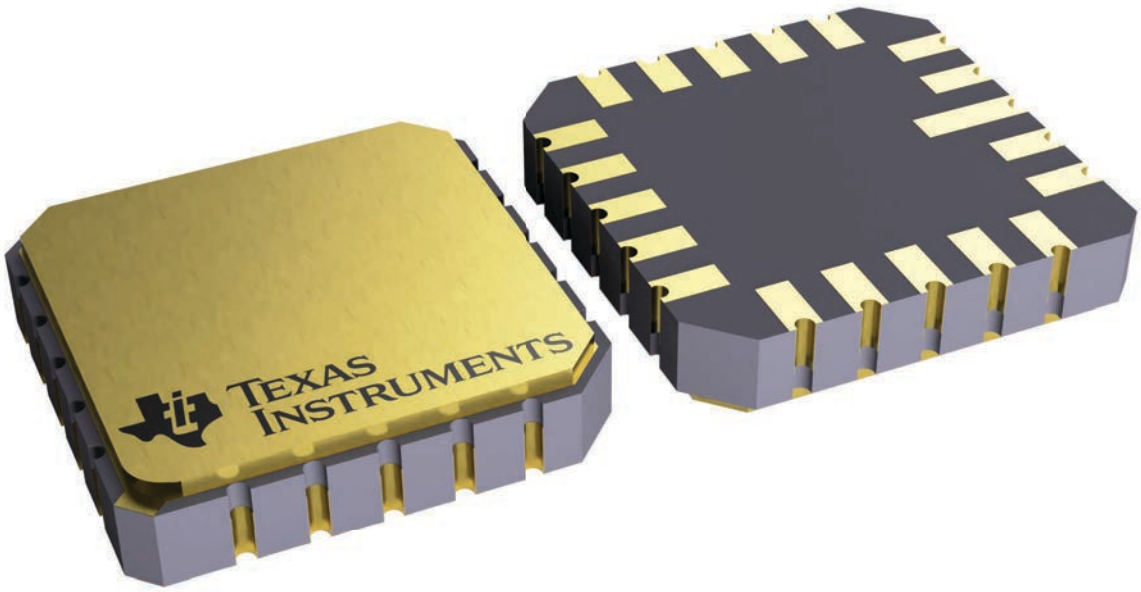
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

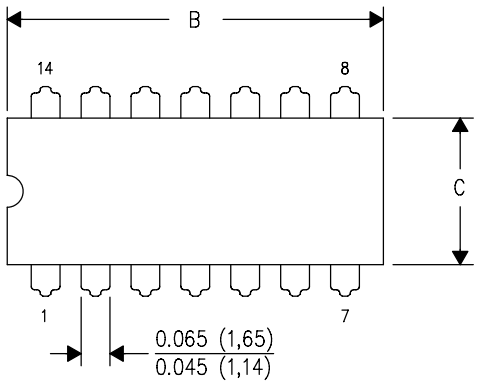


4229370VA\

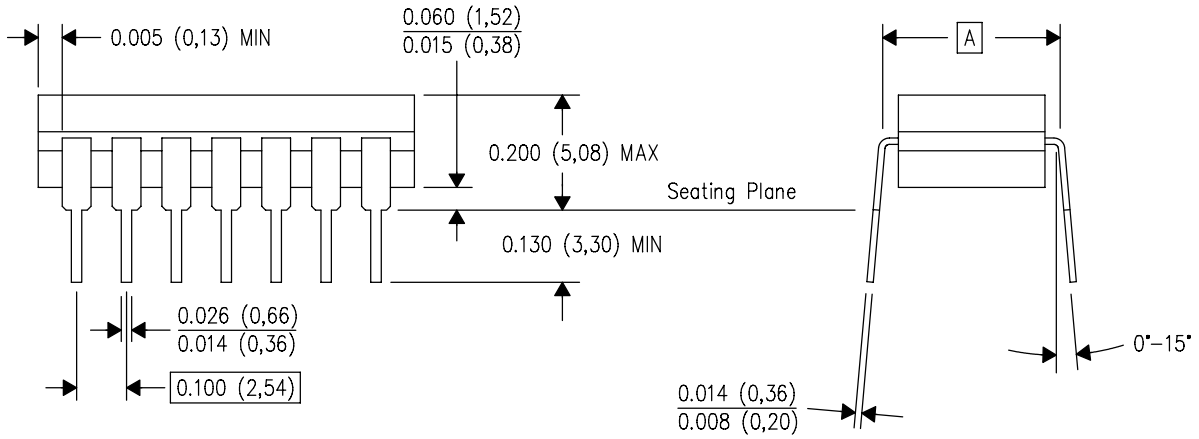
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

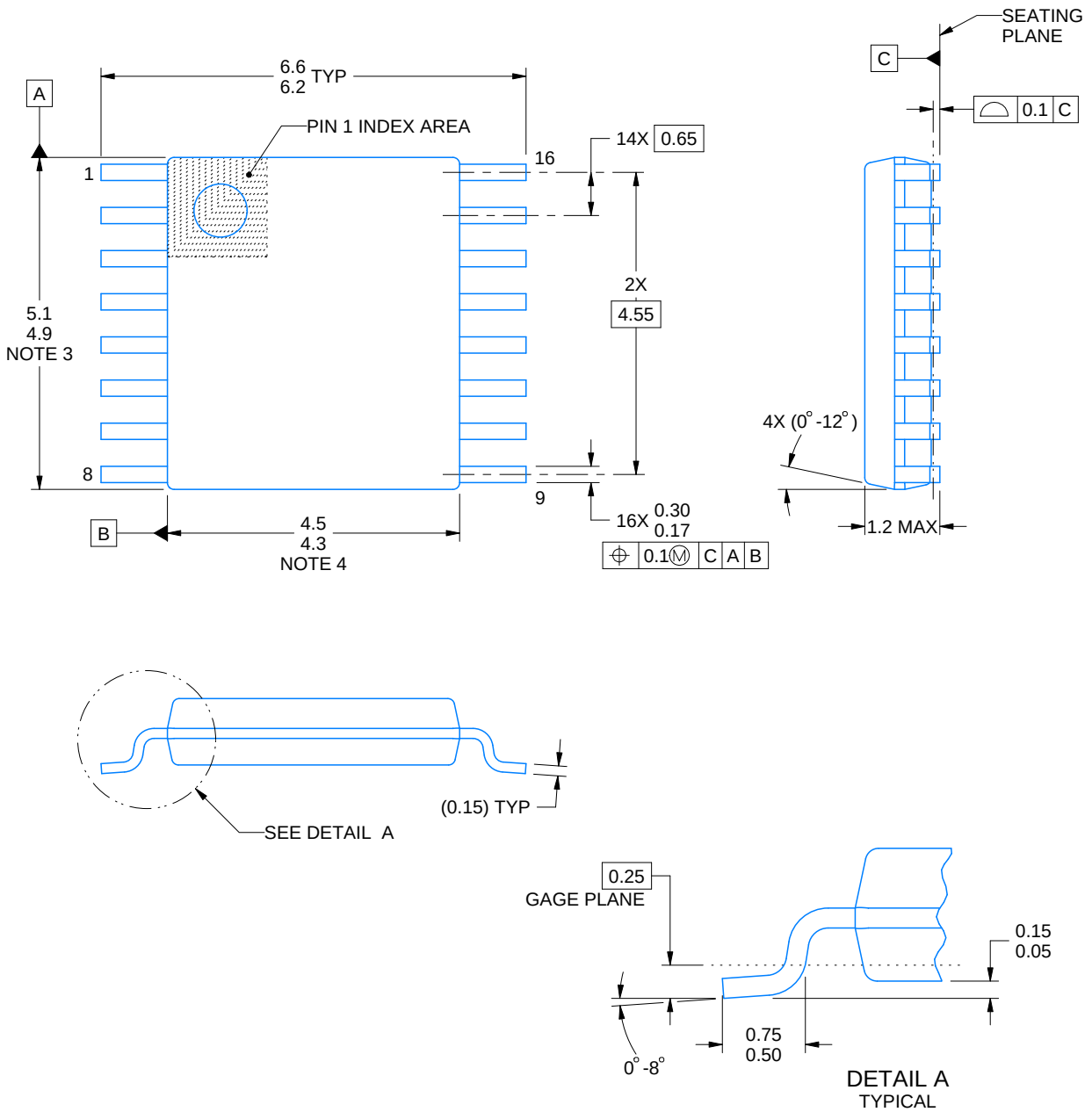
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

PW0016A

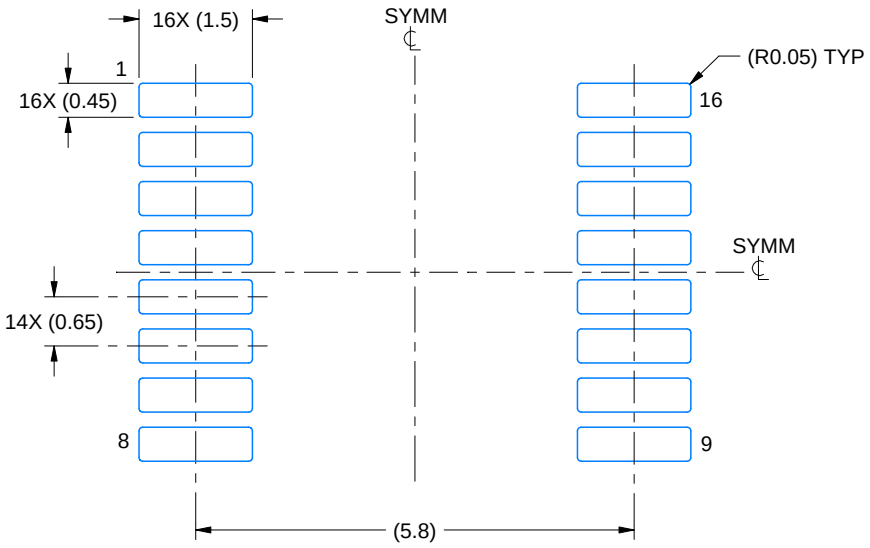
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

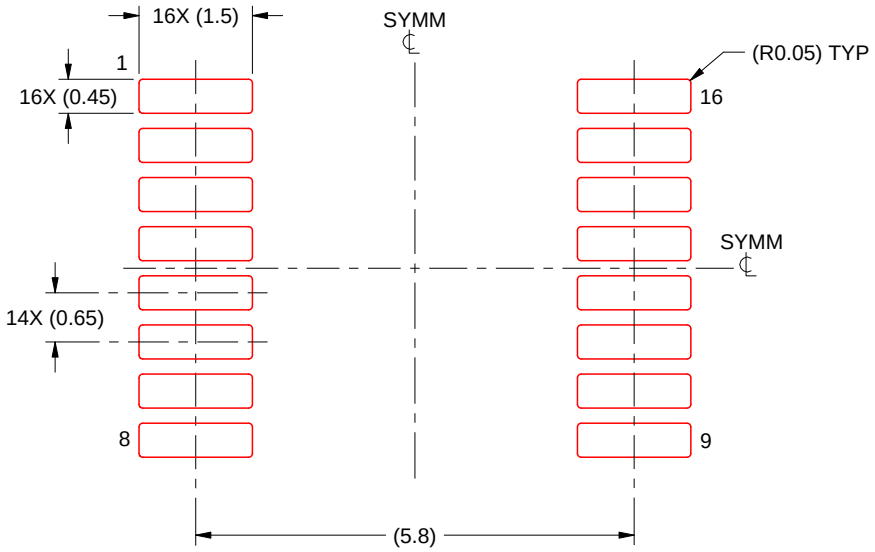


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

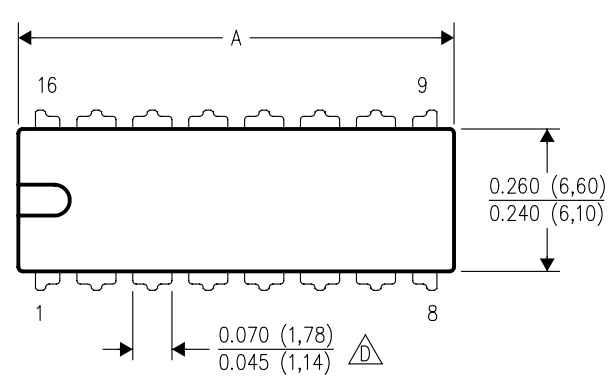
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

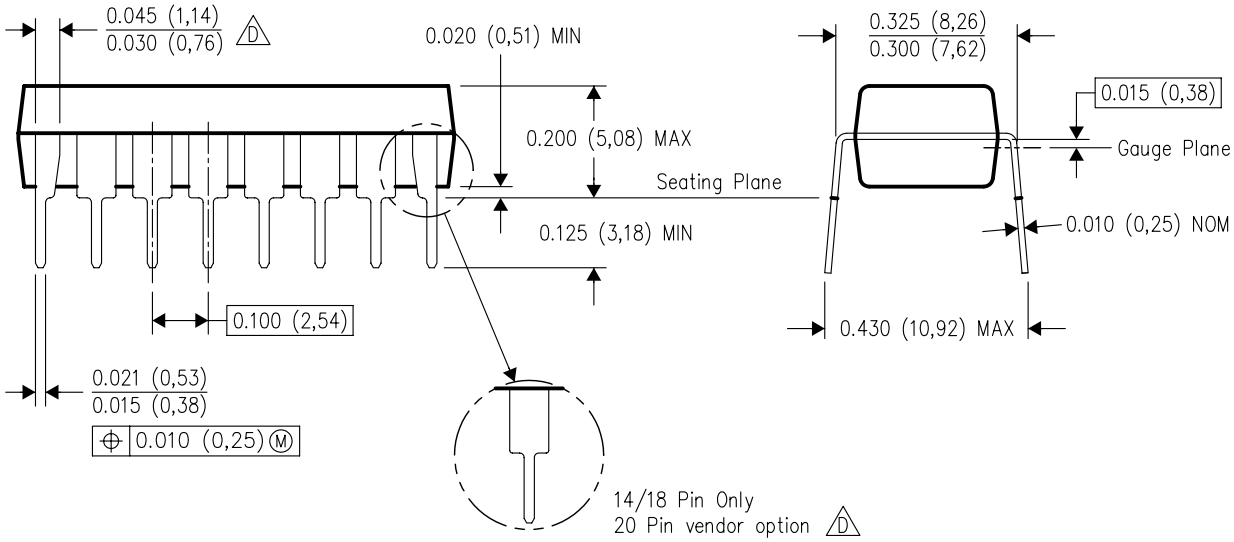
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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