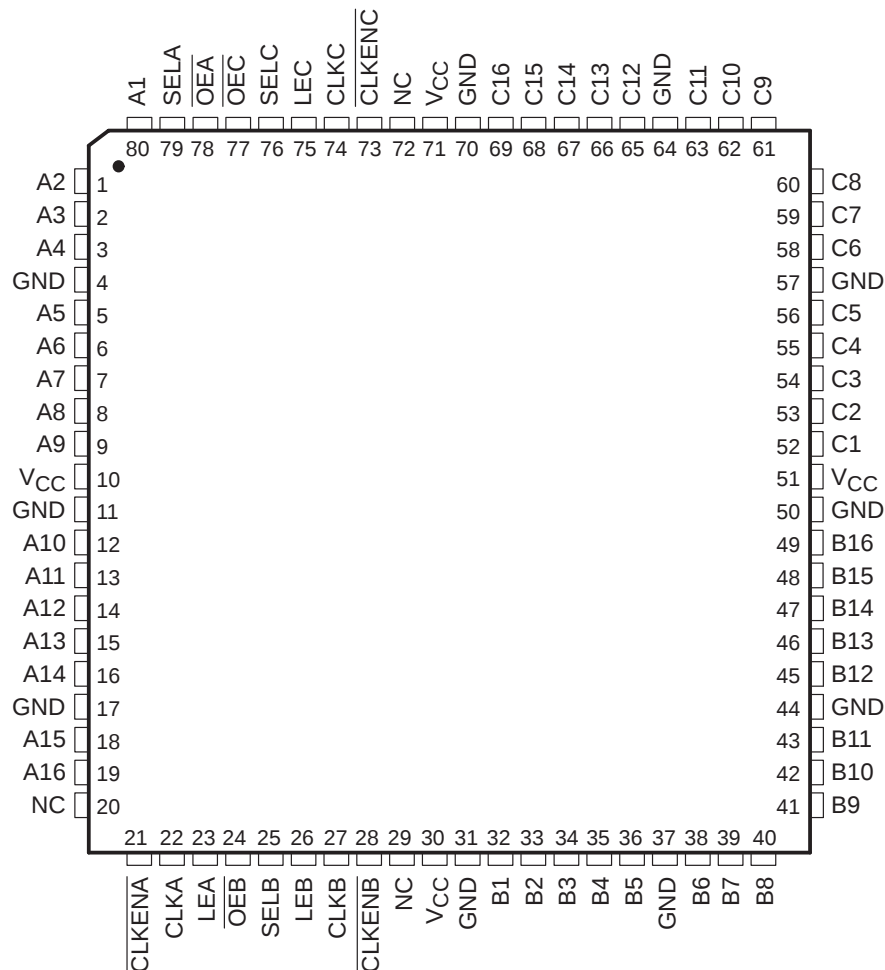


SN54ABTH32316, SN74ABTH32316 16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

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- Members of the Texas Instruments *Widebus+*™ Family
- State-of-the-Art *EPIC-II*B™ BiCMOS Design Significantly Reduces Power Dissipation
- *UBE*™ (Universal Bus Exchanger) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include 80-Pin Plastic Thin Quad Flat (PN) Package With $12 \times 12\text{-mm}$ Body Using 0.5-mm Lead Pitch and 84-Pin Ceramic Quad Flat (HT) Package

'ABTH32316 . . . PN PACKAGE
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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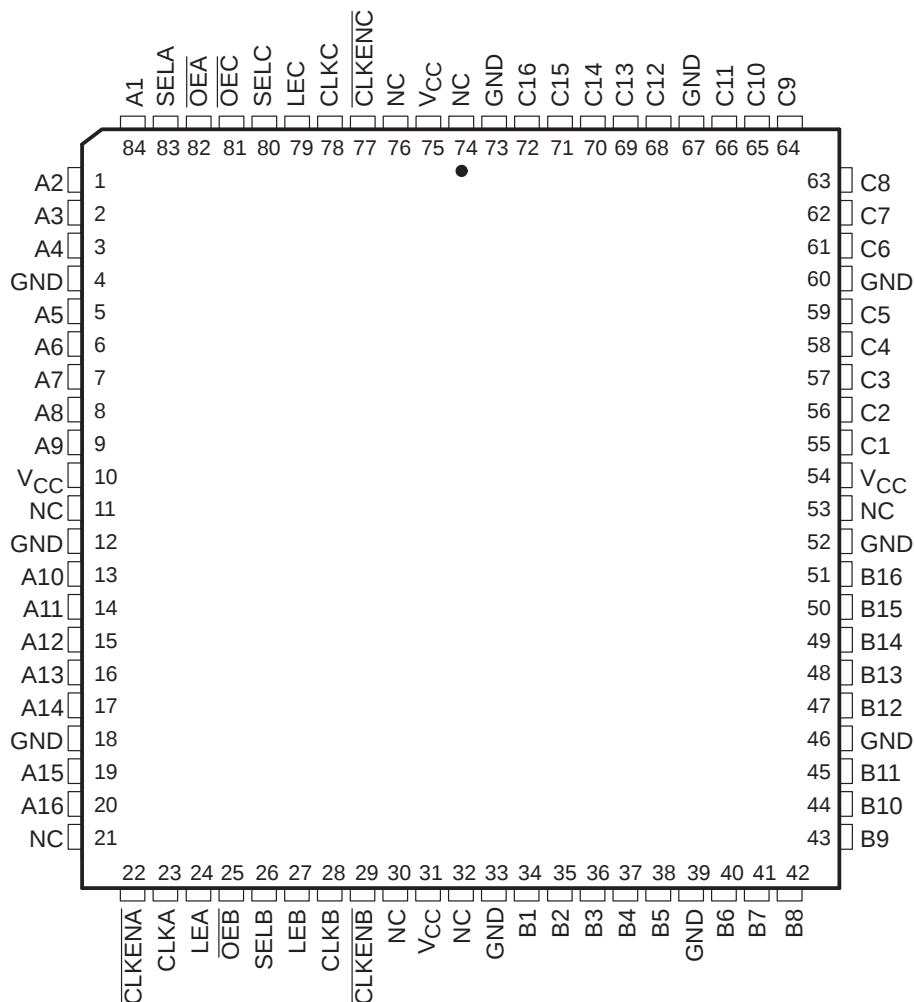
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SN54ABTH32316, SN74ABTH32316

16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

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SN54ABTH32316 . . . HT PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABTH32316 consist of three 16-bit registered input/output (I/O) ports. These registers combine D-type latches and flip-flops to allow data flow in transparent, latch, and clock modes. Data from one input port can be exchanged to one or more of the other ports. Because of the universal storage element, multiple combinations of real-time and stored data can be exchanged among the three ports.

Data flow in each direction is controlled by the output-enable ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$, and $\overline{\text{OEC}}$), select-control (SELA, SELB, and SELC), latch-enable (LEA, LEB, and LEC), and clock (CLKA, CLKB, and CLKC) inputs. The A data register operates in the transparent mode when LEA is high. When LEA is low, data is latched if CLKA is held at a high or low logic level. If LEA and clock-enable A ($\overline{\text{CLKENA}}$) are low, data is stored on the low-to-high transition of CLKA. Output data selection is accomplished by the select-control pins. All three ports have active-low output enables, so when the output-enable input is low, the outputs are active; when the output-enable input is high, the outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH32316 is characterized for operation over the full military temperature range of -55°C to 125°C .
 The SN74ABTH32316 is characterized for operation from -40°C to 85°C .

Function Tables

STORAGE[†]

INPUTS				OUTPUT
CLKENA	CLKA	LEA	A	
H	X	L	X	$Q_0^{\ddagger}$
L	$\uparrow$	L	L	L
L	$\uparrow$	L	H	H
X	H	L	X	$Q_0^{\ddagger}$
X	L	L	X	$Q_0^{\ddagger}$
X	X	H	L	L
X	X	H	H	H

[†] A-port register shown. B and C ports are similar but use CLKENB, CLKENC, CLKB, CLKC, LEB, and LEC.

[‡] Output level before the indicated steady-state input conditions were established

A-PORT OUTPUT

INPUTS		OUTPUT A
$\overline{\text{OEA}}$	SELA	
H	X	Z
L	H	Output of C register
L	L	Output of B register

B-PORT OUTPUT

INPUTS		OUTPUT B
$\overline{\text{OEB}}$	SELB	
H	X	Z
L	H	Output of A register
L	L	Output of C register

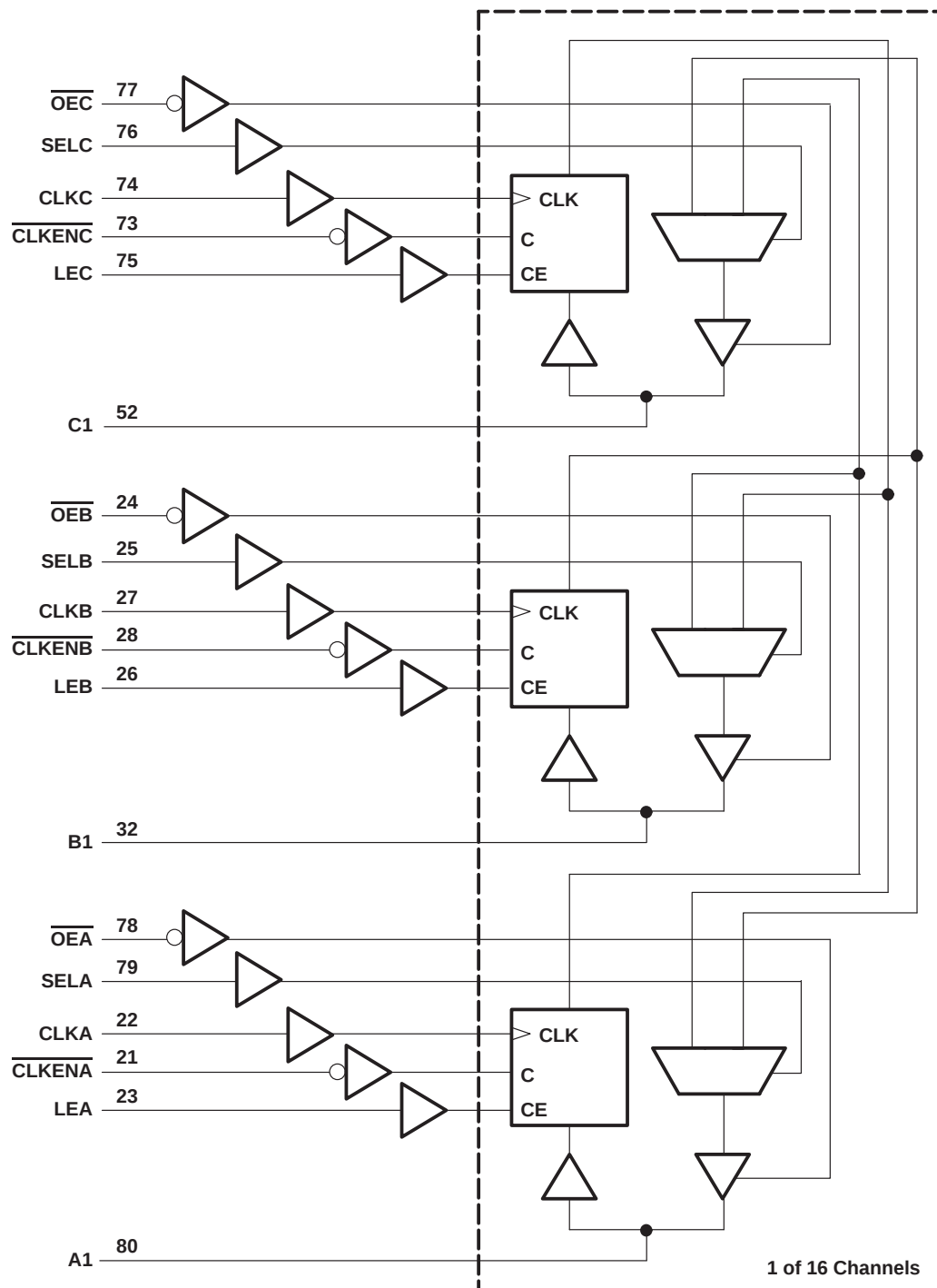
C-PORT OUTPUT

INPUTS		OUTPUT C
$\overline{\text{OEC}}$	SELC	
H	X	Z
L	H	Output of B register
L	L	Output of A register

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logic diagram (positive logic)



Pin numbers shown are for the PN package.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABTH32316	96 mA
SN74ABTH32316	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): PN package	62°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABTH32316		SN74ABTH32316		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ABTH32316			SN74ABTH32316			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5			V
		$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3			
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -24\text{ mA}$	2						
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -32\text{ mA}$				2			
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$			0.55				V
		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 64\text{ mA}$						0.55	
V_{hys}			100			100			mV
I_I	Control inputs	$V_{CC} = 0\text{ to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$			± 1			± 1	μA
	A, B, or C ports	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$			± 100			± 20	
$I_I(\text{hold})$	A, B, or C ports	$V_{CC} = 4.5\text{ V}$, $V_I = 0.8\text{ V}$	100			100			μA
		$V_{CC} = 4.5\text{ V}$, $V_I = 2\text{ V}$	-100			-100			
$I_{OZPU}^\ddagger$		$V_{CC} = 0\text{ to }2.1\text{ V}$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $\overline{OE} = X$			± 50			± 50	μA
$I_{OZPD}^\ddagger$		$V_{CC} = 2.1\text{ V to }0$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $\overline{OE} = X$			± 50			± 50	μA
I_{off}		$V_{CC} = 0$, $V_I\text{ or }V_O \leq 4.5\text{ V}$			± 100			± 100	μA
I_{CEX}		$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$, Outputs high			50			50	μA
I_O^S		$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	-50	-100	-180	-50	-100	-180	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$			2			2	mA
		Outputs high			40			40	
		Outputs disabled			1			1	
$\Delta I_{CC}^\parallel$		$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$			1			0.5	mA
C_i	Control inputs	$V_I = 2.5\text{ V or }0.5\text{ V}$			3			3	pF
C_{io}	A, B, or C ports	$V_O = 2.5\text{ V or }0.5\text{ V}$			11.5			11.5	pF

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This parameter is specified by characterization.

S Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

|| This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABTH32316		SN74ABTH32316		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	MHz
t_w	Pulse duration	LE high	3.3		3.3		ns
		CLK high or low	3.3		3.3		
t_{su}	Setup time	A, B, or C before CLK $\uparrow$	2.6		2.4		ns
		A or B before LE $\downarrow$	2.5		2.1		
		CLKEN before CLK $\uparrow$	3.5		3.2		
t_h	Hold time	A, B, or C after CLK $\uparrow$	1.8		1.4		ns
		A or B after LE $\downarrow$	2.4		2.1		
		CLKEN after CLK $\uparrow$	1.5		1.1		



SN54ABTH32316, SN74ABTH32316 16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

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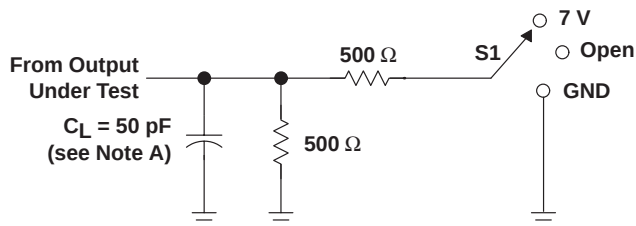
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABTH32316		SN74ABTH32316		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			150		150		MHz
t_{PLH}	A, B, or C	C, B, or A	0.8	6.5	1.4	6.1	ns
t_{PHL}			0.5	6.8	1.1	6.6	
t_{PLH}	SEL	A, B, or C	0.8	6.7	1.4	6.5	ns
t_{PHL}			0.8	6.8	1.8	6.5	
t_{PLH}	LE	A, B, or C	1.5	8	2.6	7.5	ns
t_{PHL}			1.5	7.4	2.6	6.9	
t_{PLH}	CLK	A, B, or C	1.5	8	2.5	7.5	ns
t_{PHL}			1.5	7.2	2.5	6.7	
t_{PZH}	$\overline{OE}$	A, B, or C	0.8	6.7	1.5	6.4	ns
t_{PZL}			1.5	7.1	2.4	6.8	
t_{PHZ}	$\overline{OE}$	A, B, or C	0.8	7.2	1.5	6	ns
t_{PLZ}			0.8	6.4	1.9	6.1	

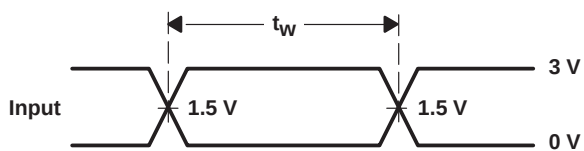
16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

SCBS179E – JUNE 1992 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION

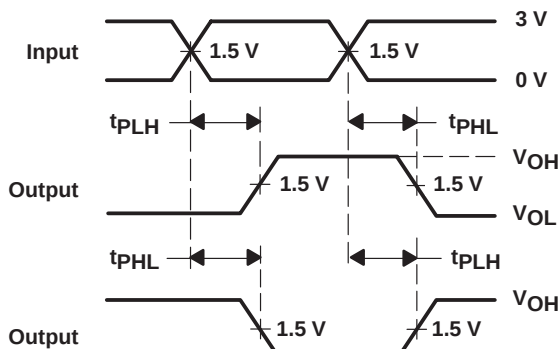


LOAD CIRCUIT



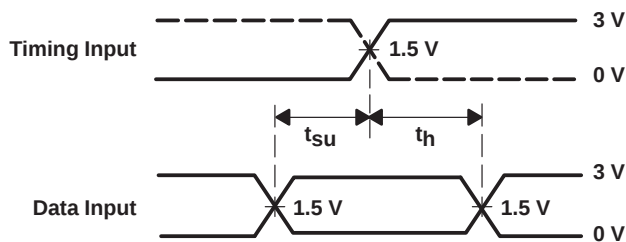
VOLTAGE WAVEFORMS

PULSE DURATION

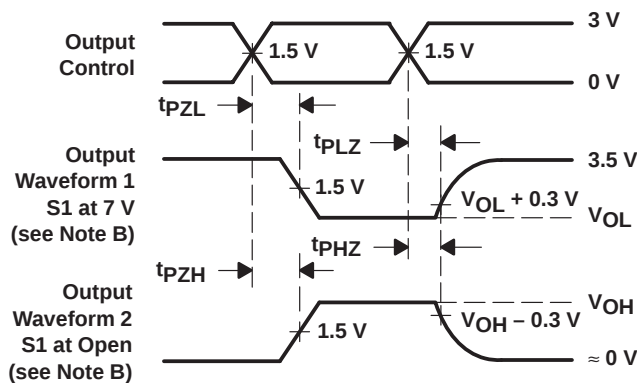


**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	7 V
tPHZ/tPZH	Open



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9680801QXA	Active	Production	CFP (HT) 84	250 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680801QX A SNJ54ABTH32316 HT
SN74ABTH32316PN	Active	Production	LQFP (PN) 80	119 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABTH32316
SN74ABTH32316PN.B	Active	Production	LQFP (PN) 80	119 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABTH32316
SNJ54ABTH32316HT	Active	Production	CFP (HT) 84	250 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9680801QX A SNJ54ABTH32316 HT

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ABTH32316, SN74ABTH32316 :

- Catalog : [SN74ABTH32316](#)
- Military : [SN54ABTH32316](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE

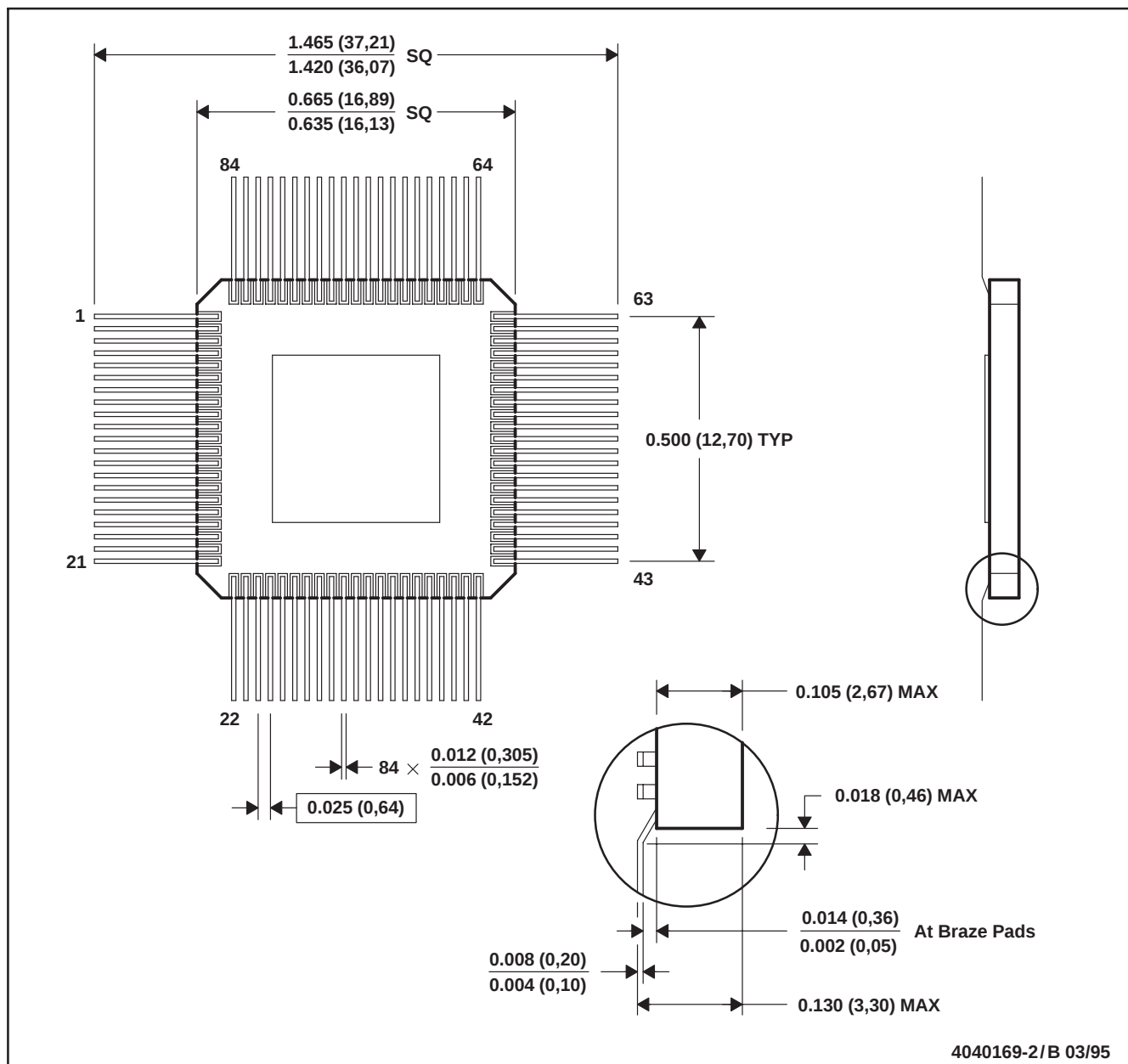


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9680801QXA	HT	CFP	84	250	506.98	17.91	12570	5.46
SNJ54ABTH32316HT	HT	CFP	84	250	506.98	17.91	12570	5.46

HT (S-CQFP-F84)

CERAMIC QUAD FLATPACK



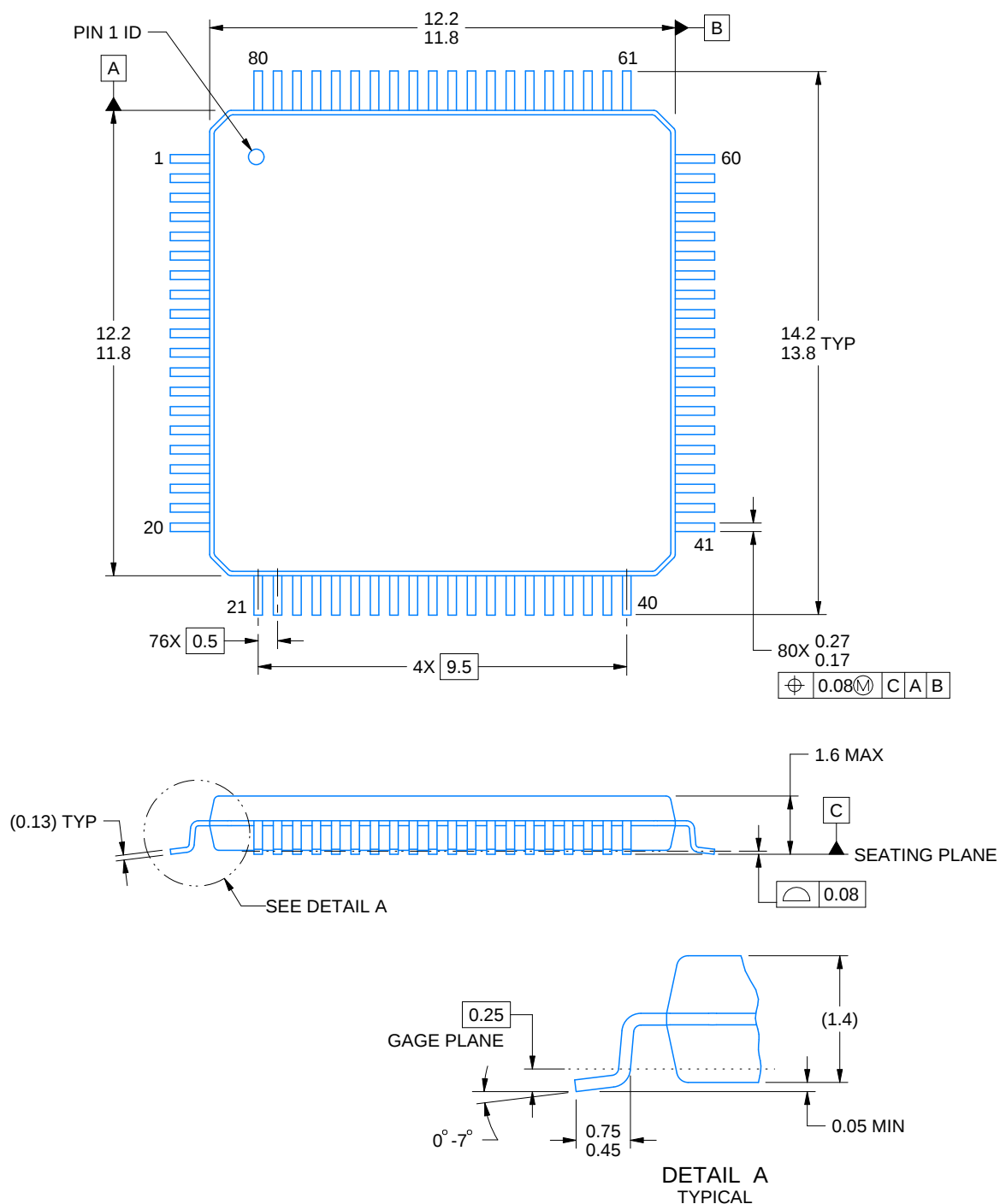
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package is hermetically sealed with a metal lid.
 D. The terminals are gold plated.
 E. Falls within JEDEC MO-090 AA



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



4215166/A 08/2022

NOTES:

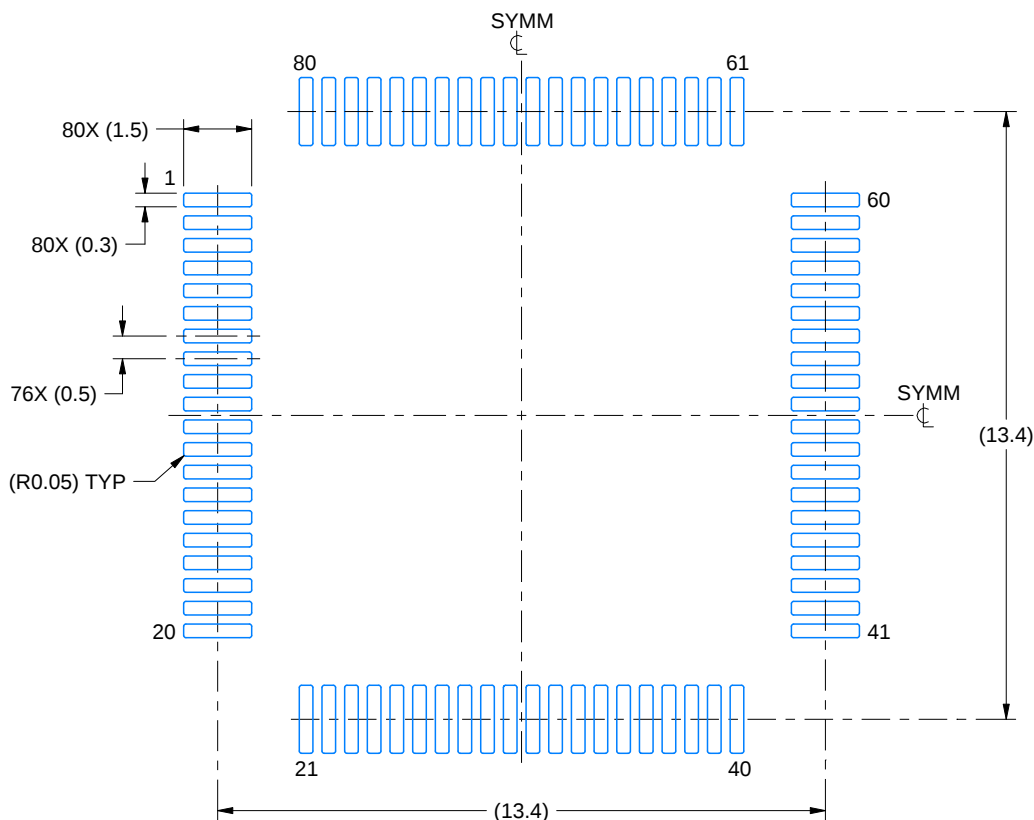
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

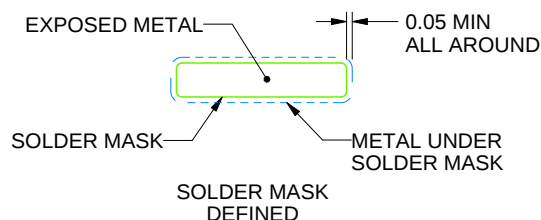
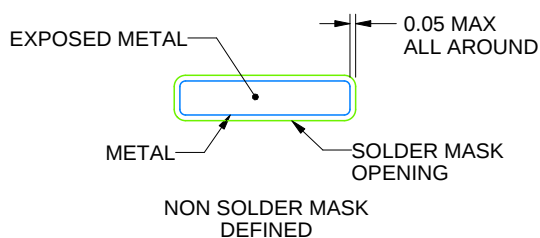
PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

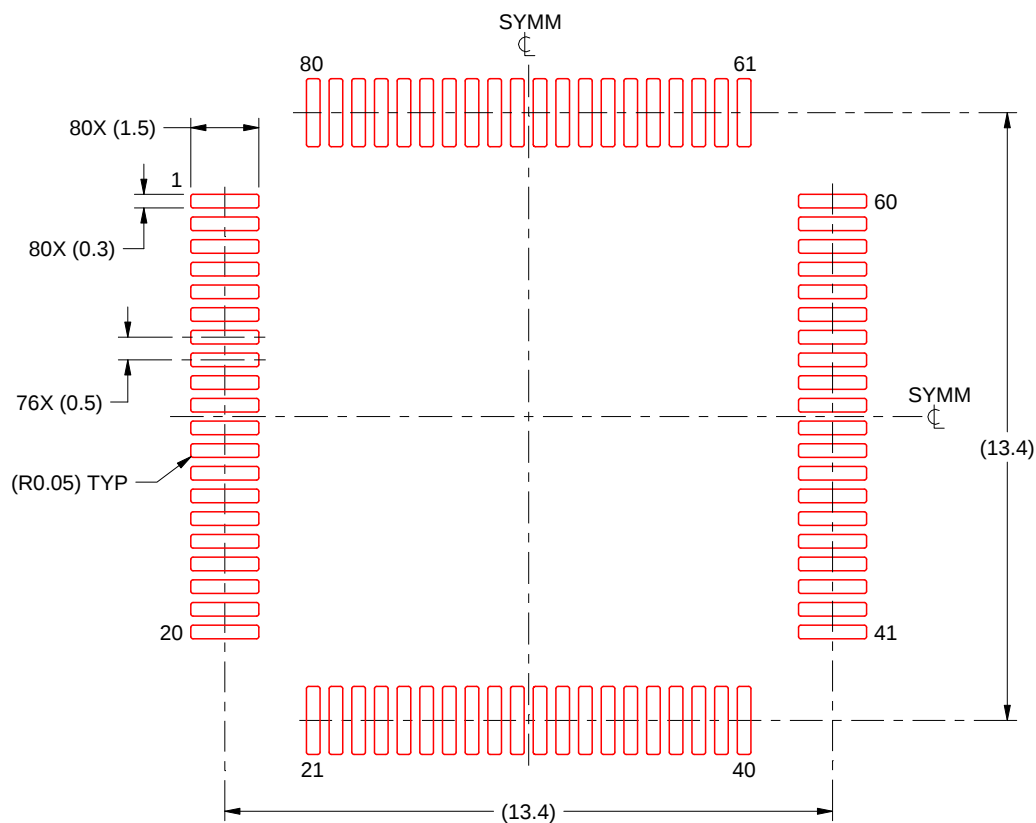
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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