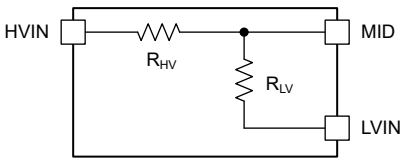
RES80A-Q1 Automotive, 2000V_{DC}, Precision Resistive Divider

1 Features

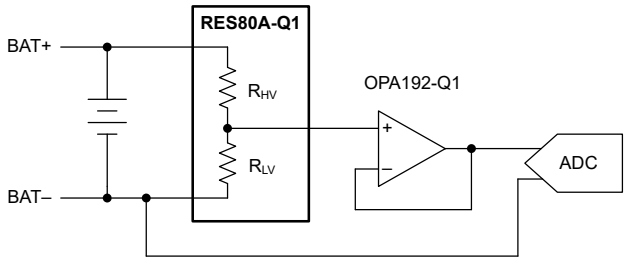
- AEC-Q200 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C
- High voltage rating:
  - Survives 3+ HiPOT tests at 4000V_{DC} (60s)
  - 1700V_{DC} creepage and clearance support between HVIN and LVIN (IEC-61010 PD 2)
    - 2000V_{DC} creepage and clearance support under Pollution Degree 1
- High dc precision with low shift and drift:
  - Initial ratio matching precision: ±0.1% (max)
  - Accurate ±0.2% across aging and temperature

2 Applications

- High-voltage bus and battery voltage monitoring
  - HEV/EV battery management system (BMS)
  - HEV/EV DC/DC converter
  - HEV/EV onboard charger (OBC)
  - HEV/EV inverter and motor control
- Nonisolated, same-ground, always-on dividers
- High common-mode range amplifiers



Functional Block Diagram



Typical Schematic

3 Description

The RES80A-Q1 is a matched resistive divider, implemented in thin-film SiCr with Texas Instruments' modern, high-performance, analog wafer process. A high quality SiO_2 insulative layer encapsulates the resistors and enables usage at extremely high voltages, up to 2000V_{DC} for sustained operation or 4000V_{DC} for HiPOT testing (60s). The device has a nominal input resistance of R_{HV} = 50MΩ, and is available in several nominal ratios to meet a wide array of system needs.

The RES80A-Q1 series features high ratio matching precision, with the measured ratio of each divider within ±0.1% (max) of the nominal. This precision is maintained over the specified temperature range and aging, with a cumulative drift of only ±0.2% (max). Therefore, the lifetime tolerance of an uncalibrated RES80A-Q1 remains within a ±0.3% (max) envelope.

The RES80A-Q1 is automotive qualified under AEC-Q200 temperature grade 1, with a specified temperature range from –40°C to +125°C. The device is offered in an 8-pin SOIC package, with nominal body size 7.5mm × 5.85mm, and features creepage and clearance distances of at least 8.5mm between the high-voltage and low-voltage pins.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
RES80A-Q1	DWV (SOIC, 8)	5.85mm × 11.5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	NOMINAL RATIO (R_{HV}:R_{LV})
RES80A145-Q1	145:1
RES80A210-Q1(1)	210:1
RES80A250-Q1(1)	250:1
RES80A315-Q1(1)	315:1
RES80A410-Q1(1)	410:1
RES80A500-Q1(1)	500:1
RES80A610-Q1(1)	610:1
RES80A100-Q1	1000:1

(1) Preview information (not Advanced Information).

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4 Pin Configuration and Functions

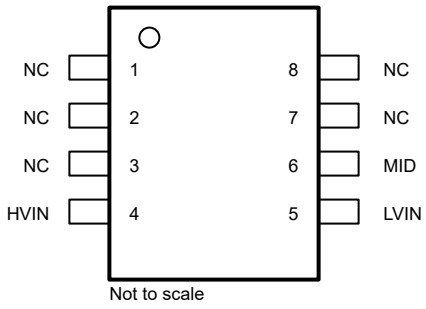


Figure 4-1. DWV Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
HVIN	4	Input	High-voltage input of divider
LVIN	5	Input	Low-voltage input of divider
MID	6	Output	Center tap of divider
NC	1, 2, 3	—	Noninternally-connected pins on high-voltage side. Solder to the PCB for best board-level reliability. The exposed metal area of these pins must be considered as part of any creepage and clearance calculations.
NC	7, 8	—	Noninternally-connected pins on low-voltage side. Solder to the PCB for best board-level reliability. The exposed metal area of these pins must be considered as part of any creepage and clearance calculations.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Maximum short-term overload voltage per divider, $V_D = V_{HVIN} – V_{LVIN}$ (100ms, T_A = 25°C, DWV package)(2)(3)	RES80A145	–2700	2700	V
		RES80A210	–2700	2700	
		RES80A250	–2700	2700	
		RES80A315	–2700	2700	
		RES80A410	–2700	2700	
		RES80A500	–2700	2700	
		RES80A610	–2700	2700	
		RES80A100	–2700	2700	
	Transient high-potential voltage, ac (50Hz, T_A = 25°C, DWV package)(4)(5)(6)	RES80A145	–3000	3000	V_{RMS}
		RES80A210	–3000	3000	
		RES80A250	–3000	3000	
		RES80A315	–3000	3000	
		RES80A410	–3000	3000	
		RES80A500	–3000	3000	
		RES80A610	–3000	3000	
		RES80A100	–3000	3000	
	Transient high-potential voltage, dc (T_A = 25°C, DWV package)(4)(5)(6)	RES80A145	–4000	4000	V_{DC}
		RES80A210	–4000	4000	
		RES80A250	–4000	4000	
		RES80A315	–4000	4000	
		RES80A410	–4000	4000	
		RES80A500	–4000	4000	
		RES80A610	–4000	4000	
		RES80A100	–4000	4000	
T_A	Ambient temperature		–55	150	°C
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	175	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Maximum short-term voltage permitted under transient conditions without performance degradation. Avoid sustained operation at or beyond these voltage levels, especially if the resulting self-heating causes T_J to exceed 150°C.
(3) Tested in production, with ±2.7kV stress for 100ms, on each device.
(4) Differential voltage from high-voltage domain (pins 1-4) to low-voltage domain (pins 5-8) of the package.
(5) Total stress duration of 180s, accumulated over lifetime in increments of no longer than 60s periods, with duty cycle ≤ 20%. For example, after 60s of continuous stress, wait 240s for device temperature to settle before repeating the stress. Repeated transient high-potential voltage testing can lead to performance degradation or device damage.
(6) Rating for Advanced-Information and preview devices only. Final value for Production-Data devices is pending.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q200-002, all pins except 5 and 6	±4000	V
		Human body model (HBM), per AEC Q200-002, pins 5 and 6	±2000	

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Maximum sustained unipolar voltage per divider (DWV package, HVIN pin to LVIN pin, 10 years at T_A = 25°C)(1)(2)	RES80A145	–2000		2000	V_{DC}
		RES80A210	–2000		2000	
		RES80A250	–2000		2000	
		RES80A315	–2000		2000	
		RES80A410	–2000		2000	
		RES80A500	–2000		2000	
		RES80A610	–2000		2000	
		RES80A100	–2000		2000	
	Maximum sustained 50Hz ac bipolar voltage per divider (DWV package, HVIN pin to LVIN pin, 10 years at T_A = 25°C)(1)(2)	RES80A145	–440		440	V_{RMS}
		RES80A210	–440		440	
		RES80A250	–440		440	
		RES80A315	–440		440	
		RES80A410	–440		440	
		RES80A500	–440		440	
		RES80A610	–440		440	
		RES80A100	–440		440	
T_A	Ambient temperature		–40		125	°C

(1) Assumes $R_{\theta JA}$ = 112.4°C/W.
(2) For more information on unipolar vs bipolar bias conditions and their impact on device reliability, refer to *Time-Dependent Dielectric Breakdown*.

5.4 Thermal Information

THERMAL METRIC(1)		RES80A-Q1 DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	40.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics

at V_D = 1000V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INITIAL RESISTANCE							
R_{HV}	Input resistance				50		MΩ
R_{LV}	Ratio-dependent resistance[1]	RES80A145			344.8		kΩ
		RES80A210			238.1		
		RES80A250			200.0		
		RES80A315			158.7		
		RES80A410			122.0		
		RES80A500			100.0		
		RES80A610			82.0		
		RES80A100			50.0		
G_{nom}	Nominal ratio	R_{HV} / R_{LV}	RES80A145		145		
			RES80A210		210		
			RES80A250		250		
			RES80A315		315		
			RES80A410		410		
			RES80A500		500		
			RES80A610		610		
			RES80A100		1000		
t_D	Initial ratio tolerance[2]	V_D = 250V to V_D = 1000V, (R_{HV} / R_{LV}) / G_{nom} – 1[3]	RES80A145	–0.1	±0.020	0.1	%
			RES80A210	–0.1		0.1	
			RES80A250	–0.1		0.1	
			RES80A315	–0.1		0.1	
			RES80A410	–0.1		0.1	
			RES80A500	–0.1		0.1	
			RES80A610	–0.1		0.1	
			RES80A100	–0.1	±0.049	0.1	
t_{abs}	Absolute tolerance (per resistor)[5]	(R_x / R_{xnom}) – 1[3]		–15	–2.5	15	%
	Absolute tolerance span	MAX(t_{absRHV}, t_{absRLV}) – MIN(t_{absRHV}, t_{absRLV})			TBD		%
RESISTANCE DRIFT							
	Ratio tolerance drift across operating lifetime[4]	10 years continuous, T_A = –40°C to +85°C, unipolar bias, V_D = 1500V, ($G_{INITIAL}$ – G_{FINAL}) / $G_{INITIAL}$[3]		–0.2	±0.02	0.2	%
TCR_{abs}	Absolute temperature coefficient of resistance (per resistor)[5][6]	(ΔR_x / $R_{x(25°C)}$) / ΔT_A, T_A = –40°C to +125°C			TBD		ppm/°C
TCR_{ratio}	Divider temperature coefficient of resistance (per divider)[2][6]	Δt_D / ΔT_A, T_A = –40°C to +85°C		–5	TBD	5	ppm/°C
		Δt_D / ΔT_A, T_A = –40°C to +125°C		–5	TBD	5	ppm/°C
VCR_{abs}	Absolute voltage coefficient of resistance (per resistor)[5][6]	ΔR_x / ΔV_{Rx}, V_D = 100V to V_D = 1000V	R_{HV}		TBD		Ω/V
			R_{LV}		TBD		Ω/V
VCR_{ratio}	Divider voltage coefficient of resistance (per divider)[2][6]	Δt_D / ΔV_D, V_D = 100V to V_D = 1000V			±0.05		ppm/V
IMPEDANCE							
C_{IN}	Pin capacitance[6][7]	HVIN, V_{LVIN} = V_{MID} = 0V			TBD		pF
		MID, V_{LVIN} = V_{HIN} = 0V			TBD		
		LVIN, V_{MID} = V_{HIN} = 0V			TBD		

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at V_D = 1000V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	–3dB bandwidth[6][8]	Normalized to attenuation at f = 100Hz, no C_{FILTER}	RES80A145		TBD		kHz
			RES80A210		TBD		
			RES80A250		TBD		
			RES80A315		TBD		
			RES80A410		TBD		
			RES80A500		TBD		
			RES80A610		TBD		
			RES80A100		TBD		
t_s	Settling time[6]	To 1%, 10V step	RES80A145		TBD		µs
			RES80A210		TBD		
			RES80A250		TBD		
			RES80A315		TBD		
			RES80A410		TBD		
			RES80A500		TBD		
			RES80A610		TBD		
			RES80A100		TBD		
		To 0.1%, 10V step	RES80A145		TBD		µs
			RES80A210		TBD		
			RES80A250		TBD		
			RES80A315		TBD		
			RES80A410		TBD		
			RES80A500		TBD		
			RES80A610		TBD		
			RES80A100		TBD		
e_N	Thermal noise density[7]	f = 1kHz	RES80A145		72.5		nV/√Hz
			RES80A210		60.3		
			RES80A250		55.3		
			RES80A315		49.3		
			RES80A410		43.2		
			RES80A500		39.1		
			RES80A610		35.4		
			RES80A100		27.7		

(1) Input resistance (R_{HV}) and nominal ratio (G_{nom}) are the controlling specifications that dictate the values of R_{LV}. Nominal values of R_{LV} are reported with three significant figures for convenience.
(2) R_{HV} / R_{LV} vs nominal ratio.
(3) The specification is the result of this expression, given as a percentage (multiplied by 100%)
(4) Specified by design and accelerated qualification testing.
(5) R_{HV} and R_{LV} vs nominal values.
(6) Specified by characterization.
(7) Specified by design.
(8) The –3dB bandwidth for a given device and application is heavily influenced by parasitic device-level and board-level capacitances. Feed-forward capacitances cause attenuation at high frequencies to fall below nominal values, resulting in gain peaking. Use a filtering capacitor in parallel with R_{LV} for gain shaping and confirm attenuation across frequency meets circuit and design goals. The value of this capacitor is best determined and verified experimentally. Refer to *Additional Protection* and *Layout Guidelines* for additional information.

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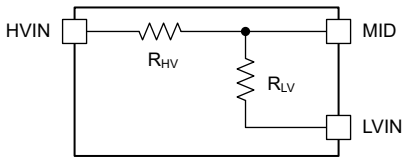
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6 Detailed Description

6.1 Overview

The RES80A-Q1 consists of two, precision, thin-film SiCr resistors, arranged to form a matched divider and encapsulated by an insulative SiO_2 layer. The device contains an *input* resistor, R_{HV}, that is nominally 50MΩ. The device also incorporates a *gain* resistor, R_{LV}, with a value that depends on the nominal ratio (R_{HV} / R_{LV}) of the RES80A-Q1.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Ratiometric Matching

The resistors of the RES80A-Q1 are described by the following two equations:

$$R_{HV} = R_{HVnom} \times (1 \pm t_{abs}) = R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr}) \quad (1)$$

$$R_{LV} = R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr}) \quad (2)$$

where

- R_{HVnom} and R_{LVnom} are the nominal values of each resistor.
- t_{abs} is an error term that describes the absolute tolerance of the resistors of the RES80A-Q1, such that $|t_{abs}| \leq 15\%$.
- t_{SiCr} is the variation in the SiCr resistivity for a wafer, and dominates the absolute tolerance for a given resistor. The two resistors of a given RES80A-Q1 are interdigitated and come from the same area of the wafer; therefore, t_{SiCr} is effectively the same for both of the two resistors, although t_{SiCr} varies on a part-to-part basis. When the divider is considered in ratiometric terms, these error terms drop out; see the following equations.
- t_{RHV} and t_{RLV} are localized per-resistor variation or offset error terms. These terms describe the remaining effective tolerances of the respective resistors for a given RES80A-Q1 device, after accounting for the universal t_{SiCr}.

$$\frac{R_{HV}}{R_{LV}} = \frac{R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})}{R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr})} = \frac{R_{HVnom} \times (1 \pm t_{RHV})}{R_{LVnom} \times (1 \pm t_{RLV})} = G_{nom} \times \frac{(1 \pm t_{RHV})}{(1 \pm t_{RLV})} = G \quad (3)$$

$$\frac{R_{HV}}{R_{LV} + R_{HV}} = \frac{R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})}{R_{LVnom} \times (1 \pm t_{RLV}) \times (1 \pm t_{SiCr}) + R_{HVnom} \times (1 \pm t_{RHV}) \times (1 \pm t_{SiCr})} = \frac{R_{HVnom} \times (1 \pm t_{RHV})}{R_{LVnom} \times (1 \pm t_{RLV}) + R_{HVnom} \times (1 \pm t_{RHV})} \quad (4)$$

The RES80A-Q1 is specified with a maximum initial divider ratio tolerance of 0.1%, meaning that the relationship between the actual divider ratio, G, and the nominal ratio, G_{nom}, of a given divider is described by the following:

$$G = G_{nom} \times (1 \pm t_D) \quad (5)$$

such that $t_D \leq 0.1\%$. Because any devices that do not meet these criteria are screened out at final test, these equations can be used with the previous equations to prove the effective bounds of t_{RHV} and t_{RLV}. Therefore, despite the device absolute end-to-end tolerance bounds of ±15%, the effective error tolerances of each resistor (for ratiometric applications) are within approximately ±0.115%, for the worst-case t_{RHV} and t_{RIV}.

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6.3.2 Ultra-Low Noise

Noise in resistors can be evaluated in two separate regions: low-frequency flicker noise and wideband thermal noise. Flicker, or 1/f noise, is extremely important for systems that require signal gain at frequencies less that 100Hz. The flicker noise for thin-film resistors, including the RES80A-Q1, is lower than that of thick-film resistor processes. Thermal noise typically dominates in the region greater than 1kHz, and increases as resistor magnitude increases. Noise is modeled as a voltage source in series with the resistor.

For a resistive divider such as the RES80A-Q1, the thermal noise as measured at the center tap of two resistors R_{HV} and R_{LV} is equivalent to the thermal noise of a resistor with value $R_{HV} \parallel R_{LV}$:

$$e_N = \sqrt{(4k_B TR)} \tag{6}$$

where:

- e_N is the thermal noise density in nV/√Hz
- T is the absolute temperature in kelvins (K)
- k_B is the Boltzmann constant, 1.381 × 10-23 J/K
- $R = R_{HV} \parallel R_{LV}$

$R_{HV} >> R_{LV}$; therefore, $R \approx R_{LV}$. As an example, for the RES80A610-Q1:

$$e_N = \sqrt{(4k_B TR)} = \sqrt{4 \times 1.38E^{-23} \frac{J}{K} \times 278K \times (50M\Omega \parallel 81.97k\Omega)} = 35.4nV/\sqrt{Hz} \tag{7}$$

6.4 Device Functional Modes

The RES80A-Q1 features a single pad for the HVIN pin and two pads for the MID and LVIN pins, with all other pads and pins electrically floating. Connect both the MID and LVIN pins to the *low-voltage domain* of the system, such as a microcontroller ADC input and chassis ground, respectively. Bias the HVIN pin to the high potential of the measured system, such as the high side of the battery stack.

HVIN and LVIN can be used to measure directly between the high side and low side of the battery. However, to avoid an overvoltage condition, verify that the downstream circuitry driven by MID is properly referenced to the low side (LVIN).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Battery Stack Measurement

The RES80A-Q1 can be used in conjunction with an automotive precision amplifier, such as the OPA192-Q1, for single-ended measurement of the high side (BAT+) of an EV battery relative to a fixed potential. For those systems where BAT– and GND are equivalent, as in Figure 7-1 (a), the configuration shown in Figure 7-2 applies. An alternative approach is to measure directly across the battery from BAT+ to BAT–, as shown in Figure 7-3. This approach is useful for systems referenced to the low side of the battery, BAT–, as in Figure 7-1 (b).

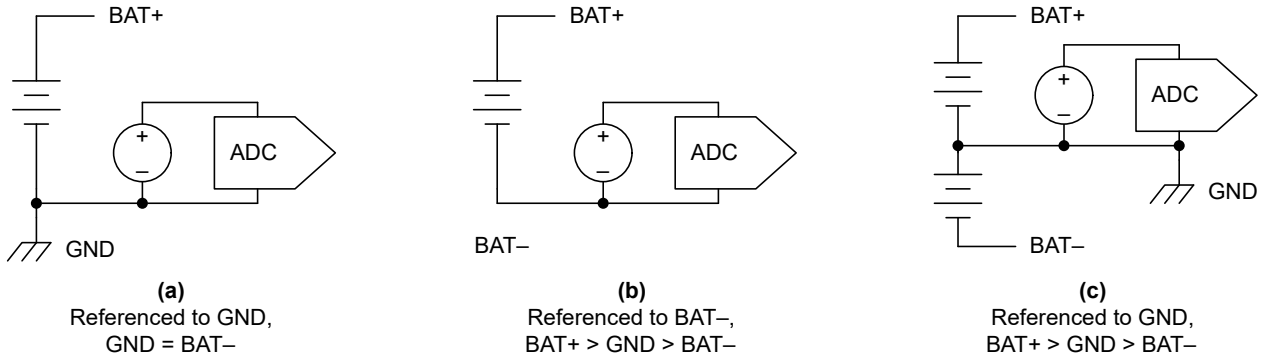


Figure 7-1. Common Battery and System Configurations

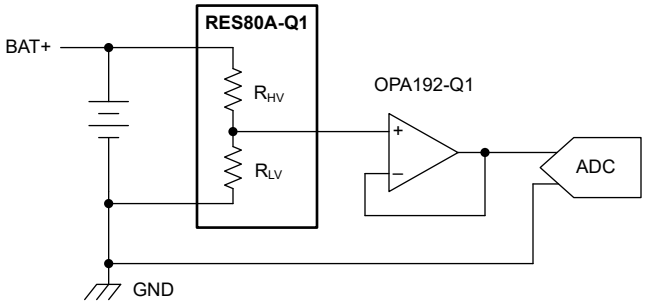


Figure 7-2. Single-Ended Measurement, BAT+ to GND

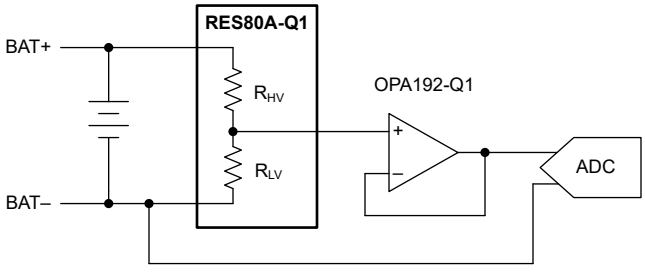


Figure 7-3. Single-Ended Measurement, BAT+ to BAT–

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For some system architectures, BAT– floats relative to the chassis GND; see also Figure 7-1 (c). If for example a microcontroller referenced to chassis ground needs to measure the voltage across the entire battery stack, a difference amplifier can be constructed using two RES80A-Q1 devices and an OPA192-Q1. Figure 7-4 shows this approach. If two ADC channels are available, two single-ended measurements can be done using two RES80A-Q1 devices and an OPA2192-Q1.

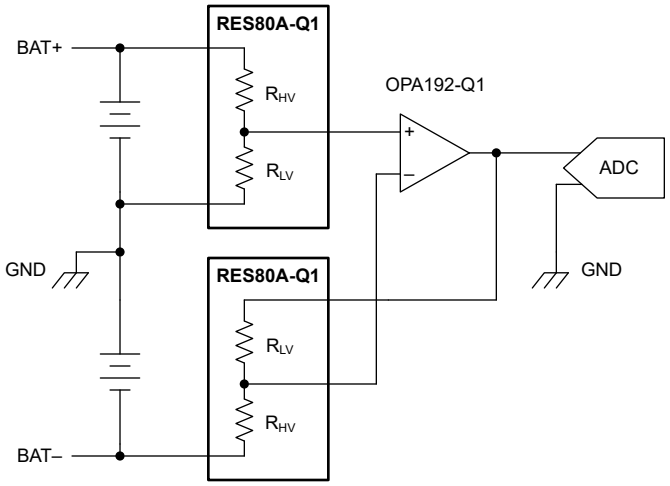


Figure 7-4. Differential Measurement, BAT+ to BAT–

Leakage in the system and quiescent current from the amplifier input reduce the precision of the measurement. In some cases, a guard buffer can be used to reduce leakage currents. Follow best practices to reduce board contamination and leakage.

For an example 800V single-ended battery measurement with RES80A500-Q1 (see also Figure 7-2), the static current through the divider is:

$$I_{STATIC} = \frac{V_{BATT}}{(R_{HV} + R_{LV})} = \frac{800V}{(50M\Omega + 100k\Omega)} = 16\mu A \quad (8)$$

Therefore, the buffer amplifier used must have a low bias current, such that $I_B << I_{STATIC}$. The low bias current of the OPA192-Q1 (5pA typical at 25°C, 5nA maximum from –40°C to +125°C) makes the device an excellent choice for this role.

7.1.2 Voltage Divider Circuit

The RES80A-Q1 is typically used to divide down a high potential to within the input full-scale range of an ADC or op-amp. This voltage divider circuit is generically drawn in the following figure.

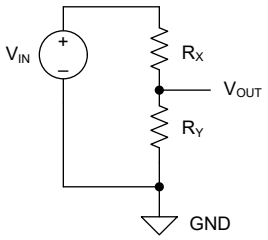


Figure 7-5. Generic Voltage Divider Circuit

$$G_{VD} = \frac{R_Y}{R_Y + R_X} \quad (9)$$

$$V_{OUT} = V_{IN} \times G_{VD} \quad (10)$$

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$$G_{VD} = G_{VD_{nom}}(1 + t_{VD}) \quad (11)$$

For the RES80A-Q1, R_{HV} and R_{LV} act as R_X and R_Y respectively in this circuit. Substituting these terms gives a transfer function of:

$$G_{VD} = \frac{R_{LV}}{R_{LV} + R_{HV}} = \frac{1}{G + 1} \quad (12)$$

Because G_{VD} is a direct function of G, the ratio tolerance error t_{VD} of these voltage-divider circuits is a direct function of t_D. Typical and maximum parameter values for t_{VD} in this configuration are calculated from a given t_D value as follows:

$$t_{VD} = \frac{-G_{nom} \times t_D}{G_{nom} \times t_D + G_{nom} + 1} \quad (13)$$

For example, if a RES80A210-Q1 with t_D = 0.0290% is used in this configuration, the associated t_{VD} error is –0.0288% (288ppm).

$$t_{VD} = \frac{-G_{nom} \times t_D}{G_{nom} \times t_D + G_{nom} + 1} = \frac{-210 \times 0.00029}{210 \times 0.00029 + 210 + 1} \quad (14)$$

The sign change occurs because a positive t_{Dx} error means $R_{HV} > R_{HVnom}$ or $R_{LV} < R_{LVnom}$. Since the resulting G_{VD} is less than the nominal value, the error term is negative. Due to the high ratiometric gain *G* of each RES80A-Q1, t_{VD} is found to be approximately equal in magnitude to t_D; specifically, the magnitude of t_{VD} is always slightly less than that of t_D. To be conservative and simplify calculations, t_D can be used directly for basic circuit error analysis. For more detailed calculations and error analysis, utilize the *HV RES Error Calculator*.

7.1.2.1 Voltage-Divider Circuit Drift

As discussed in Section 7.1.2, the voltage-divider circuit error t_{VD} of the RES80A-Q1 is related to the gain-circuit error t_D by the following expression:

$$G_{VDx} = \frac{R_{IN}}{R_{IN} + R_G} = G_{VD_{nom}}(1 + t_{VD}) \rightarrow t_{VD} = \frac{-G_{nom} \times t_D}{G_{nom} \times t_D + G_{nom} + 1} \quad (15)$$

Therefore, the change in the voltage divider transfer function G_{VD} with temperature is a direct function of the change in t_D with temperature. Multiplying the temperature coefficient TCR_{ratio} by the change in ambient temperature gives the change in t_D, which is in turn substituted in the appropriate equation to calculate the change in t_{VD}. The change in t_{VD} directly describes the change in G_{VD}.

As an example, consider a RES80A210-Q1 with G_{nom} = 210 and a circuit configuration as shown in Figure 7-5, with $R_X = R_{HV}$ and $R_Y = R_{LV}$. Assume t_D is initially 0.0290% and increases by 15ppm due to a 30°C increase in ambient temperature. The initial value of t_{VD}, before the temperature change, is calculated as:

$$t_{VD} = \frac{-G_{nom} \times t_D}{G_{nom} \times t_D + G_{nom} + 1} = \frac{-210 \times 0.00029}{210 \times 0.00029 + 210 + 1} = -0.000288 = -288\text{ppm} \quad (16)$$

The new value of t_{VD} after the temperature change is calculated as:

$$t_{VD} = \frac{-G_{nom} \times t_D}{G_{nom} \times t_D + G_{nom} + 1} = \frac{-210 \times 0.000305}{210 \times 0.000305 + 210 + 1} = -0.000303 = -303\text{ppm} \quad (17)$$

In this scenario, the shift in t_D of 15ppm causes a shift in t_{VD} of approximately –15ppm. Once again, to simplify calculations, TCR_{ratio} can be used directly with t_D for basic circuit error analysis. The *HV RES Error Calculator* is useful for more complex error analysis across temperature and voltage stresses.

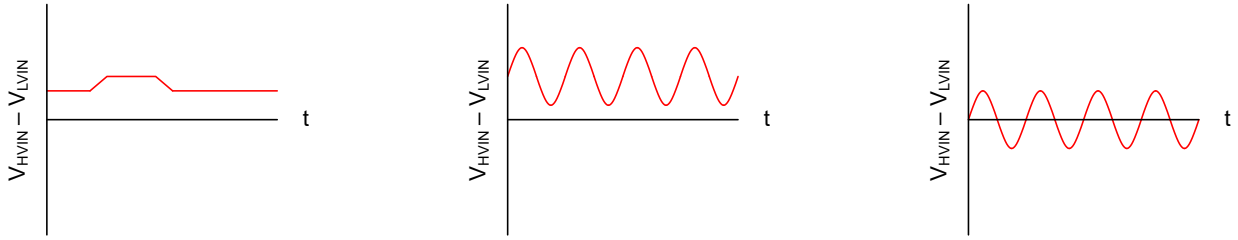
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7.1.3 Time-Dependent Dielectric Breakdown

The thin-film SiCr, SiO_2-insulated, analog wafer process used for the RES80A-Q1 has been intrinsically qualified for sustained high-voltage operation through Time-Dependent Dielectric Breakdown (TDDB) testing. TDDB is performed by stressing dedicated test structures at a constant high ac or dc voltage for a long duration, until the devices wear out and fail by electrical short. By testing TDDB at multiple voltages, the process lifetime at a given working voltage is determined by extrapolation using the Weibull method. TDDB testing has shown two different biasing conditions, *unipolar* signals and *bipolar* signals, result in differing operational lifetimes for the process and thus for the RES80A-Q1. The characteristics of the bias or input signals must therefore be considered as part of device reliability analysis.



(a) Dynamic dc bias, Unipolar signal

(b) Dynamic ac bias, Unipolar signal

(c) Dynamic ac bias, Bipolar signal

Figure 7-6. Examples of Unipolar and Bipolar Bias for RES80A-Q1

In *unipolar* use cases, the voltage at the input of the RES80A-Q1 (V_{HVIN}) is consistently at a potential either above or below the substrate voltage, V_{LVIN}. For most dc measurement applications, such as EV battery stack measurements, either $V_{HVIN} > V_{LVIN}$ or $V_{HVIN} < V_{LVIN}$ on a consistent basis. Many time-varying signals, such as battery voltages that shift over time or motor phase voltage measurements relative to BAT–, also are considered unipolar as long as V_{HVIN} does not *cross* above or below V_{LVIN} in typical operation. Unipolar operation is therefore associated with a uniform *direction* of the magnetic field between the device input and substrate, even if the *magnitude* of the field can vary with time. Unipolar operation results in the longest operating lifetime and lowest modeled defect rate, and is the most common use case for the RES80A-Q1. For continuous unipolar operation, the maximum recommended operating voltage of the RES80A-Q1 is 2000Vdc.

In *bipolar* use cases, voltage at the input of the RES80A-Q1 (V_{HVIN}) repeatedly crosses or swings above and below the substrate voltage, V_{LVIN}. As the polarity from V_{HVIN} to V_{LVIN} is reversed, the change in direction of the electric field stresses the device substrate and leads to a different wearout mechanism when compared to unipolar operation (where the electric field direction is consistent). Examples of bipolar measurements include ac mains voltage line measurements relative to a fixed neutral potential, or some split-pack architectures where BAT– < V_{LVIN} < BAT+ and the HVIN pin of a *single* RES80A-Q1 is switched between BAT+ and BAT– *rapidly*. For continuous bipolar operation, the maximum recommended operating voltage of the RES80A-Q1 is 440Vrms.

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7.2 Typical Application

The RES80A-Q1 can be configured with an isolated amplifier such as the AMC1311B-Q1 for measurements requiring reinforced isolation. Figure 7-7 shows an example circuit configuration for such an application, where the RES80A-Q1 attenuates the input voltage and the AMC1311B-Q1 crosses the isolation barrier. A discrete difference amplifier with RES11A-Q1 and OPA388-Q1 is used to adapt the differential output voltage of the AMC1311B-Q1 for use with a single-ended 5V ADC.

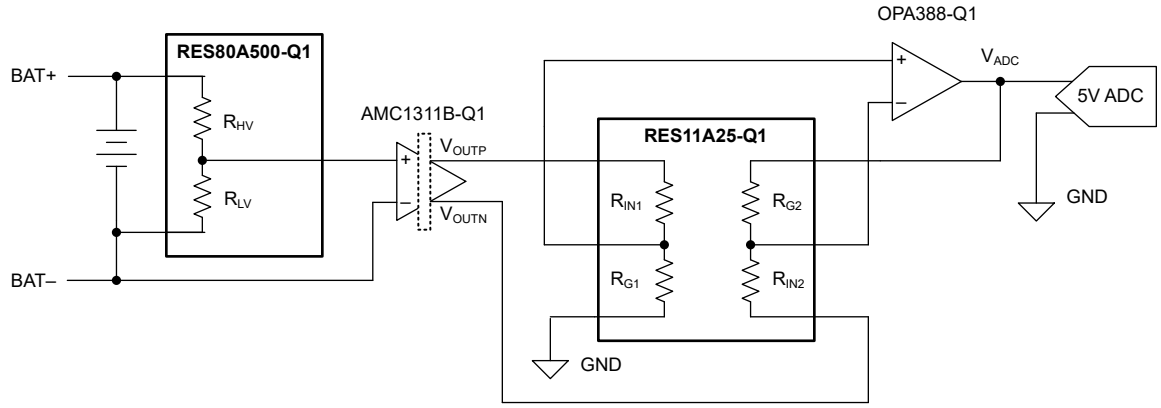


Figure 7-7. DC Bus Measurement With the RES80A-Q1 and AMC1311B-Q1

7.2.1 Design Requirements

PARAMETER	DESIGN GOAL
DC bus voltage range	0V to 1000V
Output (V_{ADC}) full-scale range	0V to 5V
Attenuation (nominal ratio)	500:1
Uncalibrated initial measurement error	±0.5% FSR

7.2.2 Detailed Design Procedure

This design attenuates the high common-mode voltage of the bus to a level that falls within the linear input range of the AMC1311B-Q1. Some key possible circuit error sources can be considered as follows:

- The AMC1311B-Q1 has a typical input bias current of 3.5nA. With R_{LV} = 100kΩ, this input bias current manifests appears as an 350µV offset error at MID. When this offset is calculated in a root-sum-of-squares with the 400µV typical input offset voltage of the AMC1311B-Q1, a 532µV offset results. This offset represents 0.0266% of the 2V full-scale range, and is typically not the dominating error factor.
- The gain error and integrated nonlinearity error of the AMC1311B-Q1 can be approximated using the Isolated Amplifier Voltage Sensing Excel Calculator. For this example, the typical FSR error is calculated as 0.07%.
- The anticipated typical initial ratiometric gain tolerance of the RES80A500-Q1 is approximately 0.02%, which sums with the previously mentioned errors of the AMC1311B-Q1 in a root-sum-of-squares manner to give a total typical FSR error of 0.078%.
- The level-shifting circuit introduces additional errors, and applies a gain factor to the previously discussed errors. However, due to the low offset of the OPA388-Q1 and high precision of the RES11A-Q1, these additional errors (0.014% FSR) are low enough to not significantly impact the final typical error. Because the errors and the full-scale range are both scaled by 2.5 in this stage, the effective error as a percentage of the full-scale range remains the same.

The final calculated result of 0.079% typical FSR error represents a 1σ value, so a ±6σ estimate gives ±0.473% FSR error. The results suggest the circuit meets the ±0.5% FSR application requirement, with margin.

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7.2.3 Application Curves

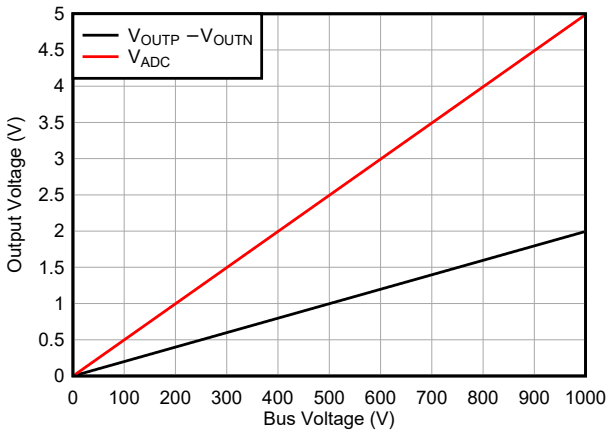


Figure 7-8. Transfer Function

7.3 Power Supply Recommendations

The RES80A-Q1 is a high-voltage resistor divider, with no active circuitry or protective diodes. There are no specific power-supply connection requirements other than respecting the limits expressed in *Absolute Maximum Ratings* and *Recommended Operating Conditions*.

7.3.1 Additional Protection

While optional, external circuit components can be used to extend the robustness of the RES80A-Q1 and further protect sensitive downstream circuitry.

- To provide additional margin against high-edge-rate transient events, such as in applications requiring extremely high ESD ratings, consider implementating a high-voltage bypass capacitor or capacitor string at the device input. This parallel path acts to shunt the high-frequency signal and bypass the RES80A-Q1, dissipating the surge energy outside the device, without impacting the dc and low-frequency precision of the device. Refer to *Layout Examples* for implementation.
  - Verify that creepage and clearance requirements are respected, and be aware that additional input capacitance can extend system step-response settling times.
  - Testing of an input protection network consisting of a ferrite bead and three 2000V, X7R bypass capacitors in series has been shown to extend ESD pass levels to more than ±12kV; refer to the *RES60A-Q1 Extended Reliability Testing* application note.
  - In some systems *upstream* capacitances such as Class-X or Class-Y capacitors, or even the stacked cells of a battery pack, fill this role and inherently provide some degree of additional protection. Select and validate the protective scheme according to the application requirements.
- During HIPOT testing and at peak input voltages, the RES80A-Q1 continues to act as a resistive divider while the high-voltage stress is applied, so the voltage at the MID pin rises accordingly. Verify that all downstream circuitry at and after MID is properly clamped with protective diodes (such as Schottky diodes) or is rated to withstand the associated voltage rise.
  - A TVS diode, such as TSD05C, between the MID and LVIN pins provides additional clamping protection against fast transients for downstream low-voltage circuitry, if necessary. Refer to the *System-Level ESD Protection Guide* and *ESD Protection Layout Guide* application notes for additional information.
- A deliberate filtering or compensation capacitor C_{FILTER} in parallel with R_{LV} permits gain-shaping at high frequency according to circuit or application needs, and helps to protect downstream circuitry from fast transients. While use of a large C_{FILTER} value causes high-frequency noise to be strongly attenuated, if C_{FILTER} is excessively large the step response of the device is slowed.
  - Parasitic board capacitances also add with C_{FILTER}, possibly resulting in a larger effective C_{LV} than intended. Therefore, choose a value of C_{FILTER} based on the application requirements, and use the final printed circuit board implementation to verify the device performance meets design goals.

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7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Reduce parasitic coupling by running sensitive traces, such as the MID connection, as far away from supply lines or noise sources as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Power dissipated in the RES80A-Q1 causes the junction temperature to rise. For reliable operation, junction temperature must be limited to 150°C, maximum. Maintaining a lower junction temperature results in higher reliability.
  - Package thermal resistance, $R_{\theta JA}$, is affected by mounting techniques and environments. Poor air circulation can significantly increase thermal resistance to the ambient environment. Best thermal performance is achieved by soldering the RES80A-Q1 onto a circuit board with wide printed circuit traces, especially for the LVIN connection, to allow greater conduction through the device leads.
- Use groove cutting to achieve an improved PCB creepage distance. For grooves wider than 1mm, the effective creepage distance is the existing creepage distance plus the width of the groove and twice the depth of the groove. This sum must equal or exceed the required creepage distance. The groove must not weaken the substrate to the point of failure to meet mechanical test requirements. All layers under the groove must be free from traces, vias, and pads to maintain the maximum creepage distance.
- Clean the PCB after board assembly for best performance. Residual flux can create parasitic leakage paths and reduce effective creepage distances.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process.
  - A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.
- Use conformal coating or potting, the deposition of an insulating polymer or other material layer over an assembled PCB, to further improve the pollution degree around the RES80A-Q1. This process reduces the requirements for creepage and clearance distances by eliminating or reducing the influence of pollutants.

7.4.2 Layout Example

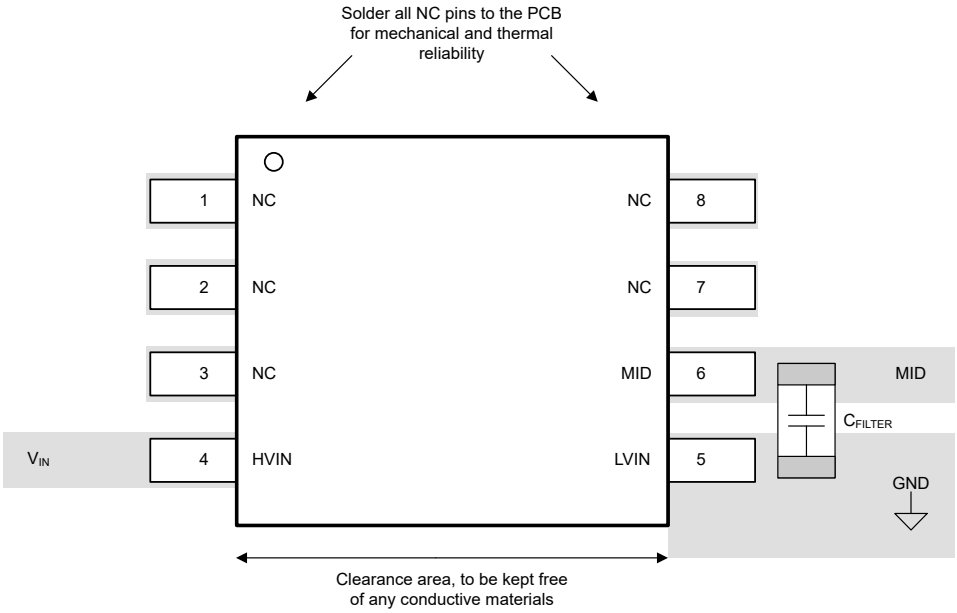


Figure 7-9. Layout Example, DWV Package

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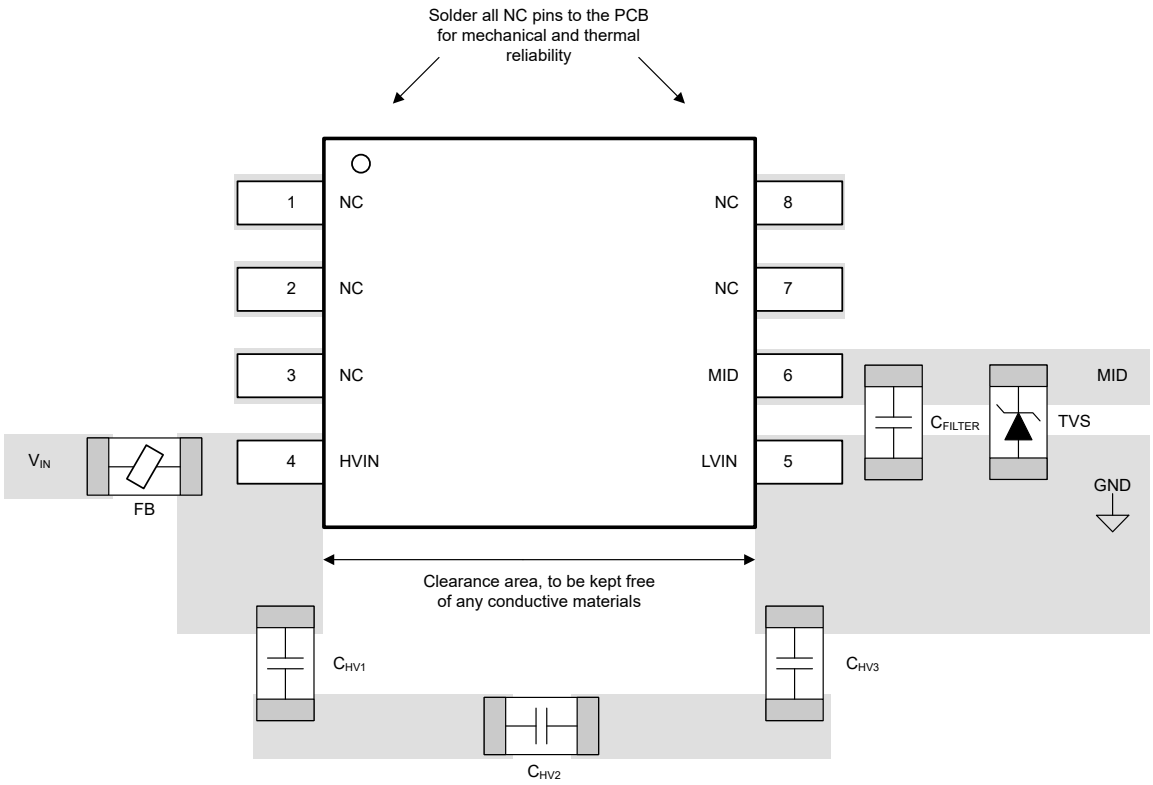


Figure 7-10. Layout Example, DWV Package with Additional Protection

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.1.1.3 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

8.1.1.4 Analog Filter Designer

Available as a web-based tool from the Design and simulation tool web page, the Analog Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *RES60A-Q1 Extended Reliability Testing* application note
- Texas Instruments, *RES60EVM* evaluation module
- Texas Instruments, *What Are Creepage And Clearance?* TI Precision Labs video
- Texas Instruments, *RES11A-Q1 Automotive, Low-Noise, Precision, Matched, Thin-Film Resistor Pairs* data sheet
- Texas Instruments, *RES21A-Q1 Automotive, Matched, Thin-Film Resistor Dividers With 10kΩ Inputs* data sheet
- Texas Instruments, *The Use and Benefits of Ferrite Beads in Gate Drive Circuits* application brief

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PRES80A100QDWVRQ1	Active	Preproduction	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PRES80A145QDWVRQ1	Active	Preproduction	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

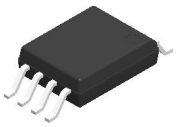
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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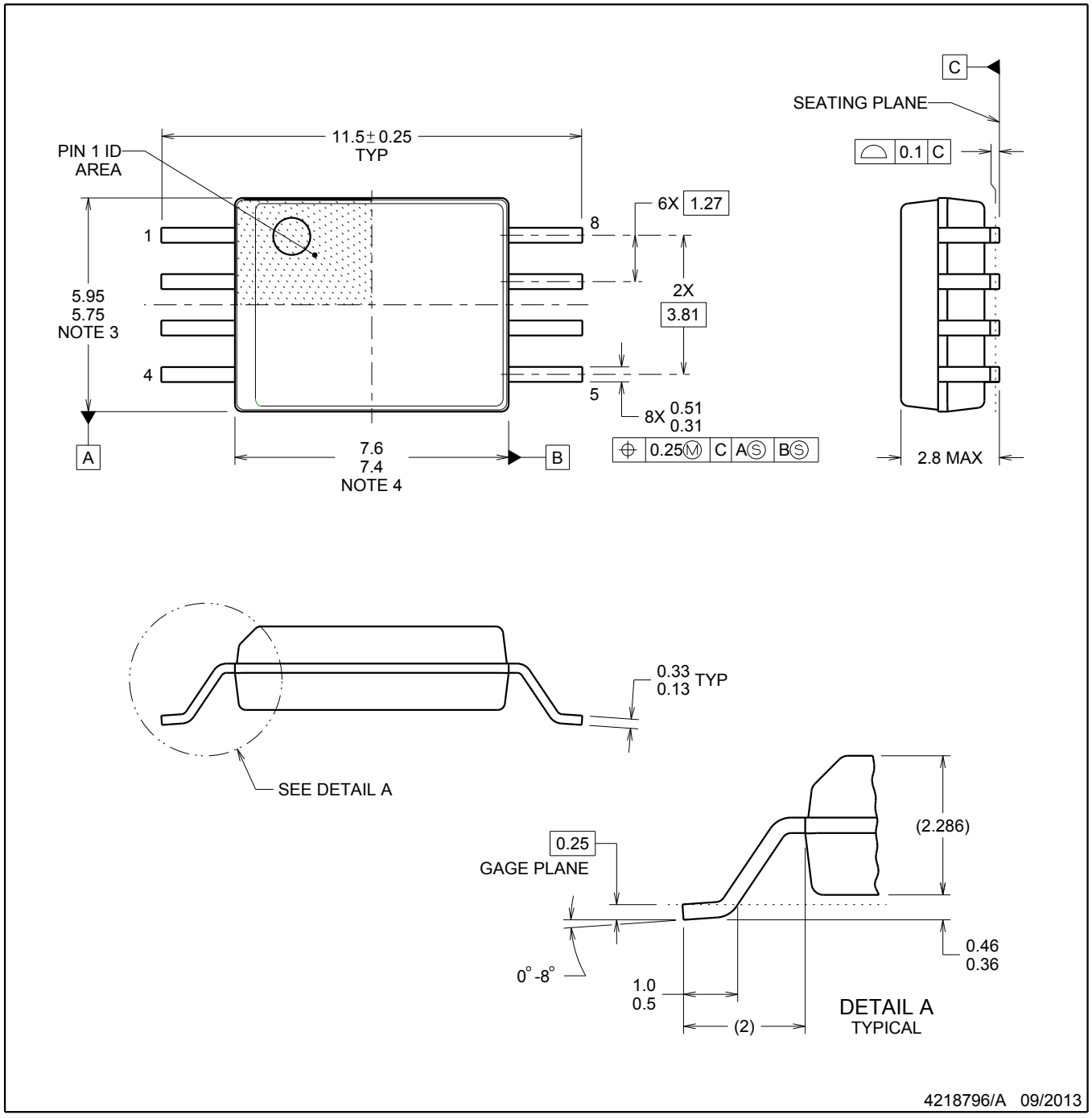
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DWV0008A

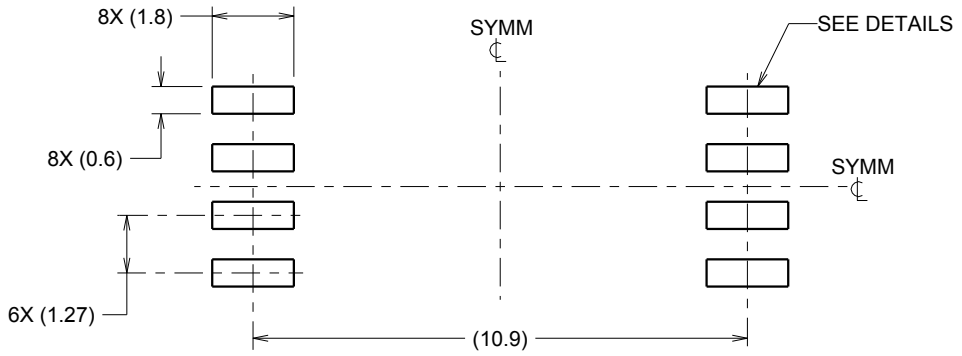
SOIC - 2.8 mm max height

SOIC

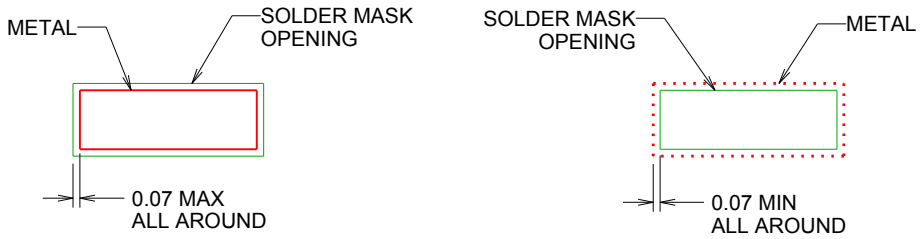


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

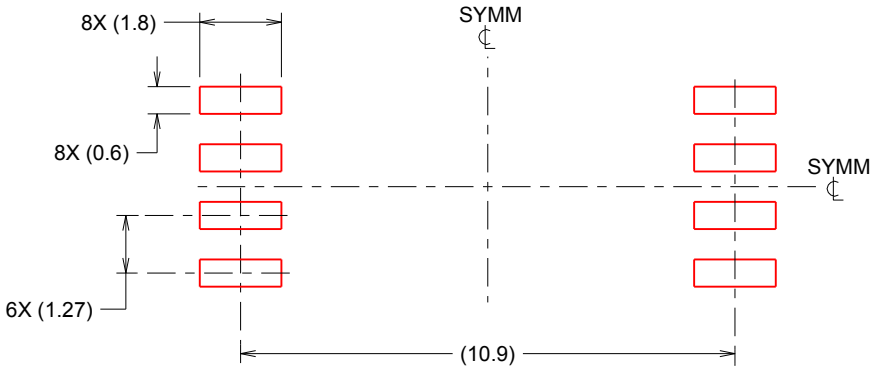
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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