OPA4277-SP Radiation-Hardened, High-Precision Operational Amplifier

1 Features

- QMLV qualified: 5962-16209
  - Radiation hardness assurance (RHA) up to total ionizing dose (TID) 50krad(Si)
  - ELDRS-Free (See Radiation Report)
  - Single event latch-up (SEL) Immune to LET = 85MeV-cm^2/mg
- Ultra-low offset voltage: 20µV (typical)
- Ultra-low drift: ±0.15µV/°C (typical)
- High open-loop gain: 134dB (typical)
- High common-mode rejection: 140dB (typical)
- High power-supply rejection: 130dB (typical)
- Wide supply range: ±2V to ±18V
- Low quiescent current: 790µA/amplifier (typical)
- Available in 14-lead CFP with industry-standard, quad-op-amp pinout

2 Applications

- Satellite electrical power system
- Command and data handling
- Optical imaging payload
- Lab and field instrumentation
- Space satellite temperature and position sensing
- Space precision and scientific applications:
  - Transducer amplifier
  - Bridge amplifier
  - Strain gauge amplifier
  - Precision integrator

3 Description

The OPA4277-SP precision operational amplifier replaces the industry standard LM124-SP. The OPA4277-SP offers improved noise and two orders of magnitude lower input offset voltage. Features include ultra-low offset voltage and drift, low-bias current, high common-mode rejection, and high power-supply rejection.

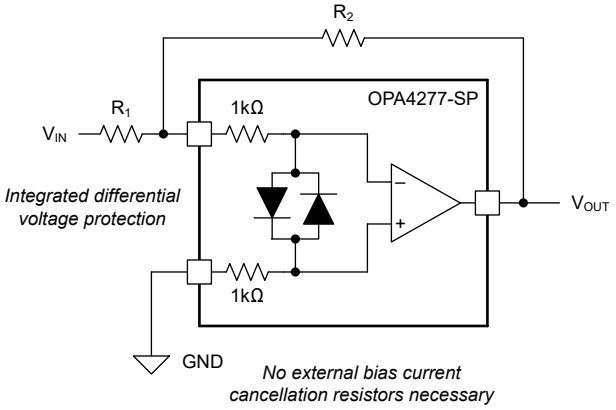
The OPA4277-SP operates from ±2V to ±18V supplies with excellent performance. Unlike most operational amplifiers that are specified at only one supply voltage, the OPA4277-SP precision operational amplifier is specified for real-world applications; a single limit applies over the ±5V to ±15V supply range. High performance is maintained as the amplifier swings to the specified limits.

The OPA4277-SP is easy to use and free from phase inversion and overload problems found in some operational amplifiers. The device is stable in unity gain and provides excellent dynamic behavior over a wide range of load conditions. The OPA4277-SP features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Device Information

PART NUMBER	GRADE	PACKAGE(1)
5962L1620901VYC	50krad(Si) ELDRS-free	14-lead CFP (HFR)
5962L1620901VXA		28-lead CDIP (JDJ)
5962L1620901V9A		KGD(2)
5962-1620901VYC	Non-RHA(3)	14-lead CFP (HFR)
OPA4277HFR/EM	Engineering samples(4)	14-lead CFP (HFR)

(1) For more information, see Section 10.
(2) KGD = known good die.
(3) Devices are processed according to full QML Class V flow, but are not screened for radiation hardness assurance.
(4) These units are intended for engineering evaluation only, and are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warrantied for performance over the full MIL specified temperature range of –55°C to +125°C or operating life.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
4.1 Bare Die Information....5
5 Specifications....6
5.1 Absolute Maximum Ratings....6
5.2 ESD Ratings....6
5.3 Recommended Operating Conditions....6
5.4 Thermal Information....6
5.5 Electrical Characteristics....7
5.6 Typical Characteristics....9
6 Detailed Description....13
6.1 Overview....13
6.2 Functional Block Diagram....13
6.3 Feature Description....13
6.4 Device Functional Modes....14
7 Application and Implementation....15
7.1 Application Information....15
7.2 Typical Application....15
7.3 Power Supply Recommendations....16
7.4 Layout....17
8 Device and Documentation Support....18
8.1 Receiving Notification of Documentation Updates....18
8.2 Support Resources....18
8.3 Trademarks....18
8.4 Electrostatic Discharge Caution....18
8.5 Glossary....18
9 Revision History....18
10 Mechanical, Packaging, and Orderable Information....19

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4 Pin Configuration and Functions

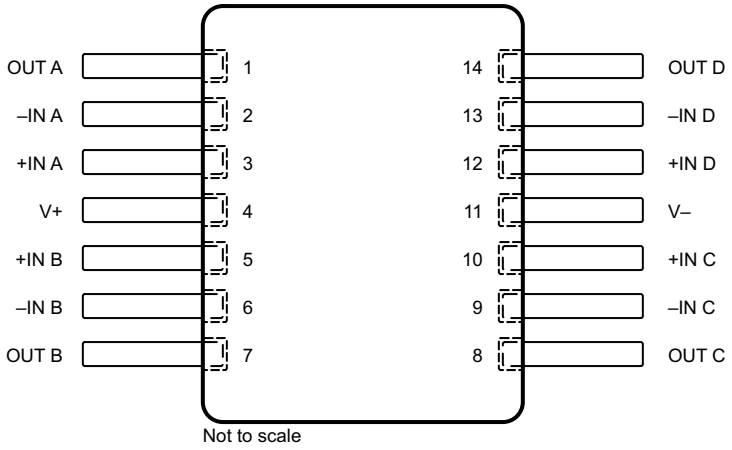


Figure 4-1. HFR Package, 14-Pin CFP (Top View)

Table 4-1. Pin Functions: CFP

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT A	Output	Output for channel A
2	–IN A	Input	Inverting input for channel A
3	+IN A	Input	Noninverting input for channel A
4	V+	—	Positive (highest) power supply
5	+IN B	Input	Noninverting input for channel B
6	–IN B	Input	Inverting input for channel B
7	OUT B	Output	Output for channel B
8	OUT C	Output	Output for channel C
9	–IN C	Input	Inverting input for channel C
10	+IN C	Input	Noninverting input for channel C
11	V–	—	Negative (lowest) power supply
12	+IN D	Input	Noninverting input for channel D
13	–IN D	Input	Inverting input for channel D
14	OUT D	Output	Output for channel D

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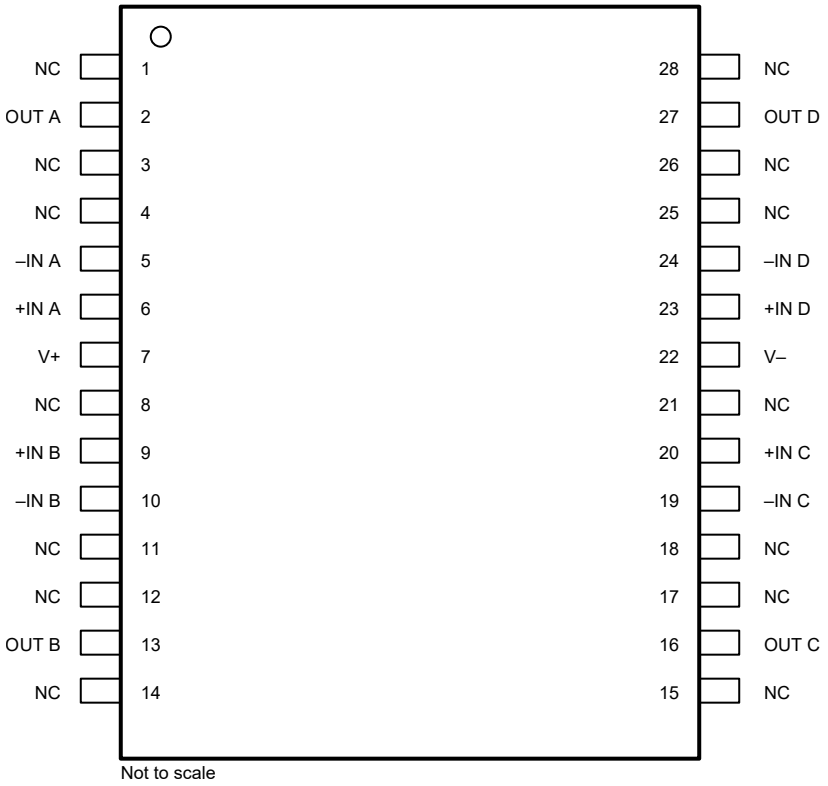


Figure 4-2. JDJ Package, 28-Pin CDIP (Top View)

Table 4-2. Pin Functions: CDIP

PIN		TYPE	DESCRIPTION
NO.	NAME		
1, 3, 4, 8, 11, 12, 14, 15, 17, 18, 21, 25, 26, 28	NC	—	Not connected
2	OUT A	Output	Output for channel A
5	–IN A	Input	Inverting input for channel A
6	+IN A	Input	Noninverting input for channel A
7	V+	—	Positive (highest) power supply
9	+IN B	Input	Noninverting input for channel B
10	–IN B	Input	Inverting input for channel B
13	OUT B	Output	Output for channel B
16	OUT C	Output	Output for channel C
19	–IN C	Input	Inverting input for channel C
20	+IN C	Input	Noninverting input for channel C
22	V–	—	Negative (lowest) power supply
23	+IN D	Input	Noninverting input for channel D
24	–IN D	Input	Inverting input for channel D
27	OUT D	Output	Output for channel D

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4.1 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Negative (lowest) power supply	AlCu (0.5%)	990 nm to 1210 nm

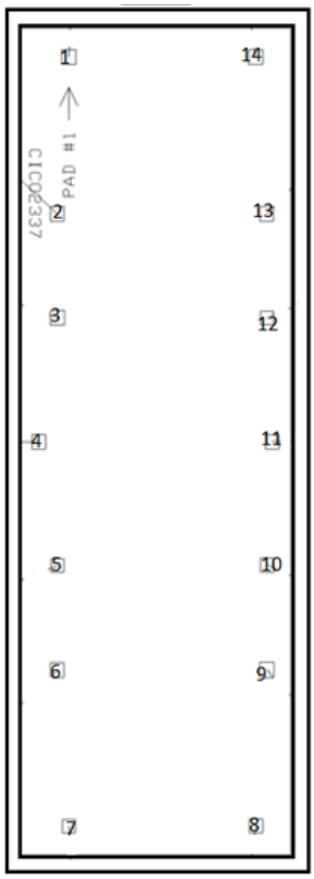


Table 4-3. Bond Pad Coordinates in Microns

PAD[1]		TYPE	DESCRIPTION	X MIN	Y MIN	X MAX	Y MAX
NO.	NAME						
1	OUT A	Output	Output for channel A	1791.042	7290.340	1901.751	7401.049
2	–IN A	Input	Inverting input for channel A	1701.719	6111.536	1807.397	6217.213
3	+IN A	Input	Noninverting input for channel A	1701.719	5326.505	1812.429	5437.215
4	V+	—	Positive (highest) power supply	1555.784	4390.507	1661.461	4498.700
5	+IN B	Input	Noninverting input for channel B	1706.752	3462.057	1807.397	3562.702
6	–IN B	Input	Inverting input for channel B	1701.719	2671.994	1807.397	2777.671
7	OUT B	Output	Output for channel B	1796.074	1498.222	1896.719	1598.867
8	OUT C	Output	Output for channel C	3278.071	1498.222	3383.748	1603.900
9	–IN C	Input	Inverting input for channel C	3362.361	2671.994	3473.071	2782.704
10	+IN C	Input	Noninverting input for channel C	3367.393	3462.057	3473.071	3567.734
11	V–	—	Negative (lowest) power supply	3407.651	4391.765	3513.329	4497.442
12	+IN D	Input	Noninverting input for channel D	3367.393	5331.537	3468.038	5432.182
13	–IN D	Input	Inverting input for channel D	3362.361	6111.536	3468.038	6217.213
14	OUT D	Output	Output for channel D	3273.039	7290.340	3383.748	7401.049

(1) Substrate must be biased to V–, negative (lowest) power supply.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)		36	V
	Input voltage	(V–) – 0.7	(V+) + 0.7	V
	Output short circuit	Continuous		
	Operating temperature	–55	125	°C
	Junction temperature		150	°C
	Lead temperature (soldering, 10s)		300	°C
T_{stg}	Storage temperature	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Machine model (MM)	±100	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Dual supply voltage	±2	±18	V
	Tested supply voltage[1]	±5	±15	V
T_J	Operating junction temperature	–55	125	°C

(1) SEL immunity characterized at 30V supply bias voltage. For more information, see the *Single-Event Effects Test Report of the OPA4277-SP High Precision Operational Amplifiers* radiation report.

5.4 Thermal Information

THERMAL METRIC[1]		OPA4277-SP		UNIT
		HFR (CFP)	JDJ (CDIP)	
		14 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.7	66.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.4	19.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.4	35.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.6	12.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.2	34.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.9	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics

at T_J = 25°C, V_S = ±5V to ±15V, and R_L = 2kΩ (unless otherwise noted). Post-irradiated specifications do not apply to non-RHA grades, including engineering samples.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_J = 25°C, pre- and post-irradiated		±20	±65	µV
		T_J = –55°C to +125°C, pre-irradiated			±140	
dV_{OS}/d_T	Input offset voltage temperature drift	T_J = –55°C to +125°C, pre-irradiated		±0.15		µV/°C
	Input offset voltage long-term stability			0.2		µV/mo
PSRR	Power-supply rejection ratio	V_S = ±2V to ±18V, T_J = 25°C, pre- and post-irradiated		±0.3	±1	µV/V
		V_S = ±2V to ±18V, T_J = –55°C to +125°C			±1	
	Channel separation	DC		0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_J = –55°C to +125°C			±17.5	nA
		T_J = 25°C, pre- and post-irradiated			±17.5	
I_{OS}	Input offset current	T_J = –55°C to +125°C			±17.5	nA
		T_J = 25°C, pre- and post-irradiated			±17.5	
NOISE						
	Input voltage noise	f = 0.1 to 10Hz		0.22		μV_{pp}
	Input voltage noise density	f = 10Hz		12		$nV/\sqrt{Hz}$
		f = 100Hz		8		
		f = 1kHz		8		
		f = 10kHz		8		
i_n	Input noise current density	f = 1kHz		0.2		$fA/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range	T_J = 25°C, pre- and post-irradiated	(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) + 2V < V_{CM} < (V+) – 2V, T_J = 25°C, pre- and post-irradiated, JDJ package and KGD	114	140		dB
		(V–) + 2V < V_{CM} < (V+) – 2V, T_J = –55°C to +125°C, JDJ package and KGD	114			
		(V–) + 2V < V_{CM} < (V+) – 2V, T_J = 25°C, pre- and post-irradiated, HFR package	100	121		
		(V–) + 2V < V_{CM} < (V+) – 2V, T_J = –55°C to +125°C, HFR package	100			
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common mode	(V–) + 2V < V_{CM} < (V+) – 2V		250 || 3		GΩ || pF
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			1		MHz
SR	Slew rate			0.8		V/µs
	Settling time	0.1%, 10V step, V_S = ±15V, G = 1		14		µs
		0.01%, 10V step, V_S = ±15V, G = 1		16		
THD + N	Total harmonic distortion + noise	1kHz, G = 1, V_O = 3.5Vrms		0.002%		

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5.5 Electrical Characteristics (continued)

at T_J = 25°C, V_S = ±5V to ±15V, and R_L = 2kΩ (unless otherwise noted). Post-irradiated specifications do not apply to non-RHA grades, including engineering samples.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_O = (V–) + 0.5V to (V+) – 1.2V, R_L = 10kΩ		140		dB
		V_O = (V–) + 1.5V to (V+) – 1.5V, R_L = 2kΩ, T_J = 25°C, pre- and post-irradiated, JDJ package and KGD	118	134		
		V_O = (V–) + 1.5V to (V+) – 1.5V, R_L = 2kΩ, T_J = –55°C to +125°C, JDJ package and KGD	118	134		
		V_O = (V–) + 1.5V to (V+) – 1.5V, R_L = 2kΩ, T_J = 25°C, pre- and post-irradiated, HFR package	100	123		
		V_O = (V–) + 1.5V to (V+) – 1.5V, R_L = 2kΩ, T_J = –55°C to +125°C, HFR package	100	123		
		V_O = (V–) + 3.4V to (V+) – 3.4V, R_L = 600Ω, V_S = ±7V, T_J = 25°C, pre- and post-irradiated, JDJ package and KGD	118	134		
		V_O = (V–) + 3.4V to (V+) – 3.4V, R_L = 600Ω, V_S = ±7V, T_J = –55°C to +125°C, JDJ package and KGD	118	134		
		V_O = (V–) + 3.4V to (V+) – 3.4V, R_L = 600Ω, V_S = ±7V, T_J = 25°C, pre- and post-irradiated, HFR package	90	114		
		V_O = (V–) + 3.4V to (V+) – 3.4V, R_L = 600Ω, V_S = ±7V, T_J = –55°C to +125°C, HFR package	90	114		
OUTPUT						
V_O	Output voltage	R_L = 10kΩ, T_J = 25°C, pre- and post-irradiated	(V–) + 0.5		(V+) – 1.2	V
		R_L = 10kΩ, T_J = –55°C to +125°C	(V–) + 0.5		(V+) – 1.2	
		R_L = 2kΩ, T_J = 25°C, pre- and post-irradiated	(V–) + 1.5		(V+) – 1.5	
		R_L = 2kΩ, T_J = –55°C to +125°C	(V–) + 1.5		(V+) – 1.5	
		T_J = 25°C, R_L = 600Ω, pre- and post-irradiated	(V–) + 3.4		(V+) – 3.4	
		R_L = 600Ω, V_S = ±7V, T_J = –55°C to +125°C	(V–) + 3.4		(V+) – 3.4	
I_{SC}	Short-circuit current			±35		mA
C_{LOAD}	Capacitive load drive	f = 350kHz, I_O = 0mA	See *Section 5.6*			
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0mA, T_J = 25°C, pre- and post-irradiated		±790	±850	μA
		I_O = 0mA, T_J = –55°C to +125°C			±900	

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5.6 Typical Characteristics

at T_J = 25°C, V_S = ±15V, R_L = 2kΩ, and pre-irradiated (unless otherwise noted)

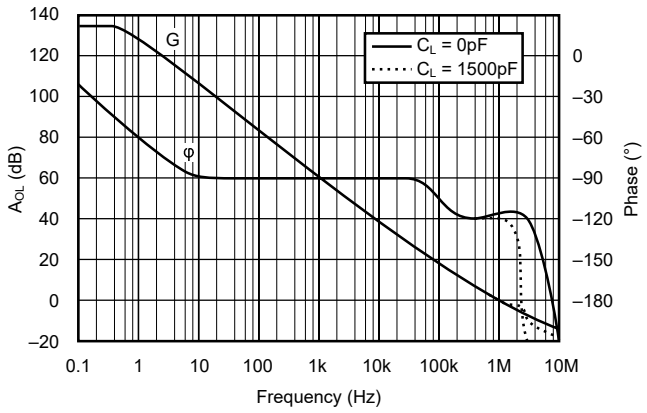


Figure 5-1. Open-Loop Gain and Phase vs Frequency

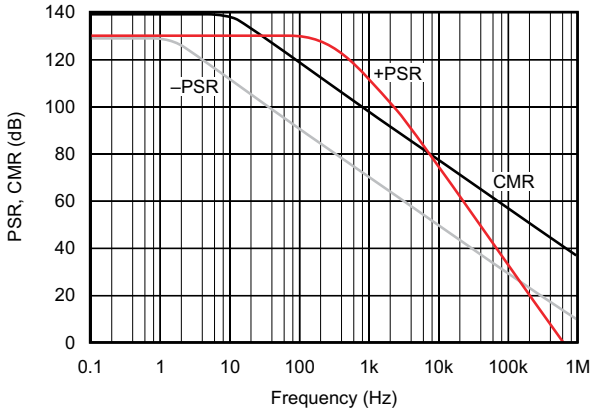


Figure 5-2. Power Supply and Common-Mode Rejection vs Frequency

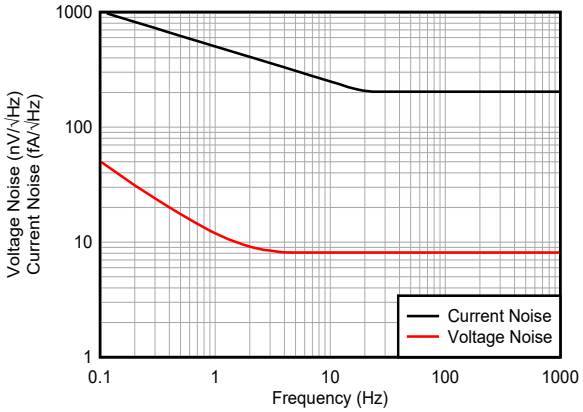
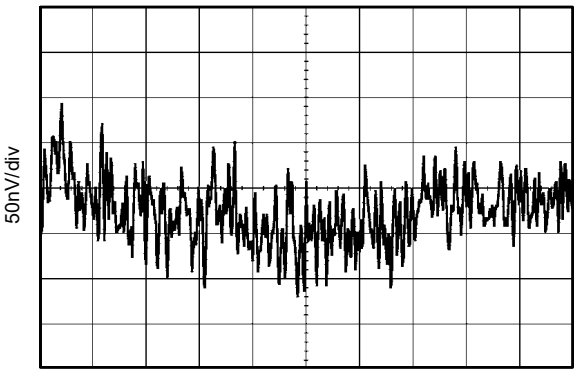
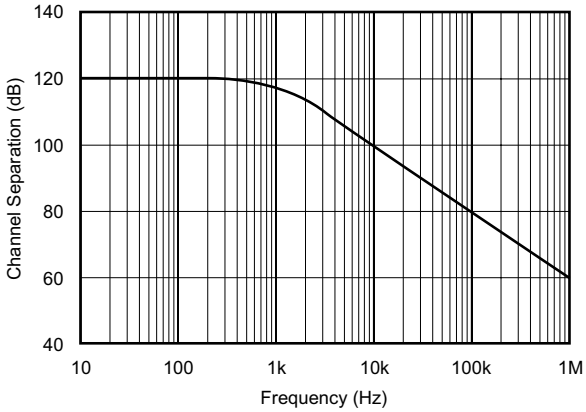


Figure 5-3. Input Noise and Current Noise Spectral Density vs Frequency



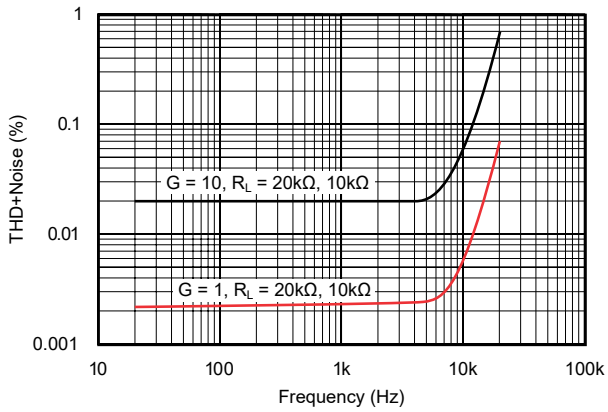
Noise signal is bandwidth limited to lie between 0.1Hz and 10Hz

Figure 5-4. Input Noise Voltage vs Time



G = 1, measured channel A to D or B to C,
other combinations yield similar or improved rejection

Figure 5-5. Channel Separation vs Frequency



V_{OUT} = 3.5Vrms

Figure 5-6. Total Harmonic Distortion + Noise vs Frequency

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5.6 Typical Characteristics (continued)

at T_J = 25°C, V_S = ±15V, R_L = 2kΩ, and pre-irradiated (unless otherwise noted)

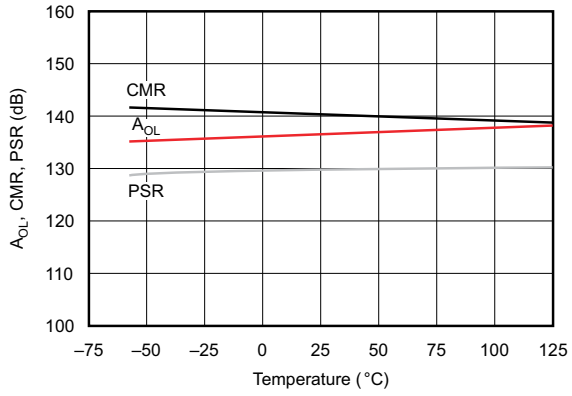
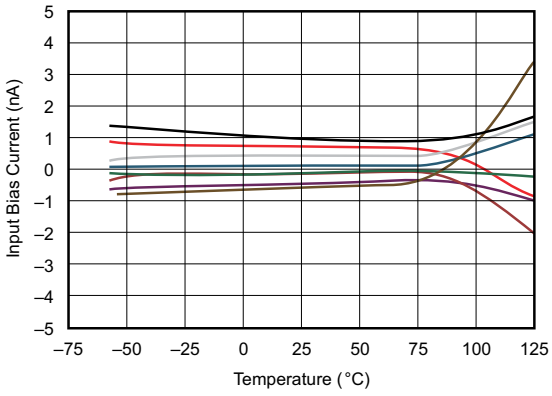


Figure 5-7. A_{OL}, CMR, PSR vs Temperature



Curves represent typical production units

Figure 5-8. Input Bias Current vs Temperature

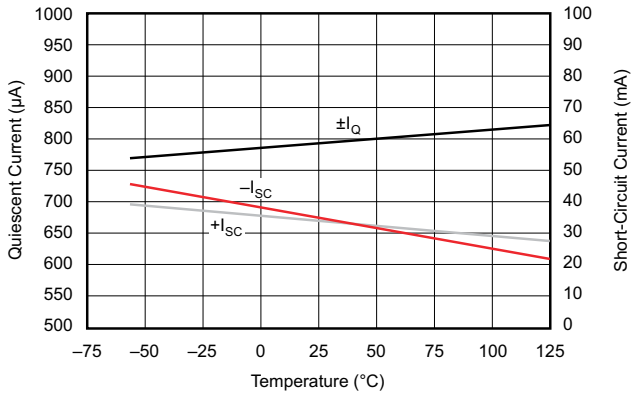
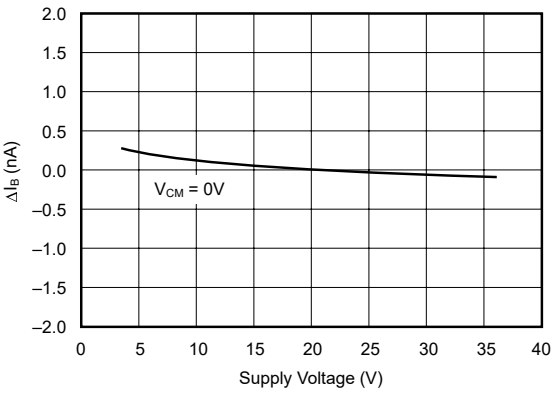
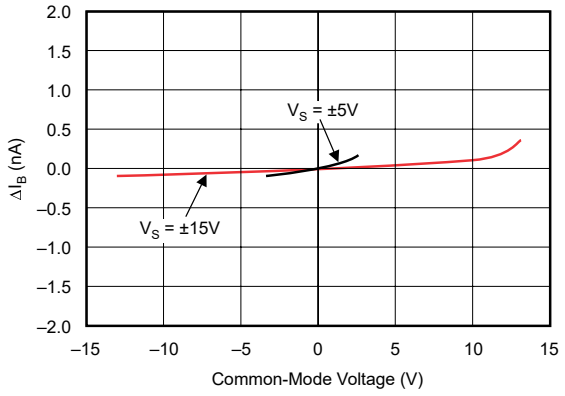


Figure 5-9. Quiescent Current and Short-Circuit Current vs Temperature



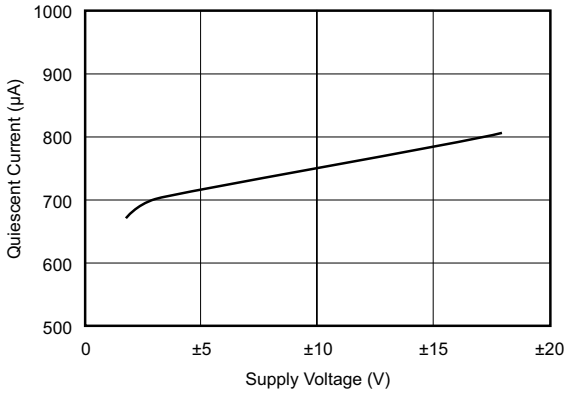
Curve shows normalized change in bias current with respect to V_S = ±10V (+20V), typical I_B ranges from –0.5nA to 0.5nA at V_S = ±10V

Figure 5-10. Change in Input Bias Current vs Power Supply Voltage



Curve shows normalized change in bias current with respect to V_{CM} = 0V, typical I_B ranges from –0.5nA to 0.5nA at V_{CM} = 0V

Figure 5-11. Change in Input Bias Current vs Common-Mode Voltage



Per amplifier

Figure 5-12. Quiescent Current vs Supply Voltage

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5.6 Typical Characteristics (continued)

at T_J = 25°C, V_S = ±15V, R_L = 2kΩ, and pre-irradiated (unless otherwise noted)

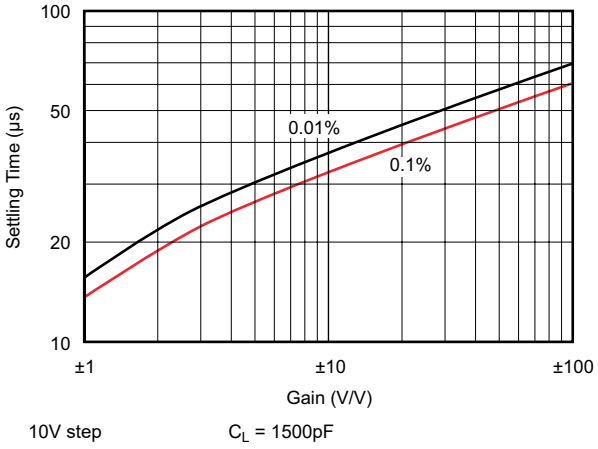


Figure 5-13. Settling Time vs Closed-Loop Gain

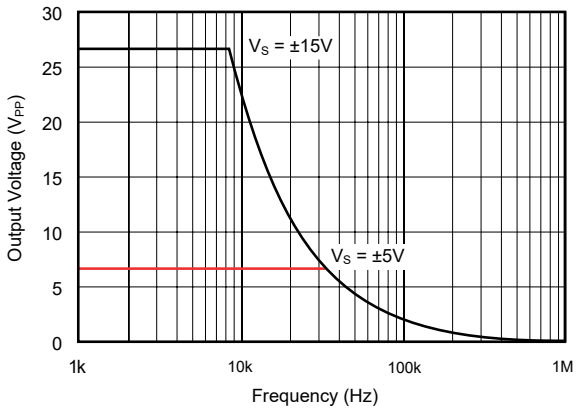


Figure 5-14. Maximum Output Voltage vs Frequency

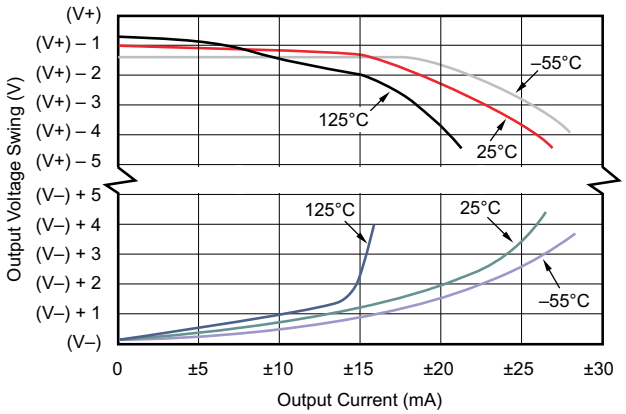


Figure 5-15. Output Voltage Swing vs Output Current

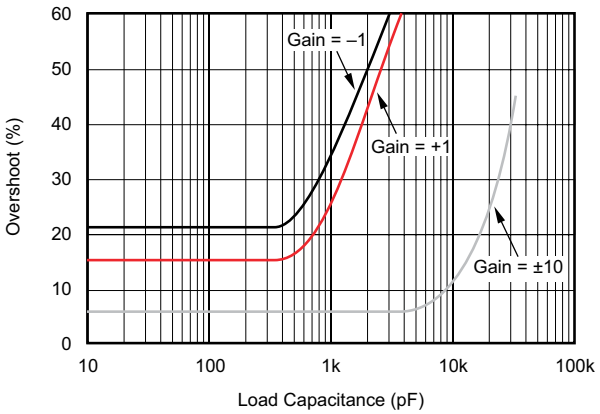


Figure 5-16. Small-Signal Overshoot vs Load Capacitance

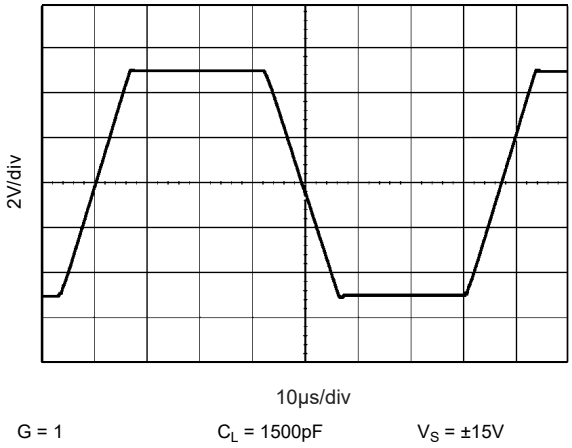


Figure 5-17. Large-Signal Step Response

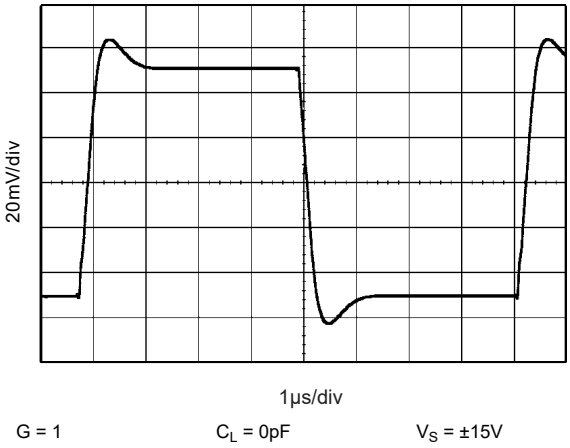


Figure 5-18. Small-Signal Step Response

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5.6 Typical Characteristics (continued)

at T_J = 25°C, V_S = ±15V, R_L = 2kΩ, and pre-irradiated (unless otherwise noted)

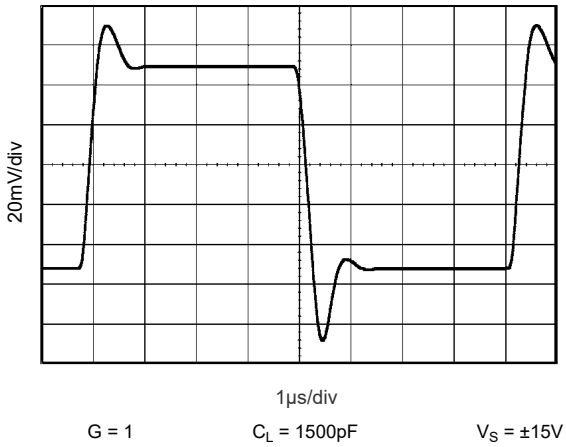


Figure 5-19. Small-Signal Step Response

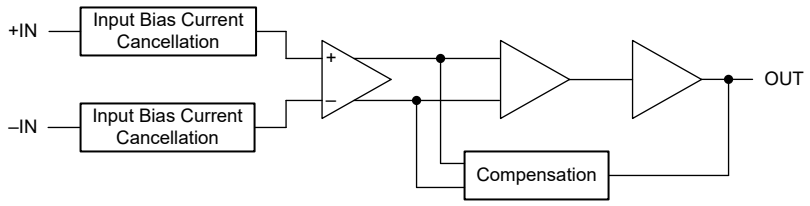
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6 Detailed Description

6.1 Overview

The OPA4277-SP precision operational amplifier replaces the industry standard LM124-SP. The OPA4277-SP offers improved noise, wider output voltage swing, and is twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power-supply rejection.

6.2 Functional Block Diagram



6.3 Feature Description

The OPA4277-SP operates from ±2V to ±18V supplies with excellent performance. Unlike most operational amplifiers that are specified at only one supply voltage, the OPA4277-SP precision operational amplifier is specified for real-world applications; a single limit applies over the ±5V to ±15V supply range. High performance is maintained as the amplifier swings to the specified limits. Because the initial offset voltage is so low (±50µV, max), user adjustment is typically not required.

6.3.1 Input Protection

The inputs of the OPA4277-SP are protected with 1kΩ series input resistors and diode clamps. The inputs can withstand ±30V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. The conducting current potentially disturbs the slewing behavior of unity-gain follower applications, but does not damage the operational amplifier.

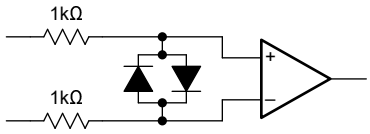


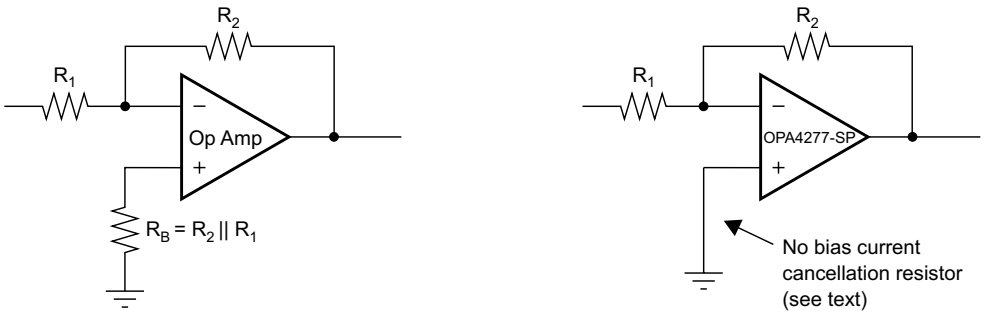
Figure 6-1. OPA4277-SP Input Protection

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6.3.2 Input Bias Current Cancellation

The input stage base current of the OPA4277-SP is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, using a bias current cancellation resistor is not necessary, as is often done with other operational amplifiers. Figure 6-2 (a) shows an op amp with an external bias current cancellation resistor and (b) shows the OPA4277-SP which requires no external bias current cancellation resistor. Be aware that a resistor added to cancel input bias current errors can actually increase offset voltage and noise.



(a)

Conventional op amp with external bias current cancellation resistor.

(b)

OPA4277-SP with no external bias current cancellation resistor.

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Figure 6-2. Input Bias Current Cancellation

6.4 Device Functional Modes

The OPA4277-SP has a single functional mode and is operational when the power-supply voltage, (V+) – (V–), is less than or equal to 36V and greater than or equal to 4V.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPA4277-SP is unity-gain stable and free from unexpected output phase reversal, making this device easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies potentially require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate.

7.2 Typical Application

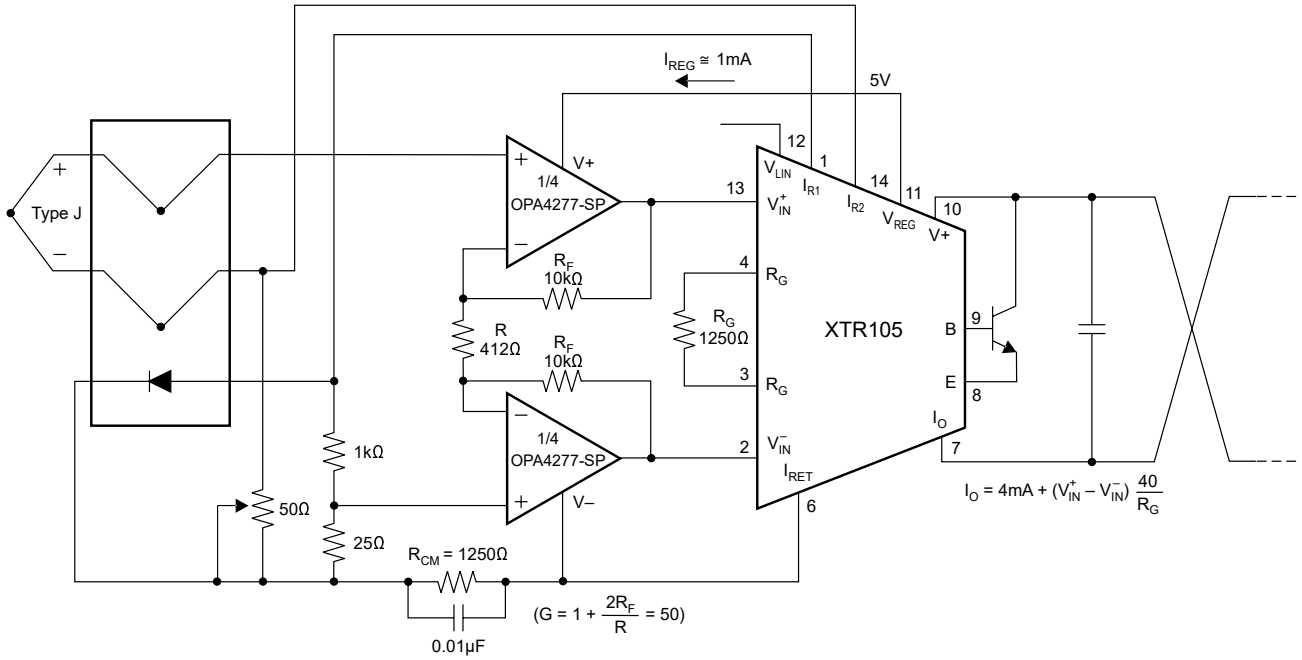


Figure 7-1. Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation

7.2.1 Design Requirements

For the thermocouple low-offset, low-drift loop measurement with diode cold junction compensation shown in Figure 7-1, a gain of 50 is desired.

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7.2.2 Detailed Design Procedure

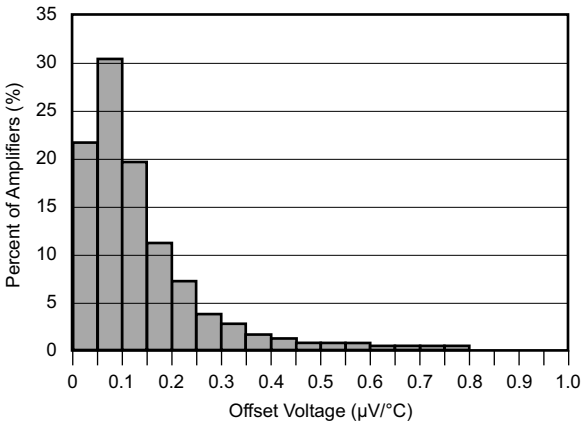
Equation 1 calculates the resistor values needed for a gain of 50. Table 7-1 lists the design parameters.

$$G = 1 + \frac{2R_F}{R} = 50 \quad (1)$$

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
R_F	10kΩ
R	412Ω

7.2.3 Application Curve



T_J = 25°C, V_S = ±15V, R_L = 2kΩ
Typical distribution of packaged units—single, dual, and quad included

Figure 7-2. Warm-Up Offset Voltage Drift

7.3 Power Supply Recommendations

The OPA4277-SP operates from ±2V to ±18V supplies with excellent performance. Unlike most operational amplifiers that are specified at only one supply voltage, the OPA4277-SP is specified for real-world applications; a single limit applies over the ±5V to ±15V supply range. Thus, operating at V_S = ±10V has the same specified performance as using ±15V supplies. In addition, key parameters are specified over the temperature range of –55°C to +125°C. Most behavior remains unchanged through the full operating voltage range (±2V to ±18V). Parameters that vary significantly with operating voltage or temperature are shown in the *Typical Characteristics* curves.

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7.4 Layout

7.4.1 Layout Guidelines

The OPA4277-SP has very-low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the OPA4277-SP. Cancel these thermal potentials by making sure that the potentials are equal in both input terminals.

- Keep the thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as cooling fans.

7.4.2 Layout Example

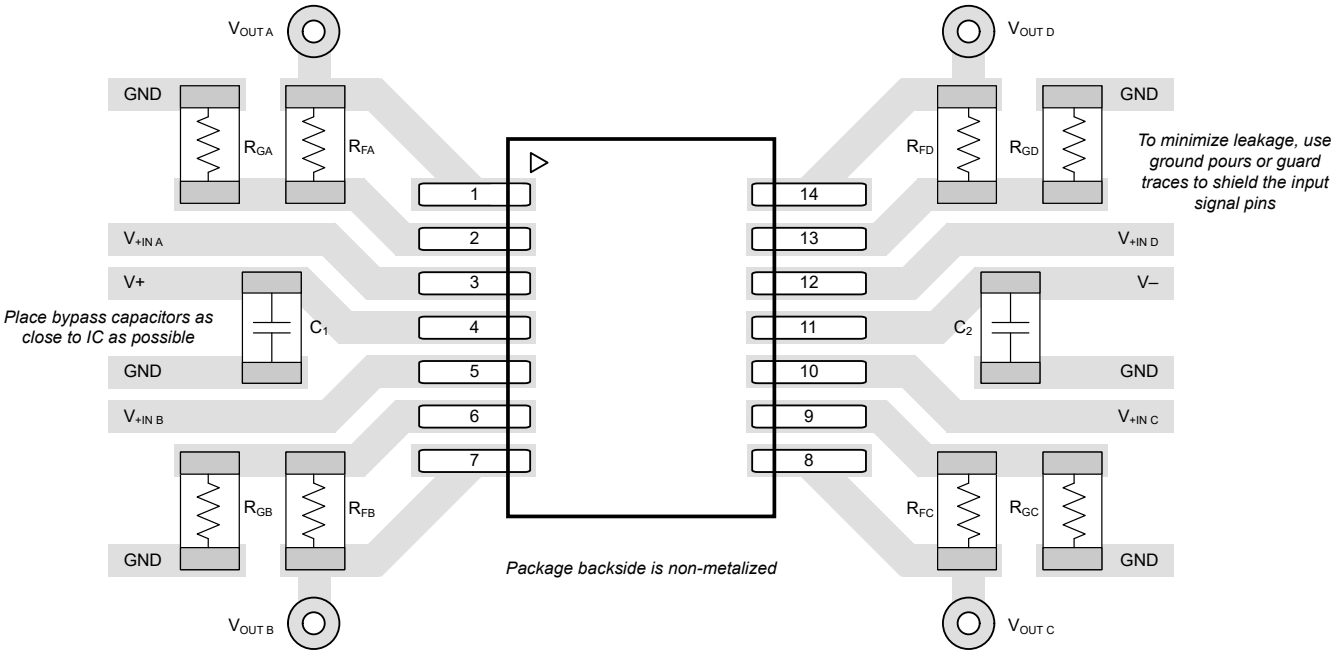


Figure 7-3. Board Layout Example

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2024) to Revision C (October 2025)	Page
• Added non-RHA 5962-1620901VYC device to *Device Information*	1
• Changed JDJ (CDIP) pin names from +VS to V+, and from –VS to V– to be consistent with other packages	3
• Added footnote to *Recommended Operating Conditions* table clarifying that SEL immunity is characterized at 30V supply	6
• Added statement clarifying that post-irradiated specifications do not apply to non-RHA orderables in *Electrical Characteristics*	7
• Changed (V_O+) to V+ and (V_O–) to V– in test conditions for A_{OL}, to correct typo	7

Changes from Revision A (January 2019) to Revision B (November 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added clarification that values are typical in *Features*	1
• Changed typical quiescent current per amplifier from 800µA to 790µA in *Features*	1
• Updated list of related end-equipments in *Applications*	1
• Updated *Simplified Schematic* to show input protection circuitry	1
• Updated incorrect pin descriptions for pins 9, 10, 23, and 24 in Table 5-1, *Pin Functions: CDIP*	3
• Updated incorrect pin names for pins 19 and 20 in Table 5-1, *Pin Functions: CDIP*	3
• Updated incorrect pin names for pins 19 and 20 in Figure 5-1, *JDJ Package, 28-Pin CDIP (Top View)*	3
• Changed $R_{\theta JB}$, ψ_{JT}, and ψ_{JB} parameter values and added $R_{\theta JC(bot)}$ thermal metric for JDJ package in *Thermal Information*	6
• Added HFR package to *Thermal Information*	6

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- Changed parameter text from "Input offset voltage" to "Input offset voltage long-term stability" for "vs time" spec in *Electrical Characteristics* 7
- Changed parameter text for PSRR from "Input offset voltage" to "Power-supply rejection ratio" in *Electrical Characteristics* 7
- Updated some CMRR and AOL parameter descriptions to specifically specify JDJ package and KGD, and clarified that some test conditions for these specifications are both pre- and post-irradiation in *Electrical Characteristics* 7
- Added minimum CMRR specification of 100dB, and typical CMRR specification of 121dB, for HFR package in *Electrical Characteristics* 7
- Added minimum AOL specifications of 100dB (2kΩ load) and 90dB (600Ω load), and typical specifications of 123dB (2kΩ load) and 114dB (600Ω load), for HFR package in *Electrical Characteristics* 7
- Deleted "specified voltage" and "operating voltage" specifications from *Electrical Characteristics*, as these specifications already appear in *Recommended Operating Conditions* 7
- Deleted duplicate title from Figure 6-3, *Input Noise and Current Noise Spectral Density vs Frequency* 9
- Updated *Functional Block Diagram* to include input bias current cancellation and compensation functional blocks..... 13
- Added minimum valid supply voltage to description of *Device Functional Modes* and clarified that maximum power-supply voltage can equal 36V..... 14
- Deleted thermal pad recommendations from *Layout Guidelines* to accurately reflect packaged-device characteristics..... 17
- Changed Figure 8-3, *Board Layout Example*, from a generic op-amp EVM layout to device-specific layout.. 17

Changes from Revision * (December 2016) to Revision A (January 2019) **Page**

- Changed *Features* section..... 1
- Added new device packages..... 1
- Updated *Pin Configurations and Functions* section..... 3
- Updated *Recommended Operating Conditions* table..... 6
- Updated Figure 6-3, *Input Noise and Current Noise Spectral Density vs Frequency* 9

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-1620901VYC	Active	Production	CFP (HFR) | 14	25 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 125	5962-1620901VYC OPA4277-SP
5962L1620901V9A	Last Time Buy	Production	XCEPT (KGD) | 0	36 | JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	-55 to 125	
5962L1620901V9A.A	Last Time Buy	Production	XCEPT (KGD) | 0	36 | JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	-55 to 125	
5962L1620901VXA	Last Time Buy	Production	CDIP SB (JDJ) | 28	12 | TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 125	5962L1620901VX A OPA4277-SP
5962L1620901VXA.A	Last Time Buy	Production	CDIP SB (JDJ) | 28	12 | TUBE	Yes	Call TI	N/A for Pkg Type	-55 to 125	5962L1620901VX A OPA4277-SP
5962L1620901VYC	Last Time Buy	Production	CFP (HFR) | 14	25 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 125	5962L1620901VYC OPA4277-SP
5962L1620901VYC.A	Last Time Buy	Production	CFP (HFR) | 14	25 | TUBE	Yes	AU	N/A for Pkg Type	-55 to 125	5962L1620901VYC OPA4277-SP
OPA4277HFR/EM	Active	Production	CFP (HFR) | 14	25 | TUBE	Yes	AU	N/A for Pkg Type	25 to 25	OPA4277HFR/EM EVAL ONLY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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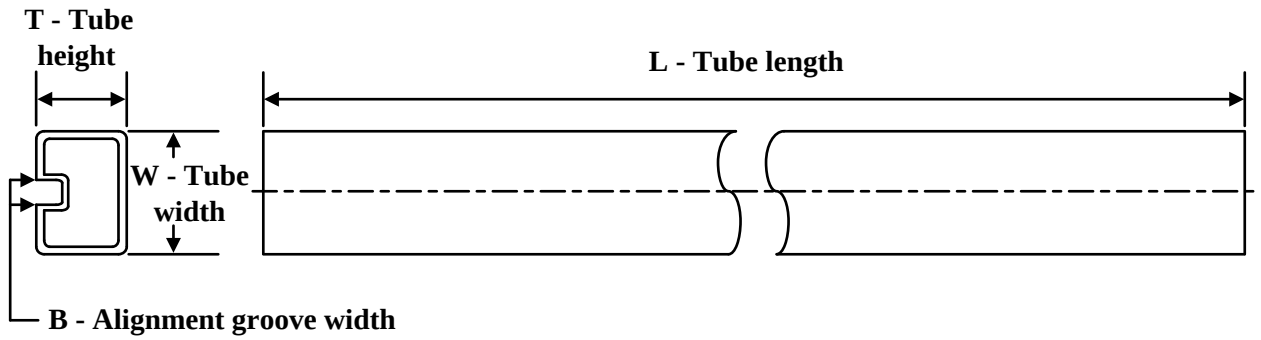
OTHER QUALIFIED VERSIONS OF OPA4277-SP :

- Catalog : OPA4277
- Enhanced Product : OPA4277-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

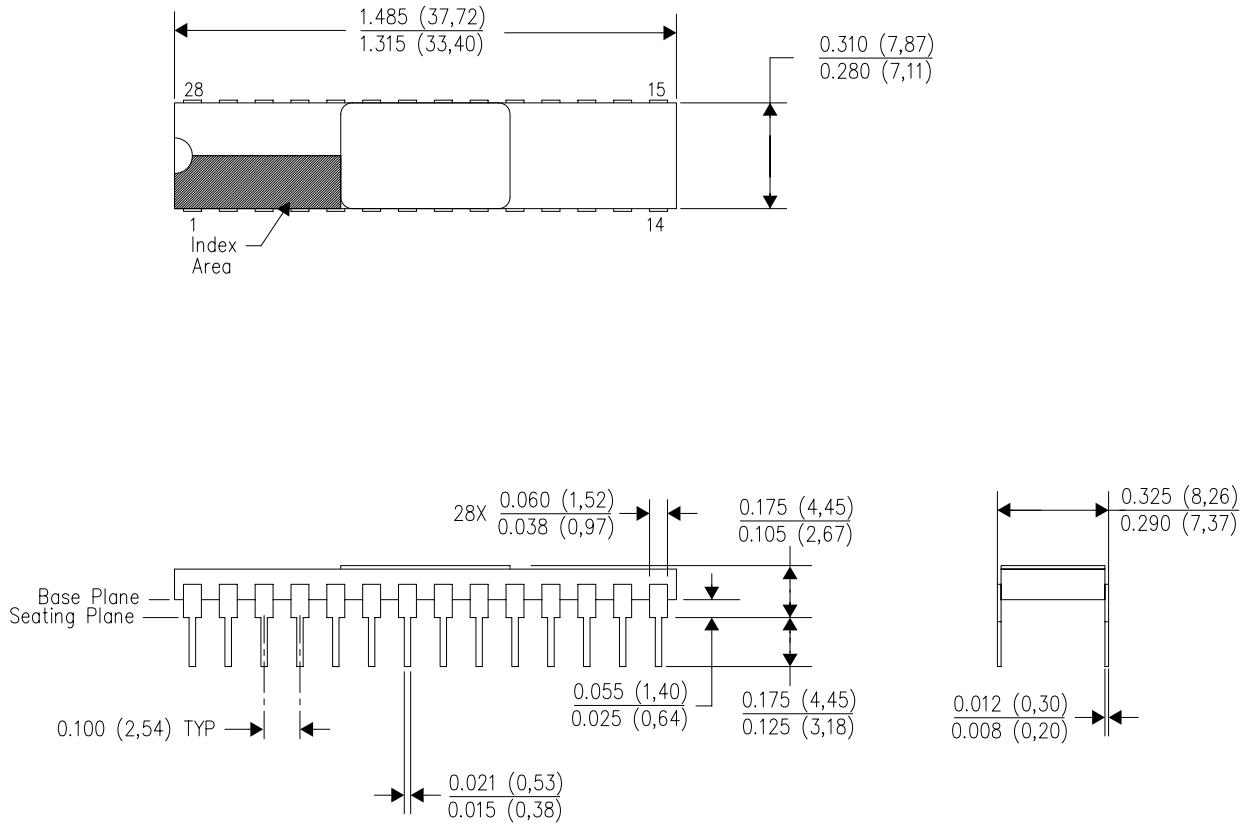
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-1620901VYC	HFR	CFP (HSL)	14	25	506.98	26.16	6220	NA
5962L1620901VXA	JDJ	CDIP SB	28	12	506.98	15.24	12290	NA
5962L1620901VXA.A	JDJ	CDIP SB	28	12	506.98	15.24	12290	NA
5962L1620901VYC	HFR	CFP (HSL)	14	25	506.98	26.16	6220	NA
5962L1620901VYC.A	HFR	CFP (HSL)	14	25	506.98	26.16	6220	NA

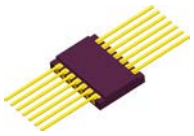
JDJ (R–CDIP–T28) CERAMIC DUAL IN–LINE PACKAGE



4202646–3/B 07/10

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Lid and heat sink are connected to GND leads.

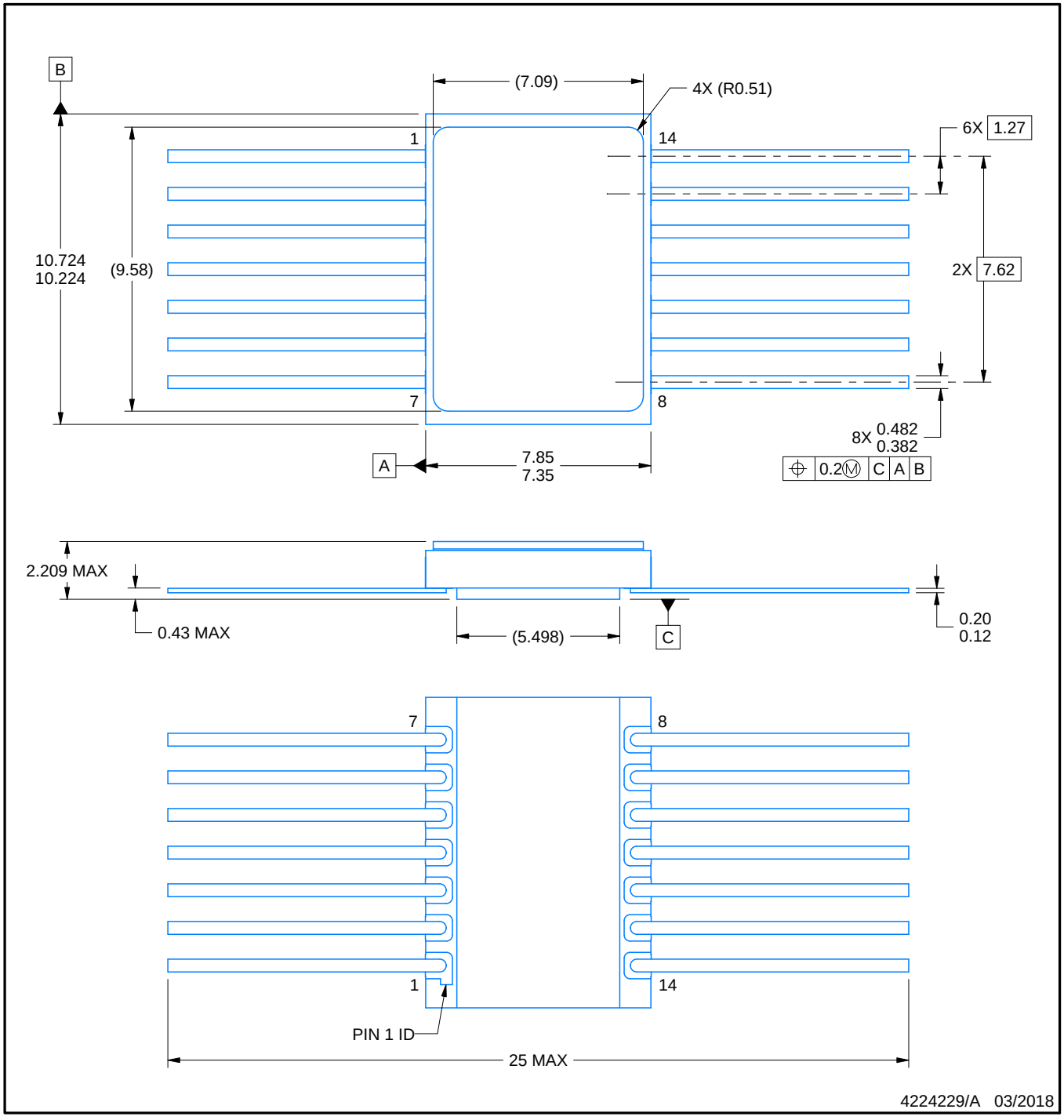
HFR0014A



PACKAGE OUTLINE

CFP - 2.209 mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.

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