OPAx237 Single-Supply Operational Amplifiers MicroAmplifier Series

1 Features

- Micro-size, miniature packages:
  - Single: SOT23-5, SO-8
  - Dual: VSSOP-8, SO-8
  - Quad: SSOP-16 (obsolete)
- Low offset voltage: 750µV max (V_S=5V)
- Wide supply range:
  - Single supply: 2.7V to 36V
  - Dual supply: ±1.35V to ±18V
- Low quiescent current: 350µA max
- Wide bandwidth: 1.5MHz

2 Applications

- Battery-powered instruments
- Portable devices
- PCMCIA cards
- Medical instruments
- Test equipment

3 Description

The OPAx237 op amp family is one of Texas Instruments' MicroAmplifier series of miniature products. In addition to small size, these devices feature low offset voltage, low quiescent current, low bias current, and a wide supply range. Single, and dual versions have identical specifications for maximum design flexibility. These devices are designed for single-supply, battery-operated, and space-limited applications, such as PCMCIA cards and other portable instruments.

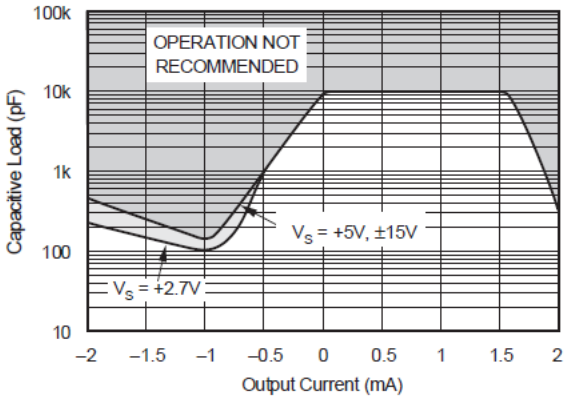
The OPAx237 series op amps operate from either single or dual supplies. When operated from a single supply, the input common-mode range extends below ground and the output can swing to within 10mV of ground. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

Single, dual, and quad versions are offered in space-saving surface-mount packages. The single version is available in the ultra-miniature 5-lead SOT23-5 and SOIC-8 surface-mount packages. The dual version comes in miniature VSSOP-8 and SO-8 surface-mount packages. The quad version is obsolete. The VSSOP-8 has the same lead count as a the SO-8, but at half the size. The SOT23-5 is even smaller, at one-fourth the size of an SOIC-8. All are specified for –40°C to +85°C operation. A macromodel is available for design analysis.

Device Information

PRODUCT	CHANNELS	PACKAGE(1)
OPA237	Single	D (SOIC, 8)
		DBV (SOT-23, 5)
OPA2237	Dual	D (SOIC, 8)
		DGK (VSSOP, 8)

(1) For more information, see Section 9.



Stability-Capacitive Load vs Output Current

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

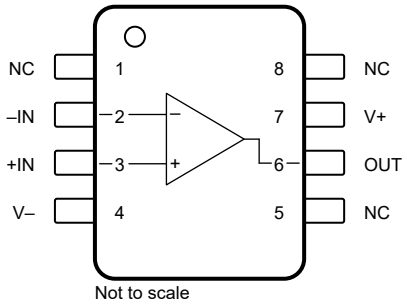

Figure 4-1. OPA237: D Package, 8-Pin SOIC (Top View)

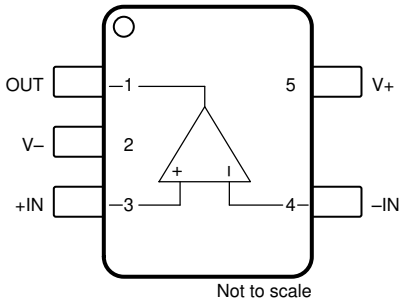

Figure 4-2. OPA237: DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions: OPA237

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC)	DBV (SOT-23)		
–IN	2	4	Input	Inverting input
+IN	3	3	Input	Noninverting input
OUT	6	1	Output	Output
V–	4	2	Power	Negative (lowest) power supply
V+	7	5	Power	Positive (highest) power supply

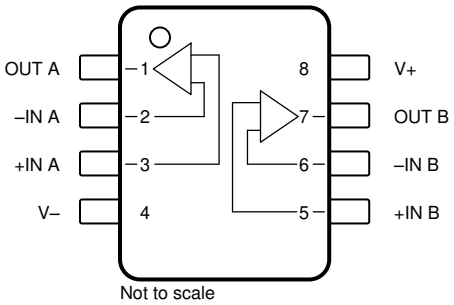

Figure 4-3. OPA2237: D Package, 8-Pin SOIC, and DGK Package, 8-Pin VSSOP (Top View)

Table 4-2. Pin Functions: OPA2237

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
+IN A	3	Input	Noninverting input, channel A
–IN B	6	Input	Inverting input, channel B
+IN B	5	Input	Noninverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V–	4	Power	Negative (lowest) power supply
V+	8	Power	Positive (highest) power supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

				MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)				36	V
	Signal input pins	Voltage	Common-mode	(V–) – 0.7	(V+) + 0.7	V
			Differential	–0.7	+0.7	
		Current			±10	mA
I_{SC}	Output short circuit[2]			Continuous		
T_A	Operating temperature			–55	125	°C
T_J	Junction temperature				150	°C
T_{stg}	Storage temperature			–55	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	2.7		36	V
T_A	Operating temperature	–40		85	°C

5.3 Thermal Information OPA237

THERMAL METRIC[1]		OPA237		UNIT
		DBV (SOT-23)	D (SOIC)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.4	102.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.9	100.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.4 Thermal Information OPA2237

THERMAL METRIC[1]		OPA2237		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.9	175.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.1	63.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.3	97.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.8	7.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.5	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics for V_S = 2.7V

at T_A = 25°C, V_O = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = 1V			±250	±950	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			±2	±7.5	µV/°C
PSRR	Power-supply rejection ratio	2.7V < V_S < 36V			10	30	µV/V
	Channel separation (dual)				0.5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current (1)	V_{CM} = 1V			–10	–40	nA
I_{OS}	Input offset current (1)	V_{CM} = 1V			±0.5	±10	nA
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			1		$µV_{PP}$
e_n	Input voltage noise density	f = 1kHz			28		nV/√Hz
i_n	Input current noise density	f = 1kHz			60		pA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.2		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	V_{CM} = (V–) – 0.2V to (V+) – 1.5V		71	85		dB
INPUT IMPEDANCE							
Z_{IN}	Input impedance	Differential			5 || 4		MΩ || pF
		Common-mode			5 || 2		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_O = 0.55V to 1.7V		75	88		dB
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1.2		MHz
SR	Slew rate	G = 1			0.45		V/µs
t_S	Settling time	G = –1, C_L = 100pF, 1V step	0.1%		5		µs
			0.01%		8		
OUTPUT							
V_O	Voltage output	R_L = 100kΩ to V–	Positive rail	(V+) – 1	(V+) – 0.75		V
			Negative rail		(V–) + 0.001	(V–) + 0.05	
		R_L = 100kΩ	Positive rail	(V+) – 1	(V+) – 0.75		
			Negative rail		(V–) + 0.02	(V–) + 0.06	
		R_L = 10kΩ	Positive rail	(V+) – 1	(V+) – 0.75		
			Negative rail		(V–) + 0.2	(V–) + 0.3	
I_{SC}	Short-circuit current	Sourcing			7		mA
		Sinking			–10		
C_L	Capacitive load drive			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current per amplifier				150	350	µA

(1) Input bias current specified by design and processing.

5.6 Electrical Characteristics for V_S = 5V

at T_A = 25°C, V_O = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = 2.5V			±250	±750	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			±2	±5	µV/°C
PSRR	Power-supply rejection ratio	2.7V < V_S < 36V			10	30	µV/V
	Channel separation (dual)				1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current (1)	V_{CM} = 2.5V			–10	–40	nA
I_{OS}	Input offset current (1)	V_{CM} = 2.5V			±0.5	±10	nA
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			1		$µV_{PP}$
e_n	Input voltage noise density	f = 1kHz			28		nV/√Hz
i_n	Input current noise density	f = 1kHz			60		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.2		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	V_{CM} = (V–) – 0.2V to (V+) – 1.5V		76	86		dB
INPUT IMPEDANCE							
Z_{IN}	Input impedance	Differential			5 || 4		MΩ || pF
		Common-mode			5 || 2		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_O = 0.5V to 4V		75	88		dB
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1.4		MHz
SR	Slew rate	G = 1			0.45		V/µs
t_S	Settling time	G = –1, C_L = 100pF, 3V step	0.1%		11		µs
			0.01%		16		
OUTPUT							
V_O	Voltage output	R_L = 100kΩ to V–	Positive rail	(V+) – 1.5	(V+) – 0.75		V
			Negative rail		(V–) + 0.001	(V–) + 0.1	
		R_L = 100kΩ	Positive rail	(V+) – 1.5	(V+) – 0.75		
			Negative rail		(V–) + 0.04	(V–) + 0.12	
		R_L =10 kΩ	Positive rail	(V+) – 1.5	(V+) – 0.75		
			Negative rail		(V–) + 0.35	(V–) + 0.6	
I_{SC}	Short-circuit current	Sourcing			8		mA
		Sinking			–10		
C_L	Capacitive load drive			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current per amplifier				170	350	µA

(1) Input bias current specified by design and processing.

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5.7 Electrical Characteristics for V_S = 30V

at T_A = 25°C, V_O = V_S / 2, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V_S/2			±350	±950	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +85°C			±2.5	±7	µV/°C
PSRR	Power-supply rejection ratio	2.7V < V_S < 36V			10	30	µV/V
	Channel separation (dual)				1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current (1)	V_{CM} = V_S/2			–8.5	–40	nA
I_{OS}	Input offset current (1)	V_{CM} = V_S/2			±0.5	±10	nA
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			1		$µV_{PP}$
e_n	Input voltage noise density	f = 1kHz			28		nV/√Hz
i_n	Input current noise density	f = 1kHz			80		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.2		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	V_{CM} = (V–) to (V+) – 1.5V		80	90		dB
INPUT IMPEDANCE							
Z_{IN}	Input impedance	Differential			5 || 4		MΩ || pF
		Common-mode			5 || 2		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_O = (V–) + 1V to (V+) – 1.2V		80	88		dB
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				1.5		MHz
SR	Slew rate	G = 1			0.44		V/µs
t_S	Settling time	G = –1, C_L = 100pF, 10V step	0.1%		20		µs
			0.01%		24		
OUTPUT							
V_O	Voltage output	R_L = 100kΩ	Positive rail	(V+) – 1.2	(V+) – 0.9		V
			Negative rail		(V–) + 0.3	(V–) + 0.5	
		R_L = 10kΩ	Positive rail	(V+) – 1.2	(V+) – 0.9		
			Negative rail		(V–) + 0.85	(V–) + 1	
I_{SC}	Short-circuit current	Sourcing			9.5		mA
		Sinking			–10		
C_L	Capacitive load drive			See *Typical Characteristics*			
POWER SUPPLY							
I_Q	Quiescent current per amplifier				200	475	µA

(1) Input bias current specified by design and processing.

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5.8 Typical Characteristics

at T_A = 25°C and R_L = 10kΩ (unless otherwise noted)

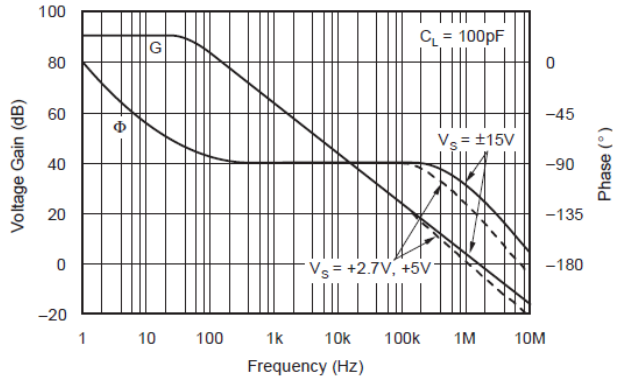

Figure 5-1. Open-Loop Gain and Phase vs Frequency

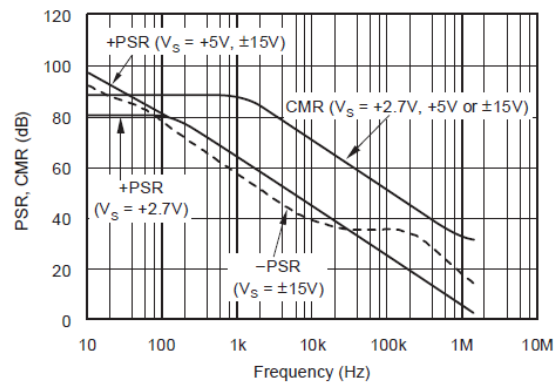

Figure 5-2. Power Supply and Common-Mode Rejection vs Frequency

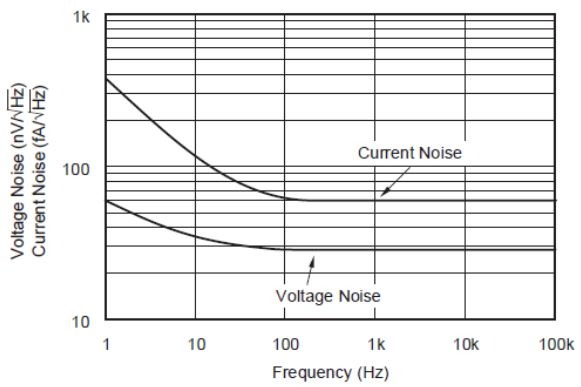

Figure 5-3. Input Noise and Current Noise Spectral Density vs Frequency

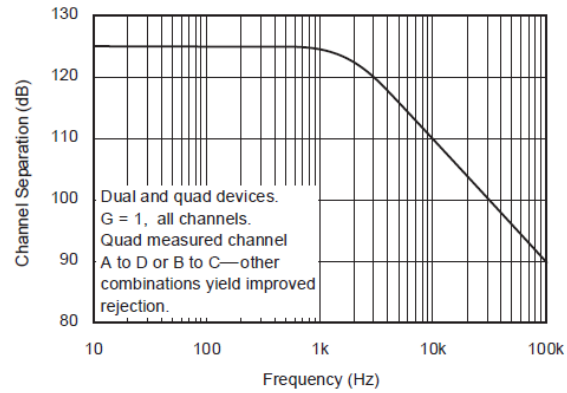

Figure 5-4. Channel Separation vs Frequency

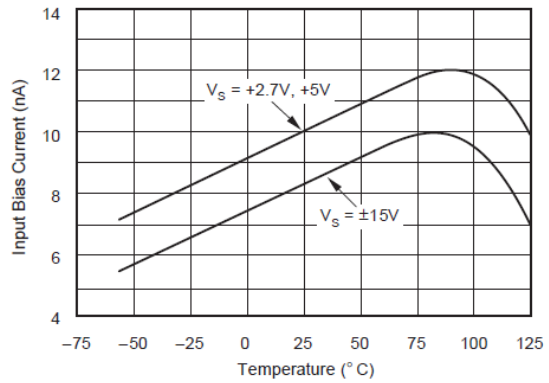

Figure 5-5. Input Bias Current vs Temperature

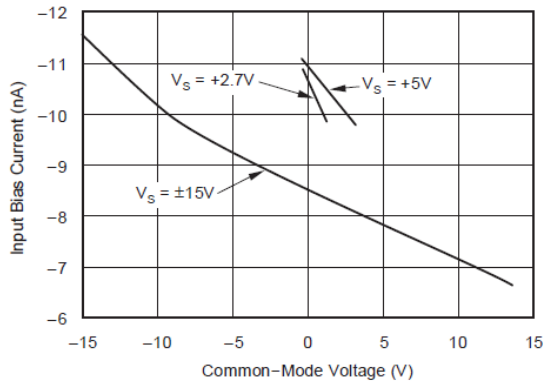

Figure 5-6. Input Bias Current vs Input Common-Mode Voltage

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5.8 Typical Characteristics (continued)

at T_A = 25°C and R_L = 10kΩ (unless otherwise noted)

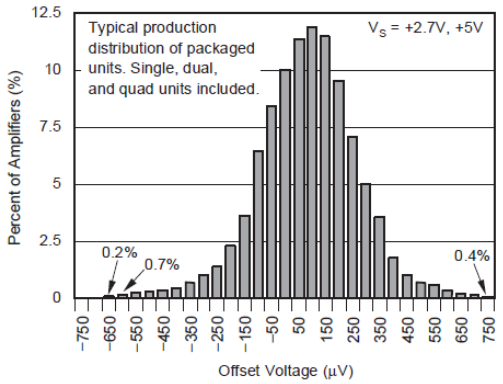


Figure 5-7. Offset Voltage Production Distribution

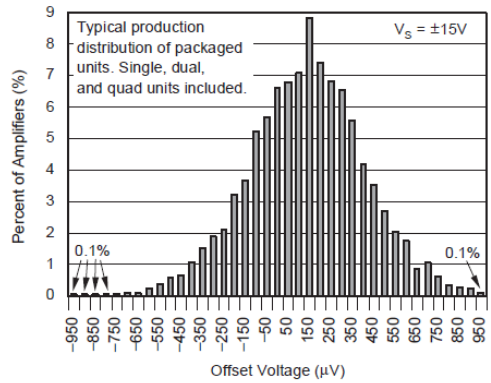


Figure 5-8. Offset Voltage Production Distribution

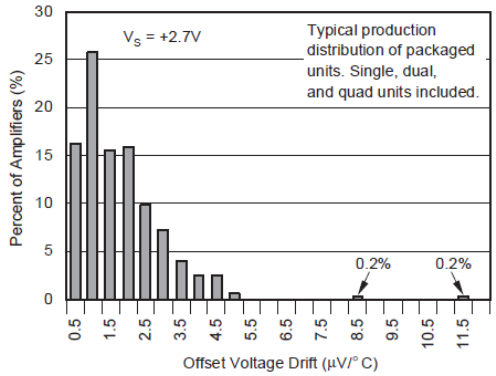


Figure 5-9. Offset Voltage Drift Production Distribution

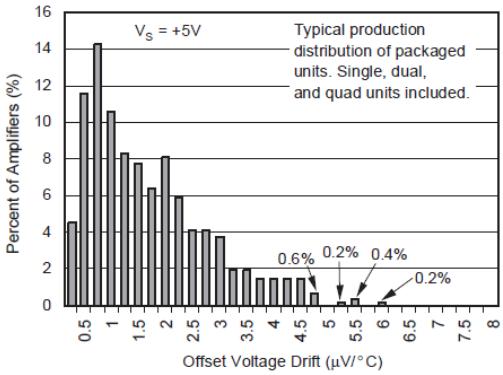


Figure 5-10. Offset Voltage Drift Production Distribution

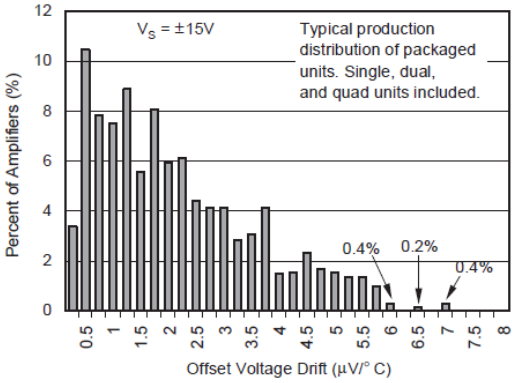


Figure 5-11. Offset Voltage Drift Production Distribution

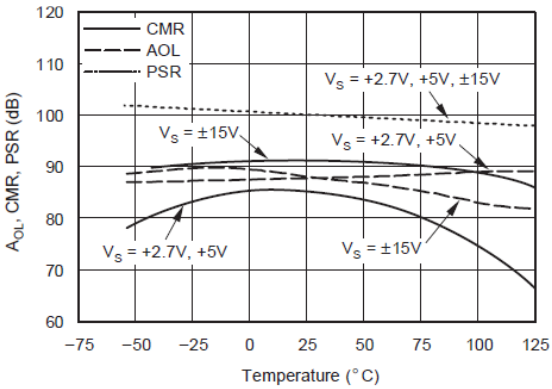
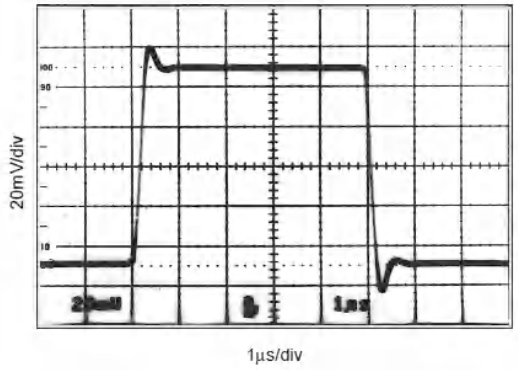


Figure 5-12. A_{OL}, CMR, PSR vs Temperature

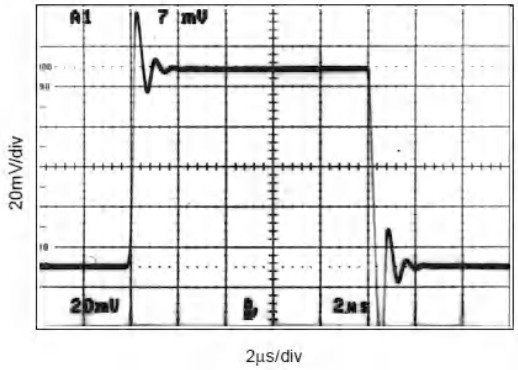
5.8 Typical Characteristics (continued)

at T_A = 25°C and R_L = 10kΩ (unless otherwise noted)



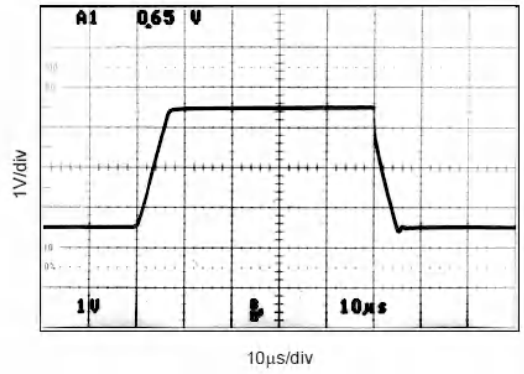
G = 1 C_L = 100pF V_S = 5V

Figure 5-13. Small-Signal Step Response



G = 1 C_L = 220pF V_S = 5V

Figure 5-14. Small-Signal Step Response



G = 1 C_L = 100pF V_S = 5V

Figure 5-15. Large-Signal Step Response

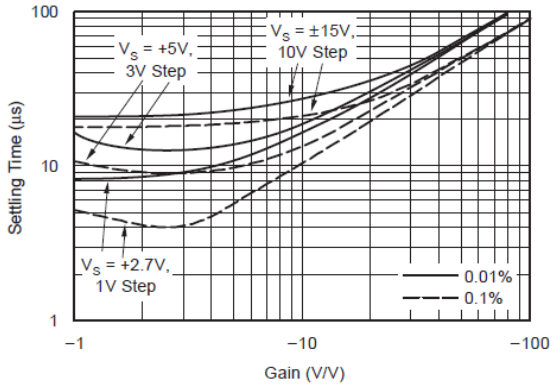


Figure 5-16. Settling Time vs Gain

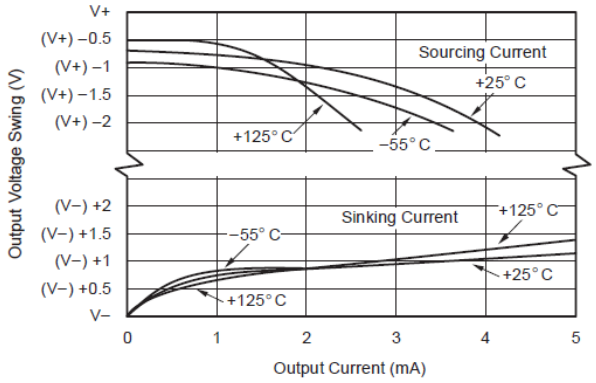


Figure 5-17. Output Voltage Swing vs Output Current

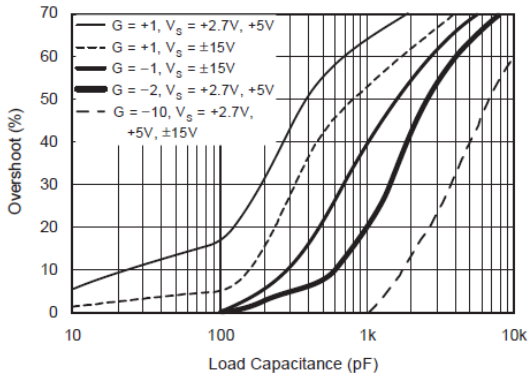


Figure 5-18. Small−Signal Overshoot vs Load Capacitance

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5.8 Typical Characteristics (continued)

at T_A = 25°C and R_L = 10kΩ (unless otherwise noted)

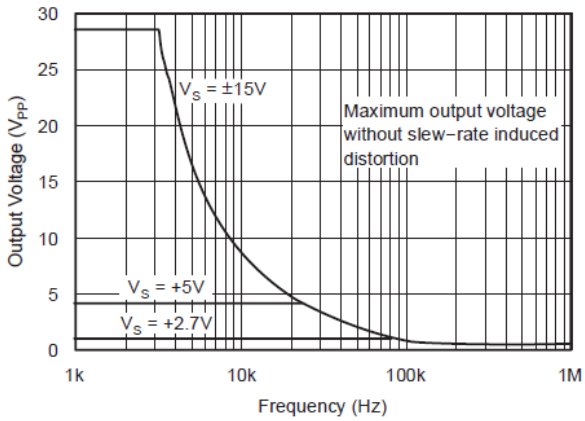

Figure 5-19. Maximum Output Voltage vs Frequency

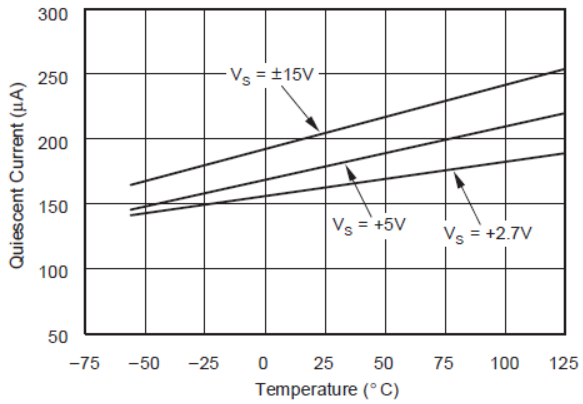

Figure 5-20. Quiescent Current vs Temperature

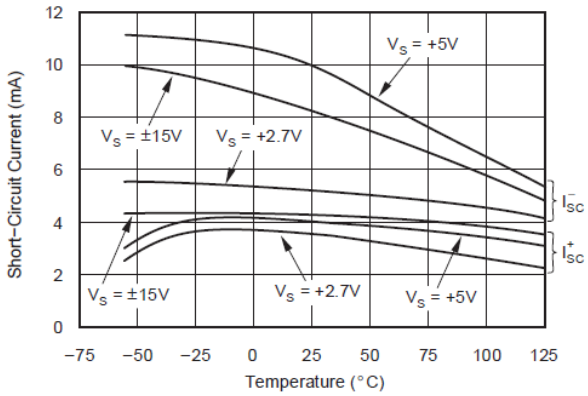

Figure 5-21. Short-Circuit Current vs Temperature

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The OPA237 series op amps are unity-gain stable and an excellent choice for a wide range of general-purpose applications. Bypass the power-supply pins with 10nF ceramic capacitors.

6.1.1 Operating Voltage

OPA237 series op amps operate from single (2.7V to 36V) or dual (±1.35V to ±18V) supplies with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in *Typical Characteristics*. Specifications are production tested with 2.7V, 5V, and ±15V supplies.

6.1.2 Output Current and Stability

OPA237 series op amps can drive large capacitive loads. However, under certain limited output conditions, any op amp can become unstable. Figure 6-2 shows the region where the OPA237 has a potential for instability. These load conditions are rarely encountered, especially for single-supply applications. For example, when a 5V supply with a 10kΩ load to $V_S/2$ is used.

OPA237 series op amps remain stable with capacitive loads up to 4,000pF, if sinking current, and up to 10,000pF, if sourcing current. Furthermore, in single-supply applications where the load is connected to ground, the op amp is only sourcing current, and as Figure 6-2 shows, the op amp can drive 10,000pF with output currents up to 1.5mA.

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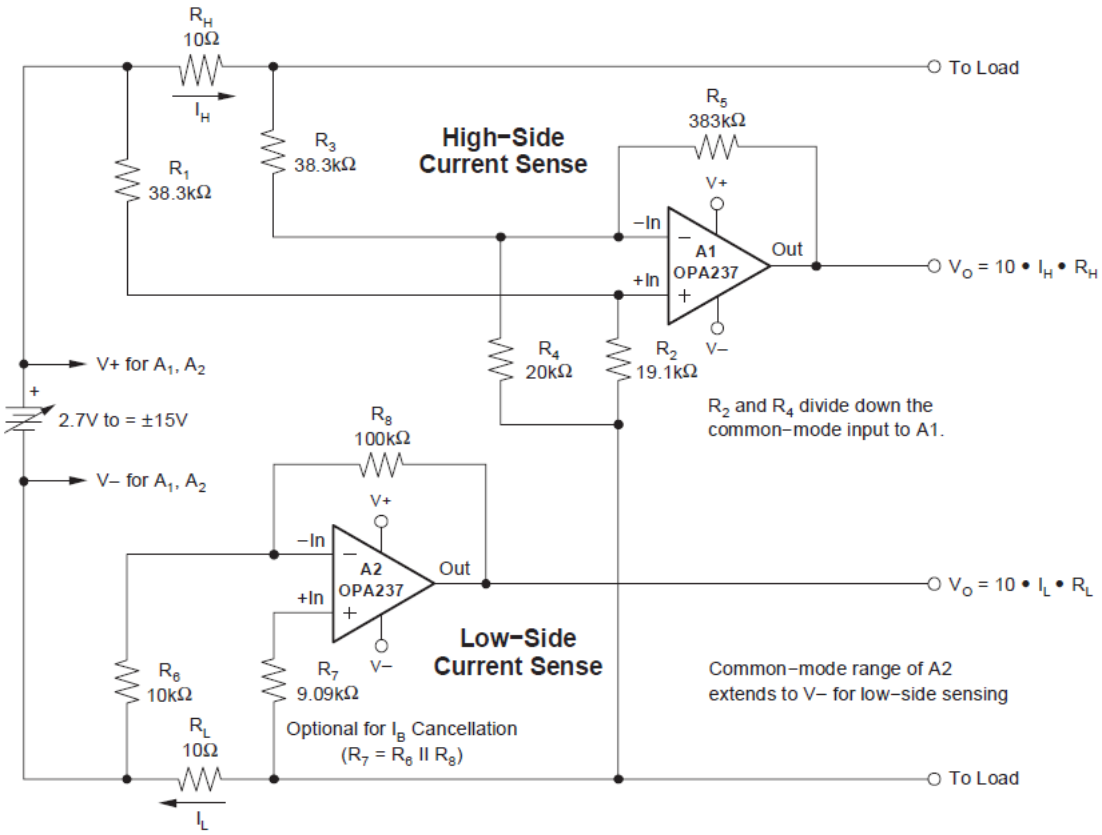
6.2 Typical Application



Note: Low-side and high−side sensing circuits can be used independently.

Figure 6-1. Low-Side and High-Side Battery Current Sensing

6.2.1 Application Curve

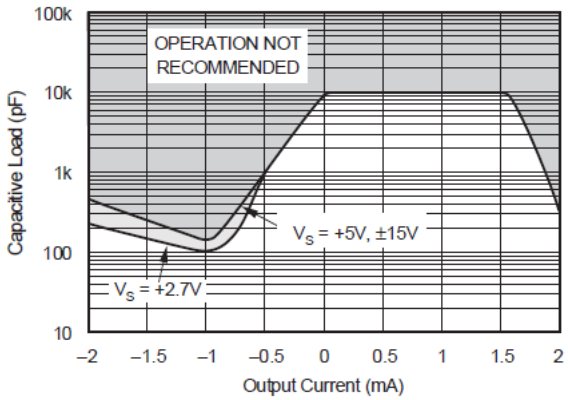


Figure 6-2. Stability-Capacitive Load vs Output Current

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2007) to Revision B (April 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed quiescent current unit from µV to µA in *Features*	1
• Updated *Pin Configurations and Functions* to latest standards and added *Pin Functions* tables	3
• Added input current to *Absolute Maximum Ratings*	4
• Added *Recommended Operating Conditions*	4
• Added *Thermal Information*	4
• Updated junction-to-ambient thermal resistance for OPA237 packages	4
• Updated junction-to-ambient thermal resistance for OPA2237 packages	4
• Updated all *Electrical Characteristics* tables to latest format	5
• Added test condition $V_O = V_S/2$	5
• Changed maximum input offset voltage from ±750µV to ±950µV	5
• Deleted table note "Specified by wafer-level test to 95% confidence"	5
• Changed maximum input offset voltage drift from 5µV/°C to 7.5µV/°C	5
• Updated table note 1	5
• Updated V_{CM} range format to refer to rails	5
• Changed minimum common-mode rejection ratio from 75dB to 71dB	5
• Changed differential input impedance from $5 \cdot 10^6 \Omega$ to 5MΩ	5
• Changed common-mode input impedance from $5 \cdot 10^9 \Omega$ to 5TΩ	5
• Changed minimum open-loop voltage gain from 80dB to 75dB	5

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- Changed test condition for open-loop voltage gain from 0.5V to 0.55V....5
- Changed typical slew rate from 0.5V/µs to 0.45V/µs....5
- Added V– to negative rail rows and moved positive and negative labels to test condtions for voltage output...5
- Changed test condition of voltage output for R_L = 100kΩ from "Ground" to V–....5
- Changed maximum voltage output for R_L = 100kΩ from negative rail from 0.01V to (V–) + 0.05V....5
- Updated short circuit current to show separated rows for source and sink....5
- Changed short-circuit sourcing current from 3.5mA to 7mA....5
- Changed short-circuit sinking current from –5mA to –10mA....5
- Changed typical quiescent current from 160µA to 150µA....5
- Added test condition $V_O = V_S/2$....6
- Deleted table note "Specified by wafer-level test to 95% confidence"....6
- Changed channel separation from 0.5µV/V to 1µV/V....6
- Updated table note 1....6
- Updated V_{CM} range format to refer to rails....6
- Changed minimum common-mode rejection ratio for from 78dB to 76dB....6
- Changed differential input impedance from $5 \cdot 10^6$Ω to 5MΩ....6
- Changed common-mode input impedance from $5 \cdot 10^9$Ω to 5TΩ....6
- Changed typical slew rate from 0.5V/µs to 0.45V/µs....6
- Added V– to negative rail rows and moved positive and negative labels to test conditions for voltage output..6
- Changed test condition of voltage output for RL = 100kΩ from "Ground" to V–....6
- Changed minimum voltage output from positive rail from (V+) – 1V to (V+) – 1.5V....6
- Changed maximum voltage output from negative rail from (V–) + 0.01V to (V–) + 0.1V....6
- Changed minimum voltage output from positive rail from (V+) – 1V to (V+) – 1.5V....6
- Changed maximum voltage output from negative rail from (V–) + 0.5V to (V–) + 0.6V....6
- Updated short circuit current to show separated rows for source and sink....6
- Changed short-circuit sourcing current from 4mA to 8mA....6
- Added test condition $V_O = V_S/2$....7
- Changed test condition for input offset voltage from V_{CM} = 0V to $V_{CM} = V_S/2$....7
- Deleted table note "Specified by wafer-level test to 95% confidence"....7
- Changed channel separation from 0.5µV/V to 1µV/V....7
- Updated table note 1....7
- Changed test condition for input bias current from V_{CM} = 0V to $V_{CM} = V_S/2$....7
- Changed test condition for input offset current from V_{CM} = 0V to $V_{CM} = V_S/2$....7
- Changed input current noise density from 60fA/$\sqrt{Hz}$ to 80fA/$\sqrt{Hz}$ 7
- Updated V_{CM} range format to refer to rails....7
- Changed differential input impedance from $5 \cdot 10^6$Ω to 5MΩ....7
- Changed common-mode input impedance from $5 \cdot 10^9$Ω to 5TΩ....7
- Changed slew rate from 0.5V/µs to 0.44V/µs....7
- Changed settling time in 0.1% from 18µs to 20µs....7
- Changed settling time in 0.01% from 21µs to 24µs....7
- Added V– to negative rail rows and moved positive and negative labels to test condtions for voltage output...7
- Updated short circuit current to show separated rows for source and sink....7
- Changed short-circuit sourcing current from 4.5mA to 9.5mA....7
- Changed short-circuit sinking current from –8mA to –10mA....7
- Deleted ± sign from quiescent current spec....7

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2237EA/2K5	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 85	B37A
OPA2237EA/2K5.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 85	B37A
OPA2237EA/2K5.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Level-2-260C-1 YEAR	-40 to 85	B37A
OPA2237UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	(OP2237, OPA) 2237UA
OPA2237UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	(OP2237, OPA) 2237UA
OPA2237UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	(OP2237, OPA) 2237UA
OPA2237UAE4	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	See OPA2237UA	
OPA237NA/3K	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 70	A37A
OPA237NA/3K.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A
OPA237NA/3K.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A
OPA237NA/3K1G4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A
OPA237NA/3K1G4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A
OPA237UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 70	(OP237, OPA) 237UA
OPA237UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 70	(OP237, OPA) 237UA
OPA237UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 70	(OP237, OPA) 237UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

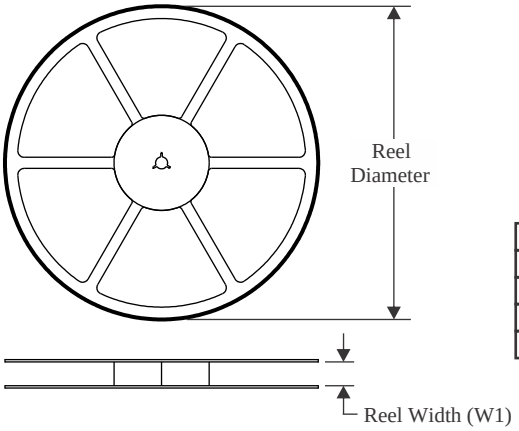
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

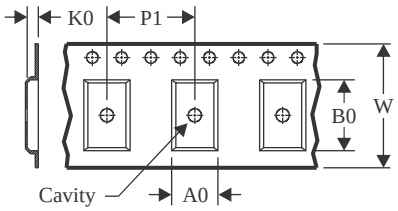
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

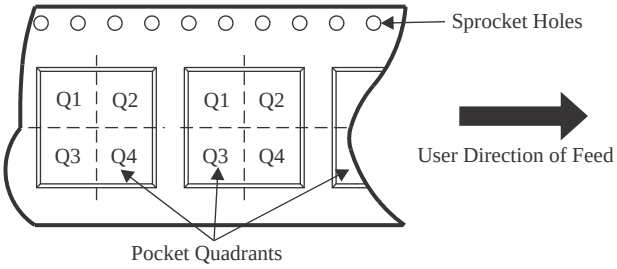


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

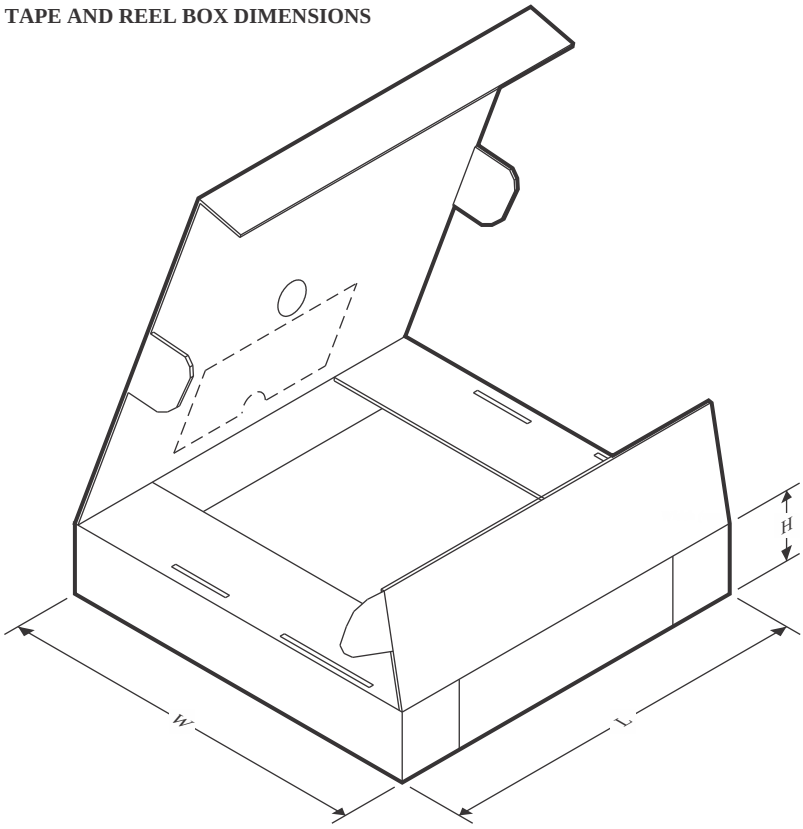
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

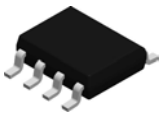
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2237EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2237UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA237NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA237NA/3K	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA237NA/3K1G4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA237UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2237EA/2K5	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2237UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA237NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA237NA/3K	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA237NA/3K1G4	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA237UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

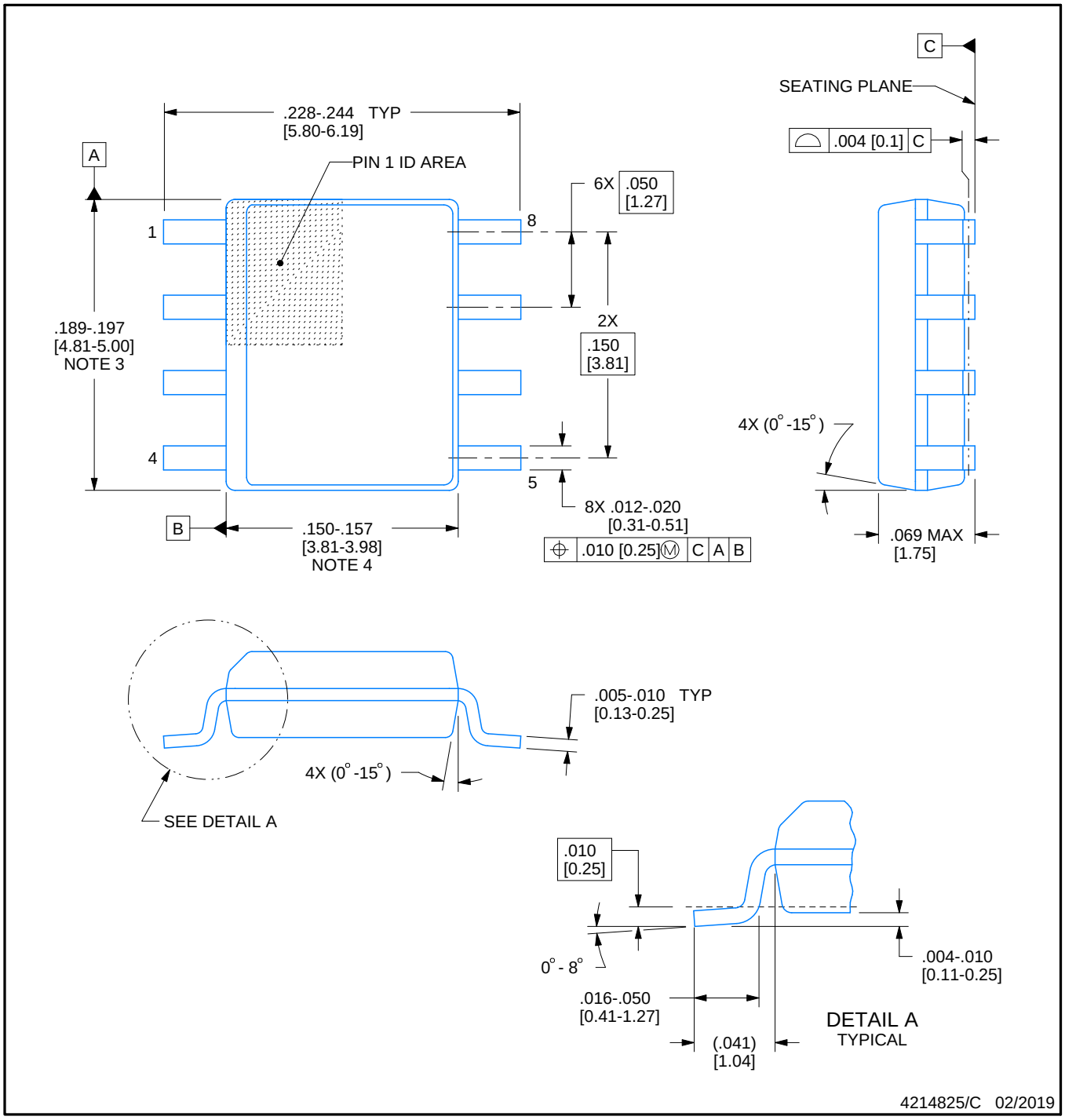


PACKAGE OUTLINE

D0008A

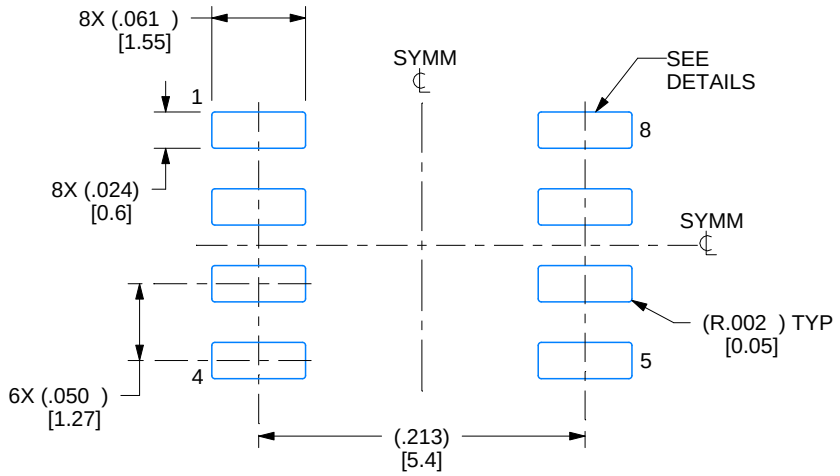
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

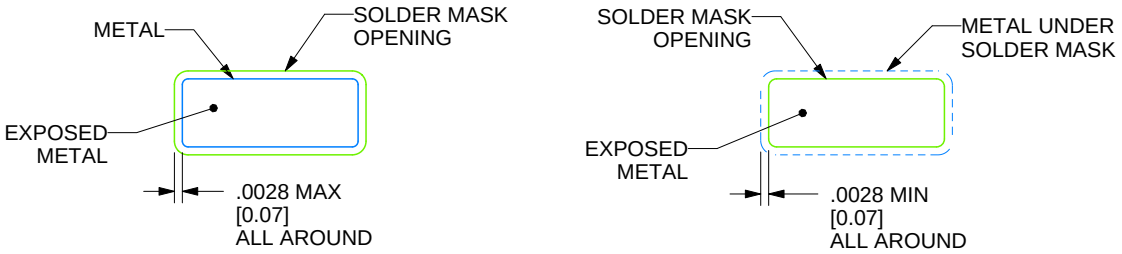


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

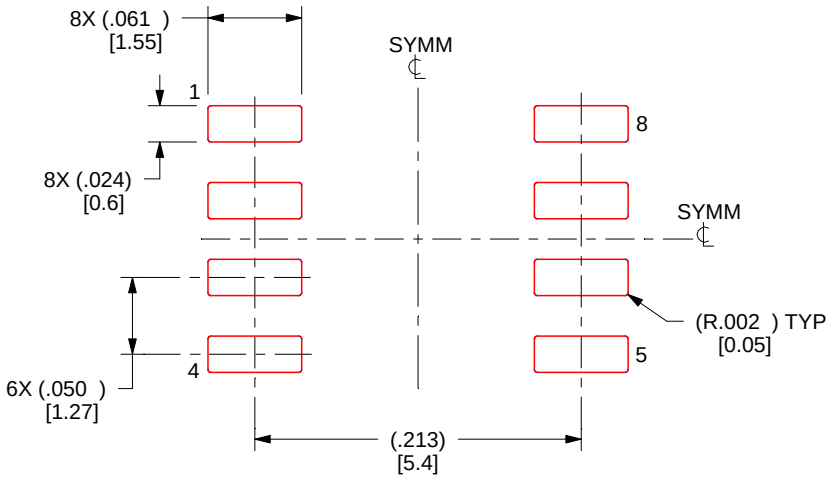


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

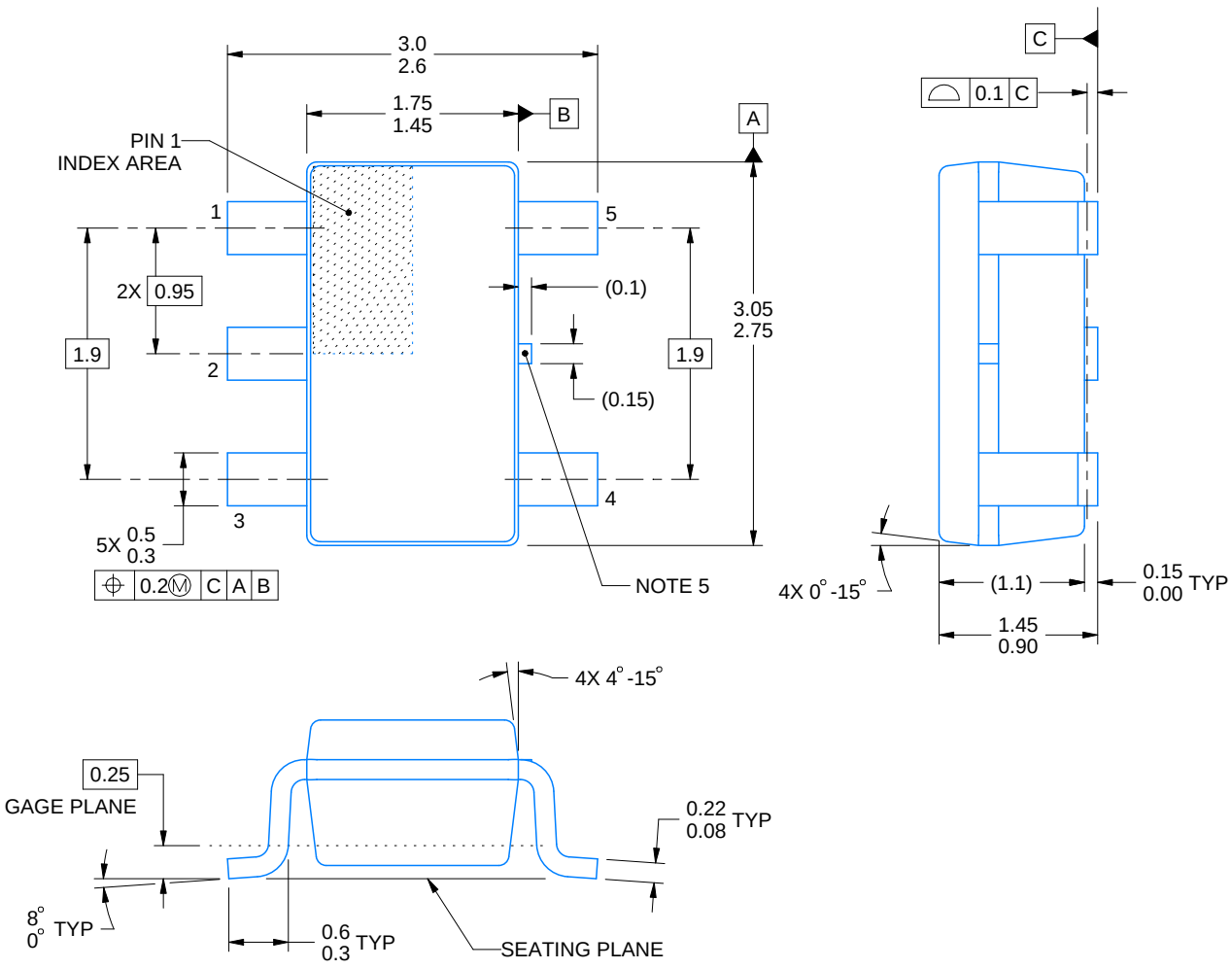


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

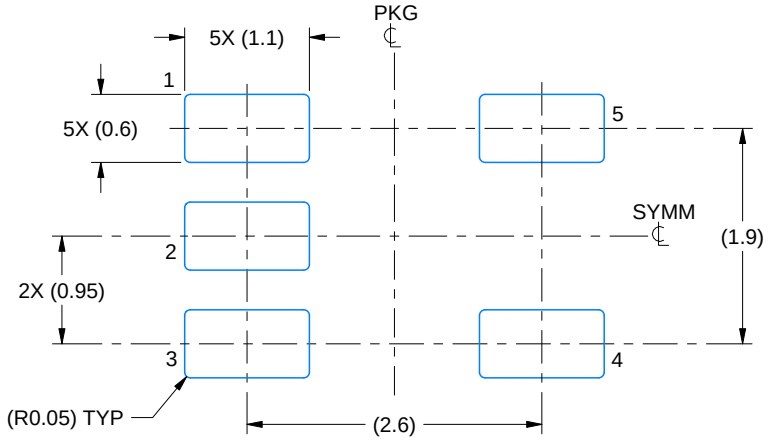
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



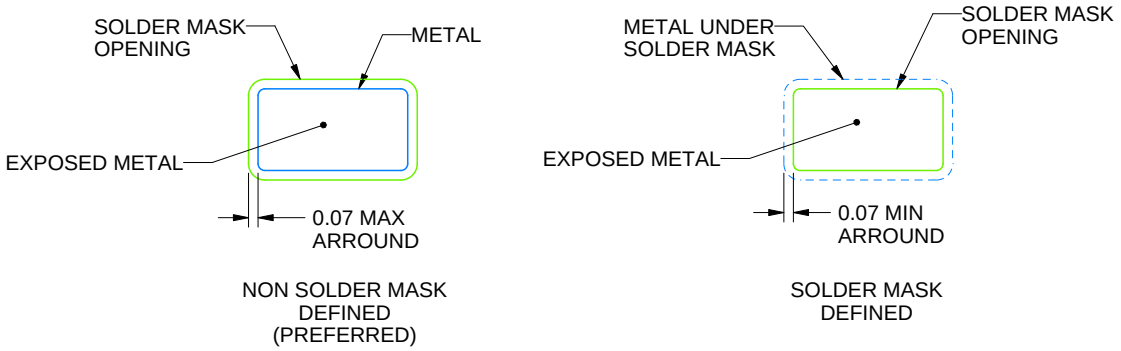
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

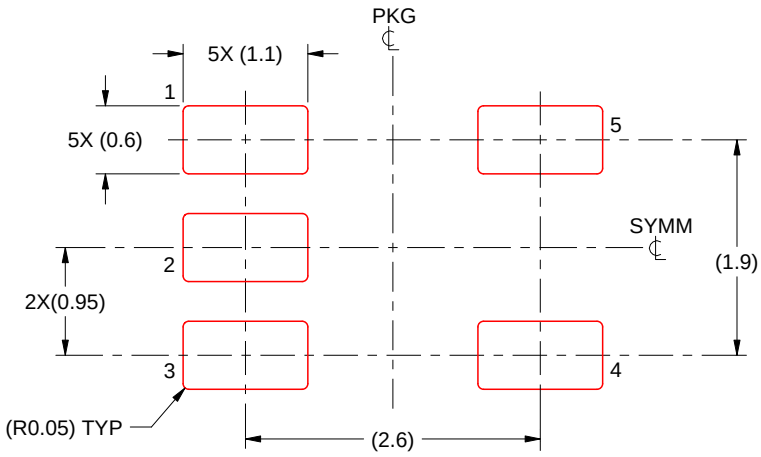


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

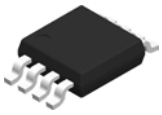
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

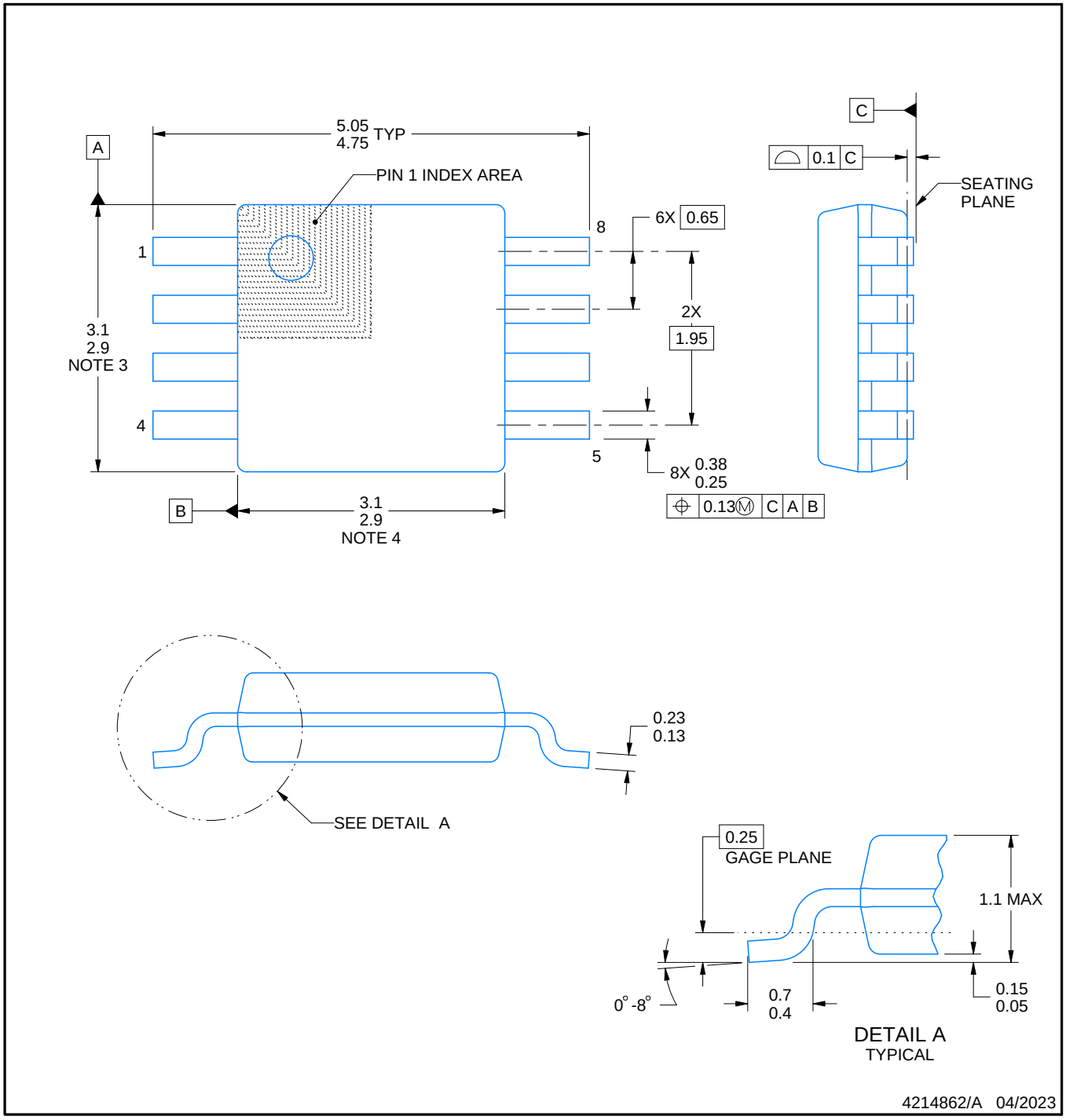
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

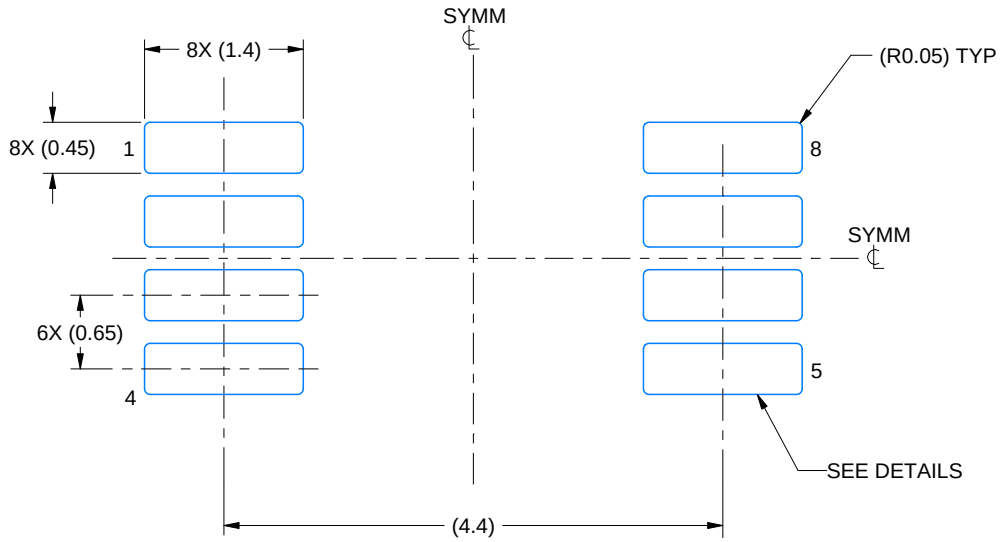
SMALL OUTLINE PACKAGE



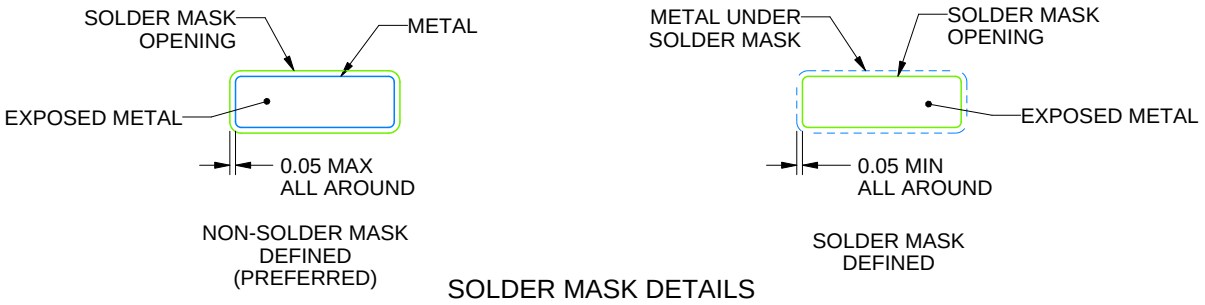
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

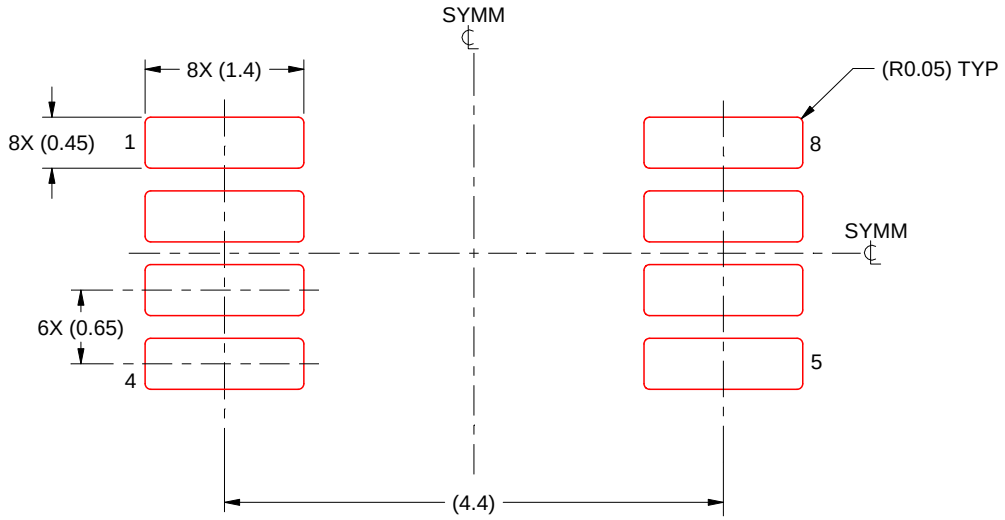


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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