TEXAS INSTRUMENTS

OPA350, OPA2350, OPA4350

SBOS099D – SEPTEMBER 2000 – REVISED DECEMBER 2015

OPAx350 High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier Series

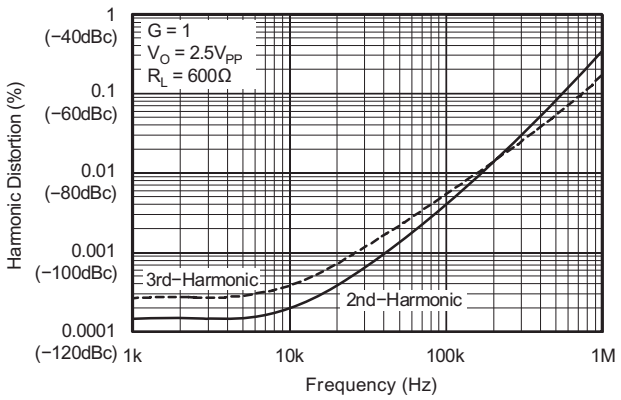
1 Features

- Rail-to-Rail Input
- Rail-to-Rail Output (Within 10 mV)
- Wide Bandwidth: 38 MHz
- High Slew Rate: 22 V/μs
- Low Noise: 5 nV/√Hz
- Low THD+Noise: 0.0006%
- Unity-Gain Stable
- MicroSize Packages
- Single, Dual, and Quad

2 Applications

- Cell Phone PA Control Loops
- Driving A/D Converters
- Video Processing
- Data Acquisition
- Process Controls
- Audio Processing
- Communications
- Active Filters
- Test Equipment

OPAx350 Harmonic Distortion



3 Description

The OPA350 series of rail-to-rail CMOS operational amplifiers are optimized for low voltage, single-supply operation. Rail-to-rail input and output, low noise (5 nV/√Hz), and high speed operation (38 MHz, 22 V/μs) make the amplifiers ideal for driving sampling Analog-to-Digital (A/D) converters. They are also suited for cell phone PA control loops and video processing (75-Ω drive capability), as well as audio and general purpose applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

The OPA350 series operates on a single supply as low as 2.5 V, with an input common-mode voltage range that extends 300 mV below ground and 300 mV above the positive supply. Output voltage swing is to within 10 mV of the supply rails, with a 10-kΩ load. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

The single (OPA350) and dual (OPA2350) come in the miniature MSOP-8 surface mount, SO-8 surface mount, and DIP-8 packages. The quad (OPA4350) packages are in the space-saving SSOP-16 surface mount and SO-14 surface mount. All are specified from −40°C to 85°C and operate from −55°C to 150°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA350	MSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm
OPA2350	MSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm
OPA4350	SSOP (16)	3.90 mm × 4.90 mm
	SOIC (14)	3.91 mm × 8.65 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

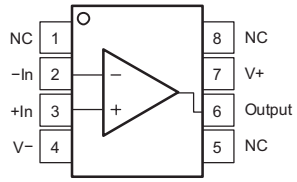
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2005) to Revision D	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

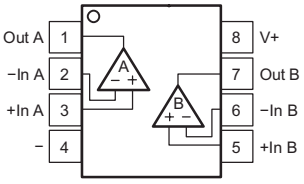
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5 Pin Configuration and Functions

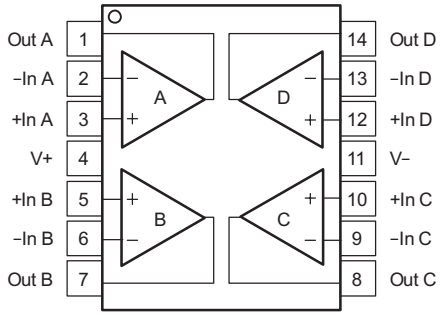
OPA350: P, D, and DGK Packages
8-Pin PDIP, SOIC, and VSSOP
Top View



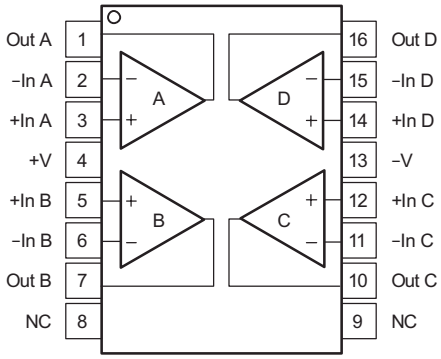
OPA2350: P, D, and DGK Packages
8-Pin PDIP, SOIC, and VSSOP
Top View



D Package
14-Pin SOIC
Top View



DBQ Package
16-Pin SSOP
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	OPA350 NO.	OPA2350 NO.	OPA4350 SO-14 NO.	OPA4350 SSOP NO.		
NC	1, 5, 8	—	—	8, 9	—	No internal connection
–In	2	—	—	—	I	Inverting input
+In	3	—	—	—	I	Noninverting input
V–	4	4	11	13	I	Negative power supply
Output	6	—	—	—	O	Output
V+	7	8	4	4	I	Positive power supply
Out A	—	1	1	1	O	Output channel A
–In A	—	2	2	2	I	Inverting input channel A
+In A	—	3	3	3	I	Noninverting input channel A
+In B	—	5	5	5	I	Noninverting input channel B
–In B	—	6	6	6	I	Inverting input channel B
Out B	—	7	7	7	O	Output channel B
Out C	—	—	8	10	O	Output channel C
–In C	—	—	9	11	I	Inverting input channel C
+In C	—	—	10	12	I	Noninverting input channel C
+In D	—	—	12	14	I	Noninverting input channel D
–In D	—	—	13	15	I	Inverting input channel D
Out D	—	—	14	16	O	Output channel D

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Supply voltage			7	V
	Signal input terminals(2)	Voltage	(V−) − 0.3	(V+) + 0.3	V
		Current		10	mA
	Open short circuit current(3)		Continuous		
	Operating temperature		–55	150	°C
	Lead temperature (soldering, 10 s)			300	°C
	Junction temperature			150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
OPA350, OPA2350, OPA4350 (ALL PACKAGE TYPES)				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
OPA350, OPA2350, OPA4350 (SOIC PACKAGES ONLY)				
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Power supply voltage, (V+)-(V-)	2.7 (±1.35)	5 (±2.5)	5.5 (±2.75)	V
Specified temperature	–40	25	85	°C
Operating temperature	–55	25	150	°C

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6.4 Thermal Information: OPA350 and OPA2350

THERMAL METRIC[1]		OPA350, OPA2350			UNIT
		DGK (VSSOP)	P (PDIP)	D (SOIC)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.2	53.1	140.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.8	42.5	89.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	89.8	30.3	80.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.5	19.7	28.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.2	30.2	80.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA4350

THERMAL METRIC[1]		OPA4350		UNIT
		D (SOIC)	DBQ (SSOP)	
		14 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.8	115.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	67	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	58.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	19.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	57.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.6 Electrical Characteristics

V_S = 2.7 V to 5.5 V; All specifications at T_A = 25°C, R_L = 1 kΩ connected to V_S/2 and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		V_S = 5 V		±150	±500	µV
		T_A = −40°C to 85°C				±1	mV
		vs Temperature	T_A = –40°C to 85°C		±4		µV/°C
PSRR	vs Power-supply rejection ratio		V_S = 2.7 V to 5.5 V, V_{CM} = 0 V		40	150	µV/V
						175	
	Channel separation (dual, quad)		DC		0.15		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±0.5	±10	pA
		vs Temperature			See *Typical Characteristics*		
I_{OS}	Input offset current				±0.5	±10	pA
NOISE							
	Input voltage noise, f = 100 Hz to 400 kHz				4		µVrms
e_n	Input voltage noise density, f = 10 kHz				7		nV/√Hz
	Input current noise density, f = 100 kHz				5		nV/√Hz
i_n	Current noise density, f = 10 kHz				4		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range		T_A = −40°C to 85°C	–0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio		V_S = 2.7 V, −0.1 V < V_{CM} < 2.8 V	66	84		dB
			V_S = 5.5 V, −0.1 V < V_{CM} < 5.6 V	74	90		
			T_A = −40°C to 85°C, V_S = 5.5 V, −0.1 V < V_{CM} < 5.6 V	74			
INPUT IMPEDANCE							
	Differential				10^{13} || 2.5		Ω || pF
	Common-mode				10^{13} || 6.5		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		R_L = 10 kΩ, 50 mV < V_O < (V+) –50 mV	100	122		dB
		T_A = –40°C to 85°C	R_L = 10 kΩ, 50 mV < V_O < (V+) –50 mV	100			
			R_L = 1 kΩ, 200 mV < V_O < (V+) –200 mV	100	120		
			R_L = 1 kΩ, 200 mV < V_O < (V+) –200 mV	100			
FREQUENCY RESPONSE (C_L = 100 pF)							
GBW	Gain-bandwidth product		G = 1		38		MHz
SR	Slew rate		G = 1		22		V/µs
	Settling time	0.1%	G = ±1, 2-V Step		0.22		µs
		0.01%			0.5		
	Overload recovery time		V_{IN} × G = V_S		0.1		µs
THD+N	Total harmonic distortion + noise		R_L = 600 Ω, V_O = 2.5 V_{PP}(2), G = 1, f = 1 kHz		0.0006%		
	Differential gain error		G = 2, R_L = 600 Ω, V_O = 1.4 V(3)		0.17%		
	Differential phase error		G = 2, R_L = 600 Ω, V_O = 1.4 V(3)		0.17		°
OUTPUT							
V_{OUT}	Voltage output swing from rail(4)		R_L = 10 kΩ, A_{OL} ≥ 100 dB		10	50	mV
		T_A = –40°C to 85°C	R_L = 10 kΩ, A_{OL} ≥ 100 dB			50	
			R_L = 1 kΩ, A_{OL} ≥ 100 dB		25	200	
I_{OUT}	Output current				±40(5)		mA
I_{SC}	short circuit current				±80		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		

(1) V_S = 5 V
(2) V_{OUT} = 0.25 V to 2.75 V
(3) NTSC signal generator used. See Figure 31 for test circuit.
(4) Output voltage swings are measured between the output and power supply rails.
(5) See Figure 17.

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Electrical Characteristics (continued)

V_S = 2.7 V to 5.5 V; All specifications at T_A = 25°C, R_L = 1 kΩ connected to $V_S/2$ and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
POWER SUPPLY							
V_S	Operating voltage range		T_A = −40°C to 85°C	2.7		5.5	V
	Minimum operating voltage				2.5		V
I_Q	Quiescent current (per amplifier)		I_O = 0		5.2	7.5	mA
		T_A = –40°C to 85°C				8.5	
TEMPERATURE RANGE							
	Specified range			–40		85	°C
	Operating range			–55		150	°C

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6.7 Typical Characteristics

All specifications at T_A = 25°C, V_S = 5 V, and R_L = 1 kΩ connected to V_S/2, unless otherwise noted.

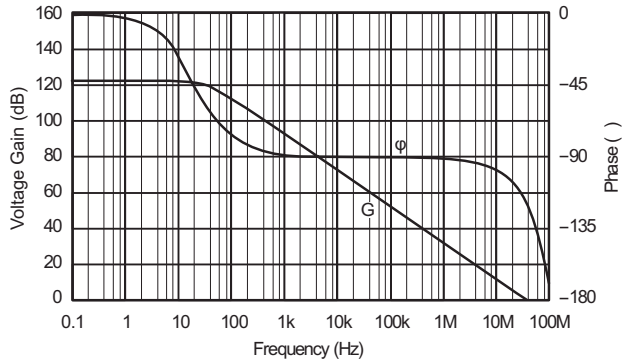


Figure 1. Open-Loop Gain and Phase vs Frequency

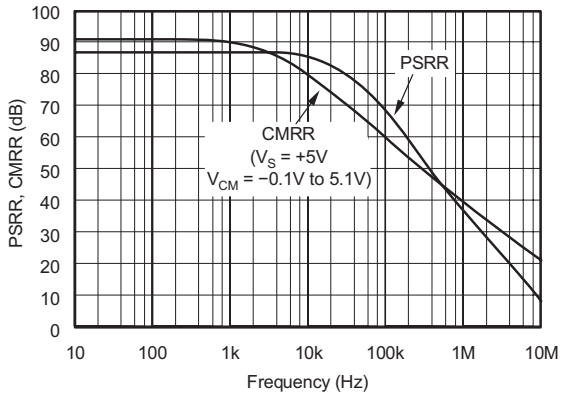


Figure 2. Power Supply and Common-Mode Rejection Ratio vs Frequency

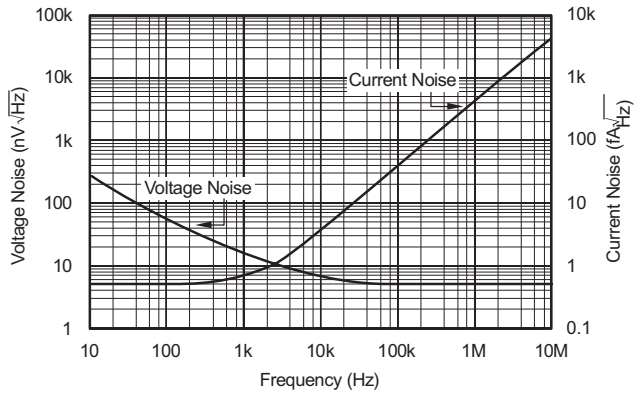


Figure 3. Input Voltage and Current Noise Spectral Density vs Frequency

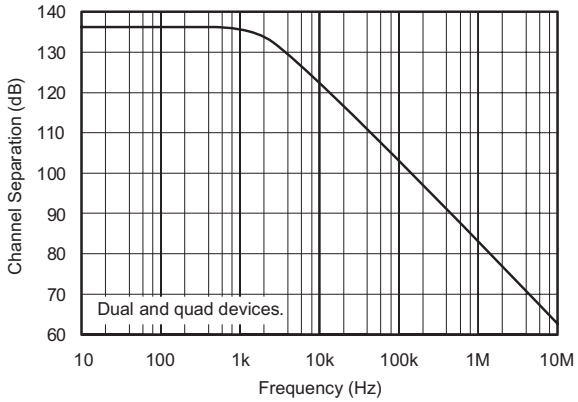


Figure 4. Channel Separation vs Frequency

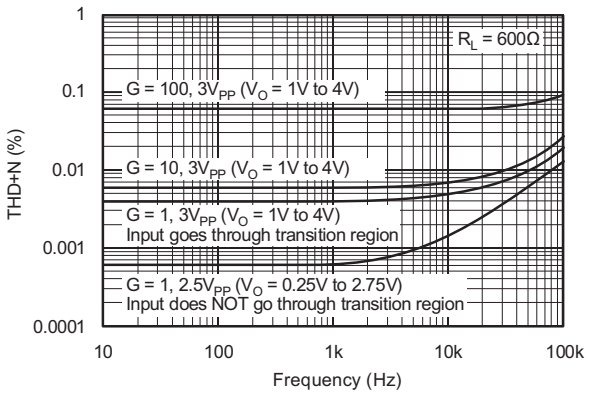


Figure 5. Total Harmonic Distortion + Noise vs Frequency

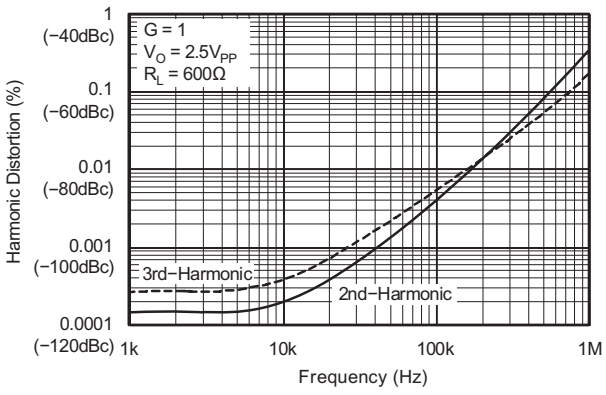


Figure 6. Harmonic Distortion + Noise vs Frequency

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Typical Characteristics (continued)

All specifications at T_A = 25°C, V_S = 5 V, and R_L = 1 kΩ connected to V_S/2, unless otherwise noted.

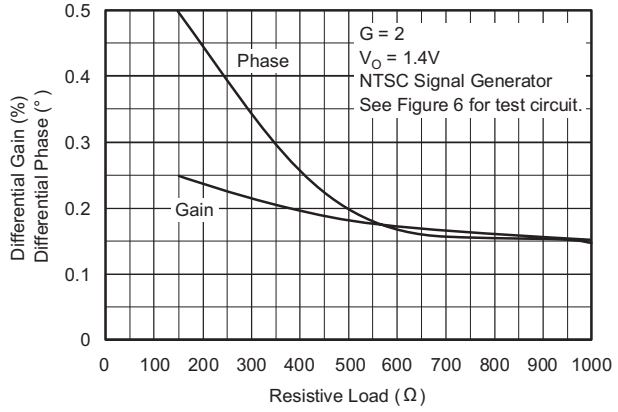


Figure 7. Differential Gain and Phase vs Resistive Load

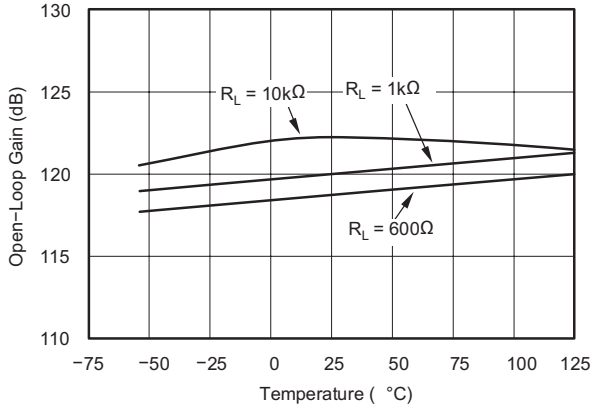


Figure 8. Open-Loop Gain vs Temperature

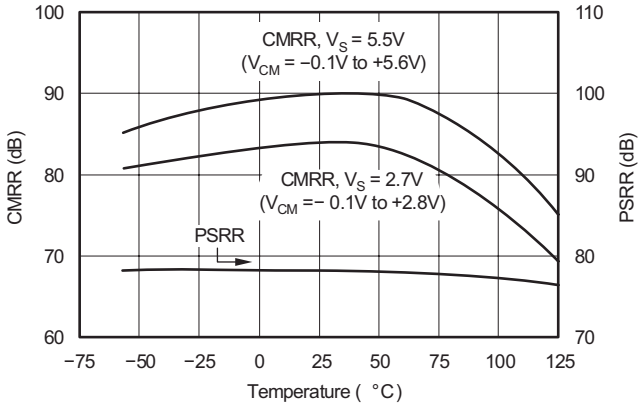


Figure 9. Common-Mode and Power-Supply Rejection Ratio vs Temperature

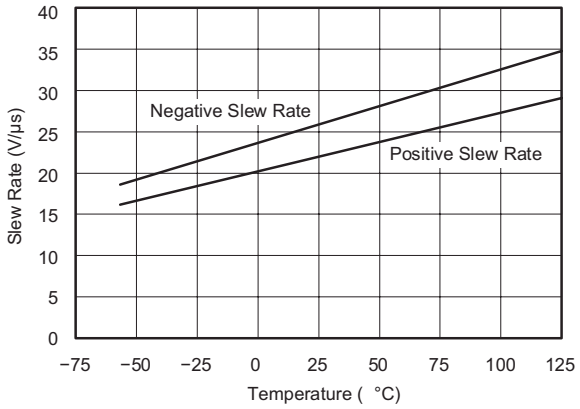


Figure 10. Slew Rate vs Temperature

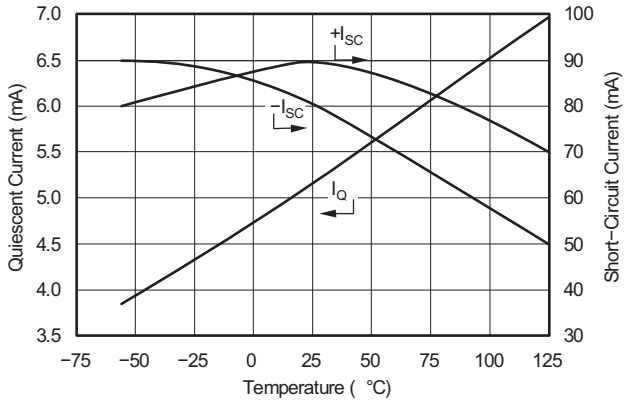


Figure 11. Quiescent Current and short circuit Current vs Temperature

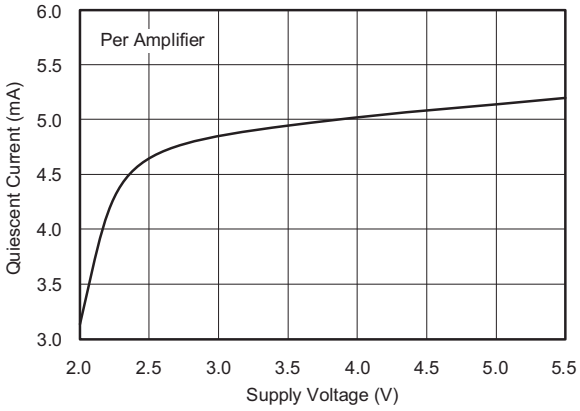


Figure 12. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

All specifications at T_A = 25°C, V_S = 5 V, and R_L = 1 kΩ connected to V_S/2, unless otherwise noted.

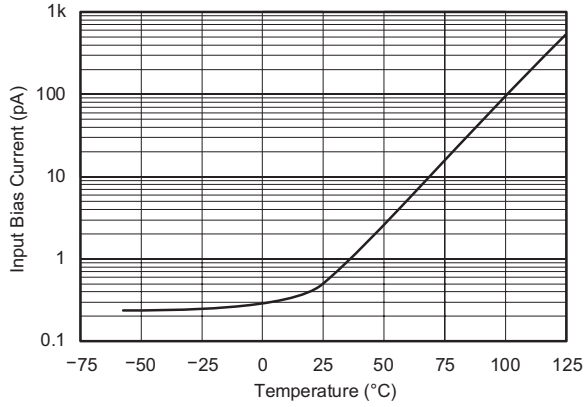


Figure 13. Input Bias Current vs Temperature

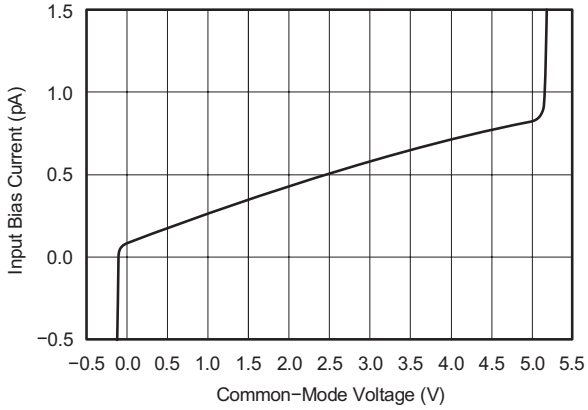


Figure 14. Input Bias Current vs Input Common-Mode Voltage

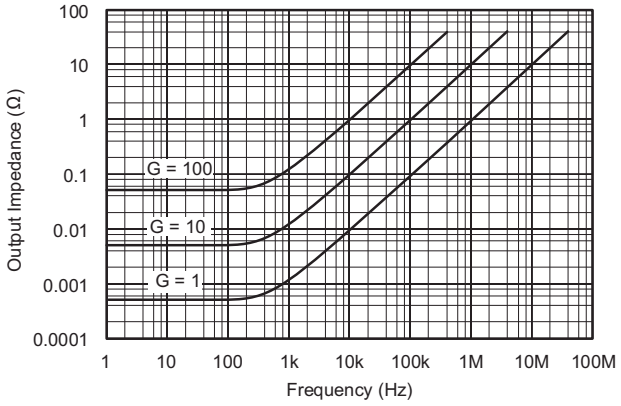


Figure 15. Closed-Loop Output Impedance vs Frequency

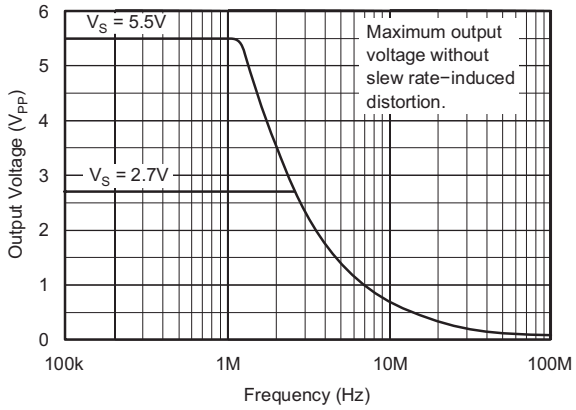


Figure 16. Maximum Output Voltage vs Frequency

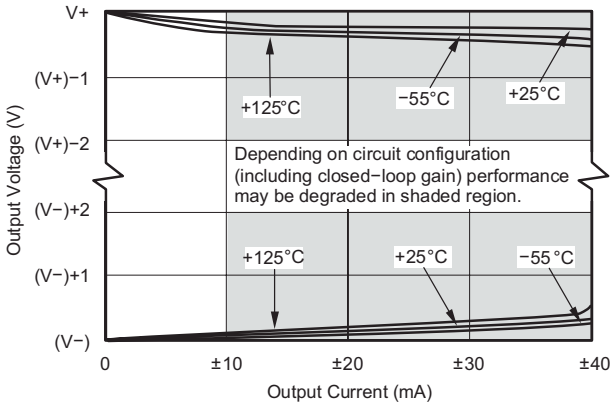


Figure 17. Output Voltage Swing vs Output Current

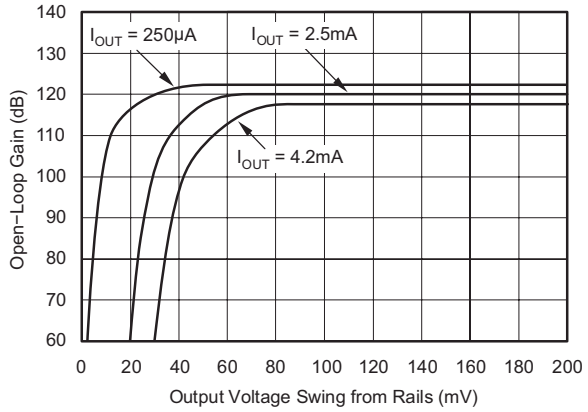


Figure 18. Open-Loop Gain vs Output Voltage Swing

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Typical Characteristics (continued)

All specifications at T_A = 25°C, V_S = 5 V, and R_L = 1 kΩ connected to V_S/2, unless otherwise noted.

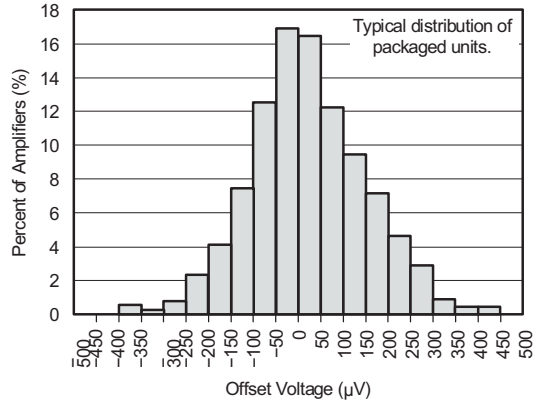


Figure 19. Offset Voltage Production Distribution

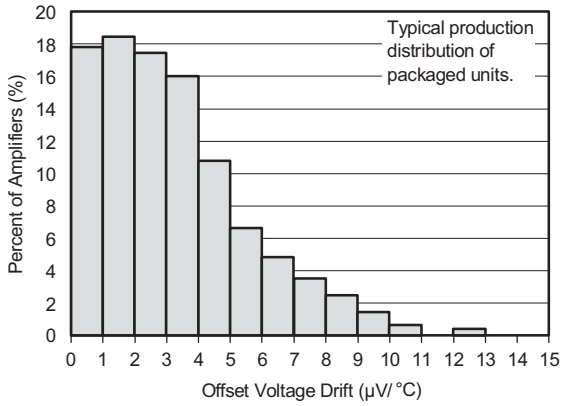


Figure 20. Offset Voltage Drift Production Distribution

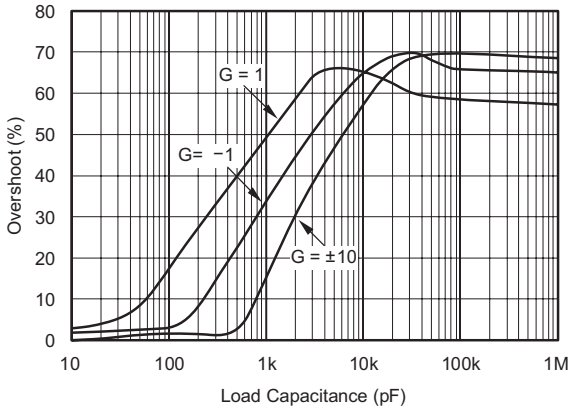


Figure 21. Small-Signal Overshoot vs Load Capacitance

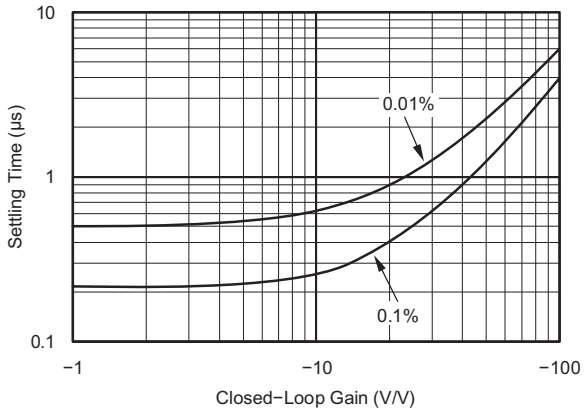


Figure 22. Settling Time vs Closed-Loop Gain

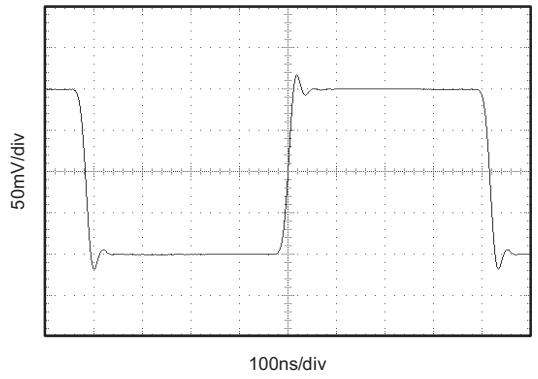


Figure 23. Small-Signal Step Response
C_L = 100 pF

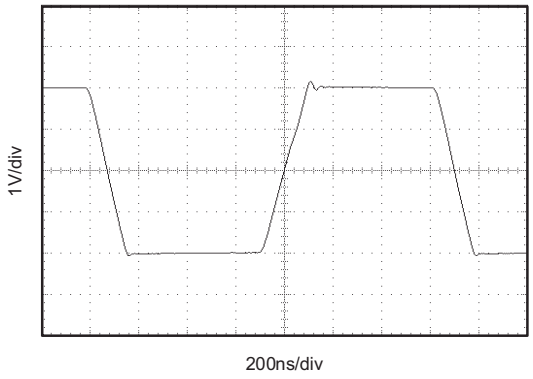


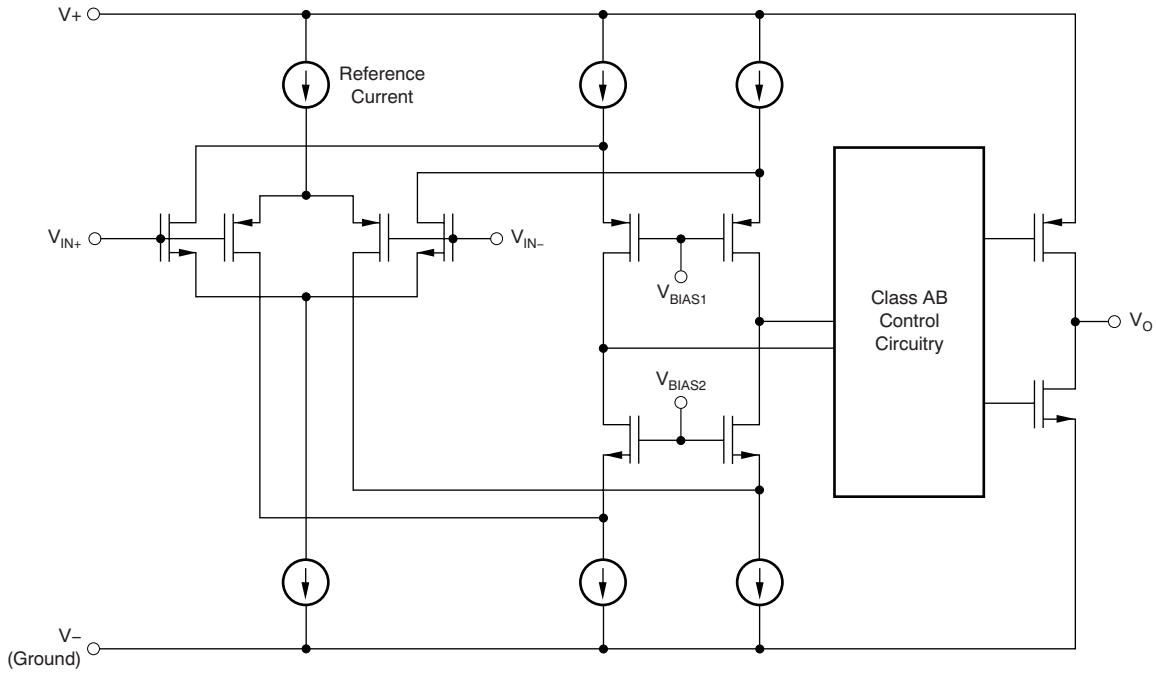
Figure 24. Large-Signal Step Response
C_L = 100 pF

7 Detailed Description

7.1 Overview

The OPA350 series rail-to-rail CMOS operational amplifiers are optimized for low voltage, single-supply operation. Rail-to-rail input and output, low noise (5 nV/√Hz), and high speed operation (38 MHz, 22 V/µs) make the amplifiers ideal for driving sampling Analog-to-Digital (A/D) converters. They are also suited for cell phone PA control loops and video processing (75-Ω drive capability), as well as audio and general purpose applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

7.2 Functional Block Diagram



7.3 Feature Description

The OPA350 series of operational amplifiers (op amps) are fabricated on a state-of-the-art 0.6 micron CMOS process. They are unity-gain stable and suitable for a wide range of general purpose applications. Rail-to-rail input and output make them ideal for driving sampling A/D converters. They are also suited for controlling the output power in cell phones. These applications often require high speed and low noise. In addition, the OPA350 series offers a low-cost solution for general-purpose and consumer video applications (75-Ω drive capability).

Excellent AC performance makes the OPA350 series suited for audio applications. Their bandwidth, slew rate, low noise (5 nV/√Hz), low THD (0.0006%), and small package options are ideal for these applications. The class AB output stage is capable of driving 600-Ω loads connected to any point between V+ and ground.

Rail-to-rail input and output swing significantly increases dynamic range, especially in low voltage supply applications. Figure 25 shows the input and output waveforms for the OPA350 in unity-gain configuration. Operation is from a single 5-V supply with a 1-kΩ load connected to $V_S/2$. The input is a 5 V_{PP} sinusoid. Output voltage swing is approximately 4.95 V_{PP}.

Power supply pins should be bypassed with 0.01-µF ceramic capacitors.

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Feature Description (continued)

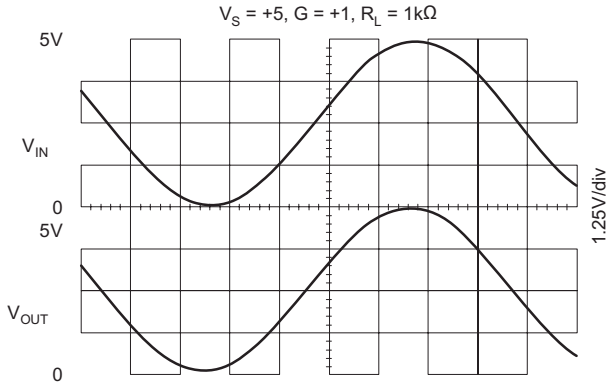


Figure 25. Rail-to-Rail Input and Output

7.3.1 Operating Voltage

OPA350 series operational amplifiers are fully specified from 2.7 V to 5.5 V. Supply voltage may range from 2.5 V to 5.5 V. Parameters are tested over the specified supply range: a feature of the OPA350 series. In addition, many specifications apply from −40°C to 85°C. Most behavior remains virtually unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage or temperature are shown in *Typical Characteristics*.

7.3.2 Rail-to-Rail Input

The tested input common-mode voltage range of the OPA350 series extends 100 mV beyond the supply rails. This is achieved with a complementary input stage: an N-channel input-differential pair in parallel with a P-channel differential pair, as shown in Figure 26. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.8 V to 100 mV above the positive supply, while the P-channel pair is on for inputs from 100 mV below the negative supply to approximately (V+) – 1.8 V. There is a small transition region, typically (V+) – 2 V to (V+) – 1.6 V, in which both pairs are on. This 400-mV transition region can vary ±400 mV with process variation. Thus, the transition region (both input stages on) can range from (V+) – 2.4 V to (V+) – 2 V on the low end, up to (V+) – 1.6 V to (V+) – 1.2 V on the high end.

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Feature Description (continued)

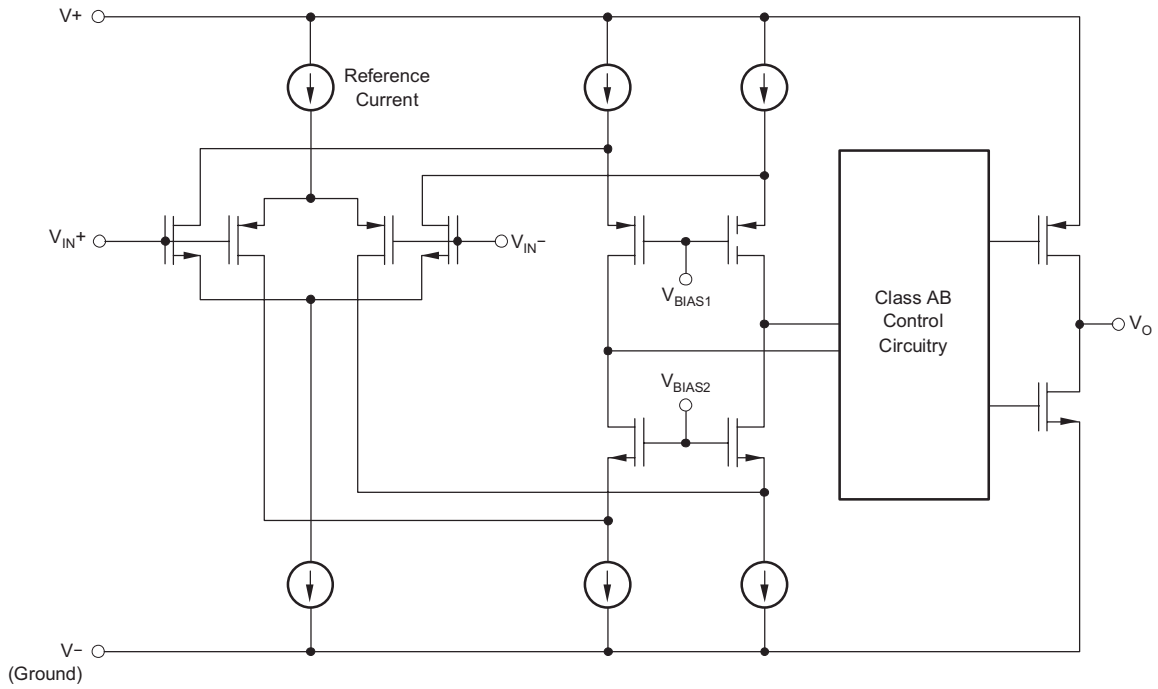


Figure 26. Simplified Schematic

OPA350 series operational amplifiers are laser-trimmed to reduce offset voltage difference between the N-channel and P-channel input stages, resulting in improved common-mode rejection and a smooth transition between the N-channel pair and the P-channel pair. However, within the 400-mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage. Normally, input bias current is approximately 500 fA. However, large inputs (greater than 300 mV beyond the supply rails) can turn on the input protection diodes, causing excessive current to flow in or out of the input pins. Momentary voltages greater than 300 mV beyond the power supply can be tolerated if the current on the input pins is limited to 10 mA. This is easily accomplished with an input resistor, as shown in Figure 27. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required.

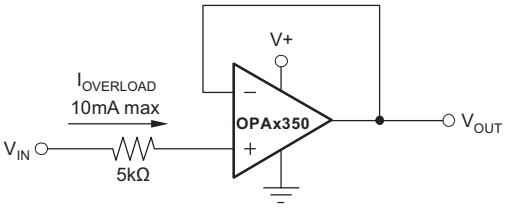


Figure 27. Input Current Protection for Voltages Exceeding the Supply Voltage

7.3.3 Rail-to-Rail Output

A class AB output stage with common-source transistors achieves rail-to-rail output. For light resistive loads (>10 kΩ), the output voltage swing is typically ten millivolts from the supply rails. With heavier resistive loads (600 Ω to 10 kΩ), the output can swing to within a few tens of millivolts from the supply rails and maintain high open-loop gain. See Figure 17 and Figure 18 for more information.

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Feature Description (continued)

7.3.4 Capacitive Load and Stability

OPA350 series operational amplifiers can drive a wide range of capacitive loads. However, all operational amplifiers under certain conditions may become unstable. operational amplifier configuration, gain, and load value are just a few of the factors to consider when determining stability. An operational amplifier in unity-gain configuration is the most susceptible to the effects of capacitive load. The capacitive load reacts with the output impedance of the operational amplifier, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin.

In unity gain, OPA350 series operational amplifiers perform well with large capacitive loads. Increasing gain enhances the ability of the amplifier to drive more capacitance. Figure 21 shows performance with a 1-kΩ resistive load. Increasing load resistance improves capacitive load drive capability.

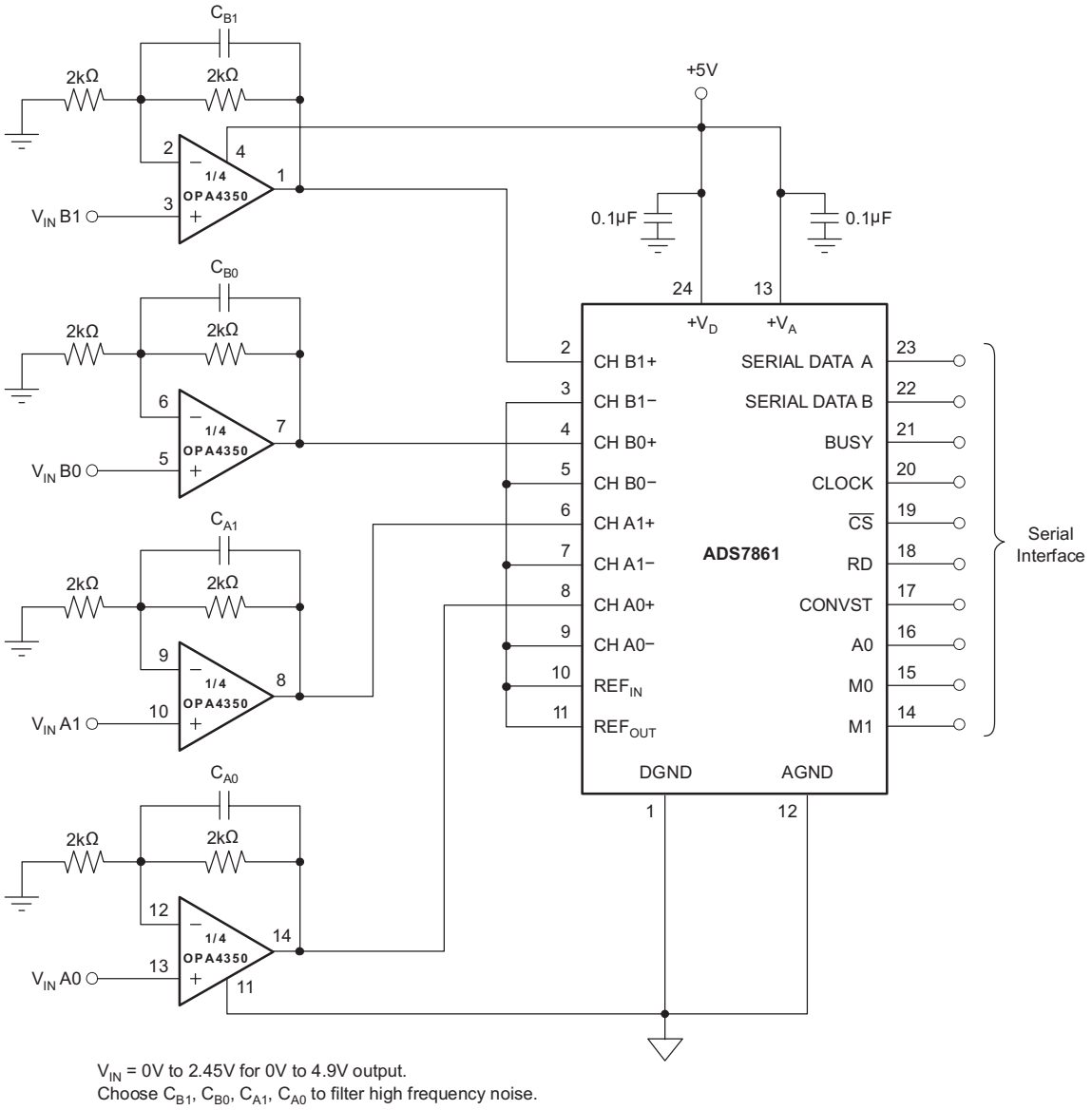
7.3.5 Driving A/D Converters

OPA350 series operational amplifiers are optimized for driving medium speed (up to 500 kHz) sampling A/D converters, and also offer excellent performance for higher speed converters. The OPA350 series provides an effective means of buffering the input capacitance of the A/D and resulting charge injection while providing signal gain.

Figure 28 shows the OPA350 driving an ADS7861. The ADS7861 is a dual, 500 kHz, 12-bit sampling converter in the tiny SSOP-24 package. When used with the miniature package options of the OPA350 series, the combination is ideal for space-limited applications. For further information, consult the ADS7861 data sheet, *Dual, 500kSPS, 12-Bit, 2 + 2 Channel, Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTER* (SBAS110).

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Feature Description (continued)



V_{IN} = 0V to 2.45V for 0V to 4.9V output.
Choose C_{B1}, C_{B0}, C_{A1}, C_{A0} to filter high frequency noise.

Figure 28. OPA4350 Driving Sampling A/D Converter

7.3.6 Output Impedance

The low-frequency open-loop output impedance of the common-source output stage of the OPA350 is approximately 1 kΩ. When the operational amplifier is connected with feedback, this value is reduced significantly by the loop gain of the operational amplifier. For example, with 122 dB of open-loop gain, the output impedance is reduced in unity-gain to less than 0.001 Ω. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount which results in a ten-fold increase in effective output impedance (see Figure 15).

At higher frequencies, the output impedance rises as the open-loop gain of the operational amplifier drops. However, at these frequencies the output also becomes capacitive due to parasitic capacitance. This prevents the output impedance from becoming too high, which can cause stability problems when driving capacitive loads. The OPA350 has excellent capacitive load drive capability for an operational amplifier with its bandwidth.

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7.4 Device Functional Modes

The OPAx350 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (±1.35 V). The maximum power supply voltage for the OPAx350 is 5.5V (±2.75 V).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Low pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPAx350 are ideally suited to construct high speed, high precision active filters. Figure 29 illustrates a second order low pass filter commonly encountered in signal processing applications.

8.2 Typical Applications

8.2.1 Second Order Low Pass Filter

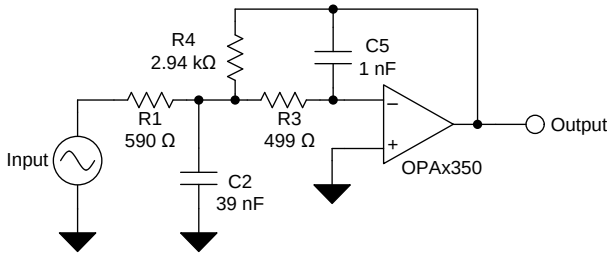


Figure 29. Second Order Low Pass Filter

8.2.1.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain).
- Low pass cutoff frequency = 25 kHz.
- Second order Chebyshev filter response with 3-dB gain peaking in the passband.

8.2.1.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Equation 1. Use Equation 2 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit the gain at DC and the low pass cutoff frequency can be calculated using Equation 2.

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners. Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

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Typical Applications (continued)

8.2.1.3 Application Curve

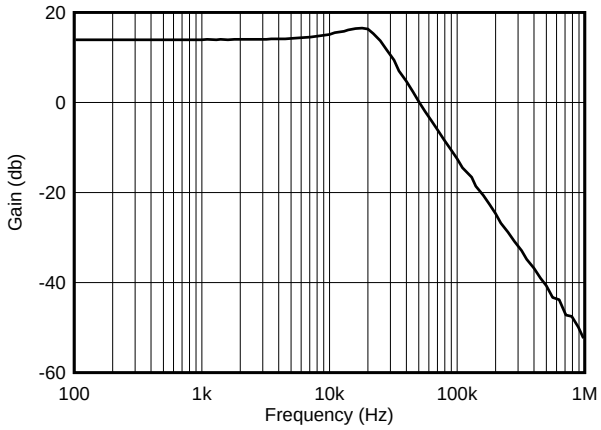


Figure 30. OPAx350 2nd Order 25-kHz, Chebyshev, Low-Pass Filter

8.2.2 Single-Supply Video Line Driver

Figure 31 shows a circuit for a single supply, G = 2 composite video line driver. The synchronized outputs of a composite video line driver extend below ground. As shown, the input to the operational amplifier should be AC-coupled and shifted positively to provide adequate signal swing to account for these negative signals in a single-supply configuration.

The input is terminated with a 75-Ω resistor and AC-coupled with a 47-µF capacitor to a voltage divider that provides the DC bias point to the input. In Figure 31, this point is approximately (V−) + 1.7 V. Setting the optimal bias point requires some understanding of the nature of composite video signals. For best performance, avoid the distortion caused by the transition region of the complementary input stage of the OPA350. See the discussion of rail-to-rail input in *Rail-to-Rail Input*.

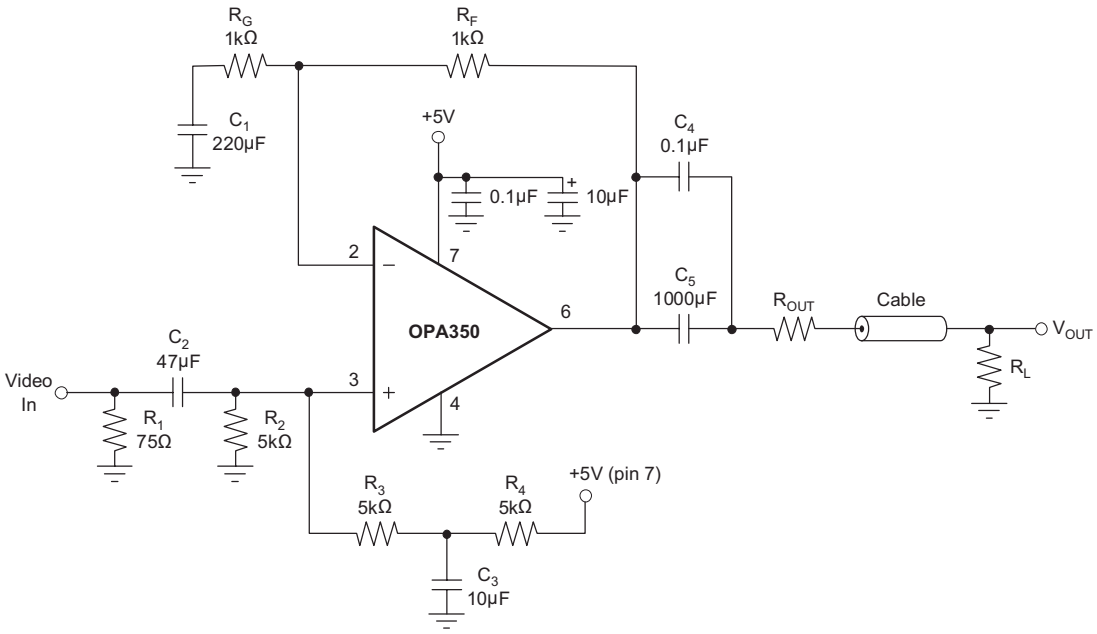


Figure 31. Single-Supply Video Line Driver

Typical Applications (continued)

8.2.3 Adding a Feedback Capacitor to Improve Response

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 32. This capacitor compensates for the zero created by the feedback network impedance and the input capacitance of the OPA350 (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.

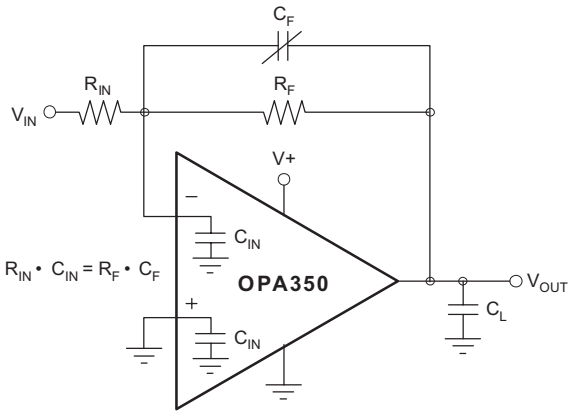


Figure 32. Feedback Capacitor Improves Dynamic Performance

A variable capacitor can be used for the feedback capacitor, because input capacitance may vary between operational amplifiers and layout capacitance is difficult to determine. For the circuit shown in Figure 32, the value of the variable feedback capacitor should be chosen so that the input resistance times the input capacitance of the OPA350 (typically 9 pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$$R_{IN} \times C_{IN} = R_F \times C_F \quad (3)$$

where

- C_{IN} is equal to the input capacitance of the OPA350 (sum of differential and common-mode) plus the layout capacitance.

The capacitor can be varied until optimum performance is obtained.

8.2.4 Two Op-Amp Instrumentation Amplifier With Improved High-Frequency Common-Mode Rejection

The OPAx350 is well suited for high input impedance applications such as an instrumentation amplifier. The two amplifier configuration shown in Figure 33 rejects any common mode signals and senses the small differential input voltage developed by the resistive bridge. The voltage reference sets the output to 2.5 V when the differential signal developed by the bridge is zero. The high common mode rejection versus frequency response of the OPAx350, rejects and common mode noise that may be coupled into the bridge circuit from the bridge excitation source. The gain of the circuit is determined by R_G according to the equation shown in Figure 33.

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Typical Applications (continued)

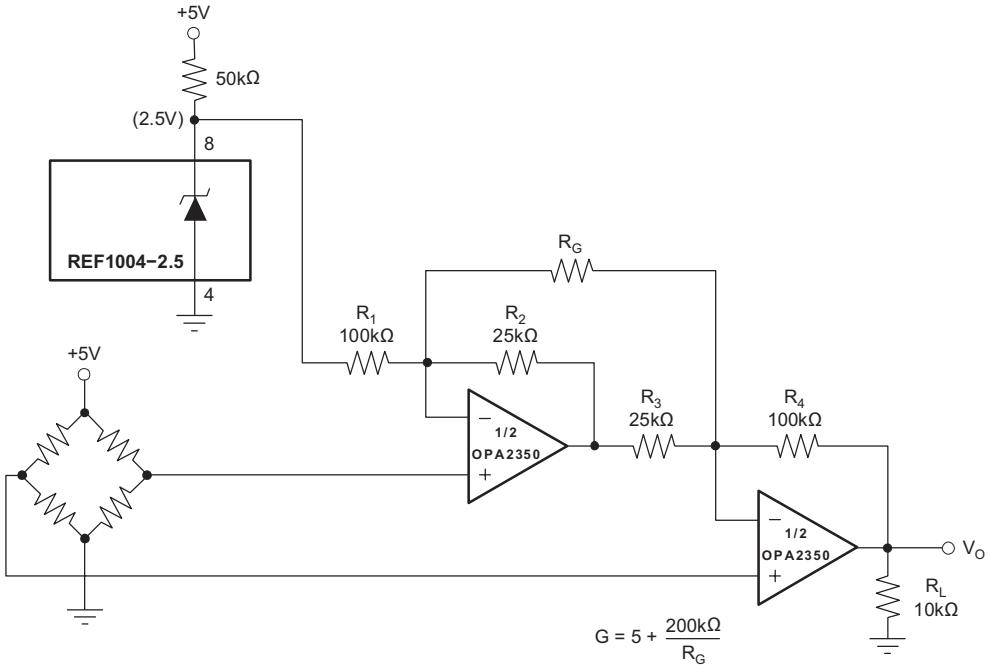


Figure 33. Two Op-Amp Instrumentation Amplifier With Improved High-Frequency Common-Mode Rejection Schematic

8.2.5 10-kHz High-Pass Filter

High-pass filters are used to reject DC signals and low-frequency time varying signals such as drift versus temperature. Figure 34 illustrates a high-pass filter with a 10 kHz low-frequency cutoff frequency.

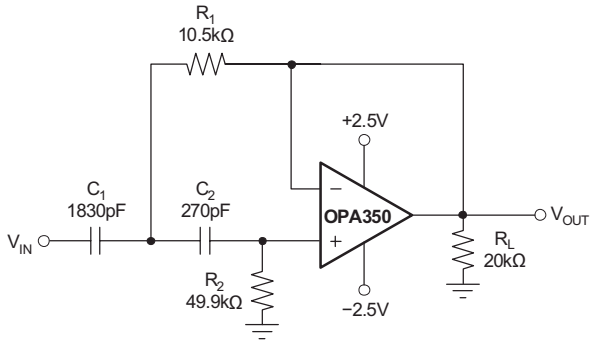


Figure 34. 10-kHz High-Pass Filter

9 Power Supply Recommendations

The OPAx350 are specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.75 V); many specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

10 Layout

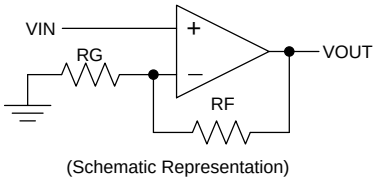
10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 35, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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10.2 Layout Example



(Schematic Representation)

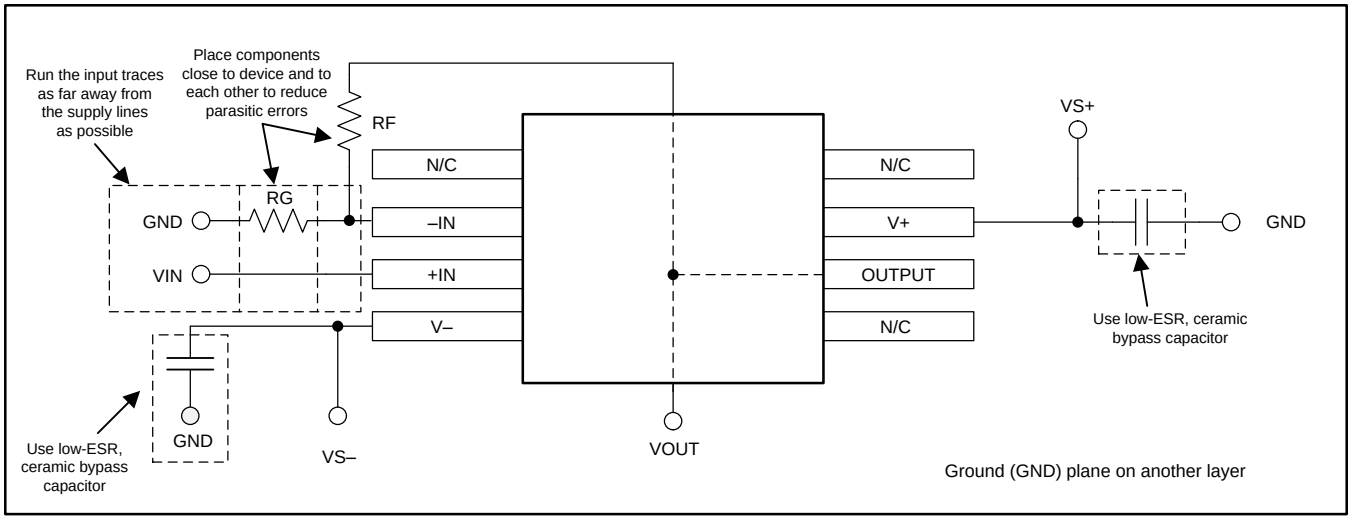


Figure 35. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners. Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 TI Precision Designs

The OPA350 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Circuit Board Layout Techniques*, SLOA089
- *Op Amps for Everyone*, SLOD006
- *Compensate Transimpedance Amplifiers Intuitively*, SBOS055
- *Noise Analysis for High Speed op Amps*, SBOA066

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA350	Click here	Click here	Click here	Click here	Click here
OPA2350	Click here	Click here	Click here	Click here	Click here
OPA4350	Click here	Click here	Click here	Click here	Click here

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11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2350EA/250	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D50
OPA2350EA/250.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D50
OPA2350EA/250G4	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D50
OPA2350EA/2K5	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D50
OPA2350EA/2K5.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D50
OPA2350EA/2K5G4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	D50
OPA2350UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2350UA
OPA2350UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2350UA
OPA2350UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2350UA
OPA2350UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2350UA
OPA2350UA/2K5G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2350UA
OPA2350UAG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2350UA
OPA350EA/250	Last Time Buy	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C50
OPA350EA/250.B	Last Time Buy	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C50
OPA350EA/250G4	Last Time Buy	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	Call TI | Nipdauag | Nipdau	Level-2-260C-1 YEAR	-40 to 85	C50
OPA350EA/250G4.B	Last Time Buy	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C50
OPA350EA/250G4.B	Last Time Buy	Production	VSSOP (DGK) | 8	250 | SMALL T&R	No	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C50
OPA350EA/2K5	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C50
OPA350EA/2K5.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C50

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA350EA/2K5G4	Last Time Buy	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C50
OPA350EA/2K5G4.B	Last Time Buy	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C50
OPA350UA	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 350UA
OPA350UA.B	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 350UA
OPA350UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 350UA
OPA350UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 350UA
OPA350UA/2K5G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 350UA
OPA350UAG4	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 350UA
OPA4350EA/250	Last Time Buy	Production	SSOP (DBQ) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	OPA 4350EA
OPA4350EA/250.B	Last Time Buy	Production	SSOP (DBQ) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4350EA
OPA4350EA/250G4	Last Time Buy	Production	SSOP (DBQ) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4350EA
OPA4350EA/250G4.B	Last Time Buy	Production	SSOP (DBQ) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4350EA
OPA4350EA/2K5	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4350EA
OPA4350EA/2K5.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 4350EA
OPA4350UA	Last Time Buy	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-	OPA4350UA
OPA4350UA.B	Last Time Buy	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4350UA
OPA4350UA/2K5	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	OPA4350UA
OPA4350UA/2K5.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4350UA
OPA4350UA/2K5G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See OPA4350UA/2K5	OPA4350UA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA4350UAG4	Last Time Buy	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4350UA
OPA4350UAG4.B	Last Time Buy	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4350UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

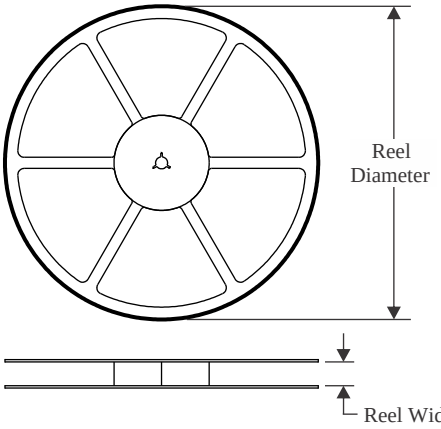
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

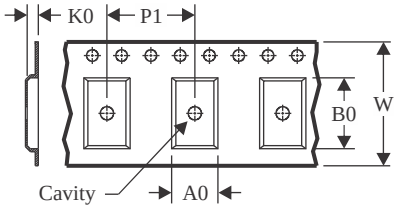
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

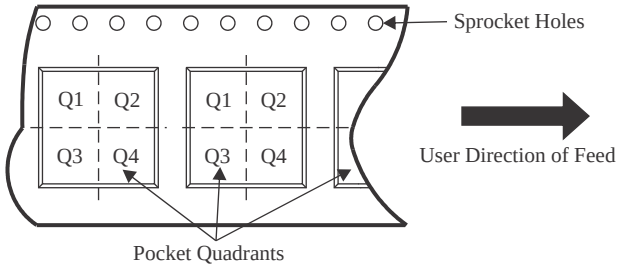


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

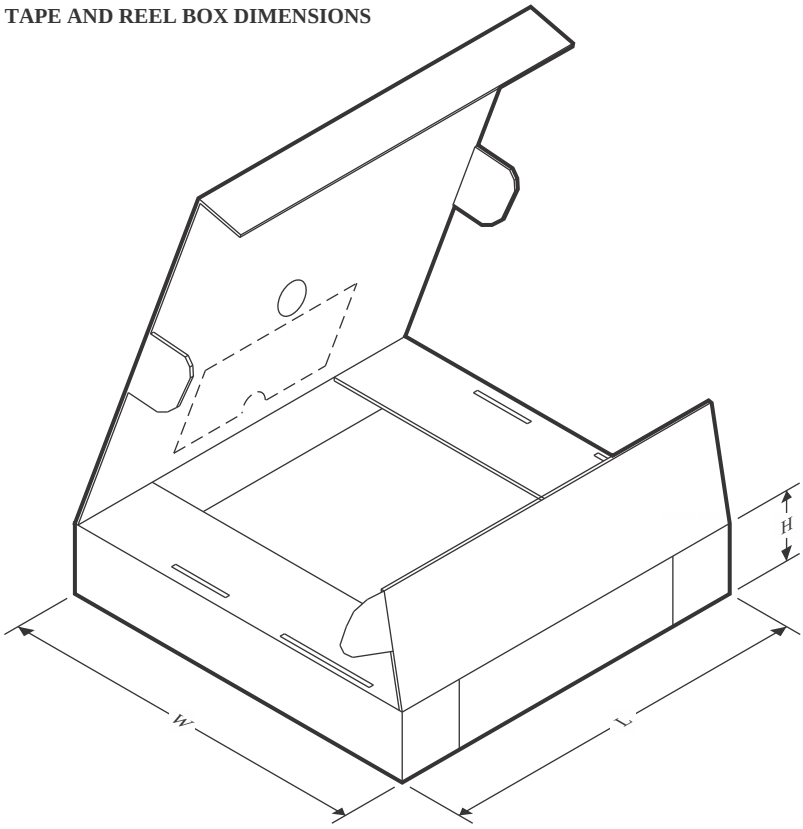
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2350EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2350EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2350UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA350EA/250	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA350EA/250G4	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA350EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA350EA/2K5G4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA350UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4350EA/250	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4350EA/250G4	SSOP	DBQ	16	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4350EA/2K5	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4350UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

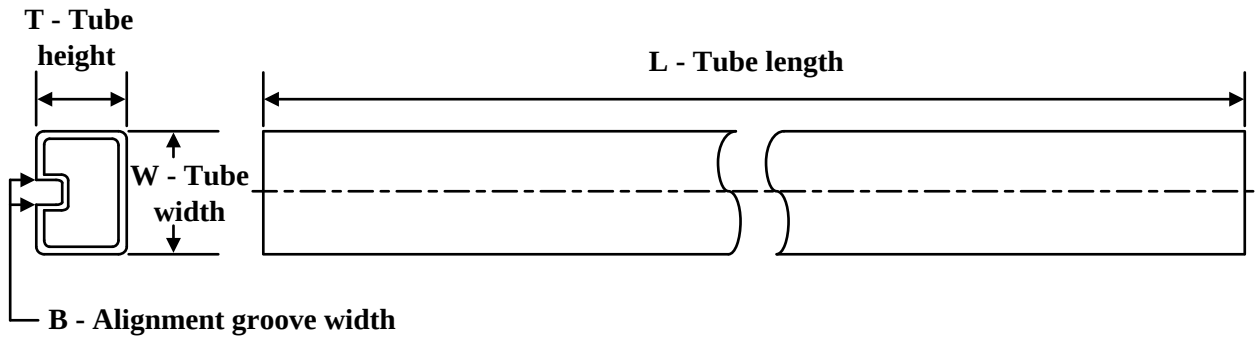
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2350EA/250	VSSOP	DGK	8	250	213.0	191.0	35.0
OPA2350EA/2K5	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2350UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA350EA/250	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA350EA/250G4	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA350EA/2K5	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA350EA/2K5G4	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA350UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA4350EA/250	SSOP	DBQ	16	250	213.0	191.0	35.0
OPA4350EA/250G4	SSOP	DBQ	16	250	213.0	191.0	35.0
OPA4350EA/2K5	SSOP	DBQ	16	2500	353.0	353.0	32.0
OPA4350UA/2K5	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

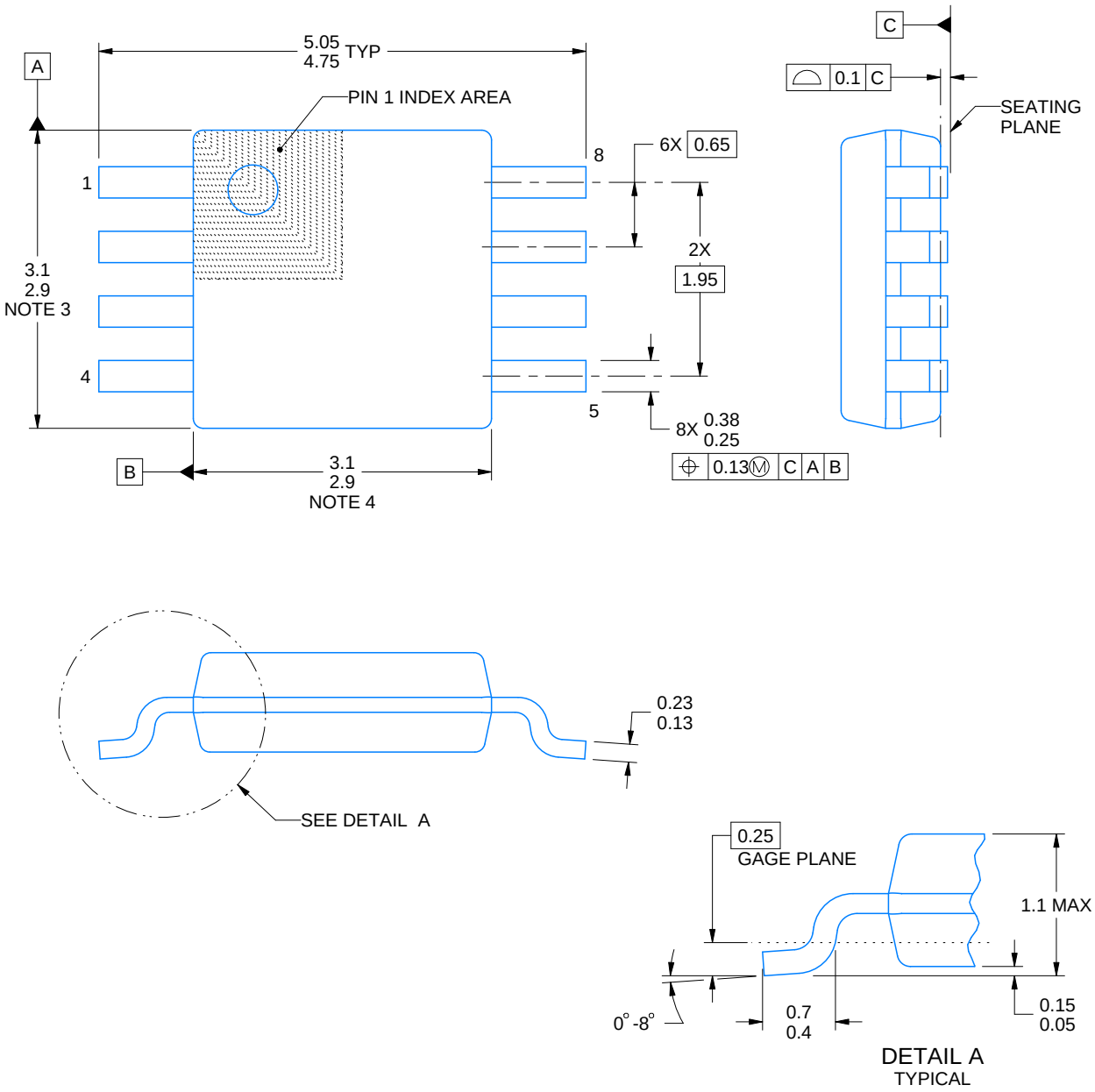
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2350UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2350UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2350UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA350UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA350UA.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA350UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA4350UA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4350UA.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4350UAG4	D	SOIC	14	50	506.6	8	3940	4.32
OPA4350UAG4.B	D	SOIC	14	50	506.6	8	3940	4.32

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

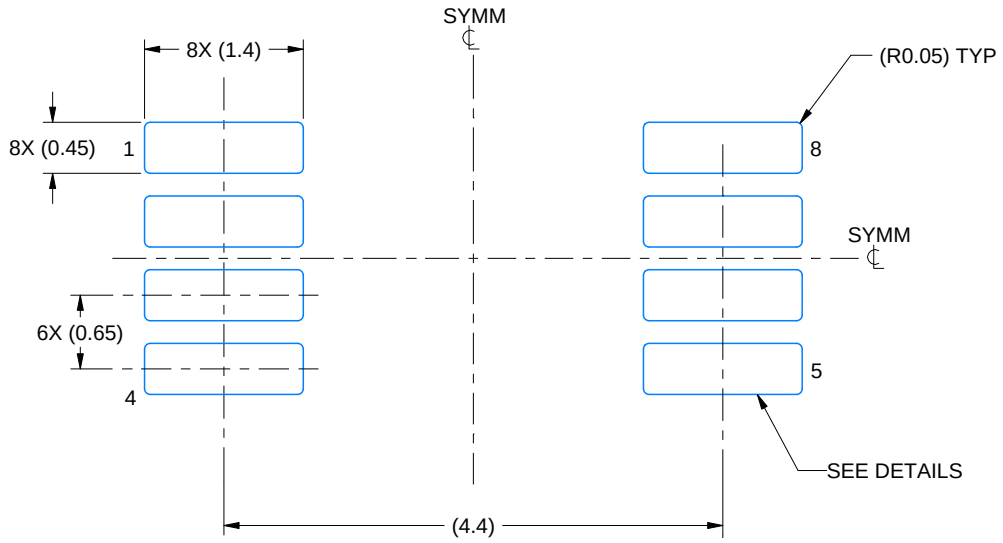
SMALL OUTLINE PACKAGE



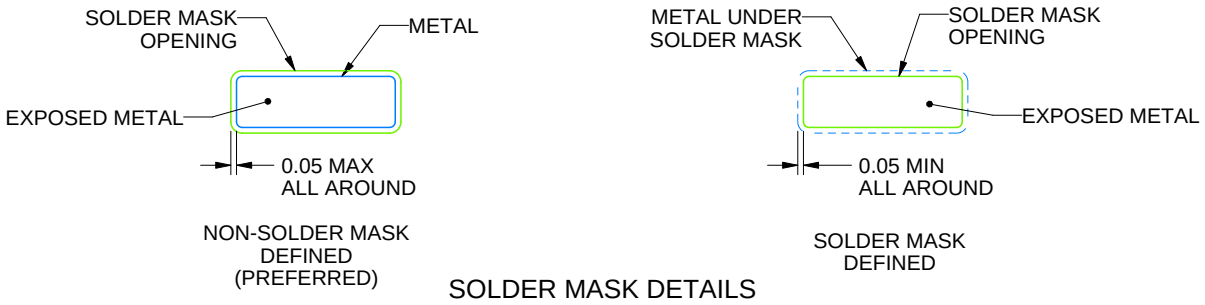
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

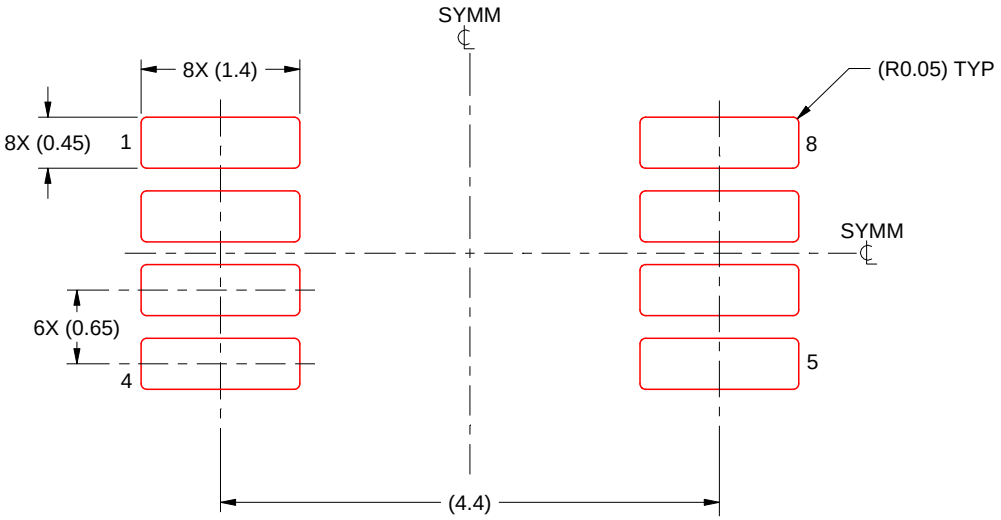


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

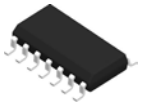


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

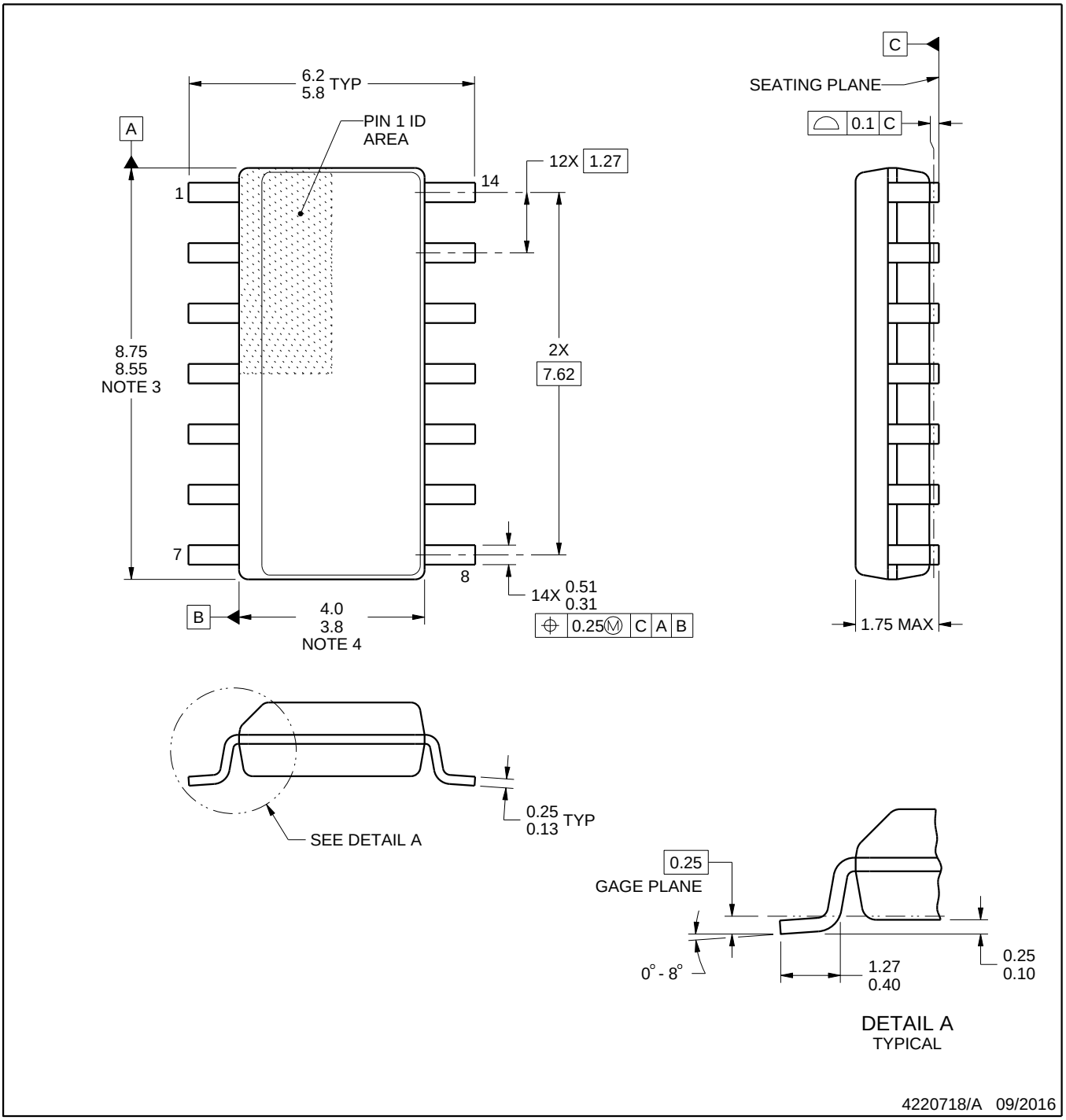


PACKAGE OUTLINE

D0014A

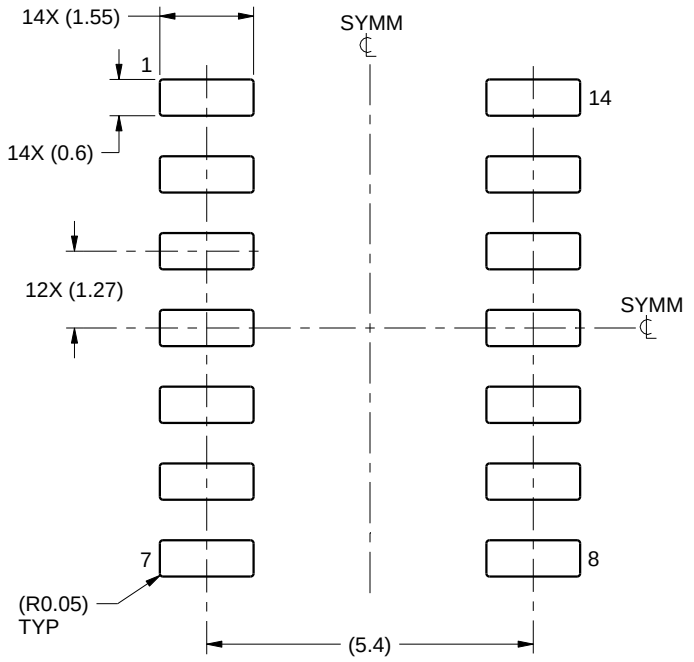
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

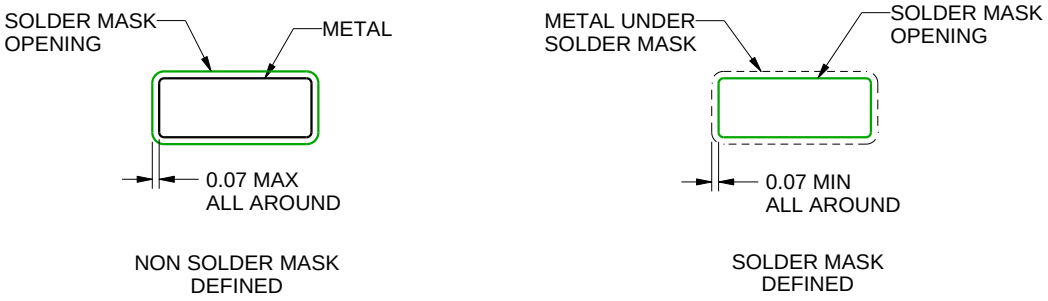


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

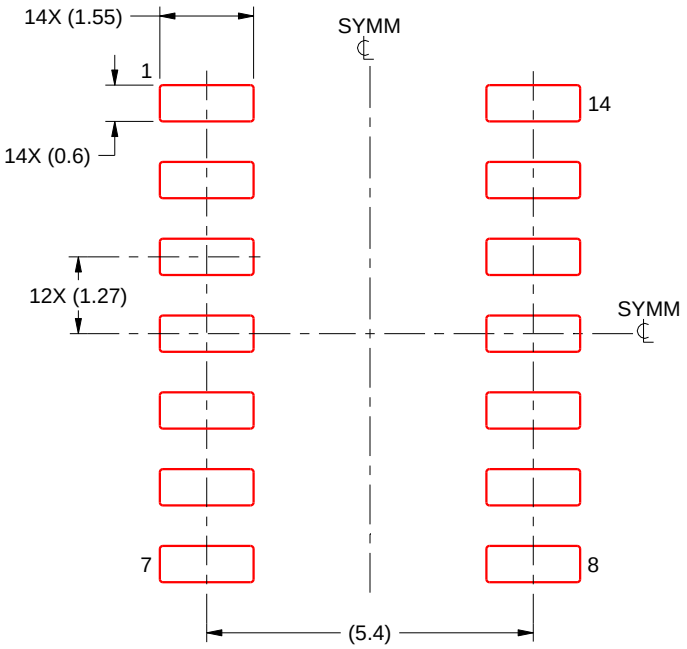
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

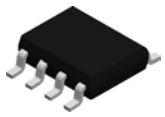


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

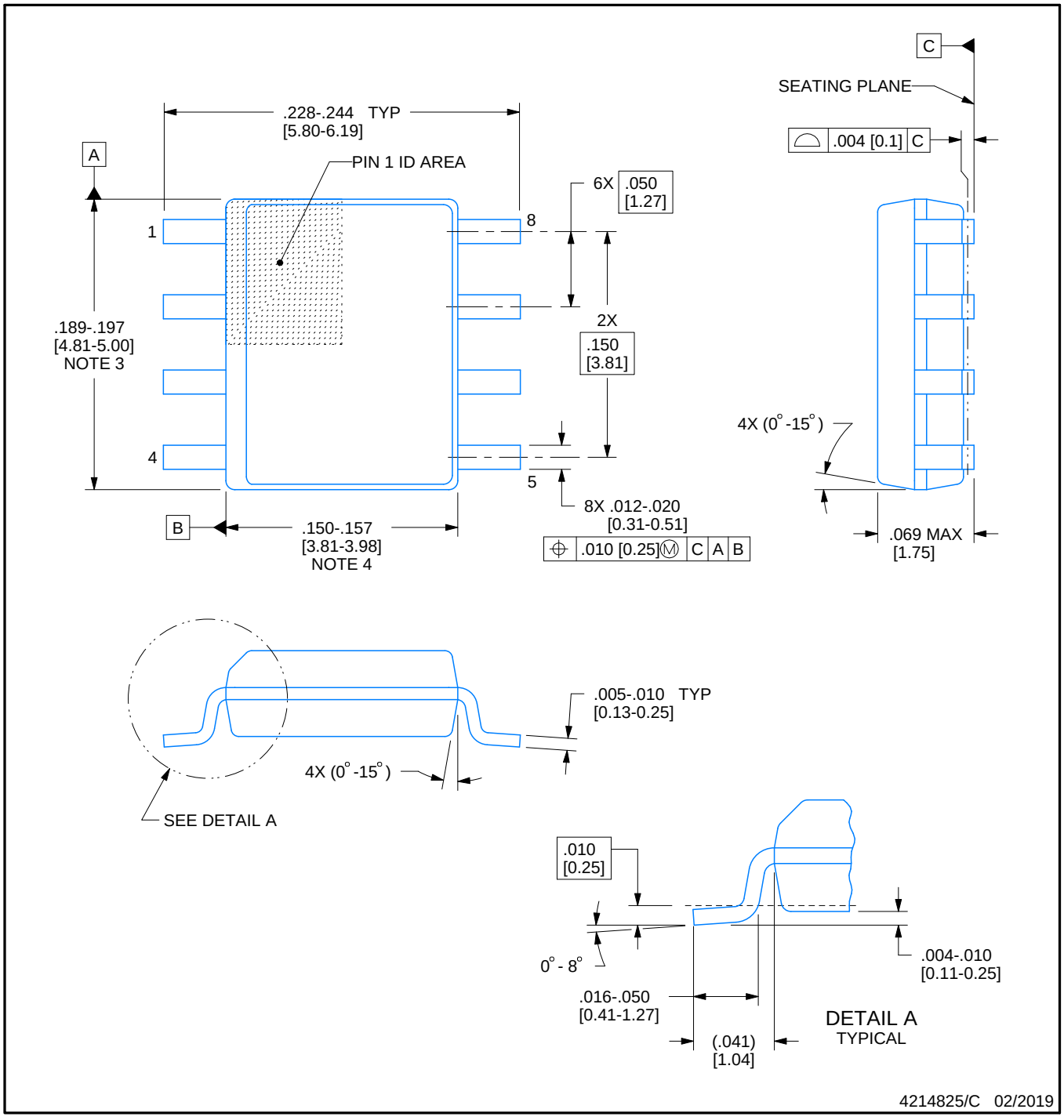


PACKAGE OUTLINE

D0008A

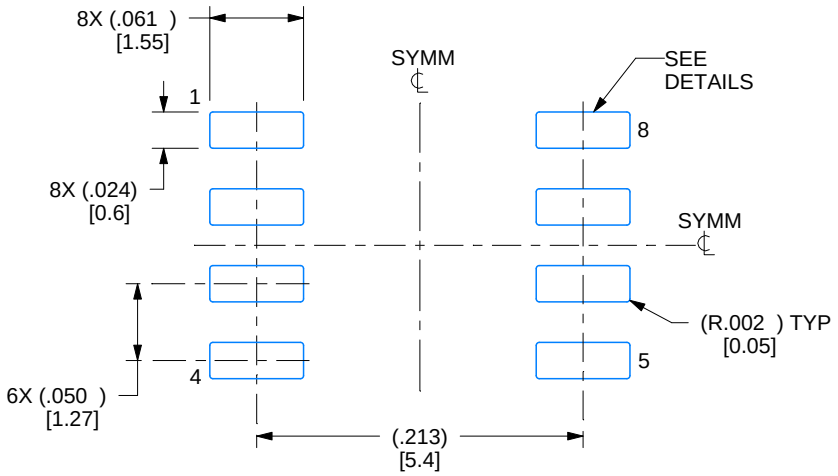
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

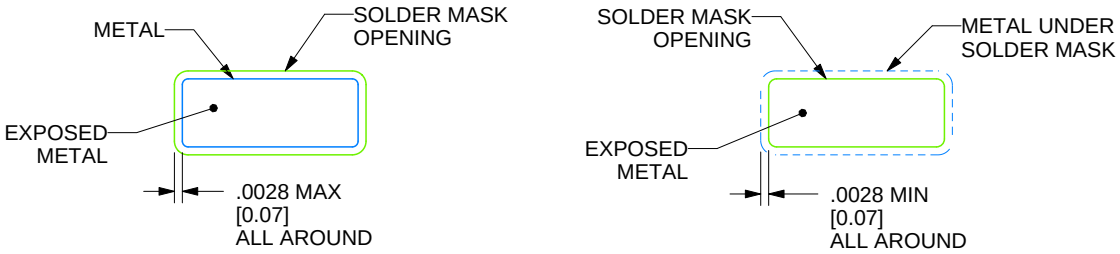


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

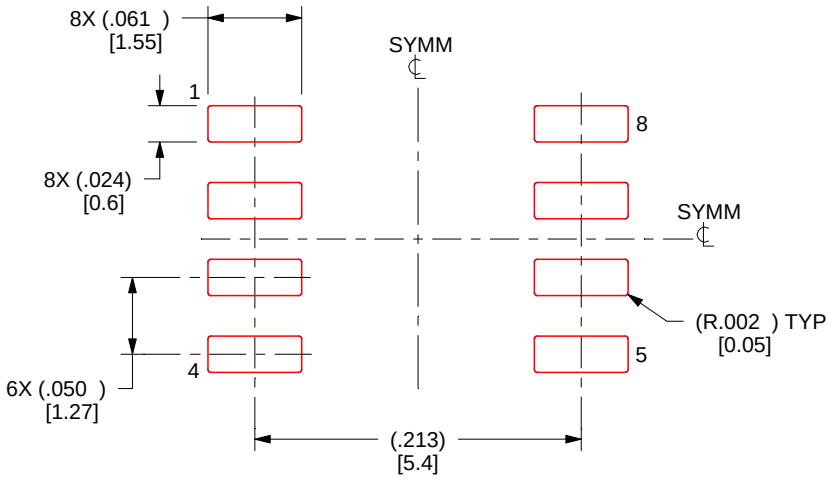
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

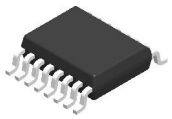


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

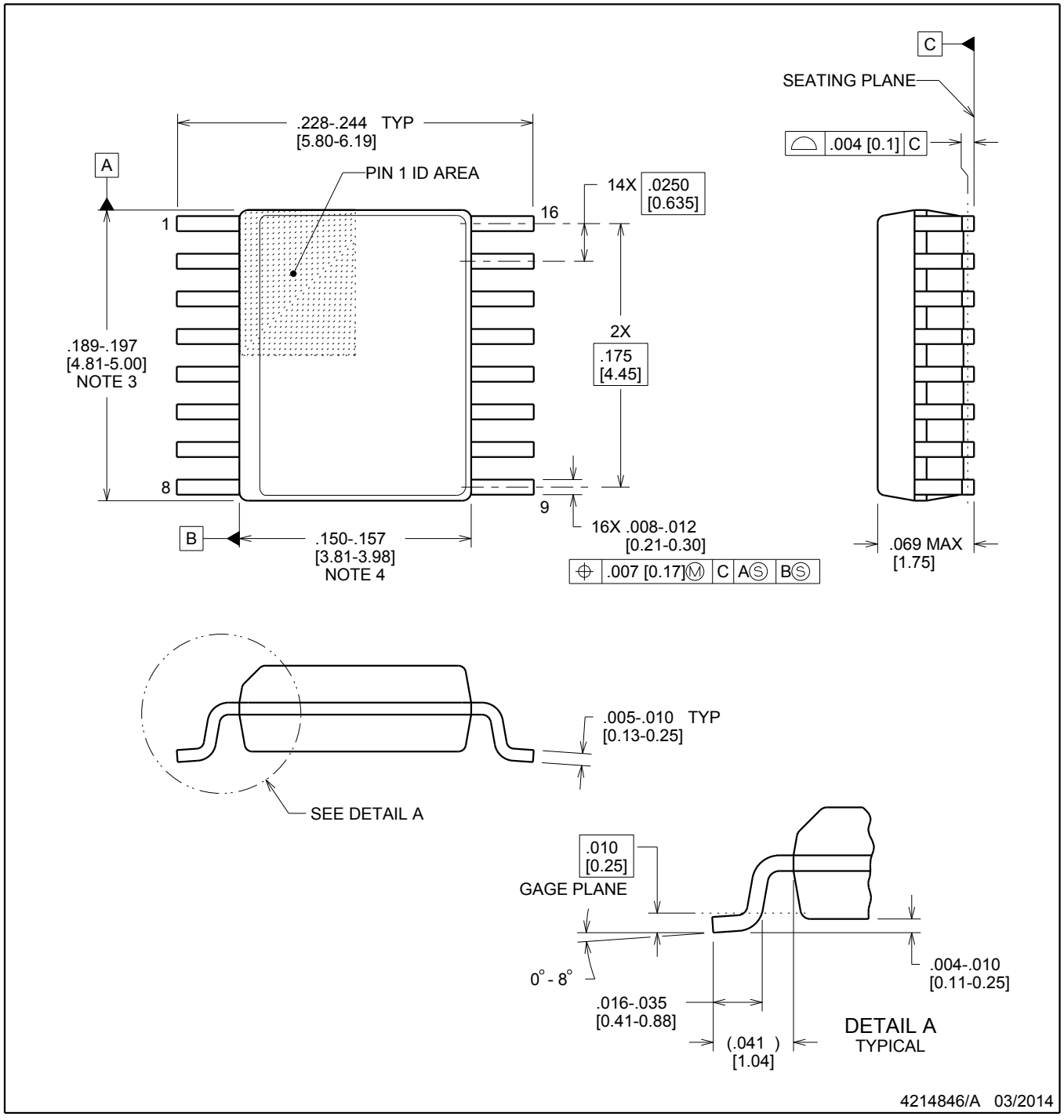


PACKAGE OUTLINE

DBQ0016A

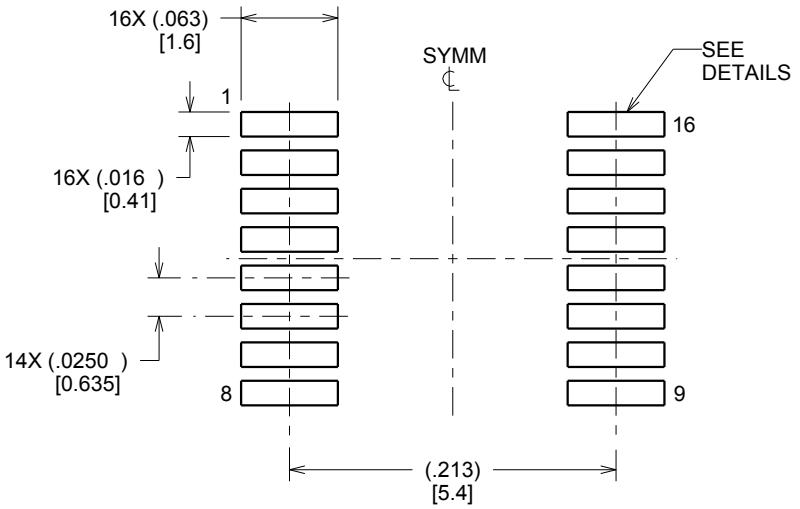
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

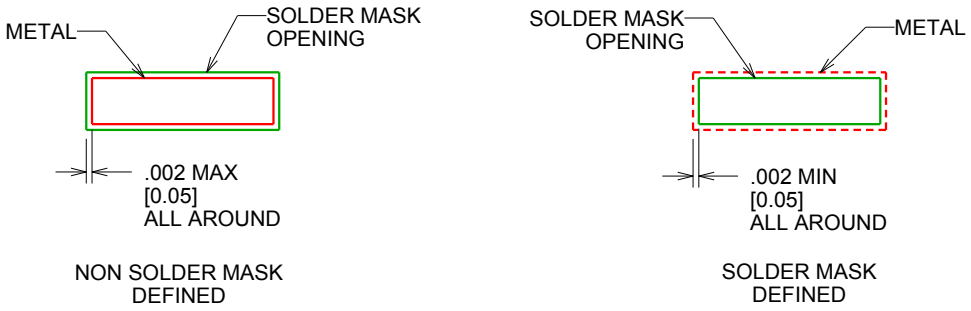


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

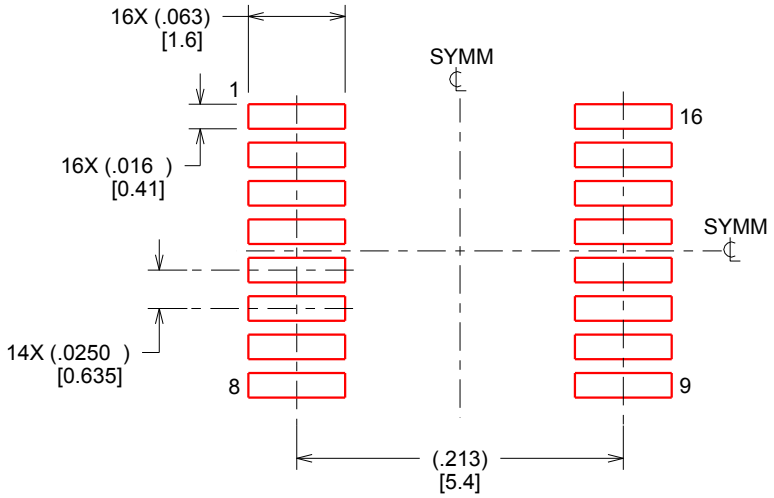
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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