

OPAx180 0.1 μ V/ $^{\circ}$ C Drift, Low-Noise, Rail-to-Rail Output, 36V, Zero-Drift Operational Amplifiers

1 Features

- Low offset voltage: 75 μ V (maximum)
- Zero-drift: 0.1 μ V/ $^{\circ}$ C
- Low noise: 10nV/ $\sqrt{\text{Hz}}$
- Very low 1/f noise
- Excellent dc precision:
 - PSRR: 126dB
 - CMRR: 114dB
 - Open-loop gain (A_{OL}): 120dB
- Quiescent current: 525 μ A (maximum)
- Wide supply range: $\pm$ 2V to $\pm$ 18V
- Rail-to-rail output:
 - input includes negative rail
- Low bias current: 250pA (typical)
- RFI filtered inputs
- *Micro*SIZE packages

2 Applications

- Bridge Amplifiers
- Strain Gauges
- Test Equipment
- Transducer Applications
- Temperature Measurement
- Electronic Scales
- Medical Instrumentation
- Resister Thermal Detectors
- Precision Active Filters

3 Description

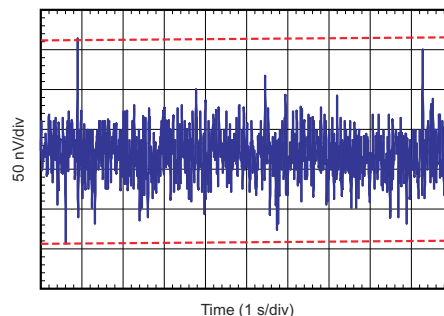
The single OPA180, dual OPA2180, and quad OPA4180 (OPAx180) operational amplifiers (op amps) use TI's proprietary [zero-drift](#) techniques to simultaneously provide low offset voltage (75 μ V), and near zero-drift over time and temperature. These miniature, high-precision, low-quiescent-current op amps offer high input impedance and rail-to-rail output swing within 18mV of the rails. The input common-mode range includes the negative rail. These devices use single or dual supplies ranging from 4V to 36V ($\pm$ 2V to $\pm$ 18V).

The dual-channel version is offered in VSSOP-8 packages and SOIC-8 packages. The quad-channel version is offered in SOIC-14 and TSSOP-14 packages. The single and quad package offerings (OPA180 and OPA4180) are specified from -40°C to $+125^{\circ}\text{C}$, and the dual package (OPA2180) is specified from -40°C to $+105^{\circ}\text{C}$.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE ⁽¹⁾
OPA180	Single	D (SOIC, 8)
		DBV (SOT-23, 5)
		DGK (VSSOP, 8)
OPA2180	Dual	D (SOIC, 8)
		DGK (VSSOP, 8)
OPA4180	Quad	D (SOIC, 14)
		PW (TSSOP, 14)

(1) For more information, see [Section 11](#).



Low Noise (Peak-to-Peak Noise = 250nV)



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4 Device Comparison Table

Table 4-1. Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE (μV)	OFFSET VOLTAGE DRIFT ($\mu\text{V}/^\circ\text{C}$)	BANDWIDTH (MHz)
Single	OPA188 (4V to 36V)	25	0.085	2
	OPA180 (4V to 36V)	75	0.35	2
	OPA333 (5V)	10	0.05	0.35
	OPA378 (5V)	50	0.25	0.9
	OPA735 (12V)	5	0.05	1.6
Dual	OPA2188 (4V to 36V)	25	0.085	2
	OPA2180 (4V to 36V)	75	0.35	2
	OPA2333 (5V)	10	0.05	0.35
	OPA2378 (5V)	50	0.25	0.9
	OPA2735 (12V)	5	0.05	1.6
Quad	OPA4188 (4V to 36V)	25	0.085	2
	OPA4180 (4V to 36V)	75	0.35	2
	OPA4330 (5V)	50	0.25	0.35

5 Pin Configuration and Functions

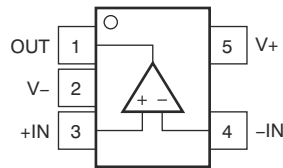


Figure 5-1. OPA180 DBV (5-Pin SOT-23) Package, Top View

Table 5-1. Pin Functions: OPA180

PIN		I/O	DESCRIPTION
NAME	DBV		
-IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
V-	2	—	Negative supply or ground (for single-supply operation)
V+	5	—	Positive supply or ground (for single-supply operation)

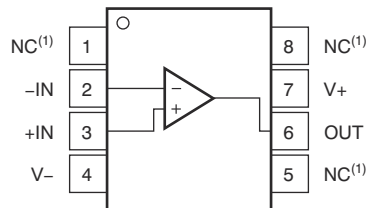


Figure 5-2. OPA180D (8-Pin SOIC) and DGK Packages (8-Pin VSSOP) Packages, Top View

Table 5-2. Pin Functions: OPA180

PIN		DESCRIPTION
NAME	NO.	
-IN	2	Inverting input
+IN	3	Noninverting input
NC	1, 5, 8	No connection
OUT	6	Output
V-	4	Negative power supply
V+	7	Positive power supply

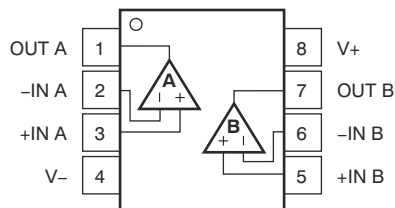


Figure 5-3. OPA2180D (8-Pin SOIC) and DGK Packages (8-Pin VSSOP) Packages, Top View

Table 5-3. Pin Functions: OPA2180

PIN		DESCRIPTION
NAME	NO.	
-IN A	2	Inverting input, channel A
+IN A	3	Noninverting input, channel A
-IN B	6	Inverting input, channel B
+IN B	5	Noninverting input, channel B
OUT A	1	Output, channel A
OUT B	7	Output, channel B
V-	4	Negative power supply
V+	8	Positive power supply

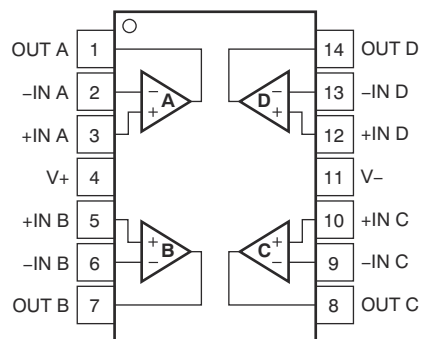


Figure 5-4. OPA4180D (14-Pin SOIC) and PW (14-Pin TSSOP) Packages , Top View

Table 5-4. Pin Functions: OPA4180

PIN		DESCRIPTION
NAME	NO.	
-IN A	2	Inverting input, channel A
+IN A	3	Noninverting input, channel A
-IN B	6	Inverting input, channel B
+IN B	5	Noninverting input, channel B
-IN C	9	Inverting input, channel C
+IN C	10	Noninverting input, channel C
-IN D	13	Inverting input, channel D
+IN D	12	Noninverting input, channel D
OUT A	1	Output, channel A
OUT B	7	Output, channel B
OUT C	8	Output, channel C
OUT D	14	Output, channel D
V-	11	Negative supply or ground (for single-supply operation)
V+	4	Positive supply or ground (for single-supply operation)

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
	Supply voltage			±20, ±40 (single-supply)	V
	Signal input terminals	Voltage	(V ₋) – 0.5	(V ₊) + 0.5	V
		Current		±10	mA
	Output short-circuit ⁽²⁾		Continuous		
	Operating temperature		–55	125	°C
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		–65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		–65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	–1.5	1.5	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	–1	1	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted), R_L = 10kΩ connected to V_S / 2, and V_{COM} = V_{OUT} = V_S / 2, (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage [(V ₊) – (V ₋)]	Single-supply	4.5		36	V
	Bipolar-supply	±2.25		±18	V
Operating temperature		–40		125	°C

6.4 Thermal Information: OPA180

THERMAL METRIC ⁽¹⁾		OPA180			UNIT
		D (SOIC)	DBV (SOT-23)	DGK (MSOP)	
		8 PINS	5 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	115.8	158.8	180.4	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	60.1	60.7	67.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	56.4	44.8	102.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	12.8	1.6	10.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	55.9	4.2	100.3	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information: OPA2180

THERMAL METRIC ⁽¹⁾		OPA2180		UNIT
		D (SOIC)	DGK (MSOP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	111	159.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	54.9	37.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	51.7	48.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	9.3	1.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	51.1	77.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Thermal Information: OPA4180

THERMAL METRIC ⁽¹⁾		OPA4180		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.8	24.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	49.4	59.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7 Electrical Characteristics: $V_S = \pm 2V$ to $\pm 18V$ ($V_S = 4V$ to $36V$)

at $T_A = 25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, and $V_{\text{COM}} = V_{\text{OUT}} = V_S / 2$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{IO}	Input offset voltage			15	75	μV
dV _{IO} /dT	Input offset voltage drift	T _A = −40°C to +125°C		0.1	0.35	μV/°C
PSRR	Power supply rejection ratio	V _S = 4V to 36V, V _{CM} = V _S / 2		0.1	0.5	μV/V
		T _A = −40°C to +125°C, V _S = 4V to 36V, V _{CM} = V _S / 2			0.5	μV/V
	Long-term stability			4 ⁽¹⁾		μV
	Channel separation, DC			1		μV/V
INPUT BIAS CURRENT						
I _B	Input bias current	OPA2180		±0.25	±1.5	nA
		OPA2180: T _A = −40°C to +105°C			±18	nA
		OPA180, OPA4180		±0.25	±1.7	nA
		OPA180, OPA4180: T _A = −40°C to +125°C			±18	nA
I _O	Input offset current	OPA2180		±0.5	±3	nA
		OPA2180: T _A = −40°C to +105°C			±6	nA
		OPA180, OPA4180			±3.4	nA
		OPA180, OPA4180: T _A = −40°C to +125°C			±6	nA
NOISE						
	Input voltage noise	f = 0.1Hz to 10Hz		0.25		μV _{PP}
e _n	Input voltage noise density	f = 1kHz		10		nV/√ Hz
i _n	Input current noise density	f = 1kHz		10		fA/√ Hz
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage range		V−	(V+) − 1.5		V
CMRR	Common-mode rejection ratio	(V−) < V _{CM} < (V+) − 1.5V	104	114		dB
		T _A = −40°C to +125°C, (V−) + 0.5V < V _{CM} < (V+) − 1.5V	100	104		dB
INPUT IMPEDANCE						
Z _{id}	Differential			100 6		MΩ pF
Z _{ic}	Common-mode			6 9.5		10 ¹² Ω pF
OPEN-LOOP GAIN						
A _{OL}	Open-loop voltage gain	(V−) + 500mV < V _O < (V+) − 500mV R _L = 10kΩ	110	120		dB
		T _A = −40°C to +125°C (V−) + 500mV < V _O < (V+) − 500mV, R _L = 10kΩ	104	114		dB
FREQUENCY RESPONSE						
GBW	Gain bandwidth product			2		MHz
SR	Slew rate	G = 1		0.8		V/μs
t _s	Settling time	0.1%	V _S = ±18V, G = 1, 10V step	22		μs
		0.01%	V _S = ±18V, G = 1, 10V step	30		μs
t _{or}	Overload recovery time	V _{IN} × G = V _S		1		μs
THD+N	Total harmonic distortion + noise	f = 1kHz, G = 1, V _{OUT} = 1V _{RMS}		0.0001%		

at $T_A = 25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, and $V_{\text{COM}} = V_{\text{OUT}} = V_S / 2$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
Voltage output swing from rail		No load		8	18	mV
		R _L = 10kΩ		250	300	mV
		T _A = −40°C to +125°C R _L = 10kΩ		325	360	mV
I _{OS}	Short-circuit current			±18		mA
r _o	Output resistance (open loop)	f = 2MHz, I _O = 0mA		120		Ω
C _{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V _S	Operating voltage range		±2 (or 4)		±18 (or 36)	V
I _Q	Quiescent current (per amplifier)			450	525	μA
		T _A = −40°C to +125°C I _O = 0mA			600	μA
TEMPERATURE						
	Specified range		−40		105	°C
	Operating range		−40		105	°C

(1) 1000-hour life test at 125°C demonstrated randomly distributed variation in the range of measurement limits, or approximately $4\mu\text{V}$.

6.8 Typical Characteristics: Table of Graphs

Table 6-1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
I_B and I_{OS} vs Common-Mode Voltage	Figure 6-1
Input Bias Current vs Temperature	Figure 6-2
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 6-3
CMRR vs Temperature	Figure 6-4
0.1Hz to 10Hz Noise	Figure 6-5
Input Voltage Noise Spectral Density vs Frequency	Figure 6-6
Open-Loop Gain and Phase vs Frequency	Figure 6-7
Open-Loop Gain vs Temperature	Figure 6-8
Open-Loop Output Impedance vs Frequency	Figure 6-9
Small-Signal Overshoot vs Capacitive Load (100mV Output Step)	Figure 6-10 , Figure 6-11
No Phase Reversal	Figure 6-12
Positive Overload Recovery	Figure 6-13
Negative Overload Recovery	Figure 6-14
Small-Signal Step Response (100mV)	Figure 6-15 , Figure 6-16
Large-Signal Step Response	Figure 6-17 , Figure 6-18
Large-Signal Settling Time (10V Positive Step)	Figure 6-19
Large-Signal Settling Time (10V Negative Step)	Figure 6-20
Short-Circuit Current vs Temperature	Figure 6-21
Maximum Output Voltage vs Frequency	Figure 6-22
Channel Separation vs Frequency	Figure 6-23
EMIRR IN+ vs Frequency	Figure 6-24

6.9 Typical Characteristics

$V_S = \pm 18V$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10k\Omega$ connected to $V_S / 2$, and $C_L = 100pF$, unless otherwise noted.

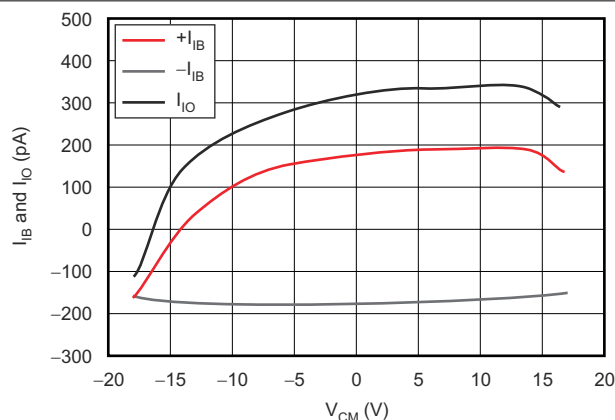


Figure 6-1. I_B and I_O vs Common-Mode Voltage

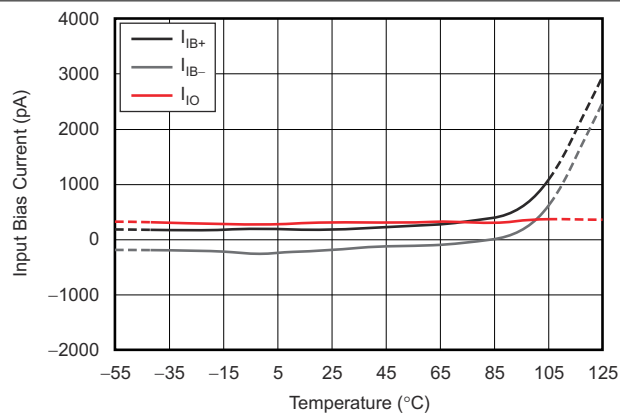


Figure 6-2. Input Bias Current vs Temperature

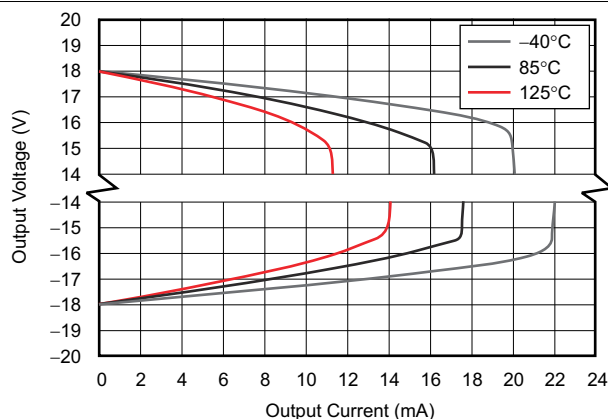
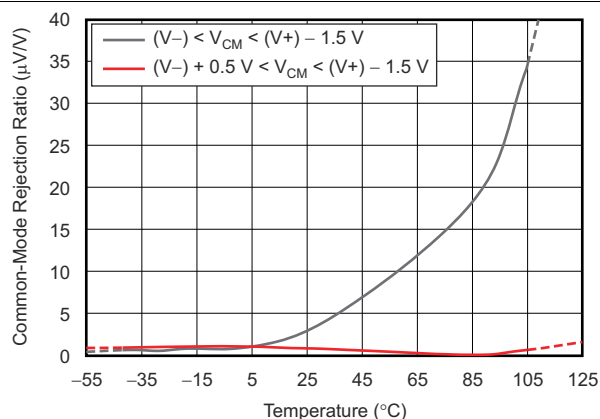


Figure 6-3. Output Voltage Swing vs Output Current (Maximum Supply)



$V_{SUPPLY} = \pm 2V$

Figure 6-4. CMRR vs Temperature

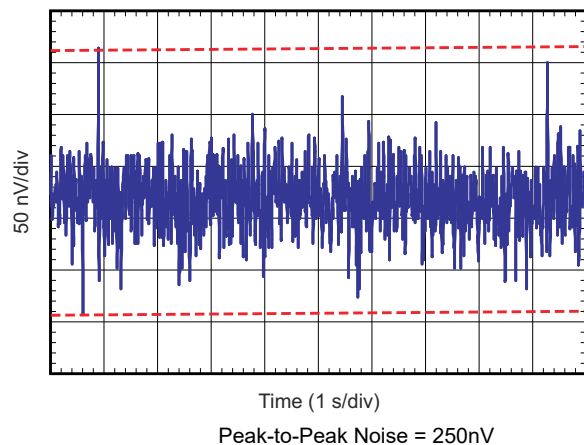


Figure 6-5. 0.1Hz to 10Hz Noise

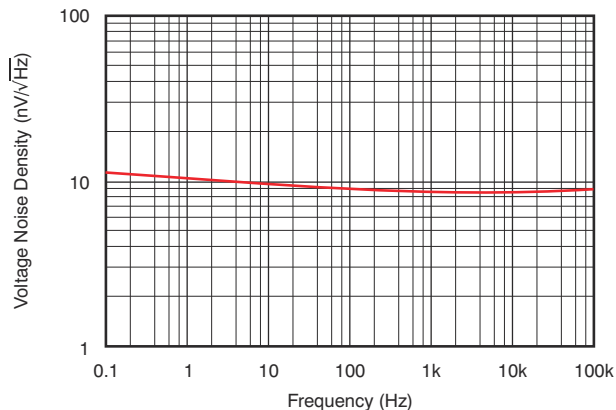


Figure 6-6. Input Voltage Noise Spectral Density vs Frequency

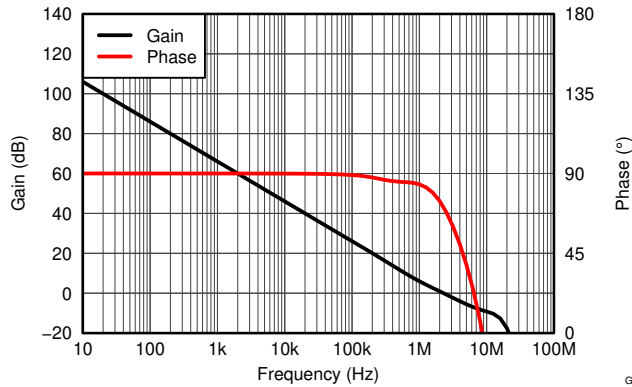


Figure 6-7. Open-Loop Gain and Phase vs Frequency

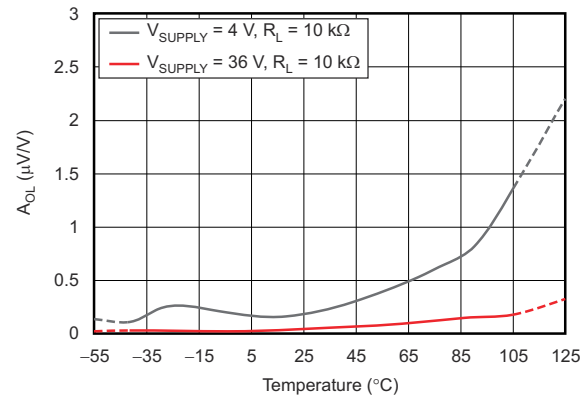


Figure 6-8. Open-Loop Gain vs Temperature

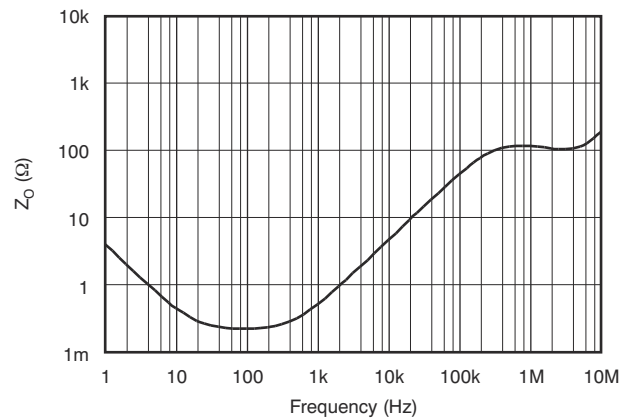


Figure 6-9. Open-Loop Output Impedance vs Frequency

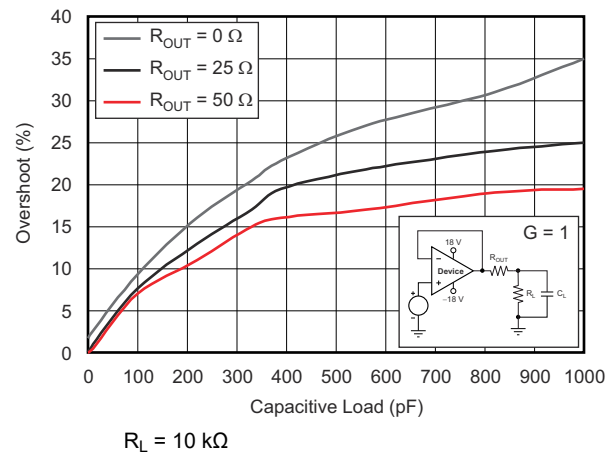


Figure 6-10. Small-Signal Overshoot vs Capacitive Load (100mV Output Step)

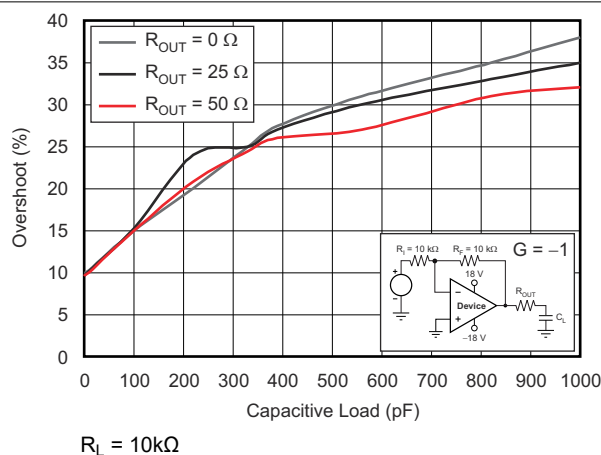


Figure 6-11. Small-Signal Overshoot vs Capacitive Load (100mV Output Step)

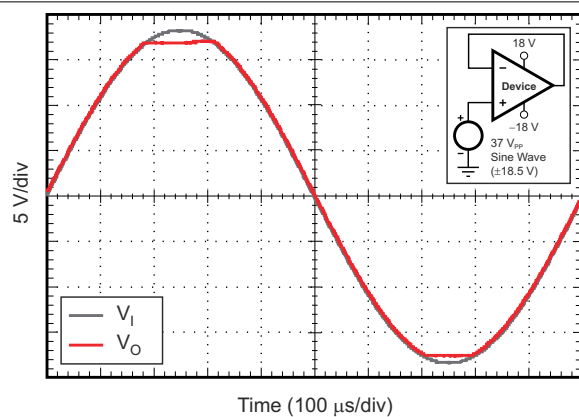


Figure 6-12. No Phase Reversal

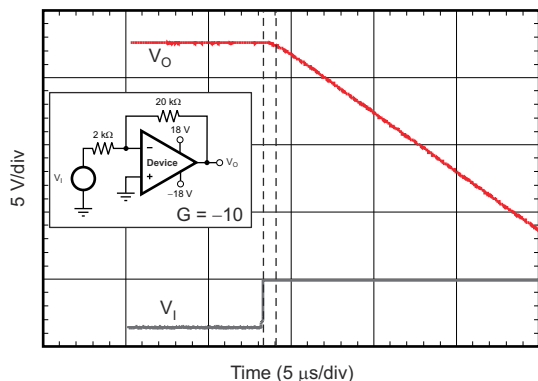


Figure 6-13. Positive Overload Recovery

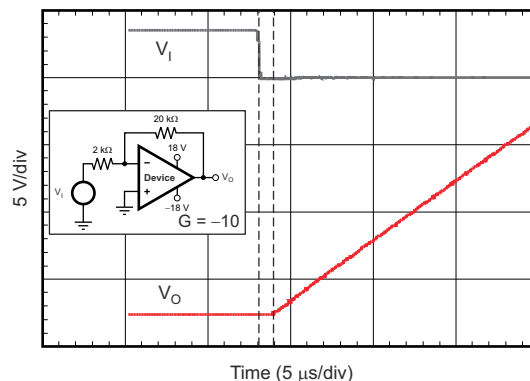


Figure 6-14. Negative Overload Recovery

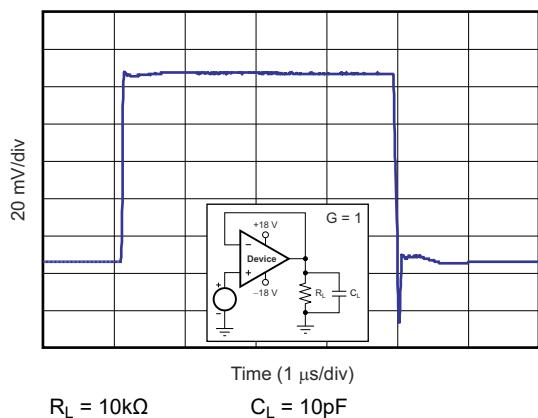


Figure 6-15. Small-Signal Step Response (100mV)

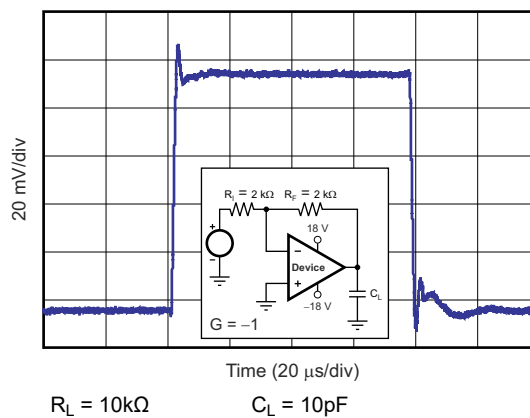


Figure 6-16. Small-Signal Step Response (100mV)

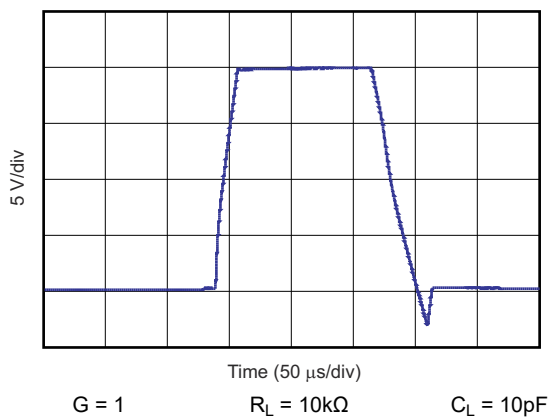


Figure 6-17. Large-Signal Step Response

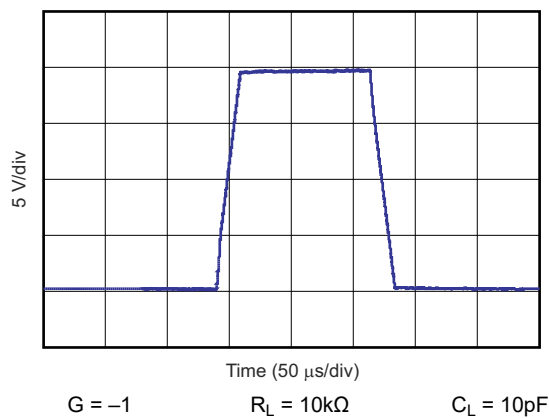


Figure 6-18. Large-Signal Step Response

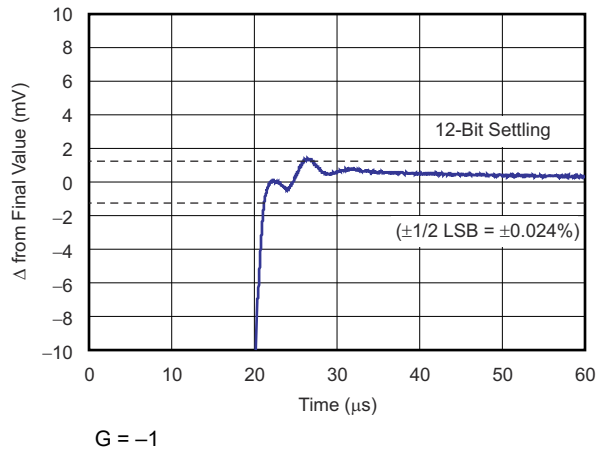


Figure 6-19. Large-Signal Settling Time (10V Positive Step)

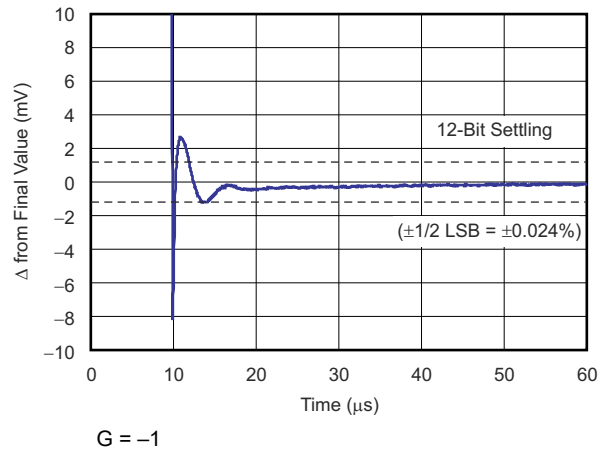


Figure 6-20. Large-Signal Settling Time (10V Negative Step)

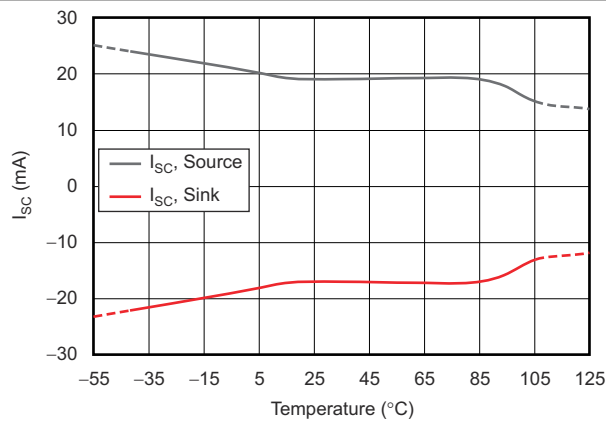


Figure 6-21. Short-Circuit Current vs Temperature

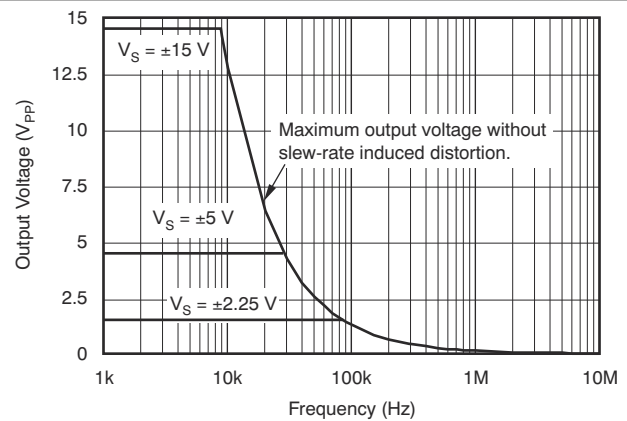


Figure 6-22. Maximum Output Voltage vs Frequency

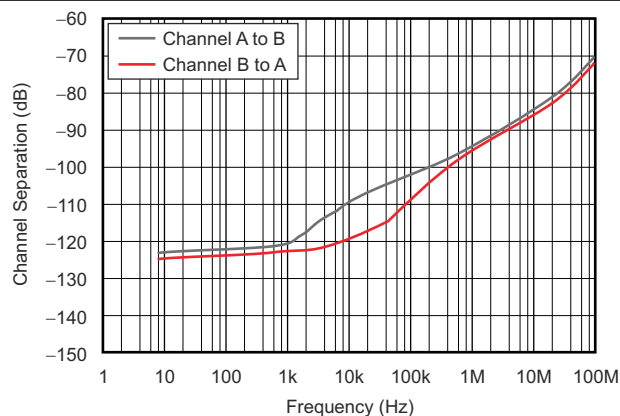


Figure 6-23. Channel Separation vs Frequency

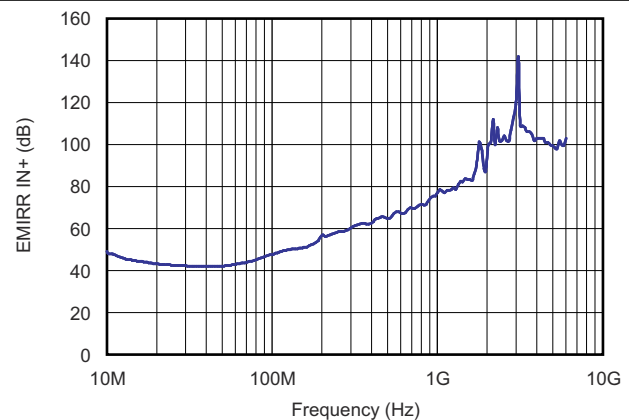


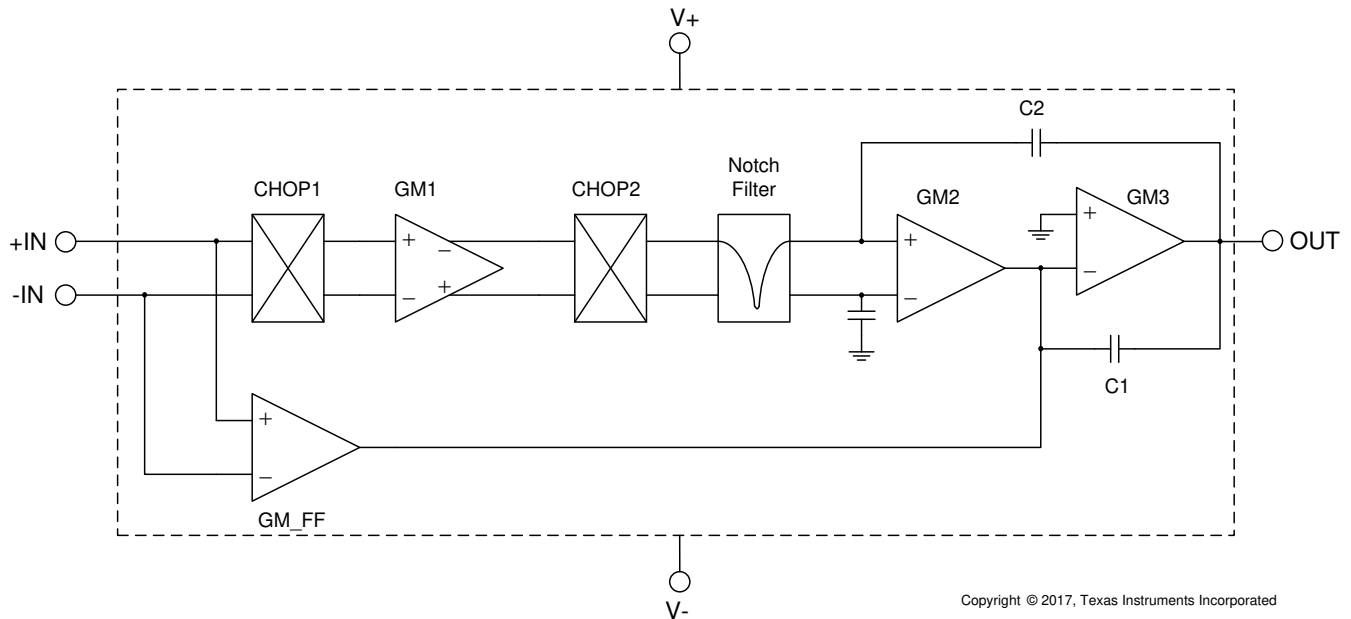
Figure 6-24. EMIRR IN+ vs Frequency

7 Detailed Description

7.1 Overview

The OPAx180 family of operational amplifiers combine precision offset and drift with excellent overall performance, making these devices a great choice for many precision applications. The precision offset drift of only 0.1 $\mu\text{V}/^\circ\text{C}$ provides stability over the entire temperature range. In addition, the devices offer excellent overall performance with high CMRR, PSRR, and A_{OL} . As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1- μF capacitors are adequate.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPAX180 family of amplifiers is specified for operation from 4V to 36V ($\pm 2V$ to $\pm 18V$). Many of the specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

7.3.2 EMI Rejection

The OPAX180 family uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely populated boards with a mix of analog signal chain and digital components. EMI immunity can improve with circuit design techniques; the OPAX180 family benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. [Figure 7-1](#) shows the results of this testing on the OPAX180 family. For more detailed information, see the [EMI Rejection Ratio of Operational Amplifiers](#) application report, available for download from [www.ti.com](#).

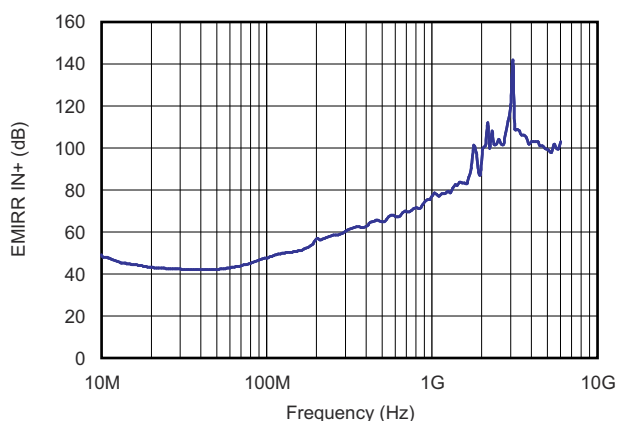


Figure 7-1. OPAx180 EMIRR Testing

7.3.3 Phase-Reversal Protection

The OPAX180 family has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAX180 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in [Figure 7-2](#).

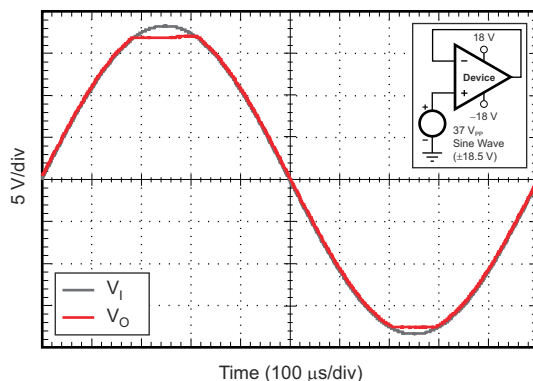


Figure 7-2. No Phase Reversal

7.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAx180 are optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50Ω) in series with the output. Figure 7-3 and Figure 7-4 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT} . See the [Feedback Plots Define Op Amp AC Performance](#), application report, available for download from the TI website, for details of analysis techniques and application circuits.

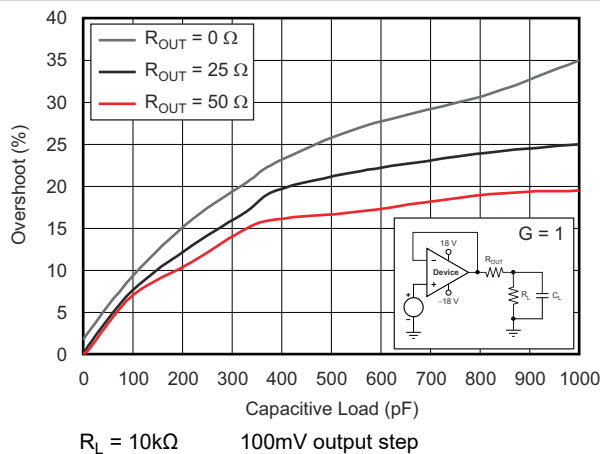


Figure 7-3. Small-Signal Overshoot Versus Capacitive Load

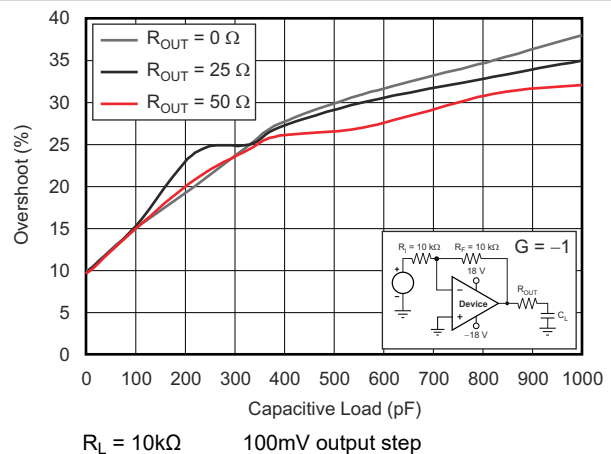


Figure 7-4. Small-Signal Overshoot Versus Capacitive Load

7.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10mA as stated in the [Absolute Maximum Ratings](#) table. Figure 7-5 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

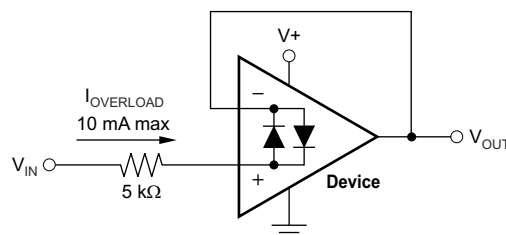


Figure 7-5. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as the pulse discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to protect the core from damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. Circumstances can arise when an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits can be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes can be added to the supply pins. The zener voltage must be selected so the diode does not turn on during normal operation.

The zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

7.4 Device Functional Modes

The OPAx180, OPA2180, and OPA4180 devices are powered on when the supply is connected. These devices can operate as a single-supply operational amplifier or dual-supply amplifier depending on the application. In single-supply operation with V_- at ground (0V), V_+ can be any value between 4V and 36V. In dual-supply operation, the supply voltage difference between V_- and V_+ is from 4V to 36V. Typical examples of dual-supply configuration are $\pm 5V$, $\pm 10V$, $\pm 15V$, and $\pm 18V$. However, the supplies must not be symmetrical. Less common examples are V_- at $-3V$ and V_+ at $9V$, or V_- at $-16V$ and V_+ at $5V$. Any combination where the difference between V_- and V_+ is at least 4V and no greater than 36V is within the normal operating capabilities of these devices.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

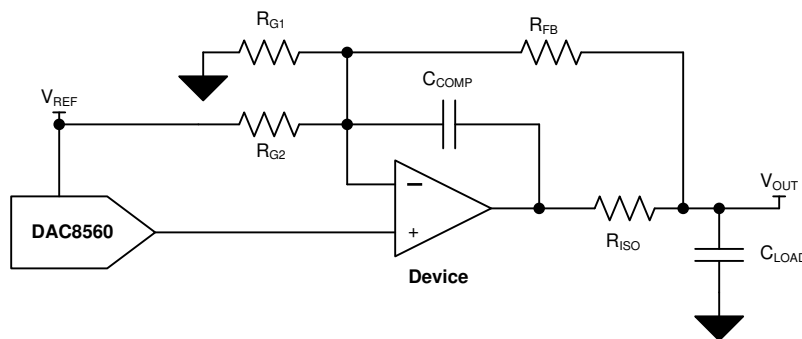
The OPAx180 family offers excellent DC precision and AC performance. These devices operate up to 36V supply rails and offer rail-to-rail output, ultra-low offset voltage, offset voltage drift and 2MHz bandwidth. These features make the OPAx180 a robust, high-performance amplifier for high-voltage industrial applications.

8.2 Typical Applications

These application examples highlight a few of the circuits where the OPAx180 family can be used.

8.2.1 Bipolar $\pm 10\text{V}$ Analog Output from a Unipolar Voltage Output DAC

This design is used for conditioning a unipolar digital-to-analog converter (DAC) into an accurate bipolar signal source using the OPAx180 family and three resistors. The circuit is designed with reactive load stability in mind, and is compensated to drive nearly any conventional capacitive load associated with long cable lengths.



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Figure 8-1. Circuit Schematic

8.2.1.1 Design Requirements

The design requirements are as follows:

- DAC supply voltage: +5V dc
- Amplifier supply voltage: $\pm 15\text{V}$ dc
- Input: 3-wire, 24-bit SPI
- Output: $\pm 10\text{V}$ dc

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Component Selection

DAC: For convenience, devices with an external reference option or devices with accessible internal references are desirable in this application because the reference creates an offset. The DAC selection in this design must primarily be based on DC error contributions typically described by offset error, gain error, and integral nonlinearity error. Occasionally, additional specifications are provided that summarize end-point errors of the DAC typically called zero-code and full-scale errors. For AC applications, slew rate and settling time can require additional consideration.

Amplifier: Amplifier input offset voltage (V_{IO}) is a key consideration for this design. V_{IO} of an operational amplifier is a typical datasheet specification, but in-circuit performance is also affected by drift over temperature, the common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSRR); thus consideration must be given to these parameters as well. For ac operation, additional considerations must be made concerning slew rate and settling time. Input bias current (I_{IB}) can also be a factor, but typically the resistor network is implemented with sufficiently small resistor values that the effects of input bias current are negligible.

Passive: Resistor matching for the op-amp resistor network is critical for the success of this design; components with tight tolerances must be selected. For this design, 0.1% resistor values are implemented, but this constraint can be adjusted based on application-specific design goals. Resistor matching contributes to offset error and gain error in this design; see [Bipolar \$\pm 10V\$ Analog Output from a Unipolar Voltage Output DAC](#) for further details. The tolerance of the R_{ISO} and C_{COMP} stability components is not critical, and 1% components are acceptable.

8.2.1.3 Application Curves

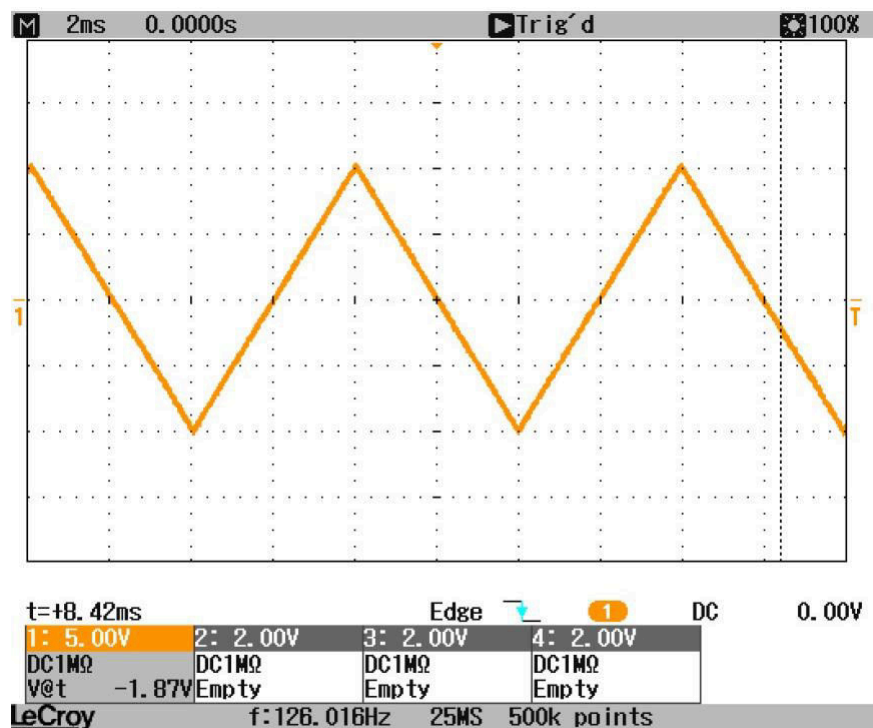
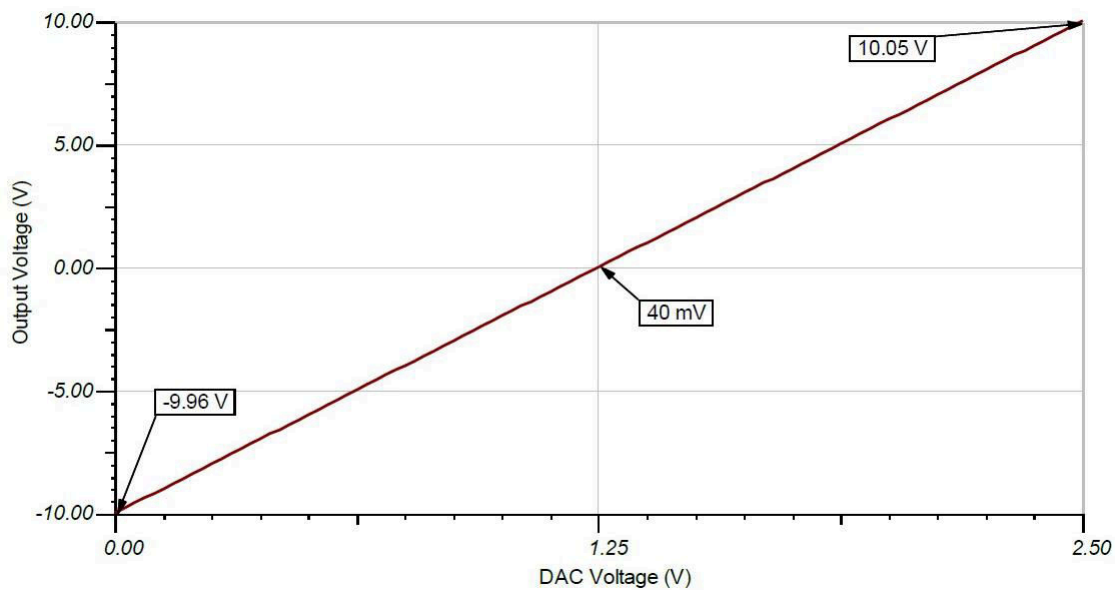


Figure 8-2. Full-Scale Output Waveform

**Figure 8-3. DC Transfer Characteristic**

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to [TI Precision Design T1PD125, Bipolar \$\pm 10V\$ Analog Output from a Unipolar Voltage Output DAC](#)

8.2.2 Discrete INA + Attenuation

The OPAX180 family can be used as a high-voltage, high-impedance front-end for a precision, discrete instrumentation amplifier with attenuation. The INA159 in [Figure 8-4](#) provides the attenuation that allows this circuit to simply interface with 3.3V or 5V analog-to-digital converters (ADCs).

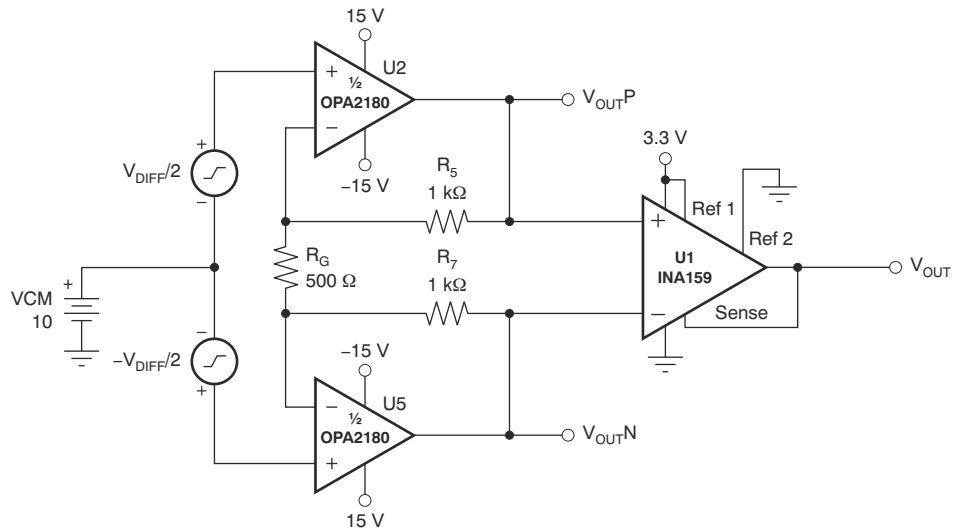
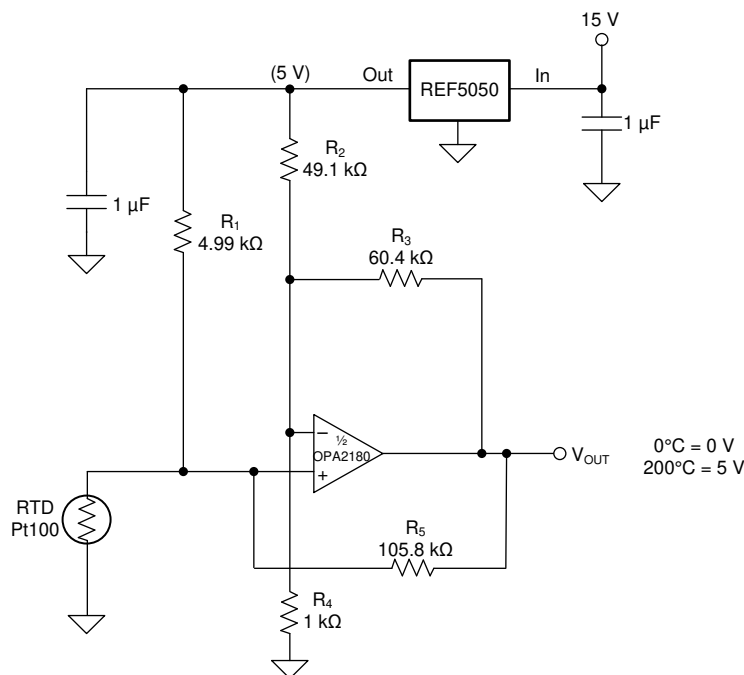


Figure 8-4. Discrete INA + Attenuation for ADC With a 3.3V Supply

8.2.3 RTD Amplifier

The OPAX180 is excellent for use in analog linearization of resistance temperature detectors (RTDs). The circuit in [Figure 8-5](#) combines the precision of the OPAX180 amplifier and the precision reference of the REF5050 to linearize a Pt100 RTD.



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NOTE: R_5 provides positive-varying excitation to linearize output.

Figure 8-5. RTD Amplifier with Linearization

8.3 Power Supply Recommendations

The OPAx180 family is specified for operation from 4V to 36V ($\pm 2V$ to $\pm 18V$); many specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in [Section 8.4](#)

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the [Absolute Maximum Ratings](#).

Place 0.1 μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Section 8.4](#).

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1 μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multi-layer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If keeping the input traces separate is not possible, crossing the sensitive trace perpendicular as opposed to in parallel with the noisy trace is much better.
- Place the external components as close to the device as possible. As shown in [Figure 8-6](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.4.2 Layout Example

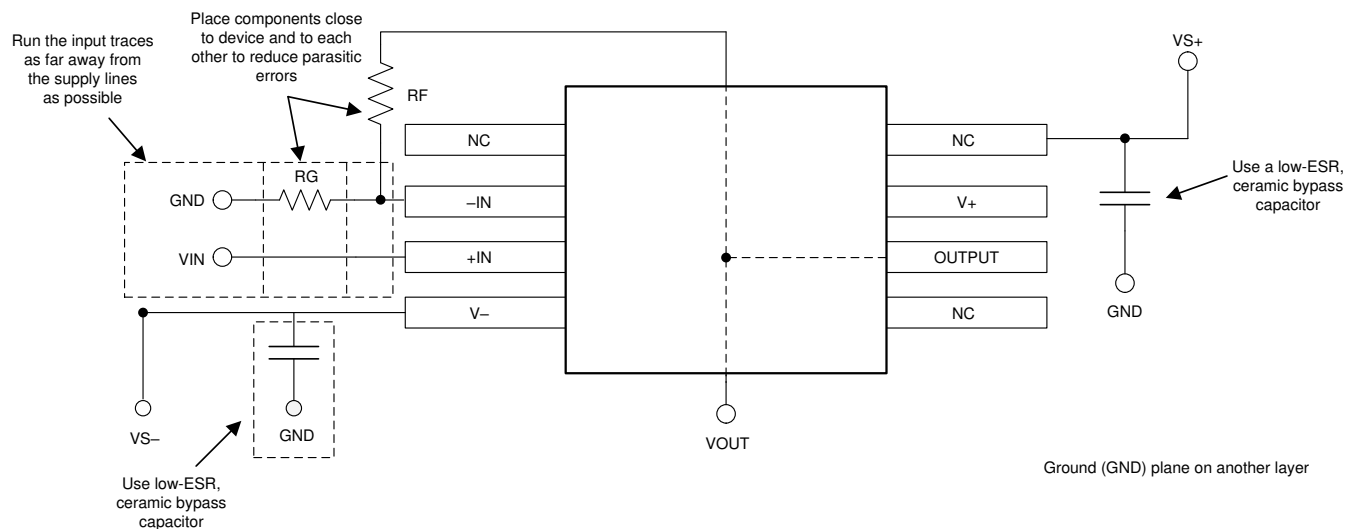


Figure 8-6. Operational Amplifier Board Layout for Noninverting Configuration

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2018) to Revision F (September 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Deleted minimum values from I_{IB} and I_{IO} in <i>Electrical Characteristics</i> table.....	9
• Changed I_{IB} maximum for OPA2180 from $\pm 1\text{nA}$ to $\pm 1.5\text{nA}$	9
• Changed I_{IO} maximum for OPA2180 from $\pm 2\text{nA}$ to $\pm 3\text{nA}$	9
• Changed I_{IB} maximum from $\pm 5\text{nA}$ ($T_A = -40^\circ\text{C}$ to 105°C) and $\pm 6\text{nA}$ ($T_A = -40^\circ\text{C}$ to 125°C) to $\pm 18\text{nA}$	9
• Changed I_{IO} maximum from $\pm 2.5\text{nA}$ ($T_A = -40^\circ\text{C}$ to 105°C) and $\pm 3\text{nA}$ ($T_A = -40^\circ\text{C}$ to 125°C) to $\pm 6\text{nA}$	9

Changes from Revision D (May 2014) to Revision E (June 2018)	Page
• Changed OPA180 and OPA4180 operating temperature from " -40°C to $+105^\circ\text{C}$ " to " -40°C to $+125^\circ\text{C}$ " in <i>Description</i> section.....	1
• Added storage temperature parameter as the last row in the <i>Absolute Maximum Ratings</i> table	7
• Changed maximum operating temperature value from 105°C to 125°C in <i>Absolute Maximum Ratings</i> table ..	7
• Changed maximum operating temperature value from 105°C to 125°C in <i>Recommended Operating Conditions</i> table	7
• Changed input offset voltage drift temperature range from $T_A = -40^\circ\text{C}$ to 105°C to $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ in <i>Electrical Characteristics</i> table.....	9
• Changed power supply rejection ratio temperature range from $T_A = -40^\circ\text{C}$ to 105°C to $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ in <i>Electrical Characteristics</i> table.....	9
• Changed OPA180 input bias current temperature range from $T_A = -40^\circ\text{C}$ to 105°C to $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ in <i>Electrical Characteristics</i> table.....	9

• Added minimum OPA2180 input bias current value of 18nA in <i>Electrical Characteristics</i> table	9
• Added minimum OPA180 input bias current value of 18nA in <i>Electrical Characteristics</i> table.....	9
• Changed OPA180 input offset current temperature range from $T_A = -40^{\circ}\text{C}$ to 105°C to $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ in <i>Electrical Characteristics</i> table.....	9
• Added minimum OPA2180 input offset current value of 6nA in <i>Electrical Characteristics</i> table	9
• Added minimum OPA180 input offset current value of 6nA in <i>Electrical Characteristics</i> table	9
• Changed common-mode rejection ratio temperature range from $T_A = -40^{\circ}\text{C}$ to 105°C to $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ in <i>Electrical Characteristics</i> table.....	9
• Changed open-loop voltage gain temperature range from $T_A = -40^{\circ}\text{C}$ to 105°C to $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ in <i>Electrical Characteristics</i> table.....	9
• Changed voltage output swing from rail temperature range from $T_A = -40^{\circ}\text{C}$ to 105°C to $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ in <i>Electrical Characteristics</i> table.....	9
• Changed quiescent current temperature range from $T_A = -40^{\circ}\text{C}$ to 105°C to $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ in <i>Electrical Characteristics</i> table.....	9
• Changed operating temperature from " -40°C to $+105^{\circ}\text{C}$ " to " -40°C to $+125^{\circ}\text{C}$ " in <i>Feature Description</i> section	17
• Updated Figure 8-5	23
• Changed operating temperature from " -40°C to $+105^{\circ}\text{C}$ " to " -40°C to $+125^{\circ}\text{C}$ " in <i>Power Supply Recommendations</i> section.....	24

Changes from Revision C (December 2012) to Revision D (May 2014)	Page
• Changed format to meet latest data sheet standards; added <i>Device Functional Modes, Application and Implementation</i> , and <i>Power Supply Recommendations</i> sections, and moved existing sections.....	1
• Added OPA180 to document.....	1
• Added Device Information table	1
• Added Pin Functions table	4
• Deleted Package Information table.....	4
• OPA180 pinout drawings	4
• Added Recommended Operating Conditions table.....	7
• Added Thermal Information: OPA180 table.....	8
• Changed Offset Voltage, <i>Long-term stability</i> parameter typical specification in <i>Electrical Characteristics</i> table.....	9
• Changed last sentence of <i>EMI Rejection</i> section.....	17

Changes from Revision B (December 2011) to Revision C (June 2012)	Page
• Changed product status from Mixed Status to Production Data.....	1
• Changed OPA4180 status to Production Data.....	1
• Added package marking to OPA2180 VSSOP-8 row in Package Information table.....	4
• Deleted ordering number and transport media columns from Package Information table.....	4
• Changed Input Bias Current section in <i>Electrical Characteristics</i> ($V_S = +4\text{V}$ to $+36\text{V}$) table.....	9

Changes from Revision A (November 2011) to Revision B (December 2011)	Page
• Changed footnote 1 of <i>Electrical Characteristics</i> table.....	9
• Updated Figure 6-7	12

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA180ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA180ID.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA180IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDBVTG4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDBVTG4.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHJ
OPA180IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHK
OPA180IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHK
OPA180IDGKT	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHK
OPA180IDGKT.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SHK
OPA180IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA180IDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA180IDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA180IDRG4.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA180
OPA2180ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180ID.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180ID.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGK	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGK.A	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGK.B	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKRG4	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKRG4.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDGKRG4.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2180IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA2180IDRG4.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2180
OPA4180ID	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180ID.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IDR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPW.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180
OPA4180IPWRG4.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4180

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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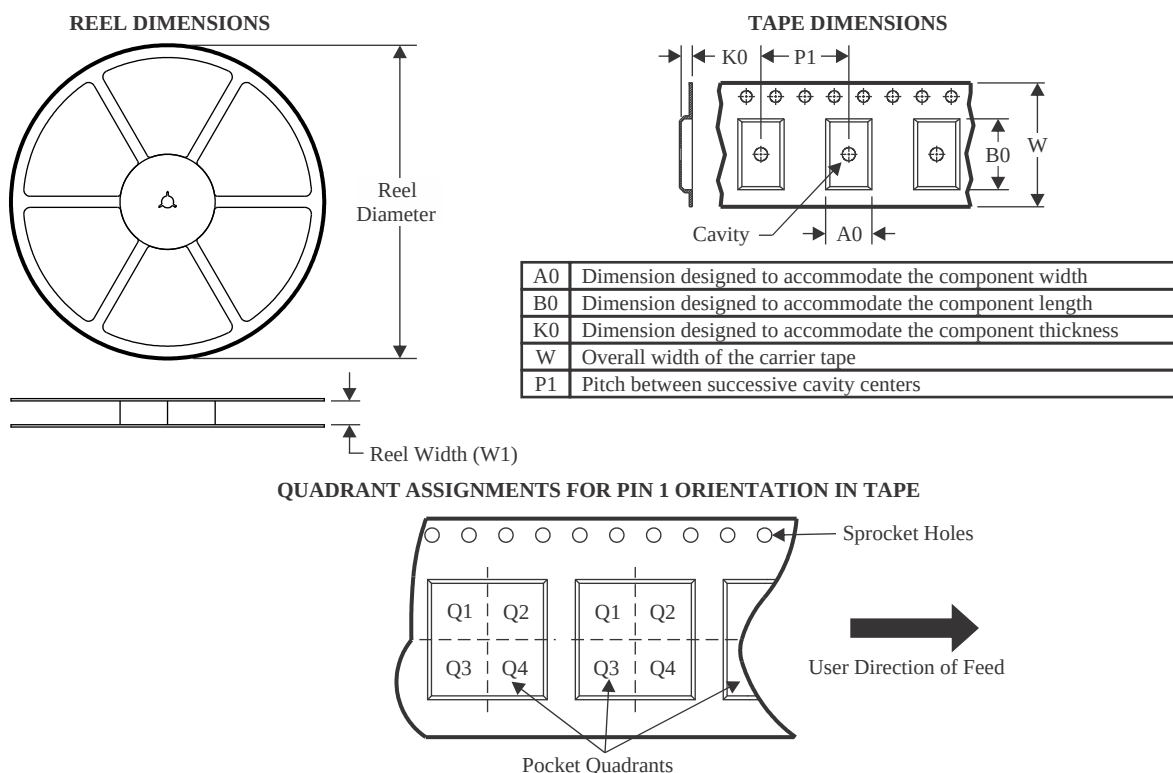
OTHER QUALIFIED VERSIONS OF OPA180, OPA2180 :

- Automotive : [OPA180-Q1](#), [OPA2180-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

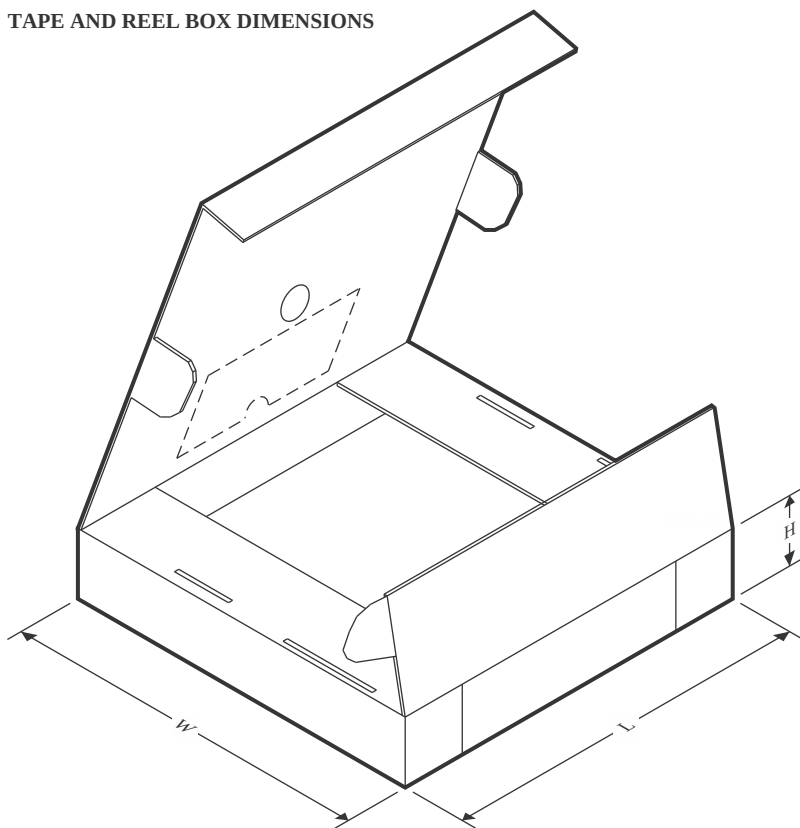
TAPE AND REEL INFORMATION



*All dimensions are nominal

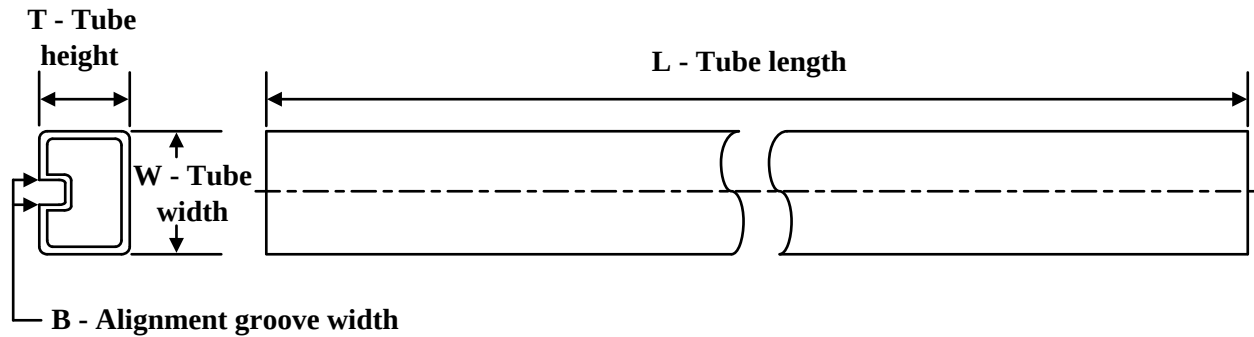
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA180IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA180IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA180IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA180IDBVTG4	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA180IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA180IDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA180IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA180IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2180IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2180IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2180IDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2180IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2180IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4180IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4180IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4180IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA180IDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA180IDBVR	SOT-23	DBV	5	3000	190.0	190.0	30.0
OPA180IDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA180IDBVTG4	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA180IDGKR	VSSOP	DGK	8	2500	346.0	346.0	29.0
OPA180IDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0
OPA180IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA180IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA2180IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2180IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2180IDGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2180IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2180IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
OPA4180IDR	SOIC	D	14	2500	353.0	353.0	32.0
OPA4180IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
OPA4180IPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE


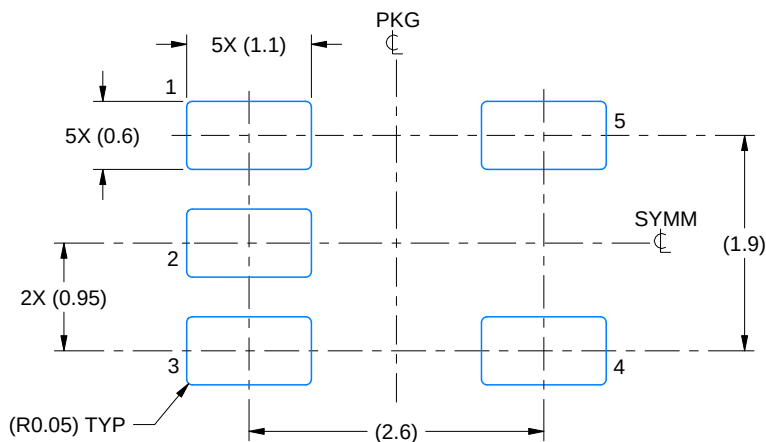
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA180ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA180ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2180ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2180ID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2180ID.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA2180IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA2180IDGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA2180IDGK.B	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA4180ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4180ID.B	D	SOIC	14	50	506.6	8	3940	4.32
OPA4180IPW	PW	TSSOP	14	90	508	8.5	3250	2.8
OPA4180IPW.B	PW	TSSOP	14	90	508	8.5	3250	2.8

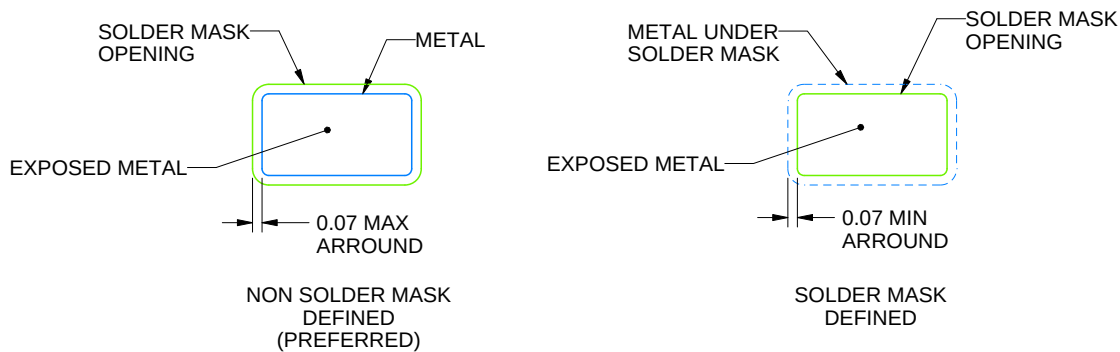
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

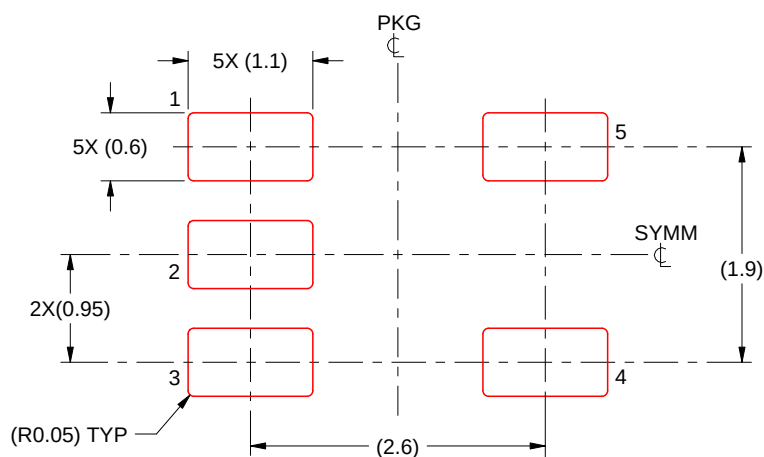
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

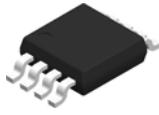


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

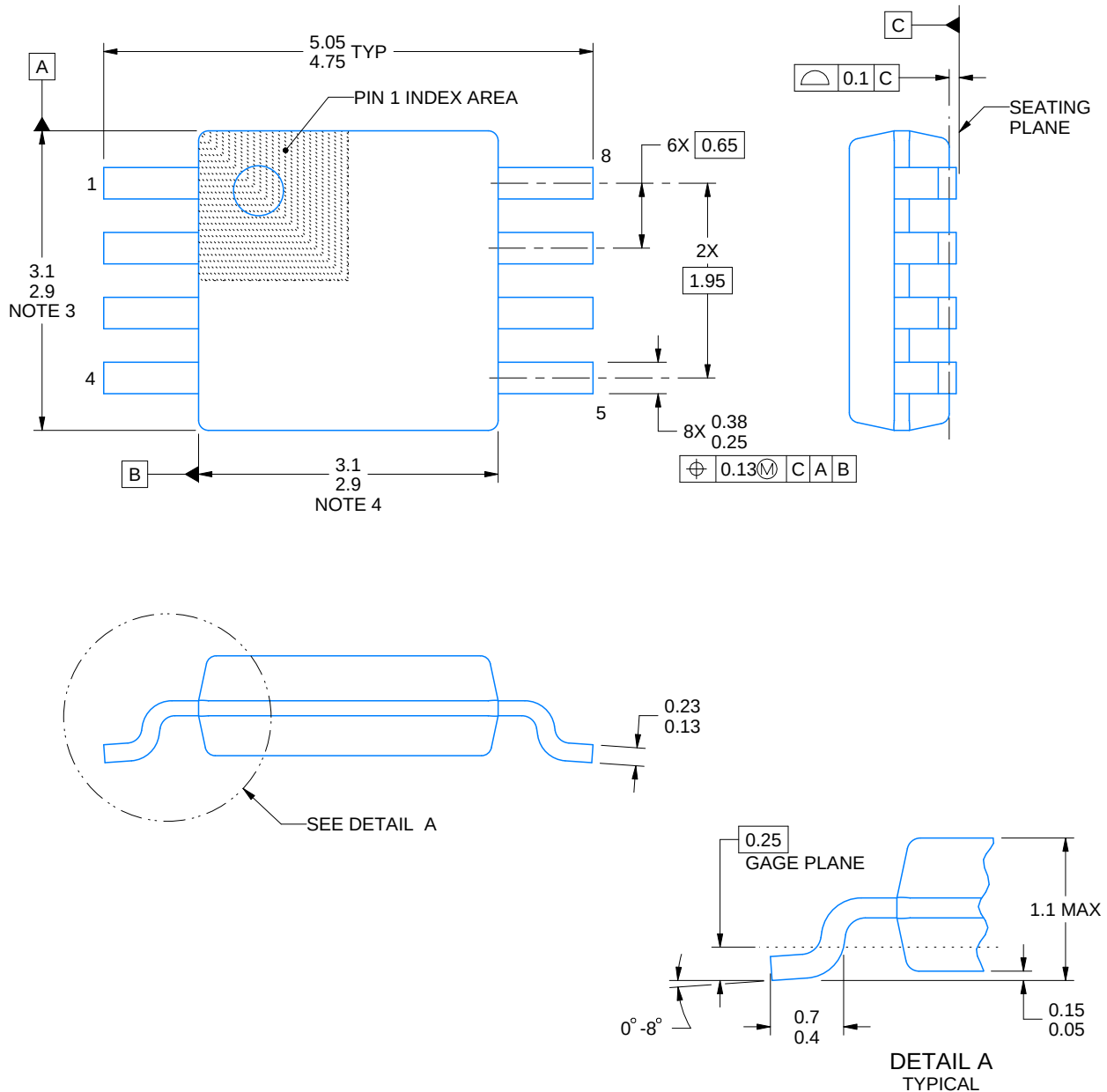
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

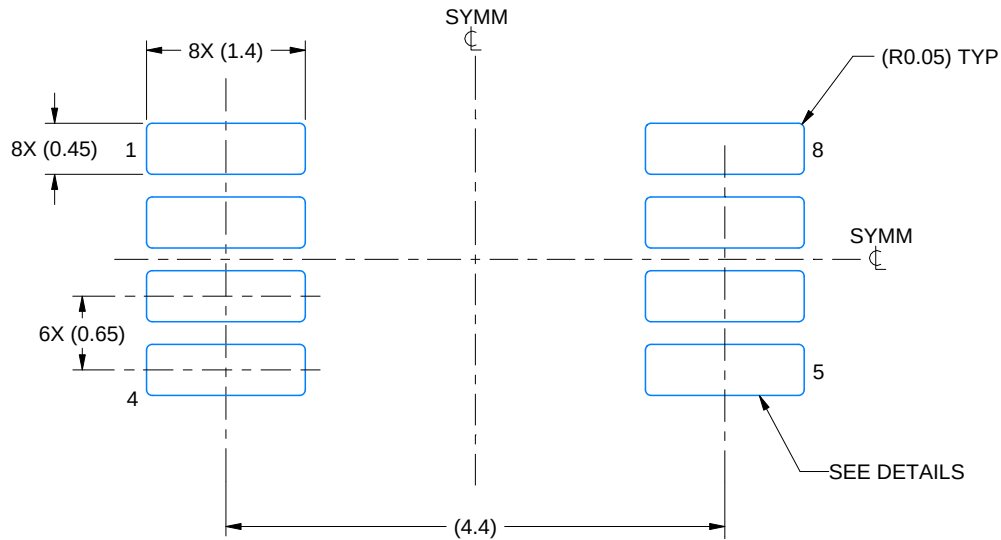
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

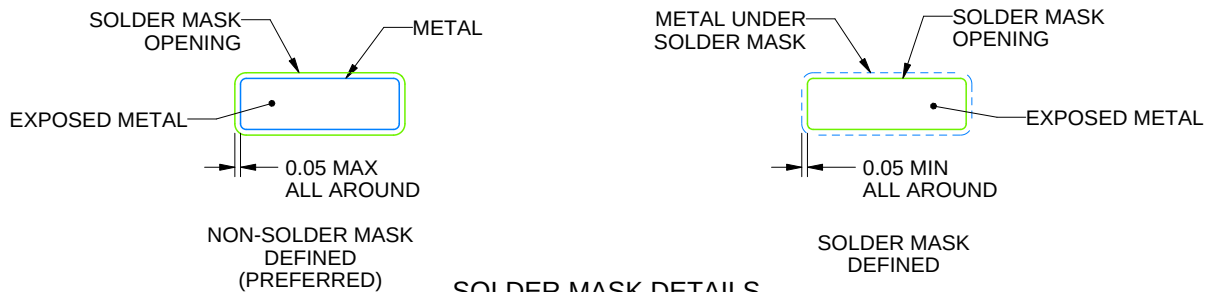
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

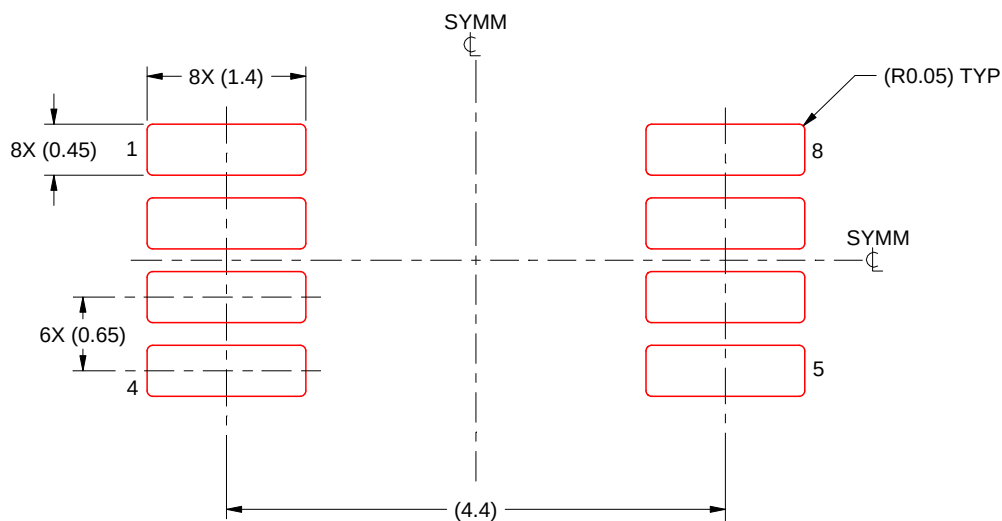
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

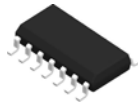


SOLDER PASTE EXAMPLE
SCALE: 15X

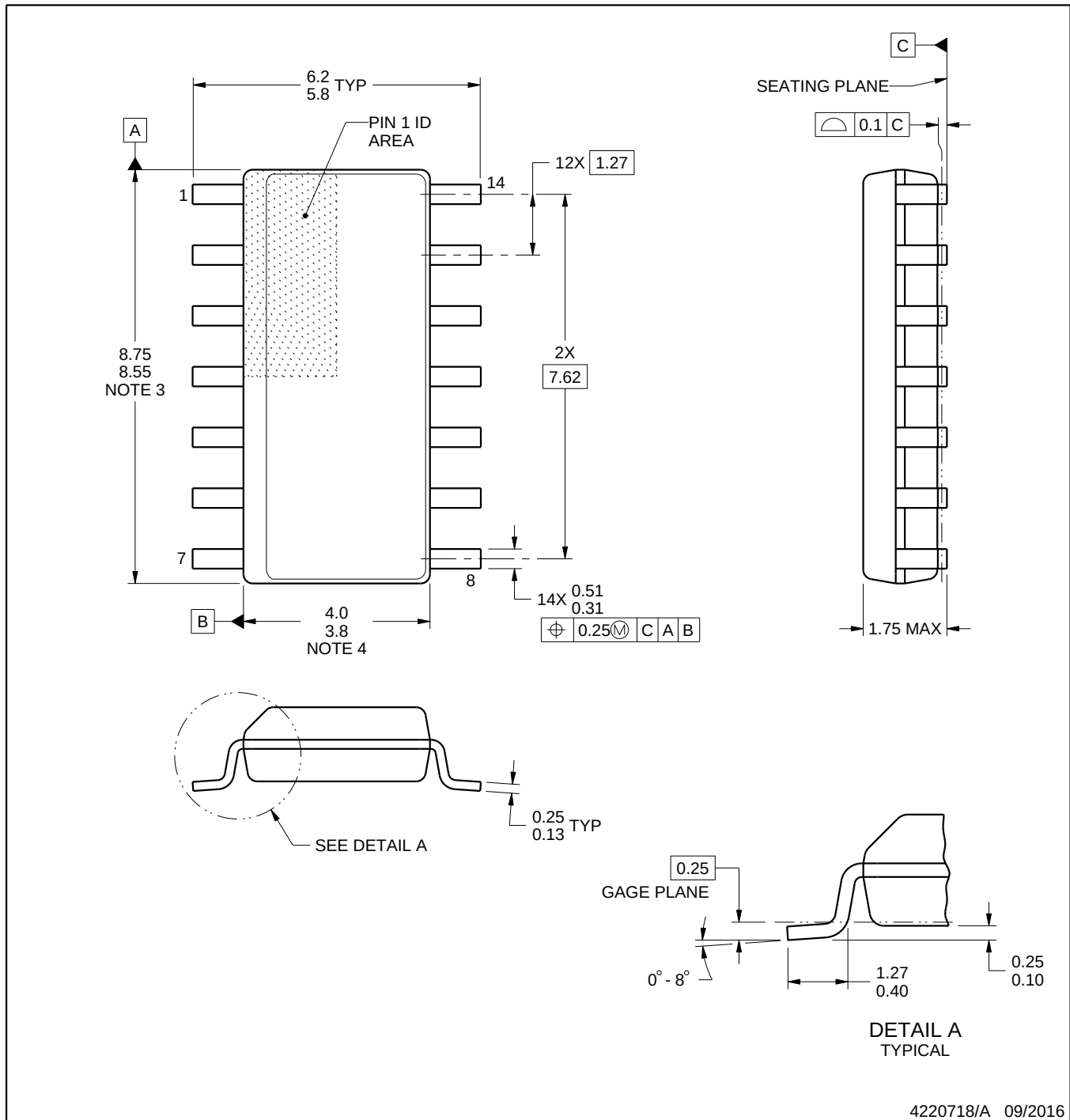
4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

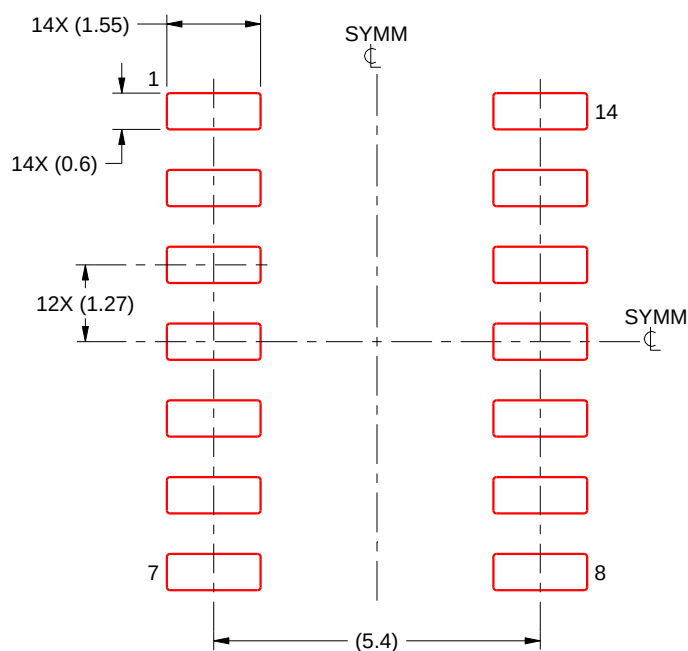
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

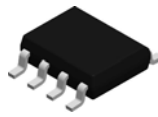


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

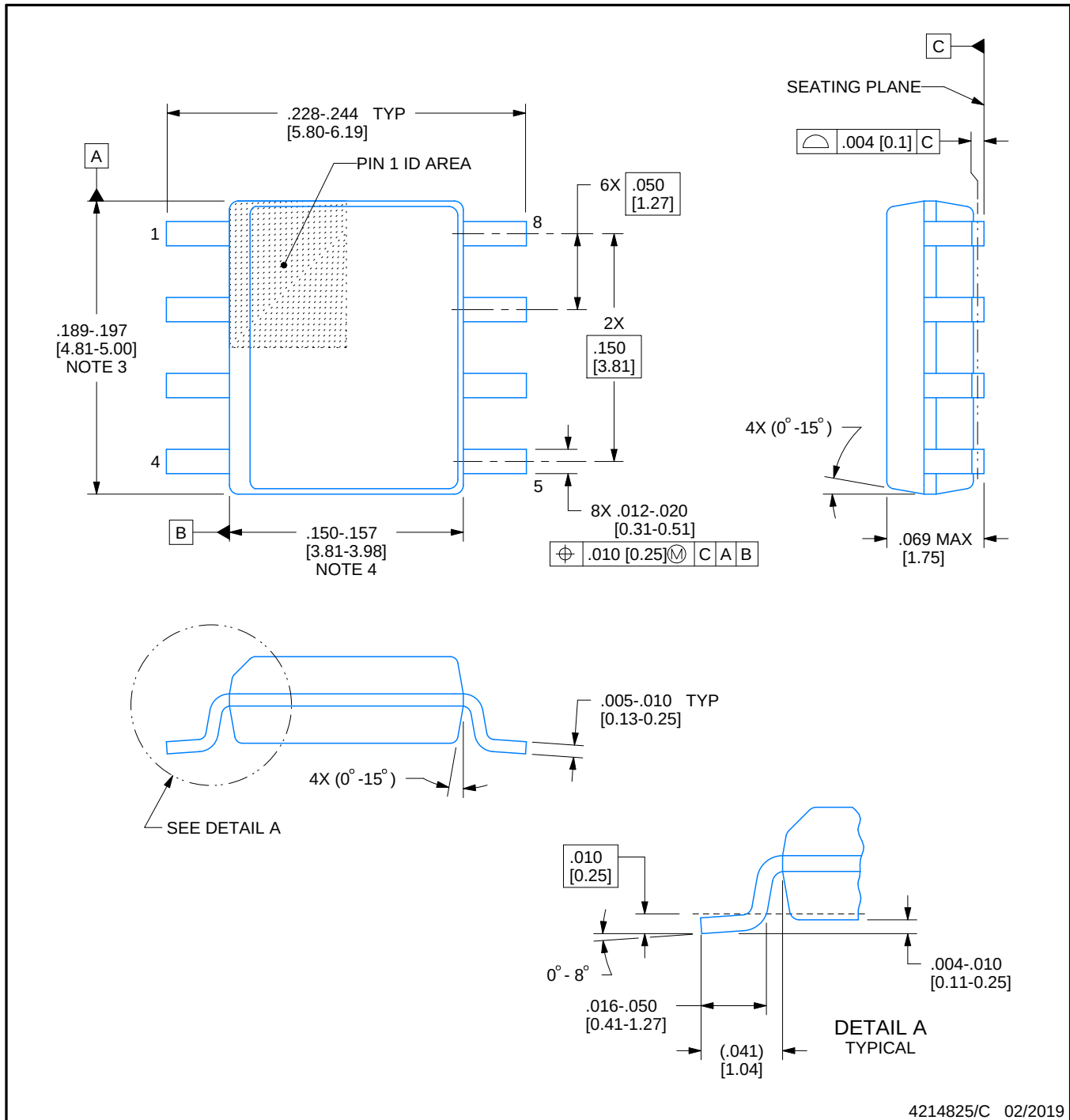


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

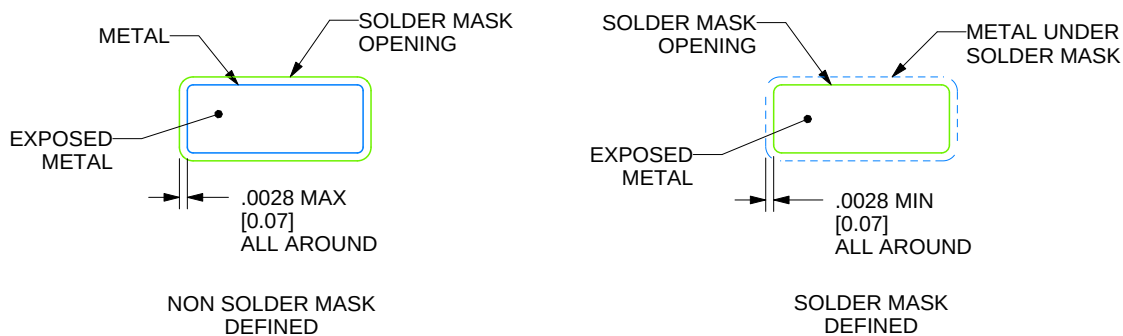
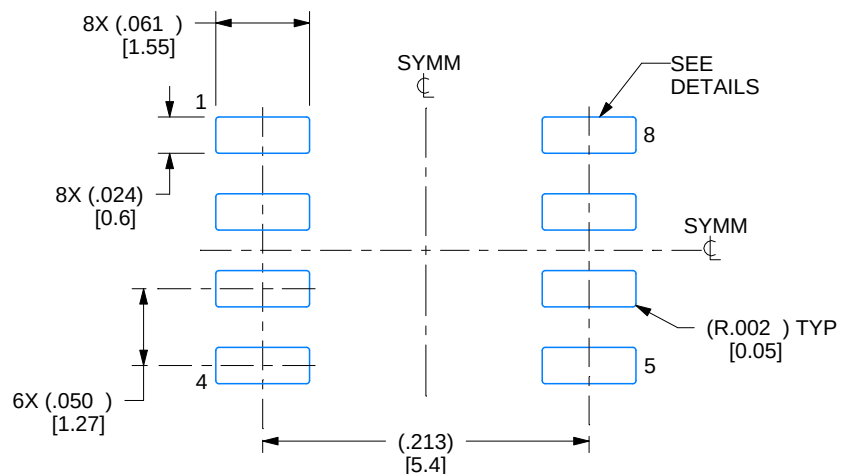
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

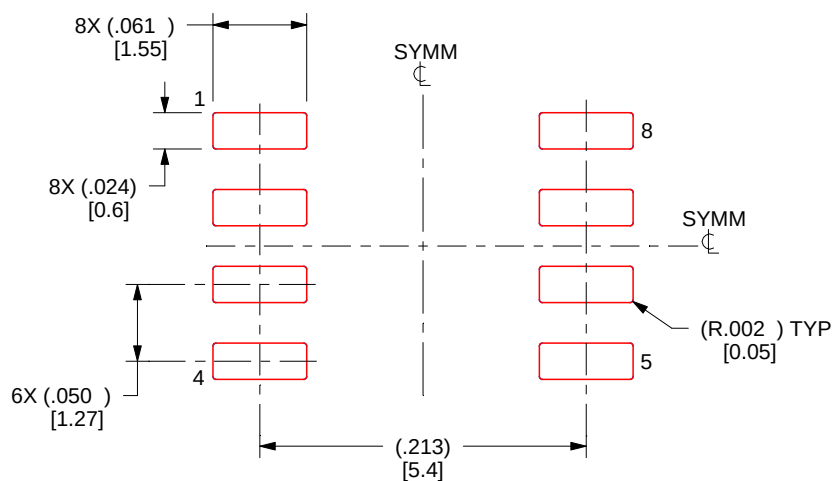
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

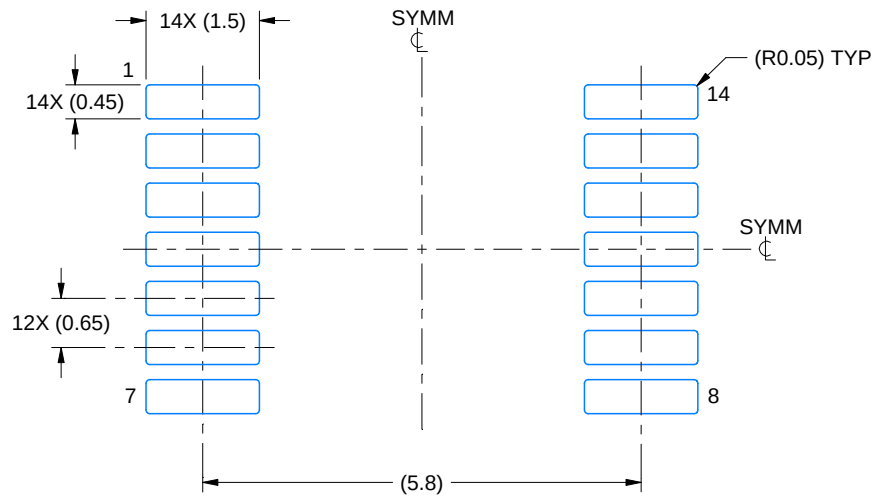
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

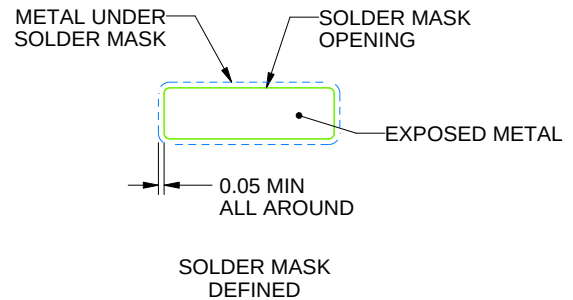
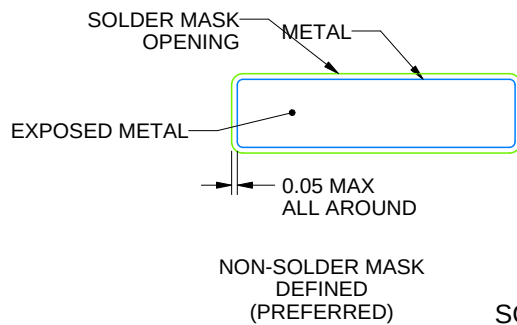
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

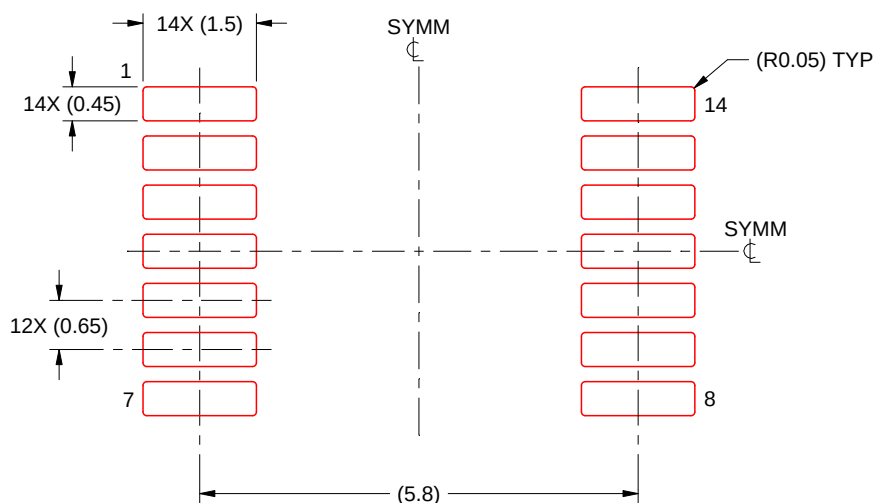
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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