11.3 Gbps Limiting Transimpedance Amplifier With RSSI

Check for Samples: ONET8521T

FEATURES

- **9 GHz Bandwidth**
- **2.4 kΩ Differential Small Signal Transimpedance**
- **-20dBm Sensitivity**
- **0.95 μA_{RMS} Input Referred Noise**
- **2.5 mA_{PP} Input Overload Current**
- **Received Signal Strength Indication (RSSI)**
- **90 mW Typical Power Dissipation**
- **CML Data Outputs with On-Chip 50Ω Back-Termination**
- **On Chip Supply Filter Capacitor**
- **Single 3.3 V Supply**
- **Die Size: 870 µm × 1036 µm**

APPLICATIONS

- **10G Ethernet**
- **8G and 10G Fibre Channel**
- **10G EPON**
- **SONET OC-192**
- **6G CPRI and OBSAI**
- **PIN Preamplifier Receivers**
- **APD Preamplifier Receivers**

DESCRIPTION

The ONET8521T is a high-speed, limiting transimpedance amplifier used in optical receivers with data rates up to 11.3Gbps. It features low input referred noise, 9GHz bandwidth, 2.4kΩ small signal transimpedance, and a received signal strength indicator (RSSI).

The ONET8521T is available in die form, includes an on-chip V_{CC} bypass capacitor and is optimized for packaging in a TO can.

The ONET8521T requires a single 3.3V ±10% supply and its power efficient design typically dissipates less than 90mW. The device is characterized for operation from –40°C to 100°C case (IC back side) temperature.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2011, Texas Instruments Incorporated

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BLOCK DIAGRAM

A simplified block diagram of the ONET8521T is shown in Figure 1.

The ONET8521T consists of the signal path, supply filters, a control block for dc input bias, automatic gain control (AGC) and received signal strength indication (RSSI). The RSSI provides the bias for the TIA stage and the control for the AGC.

The signal path consists of a transimpedance amplifier stage, a voltage amplifier, and a CML output buffer. The on-chip filter circuit provides a filtered V_{CC} for the PIN photodiode and for the transimpedance amplifier.

The dc input bias circuit and automatic gain control use internal low pass filters to cancel the dc current on the input and to adjust the transimpedance amplifier gain. Furthermore, circuitry is provided to monitor the received signal strength.

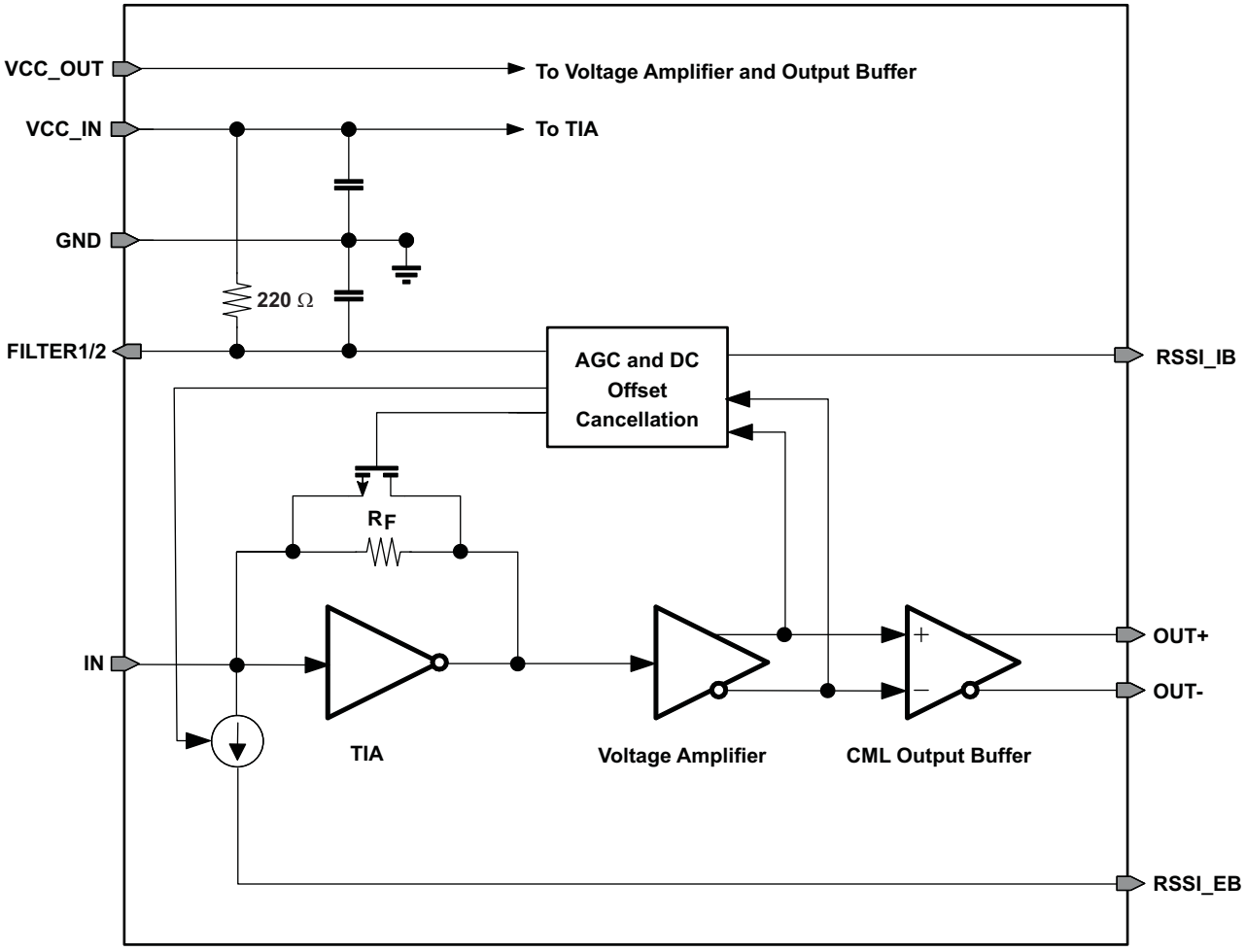


Figure 1. Simplified Block Diagram of the ONET8521T

Copyright © 2011, Texas Instruments Incorporated

BOND PAD ASSIGNMENT

The ONET8521T is available in die form. The locations of the bondpads are shown in Figure 2.

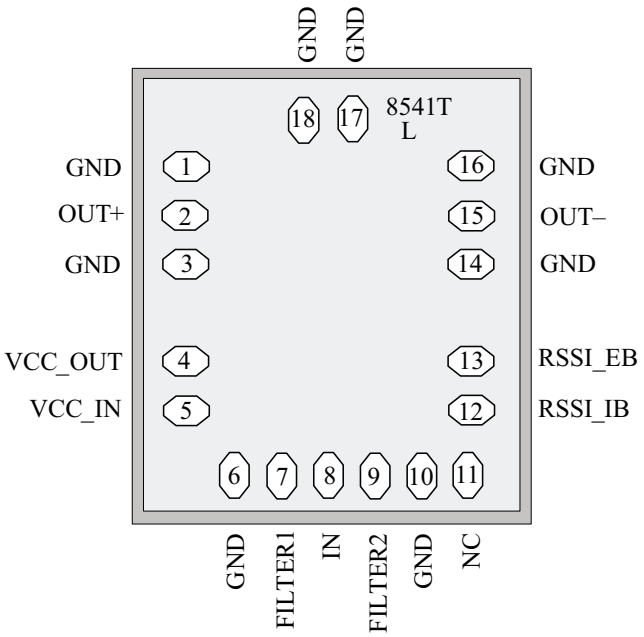


Figure 2. Bond Pad Assignment of ONET8521T

PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1, 3, 6, 10 14, 16 – 18	Supply	Circuit ground. All GND pads are connected on die. Bonding all pads is optional; however, for optimum performance a good ground connection is mandatory.
OUT+	2	Analog output	Non-inverted CML data output. On-chip 50Ω back-terminated to V_{CC}.
VCC_OUT	4	Supply	2.97V–3.63V supply voltage for the voltage and CML amplifiers.
VCC_IN	5	Supply	2.97V–3.63V supply voltage for input TIA stage.
FILTER	7, 9	Analog	Bias voltage for photodiode cathode. These pads are internally connected to an 220Ω resistor to V_{CC} and a filter capacitor to ground (GND).
IN	8	Analog input	Data input to TIA (photodiode anode).
NC	11	No Connect	Do not connect
RSSI_IB	12	Analog output	Analog output current proportional to the input data amplitude. Indicates the strength of the received signal (RSSI) if the photo diode is biased from the TIA. Connected to an external resistor to ground (GND). For proper operation, ensure that the voltage at the RSSI pad does not exceed V_{CC} – 0.65V. If the RSSI feature is not used this pad should be left open.
RSSI_EB	13	Analog output	Optional use when operated with external PD bias (e.g. APD). Analog output current proportional to the input data amplitude. Indicates the strength of the received signal (RSSI).Connected to an external resistor to ground (GND). For proper operation, ensure that the voltage at the RSSI pad does not exceed V_{CC} – 0.65V. If the RSSI feature is not used this pad should be left open.
OUT–	15	Analog output	Inverted CML data output. On-chip 50Ω back-terminated to V_{CC}.

Copyright © 2011, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC_IN}, V_{CC_OUT}	Supply voltage(2)	–0.3	4.0	V
$V_{FILTER1}$, $V_{FILTER2}$, V_{OUT+}, $V_{OUT–}$, V_{RSSI_IB}, V_{RSSI_EB}	Voltage at FILTER1, FILTER2, OUT+, OUT–, RSSI_IB, RSSI_EB(2)	–0.3	4.0	V
I_{IN}	Current into IN	–0.7	3.5	mA
I_{FILTER}	Current into FILTER1, FILTER2	–8	8	mA
I_{OUT+}, I_{OUT-}	Continuous current at outputs	–8	8	mA
ESD	ESD rating at all pins except input IN	2		kV (HBM)
	ESD rating at input IN	0.5		kV(HBM)
$T_{J,max}$	Maximum junction temperature		125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.97	3.3	3.63	V
T_A	Operating backside die temperature		–40		100(1)	°C
L_{FILTER}, L_{IN}	Wire-bond inductor at pins FILTER and IN			0.3	0.5	nH
C_{PD}	Photodiode capacitance			0.2		pF

(1) 105°C maximum junction temperature

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). Typical values are at V_{CC} = 3.3 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.97	3.3	3.63	V
I_{VCC}	Supply current	Input current i_{IN} < 1000 μA_{PP}		27	40(1)	mA
		Input current i_{IN} < 2500 μA_{PP}			45(1)	
V_{IN}	Input bias voltage		0.75	0.85	0.98	V
R_{OUT}	Output resistance	Single-ended to V_{CC}	40	50	60	Ω
R_{FILTER}	Photodiode filter resistance			220		Ω

(1) Including RSSI current

Copyright © 2011, Texas Instruments Incorporated

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). Typical values are at V_{CC} = +3.3 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{21}	Small signal transimpedance	Differential output; Input current i_{IN} = 20 μA_{PP}	1500	2400		Ω
$f_{HSS,3dB}$	Small signal bandwidth	i_{IN} = 16 μA_{PP} (1)	7	9		GHz
$f_{L,3dB}$	Low frequency –3 dB bandwidth	16 µA < i_{IN} < 2000 μA_{PP}		30	100	kHz
$i_{N,IN}$	Input referred RMS noise	10 GHz bandwidth(2)		0.95	1.4	µA
S_{US}	Unstressed sensitivity	10.3125 Gbps, PRBS31 pattern, 1310 nm, BER 10^{-12}		–20		dBm
DJ	Deterministic jitter	25 μA_{PP} < i_{IN} < 500 μA_{PP} (10.3125 Gbps, K28.5 pattern)		6	12	ps_{PP}
		500 μA_{PP} < i_{IN} < 2000 μA_{PP} (10.3125 Gbps, K28.5 pattern)		6	14	
DJ_{OL}	Overload deterministic jitter	2000 μA_{PP} < i_{IN} < 2500 μA_{PP} (10.3125 Gbps, K28.5 pattern)		7	16	ps_{PP}
$V_{OUT,D,MAX}$	Maximum differential output voltage	Input current i_{IN} = 500 μA_{PP}	180	300	420	mV_{PP}
A_{RSSI_IB}	RSSI gain internal bias	Resistive load to GND(3)	0.48	0.5	0.52	A/A
	RSSI internal bias output offset current (no light)(4)		2	7	16	µA
A_{RSSI_EB}	RSSI gain external bias	Resistive load to GND(3)	0.43		0.6	A/A
	RSSI external bias output offset current (no light)			25		µA
PSNR	Power supply noise rejection	F < 10 MHz(5), Supply filtering according to SFF8431		–15		dB

(1) The small signal bandwidth is specified over process corners, temperature, and supply voltage variation. The assumed photodiode capacitance is 0.2 pF and the bond-wire inductance is 0.3 nH. The small signal bandwidth strongly depends on environmental parasitics. Careful attention to layout parasitics and external components is necessary to achieve optimal performance.
(2) Input referred RMS noise is (RMS output noise)/ (gain at 100 MHz).
(3) The RSSI output is a current output, which requires a resistive load to ground (GND). The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation, ensure that the voltage at RSSI does not exceed V_{CC} – 0.65V.
(4) Offset is added to improve accuracy below 5µA. When measured without input current (no light) the offset can be subtracted as a constant offset from RSSI measurements.
(5) PSNR is the differential output amplitude divided by the voltage ripple on supply; no input current at IN.

Copyright © 2011, Texas Instruments Incorporated

DETAILED DESCRIPTION

SIGNAL PATH

The first stage of the signal path is a transimpedance amplifier which converts the photodiode current into a voltage. If the input signal current exceeds a certain value, the transimpedance gain is reduced by means of a nonlinear AGC circuit to limit the signal amplitude.

The second stage is a limiting voltage amplifier that provides additional limiting gain and converts the single ended input voltage into a differential data signal. The output stage provides CML outputs with an on-chip 50Ω back-termination to V_{CC}.

FILTER CIRCUITRY

The FILTER pins provide a filtered V_{CC} for a PIN photodiode bias. The on-chip low pass filter for the photodiode is implemented using a filter resistor of 220Ω and a capacitor. The corresponding corner frequency is below 5MHz. The supply voltages for the transimpedance amplifier are filtered by means of on-chip capacitors, thus avoiding the necessity to use an external supply filter capacitor. The input stage has a separate V_{CC} supply (VCC_IN) which is not connected on chip to the supply of the limiting and CML stages (VCC_OUT).

AGC AND RSSI

The voltage drop across the internal photodiode supply-filter resistor is monitored by the bias and RSSI control circuit block in the case where a PIN diode is biased using the FILTER pins.

If the dc input current exceeds a certain level then it is partially cancelled by means of a controlled current source. This keeps the transimpedance amplifier stage within sufficient operating limits for optimum performance.

The automatic gain control circuitry adjusts the voltage gain of the AGC amplifier to ensure limiting behavior of the complete amplifier.

Finally this circuit block senses the current through the filter resistor and generates a mirrored current that is proportional to the input signal strength. The mirrored current is available at the RSSI_IB output and can be sunk to ground (GND) using an external resistor. For proper operation, ensure that the voltage at the RSSI_IB pad does not exceed V_{CC} – 0.65V.

If an APD or PIN photodiode is used with an external bias then the RSSI_EB pin should be used. However, for greater accuracy under external photo diode biasing conditions, it is recommended to derive the RSSI from the external bias circuitry.

Copyright © 2011, Texas Instruments Incorporated

TYPICAL OPERATION CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

TRANSIMPEDANCE vs INPUT CURRENT

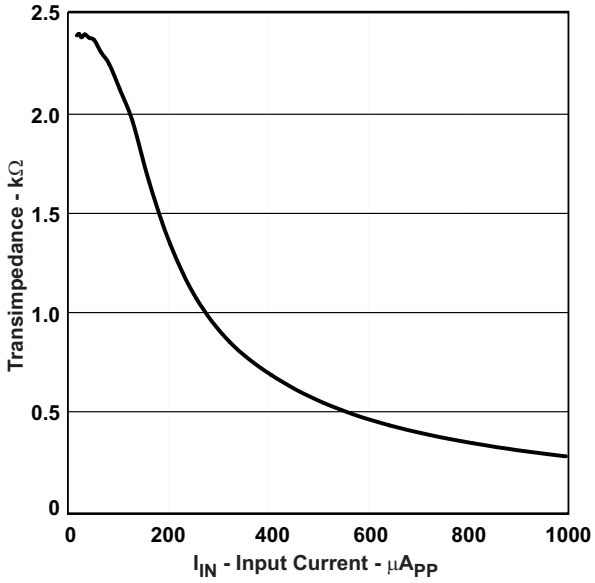


Figure 3.

SMALL SIGNAL TRANSIMPENDANCE vs AMBIENT TEMPERATURE

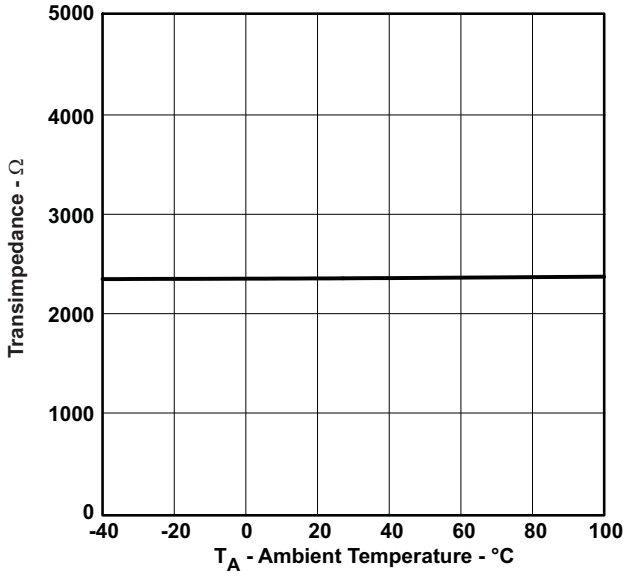


Figure 4.

SMALL SIGNAL TRANSFER CHARACTERISTICS

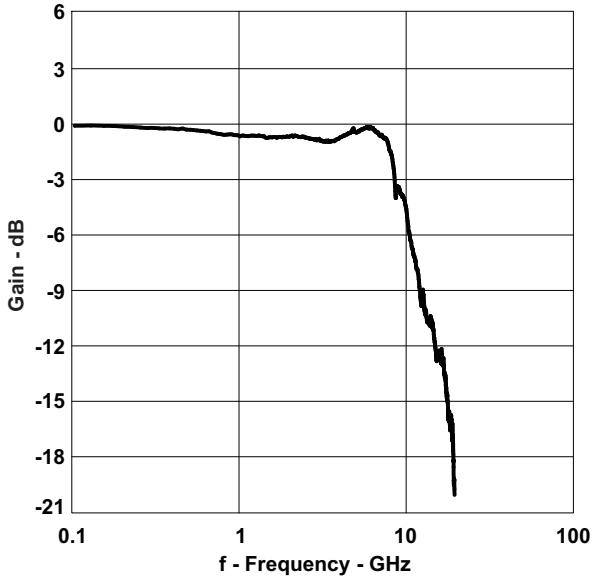


Figure 5.

SMALL SIGNAL BANDWIDTH vs AMBIENT TEMPERATURE

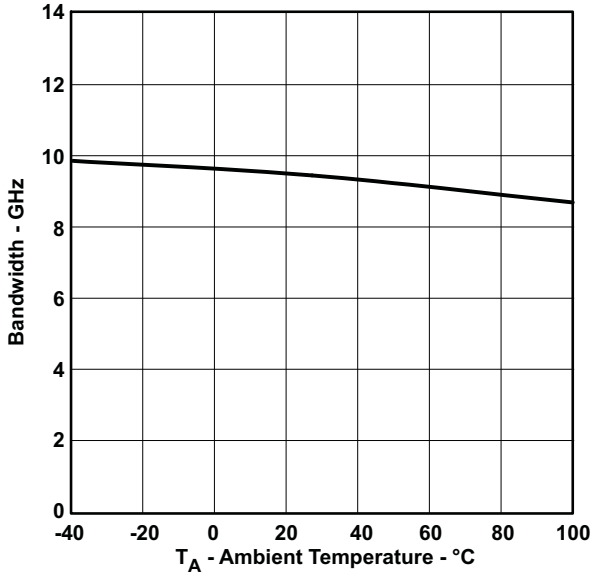


Figure 6.

Copyright © 2011, Texas Instruments Incorporated

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

OUTPUT VOLTAGE vs INPUT CURRENT

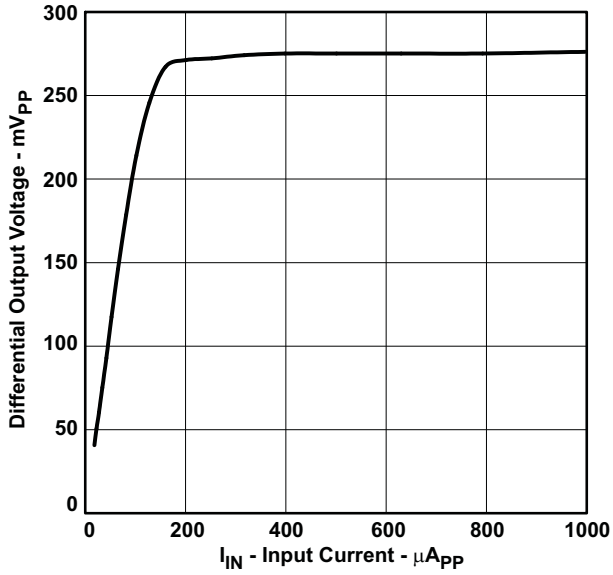


Figure 7.

DETERMINISTIC JITTER vs INPUT CURRENT

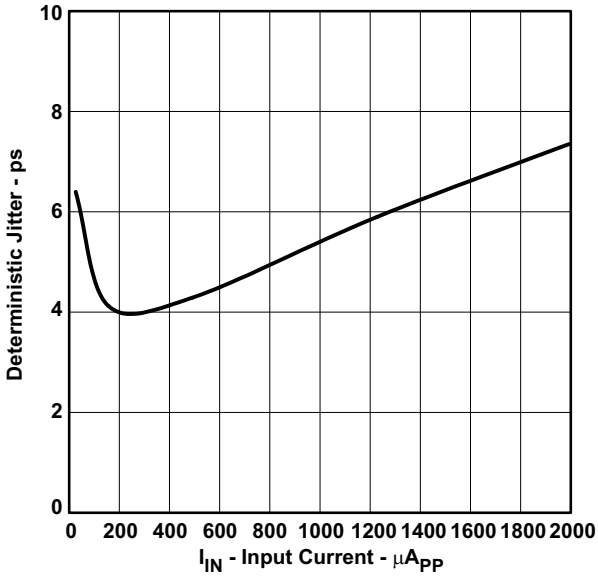


Figure 8.

INPUT REFERRED NOISE vs TEMPERATURE

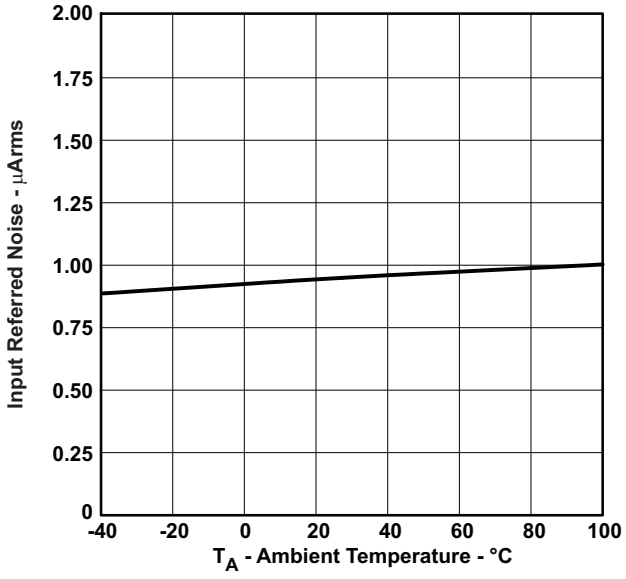


Figure 9.

RSSI_IB OUTPUT CURRENT vs AVERAGE INPUT CURRENT

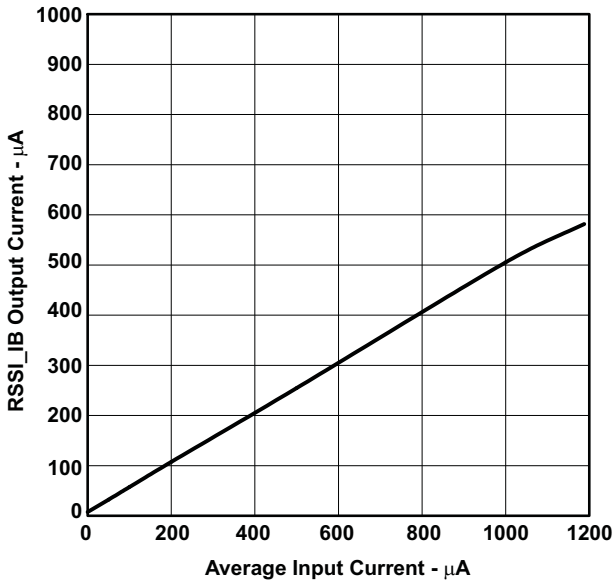


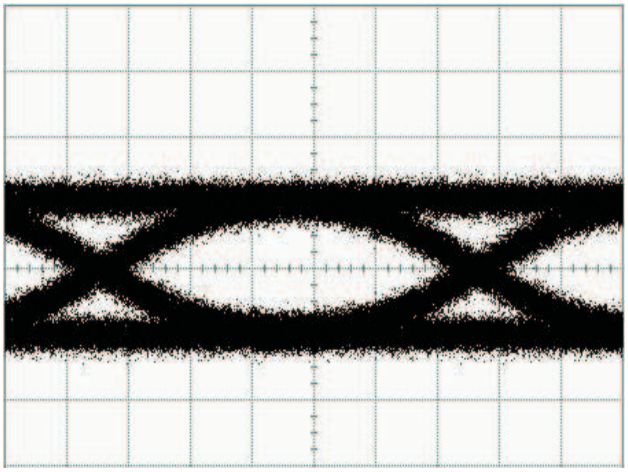
Figure 10.

Copyright © 2011, Texas Instruments Incorporated

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

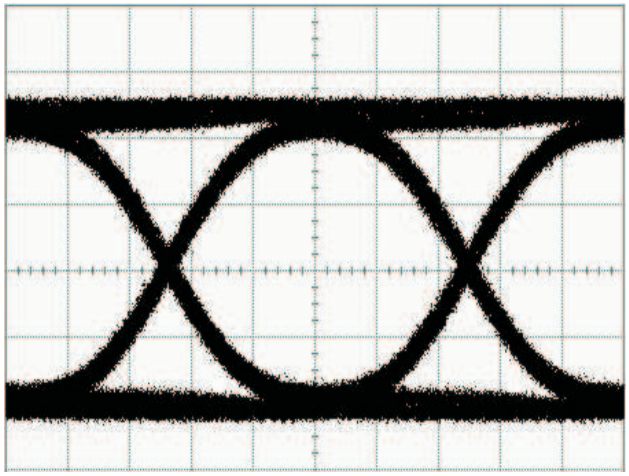
OUTPUT EYE-DIAGRAM AT 10.3 GBPS AND 20 μA_{PP} INPUT CURRENT



25 mVdiv 20 ps/div

Figure 11.

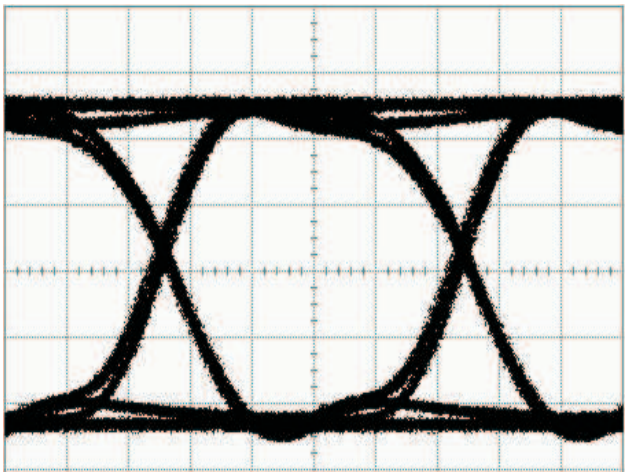
OUTPUT EYE-DIAGRAM AT 10.3 GBPS AND 100 μA_{PP} INPUT CURRENT



50 mV/div 20 ps/div

Figure 12.

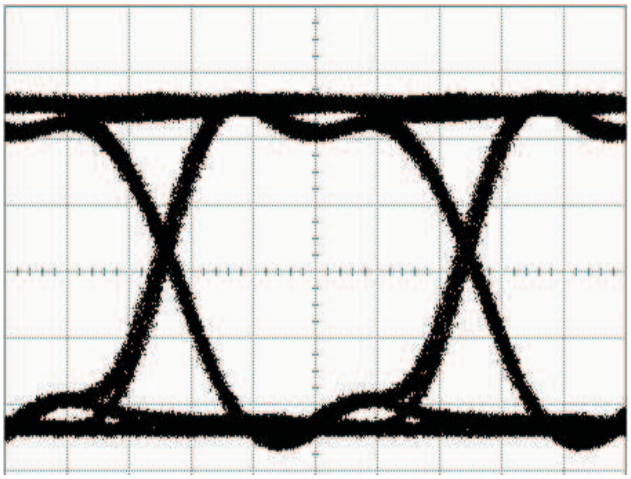
OUTPUT EYE-DIAGRAM AT 10.3 GBPS AND 500 μA_{PP} INPUT CURRENT



60 mV/div 20 ps/div

Figure 13.

OUTPUT EYE-DIAGRAM AT 10.3 GBPS AND 2 mA_{PP} INPUT CURRENT



60 mV/div 20 ps/div

Figure 14.

Copyright © 2011, Texas Instruments Incorporated

APPLICATION INFORMATION

Figure 15 shows the ONET8521T used in a typical fiber optic receiver using the internal photodiode bias. The ONET8521T converts the electrical current generated by the PIN photodiode into a differential output voltage. The FILTER inputs provide a dc bias voltage for the PIN that is low pass filtered by the combination of an internal 220Ω resistor and a capacitor. Because the voltage drop across the 220Ω resistor is sensed and used by the bias circuit, the photodiode must be connected to the FILTER pads for the bias to function correctly.

The RSSI output is used to mirror the photodiode output current and can be connected via a resistor to GND. The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation of the ONET8521T, ensure that the voltage at RSSI never exceeds V_{CC} – 0.65V. If the RSSI output is not used while operating with internal PD bias, it should be left open.

The OUT+ and OUT– pins are internally terminated by 50Ω pull-up resisters to VCC. The outputs must be ac coupled, for example by using 0.1µF capacitors, to the succeeding device.

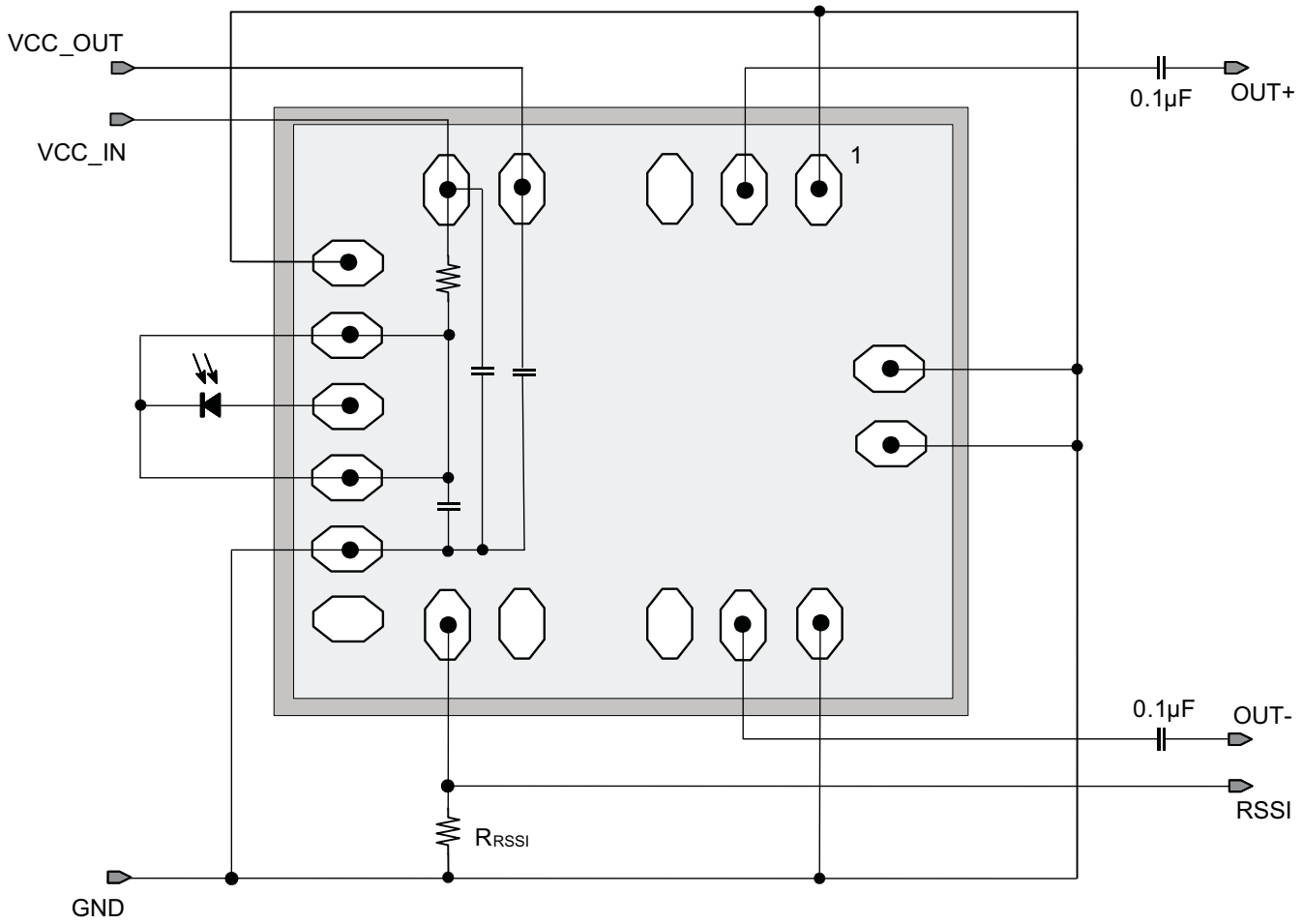


Figure 15. Basic Application Circuit for PIN Receivers

Figure 16 shows the ONET8521T being used in a typical fiber optic receiver using an external photodiode bias for an APD photodiode. This configuration can also be used for a PIN diode if desired. The external bias RSSI signal is based on a dc offset value and is not as accurate as the internal bias RSSI signal which is based upon the photodiode current.

Copyright © 2011, Texas Instruments Incorporated

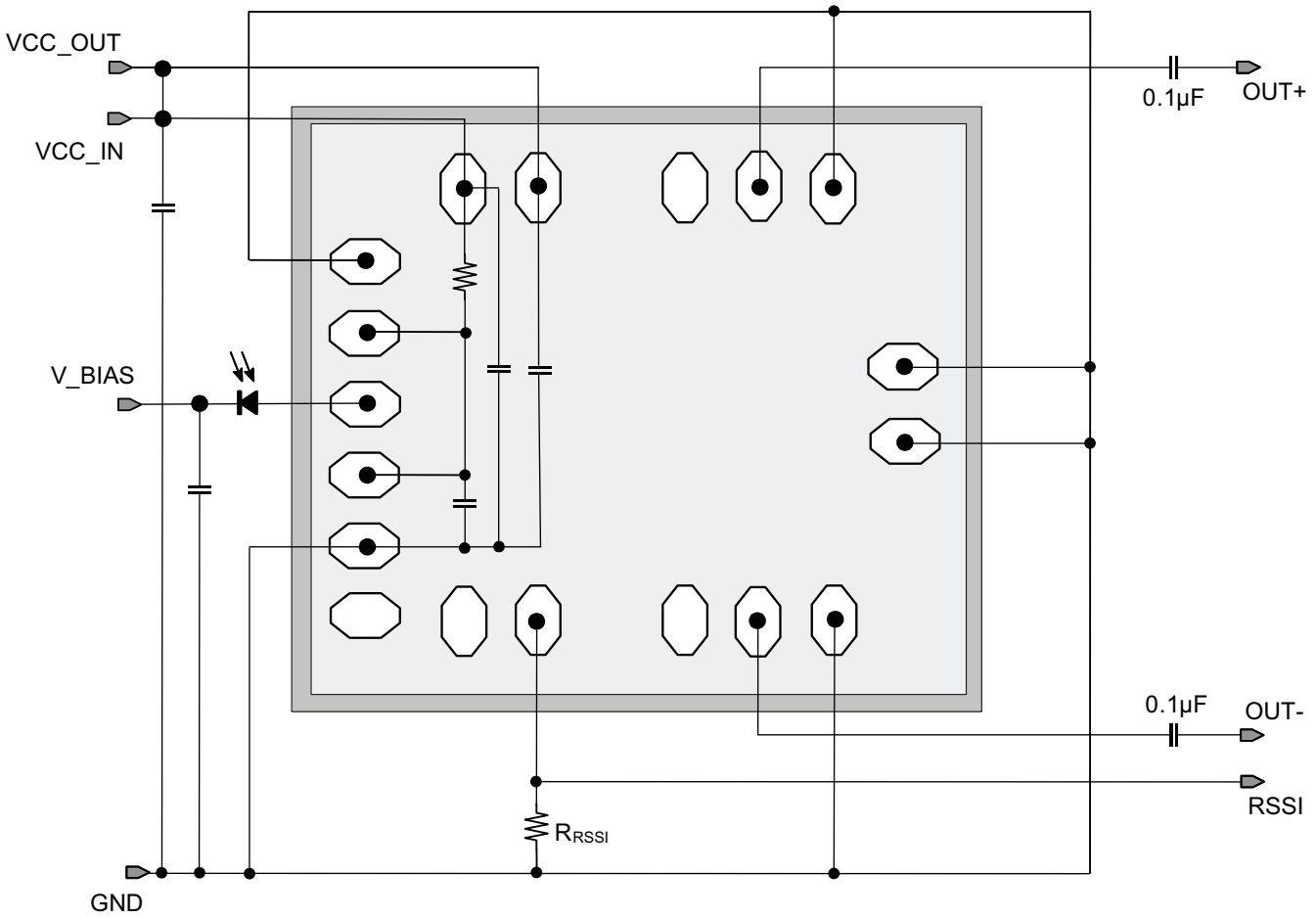


Figure 16. Basic Application Circuit for APD Receivers

ASSEMBLY RECOMMENDATIONS

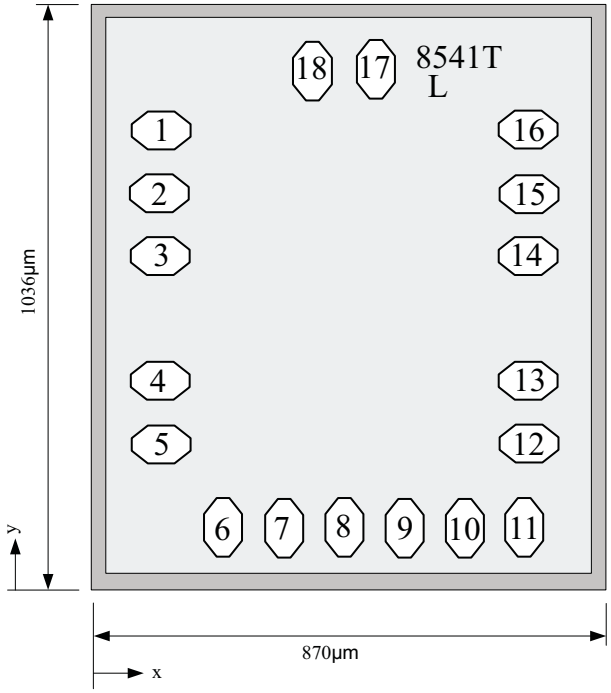
Careful attention to assembly parasitics and external components is necessary to achieve optimal performance.

Recommendations that optimize performance include:

1. Minimize the total capacitance on the IN pad by using a low capacitance photodiode and paying attention to stray capacitances. Place the photodiode close to the ONET8521T die in order to minimize the bond wire length and thus the parasitic inductance.
2. Use identical termination and symmetrical transmission lines at the ac coupled differential output pins OUT+ and OUT–.
3. Use short bond wire connections for the supply terminals VCC_IN, VCC_OUT, and GND. Supply voltage filtering is provided on chip but filtering may be improved by using an additional external capacitor.

Copyright © 2011, Texas Instruments Incorporated

CHIP DIMENSIONS AND PAD LOCATIONS



Die Thickness: 203 ± 13 µm

Pad Dimensions: 105 µm × 65 µm

Die Size: 870 ± 40 µm × 1036 ± 40 µm

PAD	COORDINATES (referenced to pad 1)		SYMBOL	TYPE	DESCRIPTION
	x (µm)	y (µm)			
1	0	0	GND	Supply	Circuit ground
2	0	-115	OUT+	Analog output	Non-inverted data output
3	0	-230	GND	Supply	Circuit ground
4	0	-460	VCC_OUT	Supply	3.3V supply voltage
5	0	-575	VCC_IN	Supply	3.3V supply voltage
6	115.5	-728	GND	Supply	Circuit ground
7	225.5	-728	FILTER1	Analog	Bias voltage for photodiode
8	335.5	-728	IN	Analog input	Data input to TIA
9	445.5	-728	FILTER2	Analog	Bias voltage for photodiode
10	555.5	-728	GND	Supply	Circuit ground
11	665.5	-728	NC	No connect	Do not connect
12	671	-575	RSSI_IB	Analog output	RSSI output signal for internally biased receivers
13	671	-460	RSSI_EB	Analog output	RSSI output signal for externally biased receivers
14	671	-230	GND	Supply	Circuit ground
15	671	-115	OUT–	Analog output	Inverted data output
16	671	0	GND	Supply	Circuit ground
17	393	109	GND	Supply	Circuit ground
18	278	109	GND	Supply	Circuit ground

Copyright © 2011, Texas Instruments Incorporated

TO46 LAYOUT EXAMPLE

An example for a layout using an external bias voltage for the photodiode in a 5 pin TO46 can is shown in Figure 17. Figure 18 shows an example with a backside cathode contact photodiode using the internal bias voltage.

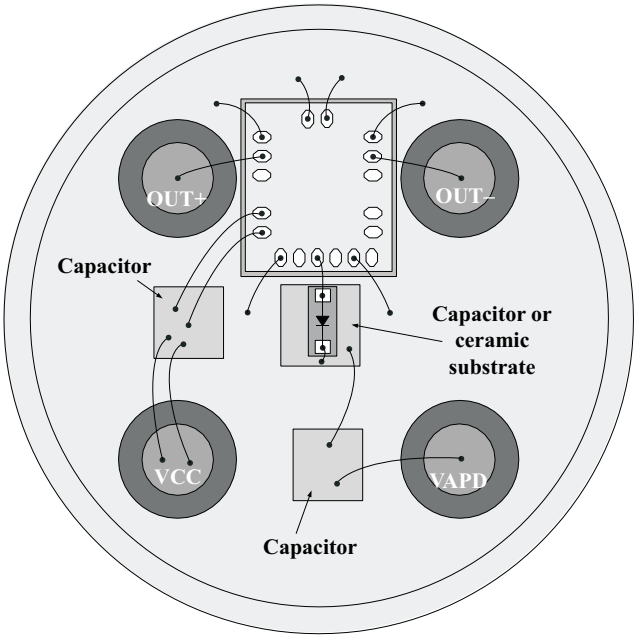


Figure 17. TO46 5 Pin Layout Using the ONET8521T with an Avalanche Photodiode

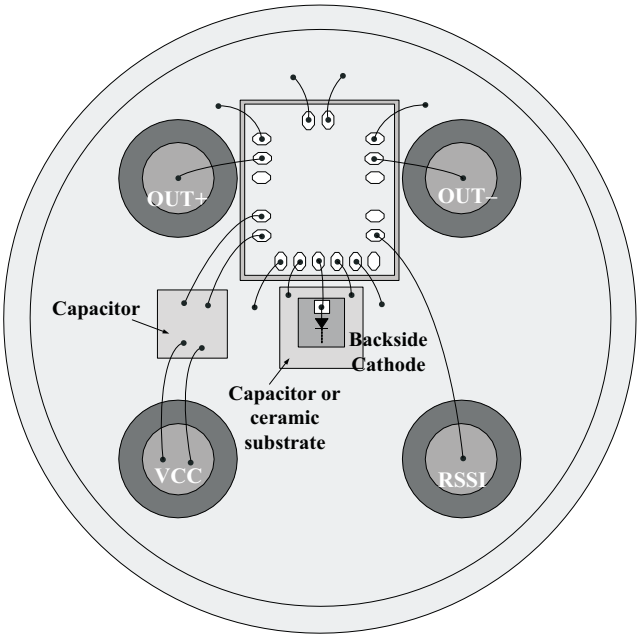


Figure 18. TO46 5 Pin Layout Using the Internal Bias Voltage for a Backside Cathode Contact Photodiode

Copyright © 2011, Texas Instruments Incorporated

REVISION HISTORY

Changes from Original (July 2011) to Revision A	Page
• Changed die size	1
• Changed die size	12

Copyright © 2011, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ONET8521TY	Obsolete	Production	DIESALE (Y) | 0	-	-	Call TI	Call TI	-40 to 100	
ONET8521TY.A	Obsolete	Production	DIESALE (Y) | 0	-	-	Call TI	Call TI	-40 to 100	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025