MSPM0L1127-Q1, MSPM0L1126-Q1 Automotive Mixed-Signal Microcontrollers

1 Features

- AEC-Q100 Grade 1 qualified for automotive applications
- **Core**
  - Arm® 32-bit Cortex®-M0+ CPU with frequency up to 32MHz
- **Operating characteristics**
  - Extended temperature: –40°C up to 125°C
  - Wide supply voltage range: 1.62V to 3.6V
- **Memories**
  - Up to 128KB of flash memory with error correction code (ECC)
  - 12KB of SRAM with ECC or parity
- **High-performance analog peripherals**
  - 12-bit 1.6Msps analog-to-digital converter (ADC), up to 26 external channels
  - Configurable 1.4V or 2.5V internal shared voltage reference (VREF)
  - Comparator (COMP) with 8-bit reference DAC
  - Integrated temperature sensor
- **Optimized low-power modes**
  - RUN: 98µA/MHz (CoreMark)
  - SLEEP: 1.3mA at 32MHz
  - STOP: 403µA at 4MHz
  - STANDBY 1.6µA with SRAM and registers fully retained
  - SHUTDOWN: 81nA with I/O wake-up capability
- **Intelligent digital peripherals**
  - 3-channel DMA controller
  - 15-channel event fabric signaling system
  - Up to eight timers supporting up to 16 PWM outputs, seven are operational down to STANDBY mode
    - One 16-bit advanced timer with deadband and the timer frequency up to 64Mhz
    - One 16-bit general purpose timer with 4 capture/compares
    - Two 16-bit general-purpose timers with 2 capture/compares
    - Four 16-bit basic timers
  - Window-watchdog timer (WWDT)
  - Independent watchdog timer (IWDT)
- **Communication interfaces**
  - Up to three UART modules, with one supporting LIN, IrDA, DALI, smart card, Manchester
  - Up to two I^2C modules supporting SMBus/ PMBus and wakeup from STOP mode, supporting up to FM+ (1Mbps)
  - Up to two SPI module supporting up to 16Mbps
- **Clock system**
  - Internal 32MHz oscillator with -2.1% to 1.6% accuracy (SYSOSC)
  - Internal 32kHz oscillator (LFOSC) with ±3% accuracy
  - External 4MHz to 32MHz crystal oscillator (HFXT)
  - External 32kHz crystal oscillator (LFXT)
  - External Low Frequency (LF) and High Frequency (HF) digital clock inputs
  - Digital clock output
- **Data integrity and encryption**
  - Cyclic redundancy checker (CRC-16)
  - AES accelerator with support for GCM/GMAC, CCM/CBC-MAC, CBC, CTR
  - Secure key storage for one 256-bit AES key or two 128-bit AES keys
- **Flexible I/O features**
  - Up to 60 total GPIOs
  - Two 5V-tolerant open-drain IOs
- **Development support**
  - 2-pin serial wire debug (SWD)
- **Package options**[1]
  - 64-pin LQFP (PM)
  - 48-pin LQFP (PT), VQFN (RGZ)
  - 32-pin VQFN (RHB)
  - 24-pin VQFN (RGE)
- **Family members**
  - MSPM0L1127-Q1: 128KB of flash, 12KB of RAM
  - MSPM0L1126-Q1: 64KB of flash, 12KB of RAM
- **Development kits and software** (also see *Tools and Software*)
  - LP-MSPM0L2117 LaunchPad™ development kit
  - MSP Software Development Kit (SDK)

2 Applications

- Automotive body electronics and Lighting
- Automotive Gateway
- Steering Wheel Systems
- Automotive Motor Control
- DC to AC Inverters
- Automotive Interior Lighting
- Door handle modules
- Kick to open modules
- Vehicle Occupancy Detection
- Seat Comfort Module

[1] QFN packages have wettable flanks.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

3 Description

MSPM0L1126/7 microcontrollers (MCUs) are part of MSP's highly integrated, ultra-low-power 32-bit MSPM0 MCU family. The microcontrollers are based on the Arm®Cortex®-M0+ 32-bit core platform, operating at up to 32MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages from 1.62V to 3.6V.

The MSPM0L1126/7 devices provide up to 128KB embedded flash program memory with built in error correction code (ECC) and 12KB SRAM with ECC and parity protection. These MCUs incorporate a high-speed on-chip oscillator with an accuracy from -2.1% to +1.6%, eliminating the need for an external crystal.

Flexible cybersecurity enablers can be used to support secure boot, IP protection (execute-only memory), key storage, and more. Hardware acceleration is provided for a variety of 128/256-bit AES symmetric cipher modes.

Additional features include a 3-channel DMA, CRC-16 accelerator, and a variety of high-performance analog peripherals such as one 12-bit 1.6Msps ADC with VDD as the voltage reference, a comparator with 8-bit reference DAC and an on-chip temperature sensor. These devices also offer intelligent digital peripherals such as one 16-bit advanced timer with deadband and timer frequency up to 64MHz, three 16-bit general purpose timer, four basic timers, one windowed watchdog timer, and a variety of communication peripherals supporting up to three UART, two SPI, and two I2C. These communication peripherals offer protocol support for LIN, IrDA, DALI, Manchester, smart card, SMBus, and PMBus.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers find the MCU that meets the project's needs. The MSPM0 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

MSPM0L1126/7 MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad available for purchase. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

For complete module descriptions, see the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See *MSP430™ System-Level ESD Considerations* for more information. The principles in this application note are applicable to MSPM0 MCUs.

Table 3-1. Package Information

PART NUMBER	PACKAGE 1	PACKAGE SIZE 2
M0L1127QPMRQ1	PM (LQFP, 64)	12mm × 12mm
M0L1126QPMRQ1		
M0L1127QPTRQ1	PT (LQFP, 48)	9mm × 9mm
M0L1126QPTRQ1		
M0L1127QRGZRQ1	RGZ (VQFN, 48)	7mm × 7mm
M0L1126QRGZRQ1		
M0L1127QRHBRQ1	RHB (VQFN, 32)	5mm x 5mm
M0L1126QRHBRQ1		

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Table 3-1. Package Information (continued)

PART NUMBER	PACKAGE 1	PACKAGE SIZE 2
M0L1127QRGERQ1	RGE (VQFN, 24)	4mm × 4mm
M0L1126QRGERQ1		

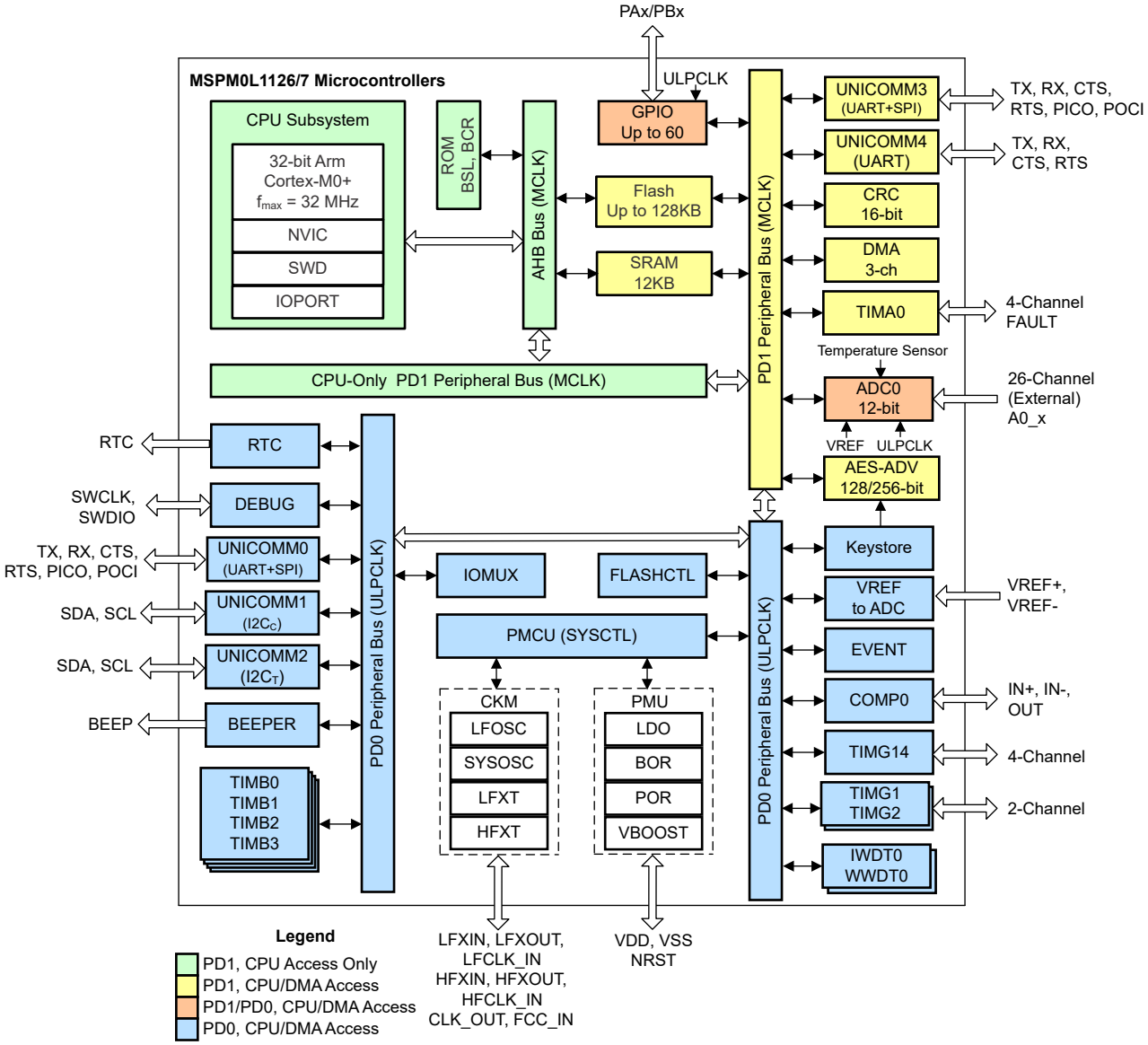
1. For more information, see Section 12.
2. The package size (length x width) is a nominal value and includes pins, where applicable.

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4 Functional Block Diagram

MSPM0L1126/7 Block Diagram shows the functional block diagram.

Figure 4-1. MSPM0L1126/7 Block Diagram



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5 Device Comparison

Table 5-1. Device Comparison Table

DEVICE NAME(1)(2)	FLASH / SRAM (KB)	ADC CHANNEL	TIMA / TIMG / TIMB	GPIO	COMP	PACKAGE(3)(4)
M0L1127QPMRQ1	128 / 12	25	1 / 3 / 4	60	1	64 LQFP (12mm × 12mm)
M0L1126QPMRQ1	64 / 12					
M0L1127QPTRQ1	128 / 12	21	1 / 3 / 4	44	1	48 LQFP (9mm × 9mm)
M0L1126QPTRQ1	64 / 12					
M0L1127QRGZRQ1	128 / 12	21	1 / 3 / 4	44	1	48 VQFN (7mm × 7mm)
M0L1126QRGZRQ1	64 / 12					
M0L1127QRHBRQ1	128 / 12	14	1 / 3 / 4	28	1	32 VQFN(5mm × 5mm)
M0L1126QRHBRQ1	64 / 12					
M0L1127QRGERQ1	128 / 12	9	1 / 3 / 4	20	1	24 VQFN (4mm × 4mm)
M0L1126QRGERQ1	64 / 12					

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum*, or see the TI website.
(2) Device Qualifications:
- Q = –40°C to 125°C

(3) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data*.
(4) The QFN packages are available with wettable flanks.

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6 Pin Configuration and Functions

The System Configuration tool provides a graphical interface to enable, configurable, and generate initialization code for pin multiplexing and simplifying pin settings. The pin diagrams shown in the data sheet show the primary peripheral functions, some of the integrated device features, and available clock signals to simplify the device pinout.

For full descriptions of the pin functions, see the *Pin Attributes* and *Signal Descriptions* sections.

6.1 Pin Diagrams

Note

For full pin configuration and functions for each package option, refer to Section 6.2 and Section 6.3.

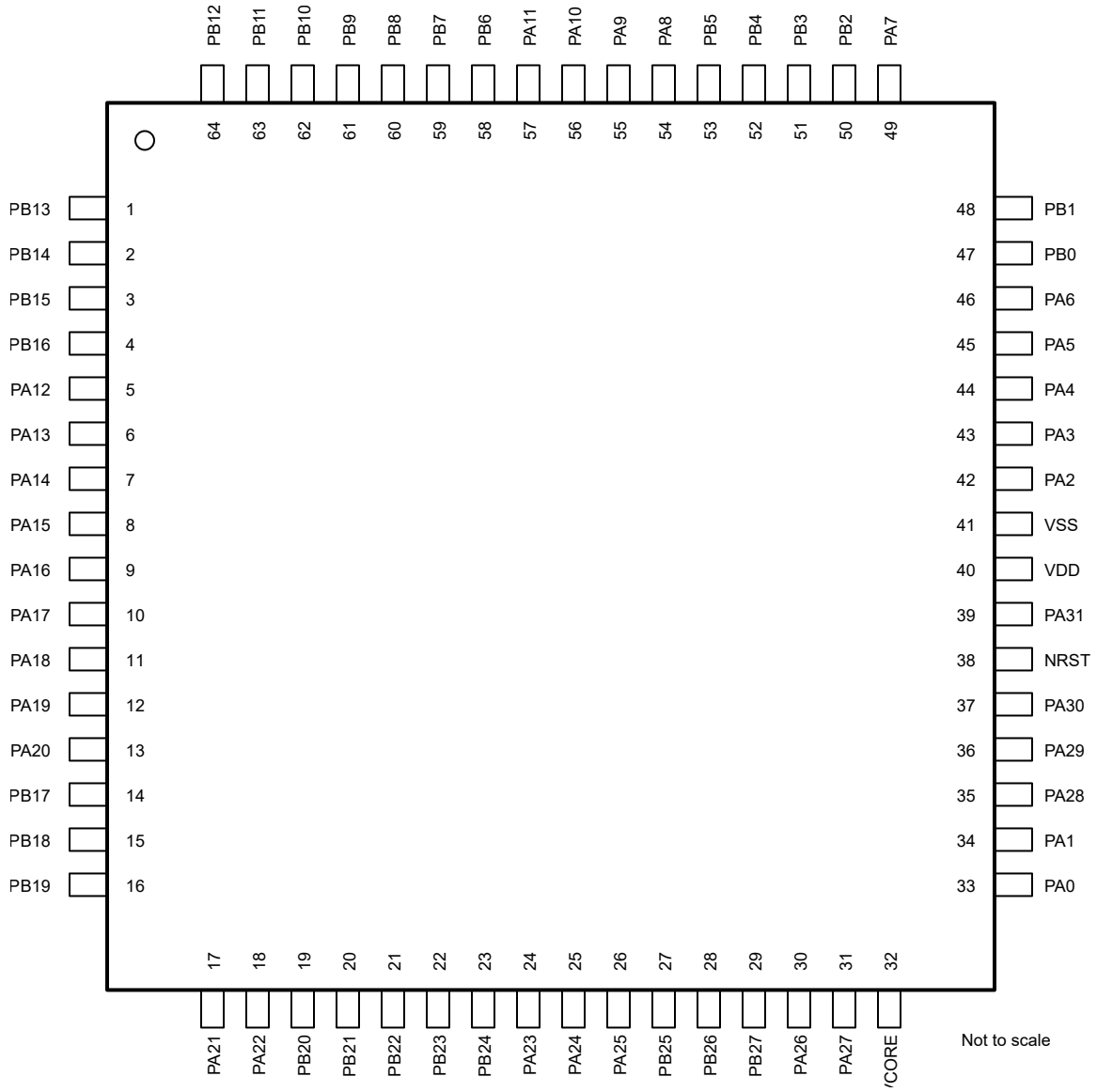


Figure 6-1. 64-pin PM (LQFP) Package

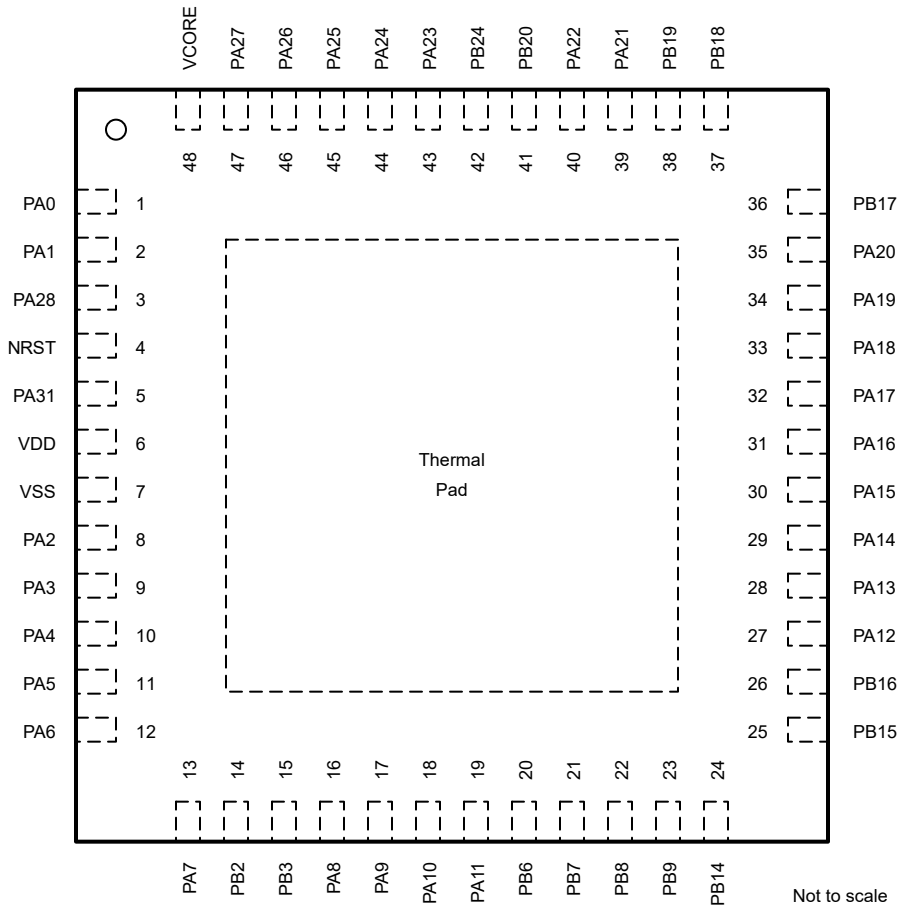


Figure 6-2. 48-pin RGZ (VQFN) Package

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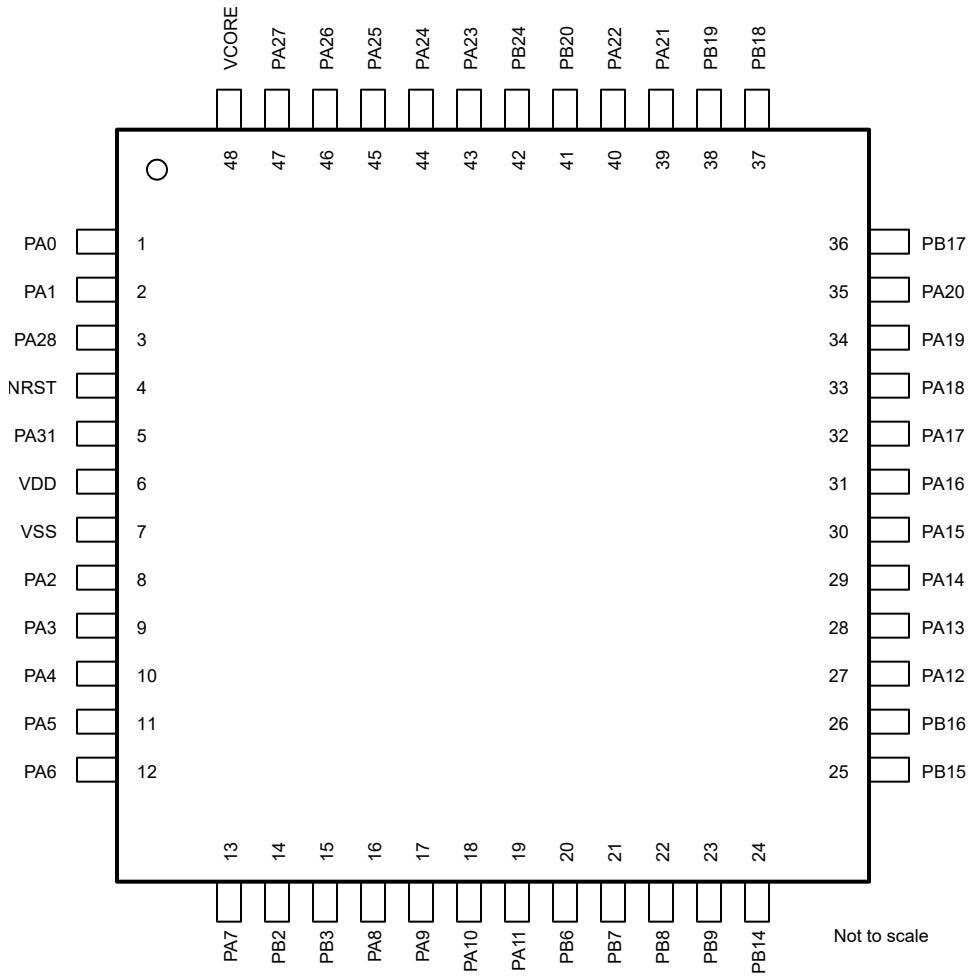


Figure 6-3. 48-pin PT (LQFP) Package

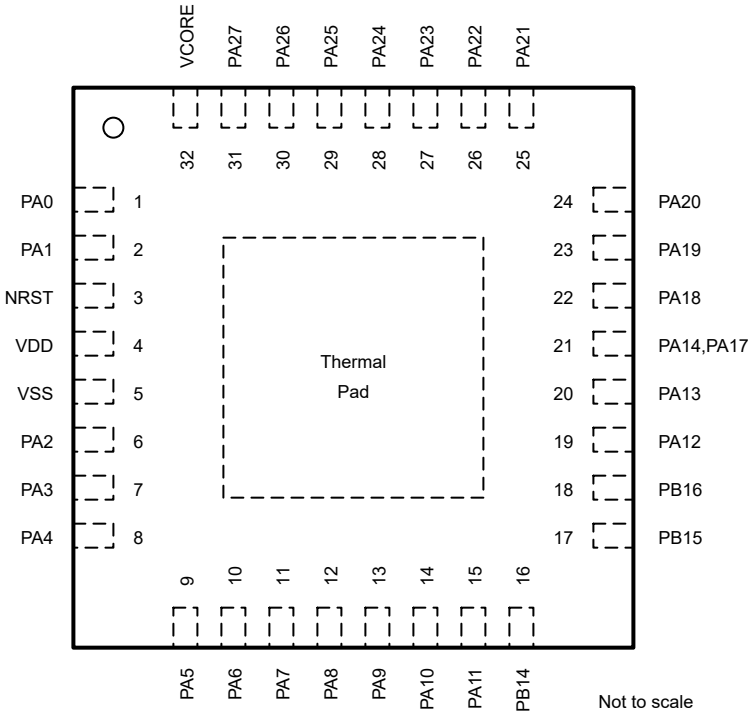


Figure 6-4. 32-pin RHB (VQFN) Package

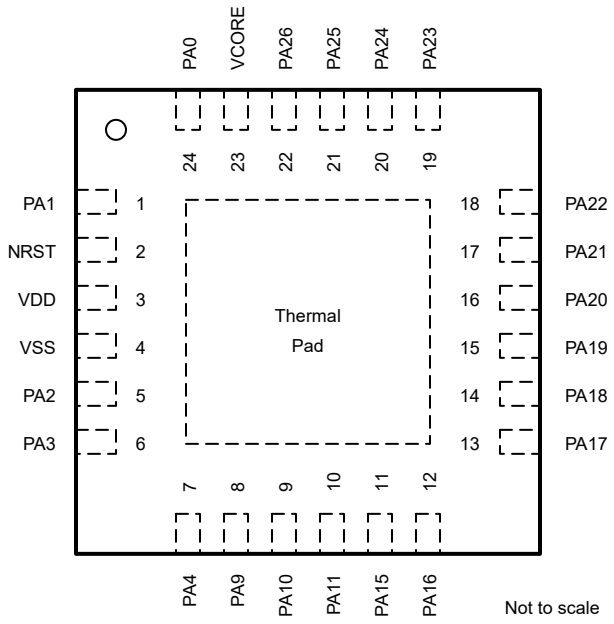


Figure 6-5. 24-pin RGE (VQFN) Package

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6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired Pin Function using the PINCM.PF control bits. The IOMUX only supports connecting one IOMUX-managed digital function to the pin at the same time. The PINCM.PF and PINCM.PC in *IOMUX* are recommended to be set to 0 when non-IOMUX managed functions (such as analog connections) are intended to be used on a pin. However, non-IOMUX managed signals (such as analog inputs and WAKE inputs) can be enabled on a pin at the same time that an IOMUX managed digital function is enabled on the pin, provided there is no contention between the functions. In this case, the designer must verify that no contention exists between the functions enabled on each pin.

Table 6-1. Digital IO Features by IO Type

BUFFER TYPE	INVERSION CONTROL	DRIVE STRENGTH CONTROL	HYSTERESIS CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR	WAKEUP LOGIC
LDIO (Low drive)	Y			Y	Y	
LDIO (Low drive) with wake	Y			Y	Y	Y
SDIO (standard drive)	Y			Y	Y	
SDIO (standard drive) with wake	Y			Y	Y	Y
HDIO (High drive)	Y			Y	Y	Y
ODIO (5V-tolerant open drain)	Y		Y		Y	Y

Table 6-2. Pin Attributes (PM, PT, RGZ, RGE, RHB Packages)

PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
38	4	4	2	3	NRST	NRST	(Non-IOMUX 1) 0	RESET	RESET
33	1	1	24	1	PA0 PINCM1 0x40428000	PA0	1	IO	ODIO (5V-tol)with wake
						UC4_PICO_TX	2	IO	
						UC6_SDA	3	IOD	
						TIMA0_C0	4	IO	
						TIMA_FAL1	5	I	
						FCC_IN	6	I	
						BEEP	8	O	
						TIMG14_C0	9	IO	
						UC7_SDA	11	IOD	
						BSLSDA	(Non-IOMUX 1) 0	IOD	
34	2	2	1	2	PA1 PINCM2 0x40428004	PA1	1	IO	ODIO (5V-tol)with wake
						UC4_SCLK_RX	2	IOD	
						UC6_SCL	3	IOD	
						TIMA0_C1	4	IO	
						TIMA_FAL2	5	I	
						TIMG14_C3	6	IO	
						TIMG14_C2	7	IO	
						TIMG14_C1	9	IO	
						UC7_SCL	11	IOD	
						BSLSCL	(Non-IOMUX 1) 0	IOD	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RGE, RHB Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
42	8	8	5	6	PA2 PINCM7 0x40428018	PA2	1	IO	LDIO
						TIMG14_C3	2	IO	
						UC4_CS0_CTS	3	IO	
						TIMG2_C1	4	IO	
						UC8_CS0	5	IO	
						TIMA0_C3N	6	O	
						TIMA0_C2N	7	O	
						TIMA_FAL0	8	I	
						TIMA_FAL1	9	I	
						TIMA0_C0	11	IO	
43	9	9	6	7	PA3 PINCM8 0x4042801c	PA3	1	IO	SDIO (standard)
						TIMG14_C2	2	IO	
						UC7_SDA	4	IOD	
						TIMA0_C1	5	IO	
						COMP0_OUT	6	O	
						TIMG2_C0	7	IO	
						TIMA0_C2	8	IO	
						UC8_PICO_TX	10	IO	
						LFXIN	(Non-IOMUX 1) 0	A	
44	10	10	7	8	PA4 PINCM9 0x40428020	PA4	1	IO	SDIO (standard)
						TIMG14_C3	2	IO	
						UC4_POCI_RTS	3	IO	
						UC7_SCL	4	IOD	
						TIMA0_C1N	5	O	
						LFCLKIN	6	I	
						TIMG2_C1	7	IO	
						TIMA0_C3	8	IO	
						UC8_SCLK_RX	10	IOD	
						UC4_CS0_CTS	11	IO	
						LFXOUT	(Non-IOMUX 1) 0	A	
45	11	11		9	PA5 PINCM10 0x40428024	PA5	1	IO	LDIO
						TIMG14_C2	2	IO	
						UC4_PICO_TX	3	IO	
						UC7_SDA	4	IOD	
						TIMG14_C0	5	IO	
						FCC_IN	6	I	
						TIMG1_C0	7	IO	
						TIMA_FAL1	8	I	
						UC4_CS0_CTS	9	IO	
						UC8_PICO_TX	11	IO	
						HFXIN	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RGE, RHB Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
46	12	12		10	PA6 PINCM11 0x40428028	PA6	1	IO	LDIO
						TIMG14_C3	2	IO	
						UC4_SCLK_RX	3	IOD	
						UC7_SCL	4	IOD	
						TIMG14_C1	5	IO	
						HFCLKIN	6	I	
						TIMG1_C1	7	IO	
						TIMA_FAL0	8	I	
						UC4_POCI_RTS	9	IO	
						TIMA0_C2N	10	O	
						UC8_SCLK_RX	11	IOD	
						HFXOUT	(Non-IOMUX 1) 0	A	
49	13	13		11	PA7 PINCM14 0x40428034	PA7	1	IO	LDIO
						COMP0_OUT	2	O	
						CLK_OUT	3	O	
						TIMG14_C2	4	IO	
						TIMA0_C2	5	IO	
						TIMG14_C3	6	IO	
						TIMG2_C1	7	IO	
						TIMA0_C1	8	IO	
						FCC_IN	10	I	
						UC4_POCI_RTS	11	IO	
54	16	16		12	PA8 PINCM19 0x40428048	PA8	1	IO	LDIO
						UC8_PICO_TX	2	IO	
						UC4_CS0_CTS	3	IO	
						UC6_SDA	4	IOD	
						TIMA0_C0	5	IO	
						TIMA_FAL2	6	I	
						TIMA_FAL0	7	I	
						TIMG2_C1	9	IO	
						HFCLKIN	10	I	
						UC4_POCI_RTS	11	IO	
55	17	17	8	13	PA9 PINCM20 0x4042804c	PA9	1	IO	LDIO
						UC8_SCLK_RX	2	IOD	
						UC4_PICO_TX	3	IO	
						UC6_SCL	4	IOD	
						TIMA0_C0N	5	O	
						CLK_OUT	6	O	
						TIMA0_C1	7	IO	
						RTC_OUT	8	O	
						TIMG2_C0	9	IO	
						UC4_CS0_CTS	11	IO	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RGE, RHB Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
56	18	18	9	14	PA10 PINCM21 0x40428050	PA10	1	IO	HDIO (high-drive)with wake
						UC4_PICO_TX	2	IO	
						UC4_POCI_RTS	3	IO	
						UC6_SDA	4	IOD	
						TIMA0_C2	5	IO	
						CLK_OUT	6	O	
						TIMG14_C0	7	IO	
						UC7_SDA	8	IOD	
						TIMA_FAL1	10	I	
						BSLTX	(Non-IOMUX 1) 0	O	
57	19	19	10	15	PA11 PINCM22 0x40428054	PA11	1	IO	HDIO (high-drive)with wake
						UC4_SCLK_RX	2	IOD	
						UC6_SCL	4	IOD	
						TIMA0_C2N	5	O	
						COMP0_OUT	6	O	
						TIMG14_C1	7	IO	
						UC7_SCL	8	IOD	
						TIMA_FAL0	10	I	
						COMP0_DAC_OUT	(Non-IOMUX 1) 0	A	
						BSLRX	(Non-IOMUX 2) 0	I	
5	27	27		19	PA12 PINCM34 0x40428084	PA12	1	IO	LDIO
						UC4_POCI_RTS	2	IO	
						UC4_SCLK_RX	3	IOD	
						COMP0_OUT	4	O	
						TIMA0_C3	5	IO	
						FCC_IN	6	I	
						TIMG14_C0	7	IO	
						UC7_SCL	8	IOD	
						TIMA0_C2	9	IO	
						ADC0_18	(Non-IOMUX 1) 0	A	
6	28	28		20	PA13 PINCM35 0x40428088	PA13	1	IO	LDIO
						TIMA0_C2N	2	O	
						UC4_POCI_RTS	3	IO	
						UC7_SDA	4	IOD	
						TIMA0_C3N	5	O	
						RTC_OUT	6	O	
						TIMG14_C1	7	IO	
						UC8_CS0	8	IO	
						UC8_POCI	9	IO	
						UC11_TX	10	IO	
						COMP0_OUT	11	O	
						ADC0_17	(Non-IOMUX 1) 0	A	
						COMP0_IN2-	(Non-IOMUX 3) 0	A	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RGE, RHB Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
7	29	29		21	PA14 PINCM36 0x4042808c	PA14	1	IO	LDIO
						UC4_CS0_CTS	2	IO	
						UC4_PICO_TX	3	IO	
						CLK_OUT	6	O	
						UC11_RX	10	IO	
						ADC0_16	(Non-IOMUX 1) 0	A	
						COMP0_IN2+	(Non-IOMUX 3) 0	A	
8	30	30	11		PA15 PINCM37 0x40428090	PA15	1	IO	LDIO
						UC4_POCI_RTS	2	IO	
						UC7_SCL	4	IOD	
						TIMA0_C2	5	IO	
						TIMG14_C2	7	IO	
						ADC0_15	(Non-IOMUX 1) 0	A	
						COMP0_IN3+	(Non-IOMUX 2) 0	A	
9	31	31	12		PA16 PINCM38 0x40428094	PA16	1	IO	LDIO
						COMP0_OUT	2	O	
						UC8_POCI	3	IO	
						UC7_SDA	4	IOD	
						TIMA0_C2N	5	O	
						FCC_IN	7	I	
						ADC0_14	(Non-IOMUX 1) 0	A	
10	32	32	13	21	PA17 PINCM39 0x40428098	PA17	1	IO	LDIO with wake
						UC8_PICO_TX	2	IO	
						UC8_SCLK_RX	3	IOD	
						UC7_SCL	4	IOD	
						TIMA0_C3	5	IO	
						TIMG2_C0	6	IO	
						TIMG14_C2	7	IO	
						ADC0_13	(Non-IOMUX 1) 0	A	
						COMP0_IN1-	(Non-IOMUX 2) 0	A	
11	33	33	14	22	PA18 PINCM40 0x4042809c	PA18	1	IO	LDIO with wake
						UC8_SCLK_RX	2	IOD	
						UC8_PICO_TX	3	IO	
						UC7_SDA	4	IOD	
						TIMA0_C3N	5	O	
						TIMG2_C1	6	IO	
						TIMG14_C3	7	IO	
						UC4_CS0_CTS	9	IO	
						ADC0_12	(Non-IOMUX 1) 0	A	
						COMP0_IN1+	(Non-IOMUX 2) 0	A	
						BSL_INVOKE	(Non-IOMUX 3) 0	I	
12	34	34	15	23	PA19 PINCM41 0x404280a0	PA19	1	IO	LDIO
						SWDIO	2	IO	
						UC8_POCI	3	IO	
						UC7_SDA	4	IOD	
						TIMA0_C2	5	IO	
						TIMG14_C0	6	IO	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RGE, RHB Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
13	35	35	16	24	PA20 PINCM42 0x404280a4	PA20	1	IO	SDIO (standard)
						SWCLK	2	I	
						UC8_SCLK_RX	3	IOD	
						UC7_SCL	4	IOD	
						TIMA0_C2N	5	O	
						TIMG14_C1	6	IO	
17	39	39	17	25	PA21 PINCM46 0x404280b4	PA21	1	IO	LDIO
						UC11_TX	2	IO	
						TIMA0_C0	5	IO	
						TIMG1_C0	6	IO	
						TIMG14_C2	10	IO	
						ADC0_8	(Non-IOMUX 1) 0	A	
						ADC0_VREF-	(Non-IOMUX 2) 0	A	
18	40	40	18	26	PA22 PINCM47 0x404280b8	PA22	1	IO	LDIO
						UC11_RX	2	IO	
						TIMA0_C0N	5	O	
						TIMG1_C1	6	IO	
						TIMA0_C1	7	IO	
						CLK_OUT	8	O	
						UC6_SCL	9	IOD	
						TIMG14_C3	10	IO	
						ADC0_7	(Non-IOMUX 1) 0	A	
24	43	43	19	27	PA23 PINCM53 0x404280d0	PA23	1	IO	LDIO
						UC11_TX	2	IO	
						TIMA0_C3	5	IO	
						TIMG14_C2	6	IO	
						TIMG2_C0	7	IO	
						TIMG14_C0	9	IO	
						ADC0_VREF+	(Non-IOMUX 1) 0	A	
25	44	44	20	28	PA24 PINCM54 0x404280d4	PA24	1	IO	LDIO
						UC11_RX	2	IO	
						TIMA0_C3N	5	O	
						TIMG14_C3	6	IO	
						TIMG2_C1	7	IO	
						TIMG14_C1	9	IO	
						ADC0_3	(Non-IOMUX 1) 0	A	
26	45	45	21	29	PA25 PINCM55 0x404280d8	PA25	1	IO	LDIO
						TIMA0_C3	5	IO	
						TIMA0_C1N	6	O	
						COMP0_OUT	7	O	
						TIMG1_C0	10	IO	
						ADC0_2	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RGE, RHB Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
30	46	46	22	30	PA26 PINCM59 0x404280e8	PA26	1	IO	LDIO
						UC8_CS0	3	IO	
						TIMG14_C2	4	IO	
						TIMA_FAL0	5	I	
						TIMA0_C3N	6	O	
						TIMG2_C0	7	IO	
						TIMG1_C1	10	IO	
						ADC0_1	(Non-IOMUX 1) 0	A	
						COMP0_IN0+	(Non-IOMUX 2) 0	A	
31	47	47		31	PA27 PINCM60 0x404280ec	PA27	1	IO	LDIO
						TIMG14_C3	4	IO	
						TIMA_FAL2	5	I	
						CLK_OUT	6	O	
						TIMG2_C1	7	IO	
						RTC_OUT	8	O	
						COMP0_OUT	9	O	
						ADC0_0	(Non-IOMUX 1) 0	A	
						COMP0_IN0-	(Non-IOMUX 2) 0	A	
35	3	3			PA28 PINCM3 0x40428008	PA28	1	IO	HDIO (high-drive)with wake
						UC4_PICO_TX	2	IO	
						UC6_SDA	3	IOD	
						TIMA0_C3	4	IO	
						TIMA_FAL0	5	I	
						TIMG2_C0	6	IO	
						TIMA0_C1	7	IO	
36					PA29 PINCM4 0x4042800c	PA29	1	IO	LDIO
						UC7_SCL	2	IOD	
						TIMG14_C2	4	IO	
						TIMG1_C0	5	IO	
						UC4_CS0_CTS	7	IO	
37					PA30 PINCM5 0x40428010	PA30	1	IO	LDIO
						UC7_SDA	2	IOD	
						TIMG14_C3	4	IO	
						TIMG1_C1	5	IO	
						UC4_POCI_RTS	7	IO	
39	5	5			PA31 PINCM6 0x40428014	PA31	1	IO	LDIO
						UC4_SCLK_RX	2	IOD	
						UC6_SCL	3	IOD	
						TIMA0_C3N	4	O	
						CLK_OUT	6	O	
						TIMG2_C1	7	IO	
47					PB0 PINCM12 0x4042802c	PB0	1	IO	SDIO (standard)
						UC4_PICO_TX	2	IO	
						UC6_SCL	4	IOD	
						TIMA0_C2	5	IO	
						TIMG14_C0	6	IO	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RGE, RHB Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
48					PB1 PINCM13 0x40428030	PB1	1	IO	SDIO (standard)
						UC4_SCLK_RX	2	IOD	
						UC6_SDA	4	IOD	
						TIMA0_C2N	5	O	
						TIMG14_C1	6	IO	
50	14	14			PB2 PINCM15 0x40428038	PB2	1	IO	LDIO
						UC7_SCL	4	IOD	
						TIMA0_C3	5	IO	
						TIMG1_C0	7	IO	
						UC11_TX	8	IO	
						HFCLKIN	10	I	
						UC4_PICO_TX	11	IO	
51	15	15			PB3 PINCM16 0x4042803c	PB3	1	IO	LDIO
						UC7_SDA	4	IOD	
						TIMA0_C3N	5	O	
						TIMG1_C1	7	IO	
						UC11_RX	8	IO	
						TIMA0_C0	10	IO	
						UC4_SCLK_RX	11	IOD	
52					PB4 PINCM17 0x40428040	PB4	1	IO	LDIO
						UC8_PICO_TX	2	IO	
						TIMA0_C1	4	IO	
						TIMA0_C2	5	IO	
						TIMG14_C0	6	IO	
						TIMG1_C0	7	IO	
53					PB5 PINCM18 0x40428044	PB5	1	IO	LDIO
						UC8_SCLK_RX	2	IOD	
						TIMA0_C1N	4	O	
						TIMA0_C2N	5	O	
						TIMG14_C1	6	IO	
						TIMG1_C1	7	IO	
58	20	20			PB6 PINCM23 0x40428058	PB6	1	IO	LDIO
						UC8_PICO_TX	2	IO	
						UC8_CS0	3	IO	
						TIMG14_C2	5	IO	
						TIMG1_C0	7	IO	
						TIMA_FAL2	8	I	
59	21	21			PB7 PINCM24 0x4042805c	PB7	1	IO	LDIO
						UC8_SCLK_RX	2	IOD	
						UC8_POCI	3	IO	
						TIMG14_C3	5	IO	
						TIMG1_C1	7	IO	
60	22	22			PB8 PINCM25 0x40428060	PB8	1	IO	LDIO
						UC8_PICO_TX	3	IO	
						TIMA0_C0	5	IO	
						COMP0_OUT	6	O	
						TIMG1_C0	7	IO	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RGE, RHB Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
61	23	23			PB9 PINCM26 0x40428064	PB9	1	IO	LDIO
						UC8_SCLK_RX	3	IOD	
						TIMA0_C0N	5	O	
						TIMA0_C1	6	IO	
						TIMG1_C1	7	IO	
62					PB10 PINCM27 0x40428068	PB10	1	IO	LDIO
						TIMG14_C0	2	IO	
						TIMG14_C2	3	IO	
						COMP0_OUT	4	O	
						TIMG1_C0	5	IO	
63					PB11 PINCM28 0x4042806c	PB11	1	IO	LDIO
						TIMG14_C1	2	IO	
						TIMG14_C3	3	IO	
						CLK_OUT	4	O	
						TIMG1_C1	5	IO	
64					PB12 PINCM29 0x40428070	PB12	1	IO	LDIO
						TIMA0_C2	3	IO	
						TIMA_FAL1	4	I	
						TIMA0_C1	5	IO	
1					PB13 PINCM30 0x40428074	PB13	1	IO	LDIO
						TIMA0_C3	3	IO	
						TIMA0_C1N	5	O	
						UC8_CS0	7	IO	
2	24	24		16	PB14 PINCM31 0x40428078	PB14	1	IO	LDIO
						UC8_SCLK_RX	2	IOD	
						UC8_POCI	3	IO	
						FCC_IN	4	I	
						TIMA0_C0	5	IO	
						TIMG14_C2	6	IO	
						TIMG14_C0	7	IO	
						COMP0_OUT	10	O	
						ADC0_21	(Non-IOMUX 1) 0	A	
3	25	25		17	PB15 PINCM32 0x4042807c	PB15	1	IO	LDIO
						UC11_TX	2	IO	
						UC8_PICO_TX	3	IO	
						UC4_POCI_RTS	4	IO	
						TIMG14_C2	5	IO	
						TIMG2_C0	6	IO	
						TIMA0_C3N	7	O	
						RTC_OUT	8	O	
						TIMG14_C1	9	IO	
						UC8_CS0	10	IO	
						ADC0_20	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RGE, RHB Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
4	26	26		18	PB16 PINCM33 0x40428080	PB16	1	IO	LDIO
						UC11_RX	2	IO	
						UC8_SCLK_RX	3	IOD	
						UC4_CS0_CTS	4	IO	
						TIMG14_C3	5	IO	
						TIMG2_C1	6	IO	
						UC4_PICO_TX	7	IO	
						CLK_OUT	8	O	
						ADC0_19	(Non-IOMUX 1) 0	A	
14	36	36			PB17 PINCM43 0x404280a8	PB17	1	IO	LDIO
						UC11_TX	2	IO	
						UC4_PICO_TX	3	IO	
						UC6_SCL	4	IOD	
						TIMA0_C2	5	IO	
						TIMG14_C0	6	IO	
						TIMG1_C0	9	IO	
						ADC0_11	(Non-IOMUX 1) 0	A	
15	37	37			PB18 PINCM44 0x404280ac	PB18	1	IO	LDIO
						UC11_RX	2	IO	
						UC4_SCLK_RX	3	IOD	
						UC6_SDA	4	IOD	
						TIMA0_C2N	5	O	
						TIMG14_C1	6	IO	
						TIMG1_C1	9	IO	
						ADC0_10	(Non-IOMUX 1) 0	A	
16	38	38			PB19 PINCM45 0x404280b0	PB19	1	IO	LDIO
						COMP0_OUT	2	O	
						UC4_POCI_RTS	3	IO	
						UC4_CS0_CTS	5	IO	
						TIMG2_C1	6	IO	
						TIMG14_C2	7	IO	
						ADC0_9	(Non-IOMUX 1) 0	A	
19	41	41			PB20 PINCM48 0x404280bc	PB20	1	IO	LDIO
						UC8_CS0	3	IO	
						TIMA0_C2	5	IO	
						TIMA_FAL1	6	I	
						TIMA0_C1	7	IO	
						UC6_SDA	9	IOD	
						ADC0_6	(Non-IOMUX 1) 0	A	
20					PB21 PINCM49 0x404280c0	PB21	1	IO	LDIO
						UC8_POCI	3	IO	
						UC6_SCL	4	IOD	
						TIMG14_C2	5	IO	
						UC8_PICO_TX	6	IO	
						ADC0_25	(Non-IOMUX 1) 0	A	

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Table 6-2. Pin Attributes (PM, PT, RGZ, RGE, RHB Packages) (continued)

PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN	PIN NAME/ IOMUX REG/ IOMUX ADDR	SIGNAL NAME	IOMUX PF	SIGNAL TYPE	BUFFER TYPE
21					PB22 PINCM50 0x404280c4	PB22	1	IO	LDIO
						UC8_PICO_TX	3	IO	
						UC6_SDA	4	IOD	
						TIMG14_C3	5	IO	
						UC8_SCLK_RX	6	IOD	
						ADC0_24	(Non-IOMUX 1) 0	A	
22					PB23 PINCM51 0x404280c8	PB23	1	IO	LDIO
						UC8_SCLK_RX	3	IOD	
						TIMA_FAL0	4	I	
						COMP0_OUT	5	O	
23	42	42			PB24 PINCM52 0x404280cc	PB24	1	IO	LDIO
						TIMA0_C3	5	IO	
						TIMA0_C1N	6	O	
						ADC0_5	(Non-IOMUX 1) 0	A	
27					PB25 PINCM56 0x404280dc	PB25	1	IO	LDIO
						UC4_CS0_CTS	2	IO	
						TIMA_FAL0	4	I	
						TIMA_FAL1	5	I	
						TIMA_FAL2	6	I	
						COMP0_OUT	7	O	
						FCC_IN	8	I	
						ADC0_4	(Non-IOMUX 1) 0	A	
28					PB26 PINCM57 0x404280e0	PB26	1	IO	LDIO
						UC4_POCI_RTS	2	IO	
						TIMA0_C0	4	IO	
						TIMA0_C3	5	IO	
						TIMG1_C0	6	IO	
						COMP0_OUT	7	O	
						FCC_IN	8	I	
						ADC0_23	(Non-IOMUX 1) 0	A	
29					PB27 PINCM58 0x404280e4	PB27	1	IO	LDIO
						COMP0_OUT	2	O	
						TIMA0_C0N	4	O	
						TIMA0_C3N	5	O	
						TIMG1_C1	6	IO	
						ADC0_22	(Non-IOMUX 1) 0	A	
32	48	48	23	32	VCORE	VCORE	(Non-IOMUX 1) 0	PWR	PWR
40	6	6	3	4	VDD	VDD	(Non-IOMUX 1) 0	PWR	PWR
41	7	7	4	5	VSS	VSS	(Non-IOMUX 1) 0	PWR	PWR

6.3 Signal Descriptions

Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
ADC0_VREF+	A	ADC0 voltage reference (VREF) power supply	24	43	43	19	27
ADC0_VREF-	A	ADC0 voltage reference (VREF) ground supply	17	39	39	17	25

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Table 6-3. Analog to Digital Converter (ADC) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
ADC0_0	A	ADC0 analog input channel 0	31	47	47		31
ADC0_1	A	ADC0 analog input channel 1	30	46	46	22	30
ADC0_2	A	ADC0 analog input channel 2	26	45	45	21	29
ADC0_3	A	ADC0 analog input channel 3	25	44	44	20	28
ADC0_4	A	ADC0 analog input channel 4	27				
ADC0_5	A	ADC0 analog input channel 5	23	42	42		
ADC0_6	A	ADC0 analog input channel 6	19	41	41		
ADC0_7	A	ADC0 analog input channel 7	18	40	40	18	26
ADC0_8	A	ADC0 analog input channel 8	17	39	39	17	25
ADC0_9	A	ADC0 analog input channel 9	16	38	38		
ADC0_10	A	ADC0 analog input channel 10	15	37	37		
ADC0_11	A	ADC0 analog input channel 11	14	36	36		
ADC0_12	A	ADC0 analog input channel 12	11	33	33	14	22
ADC0_13	A	ADC0 analog input channel 13	10	32	32	13	21
ADC0_14	A	ADC0 analog input channel 14	9	31	31	12	
ADC0_15	A	ADC0 analog input channel 15	8	30	30	11	
ADC0_16	A	ADC0 analog input channel 16	7	29	29		21
ADC0_17	A	ADC0 analog input channel 17	6	28	28		20
ADC0_18	A	ADC0 analog input channel 18	5	27	27		19
ADC0_19	A	ADC0 analog input channel 19	4	26	26		18
ADC0_20	A	ADC0 analog input channel 20	3	25	25		17
ADC0_21	A	ADC0 analog input channel 21	2	24	24		16
ADC0_22	A	ADC0 analog input channel 22	29				
ADC0_23	A	ADC0 analog input channel 23	28				
ADC0_24	A	ADC0 analog input channel 24	21				
ADC0_25	A	ADC0 analog input channel 25	20				

Table 6-4. Flash Bootstrap Loader (BSL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
BSLRX	I	BSL UART receive signal (RXD)	57	19	19	10	15
BSLSCL	IOD	BSL I2C clock signal (SCL)	34	2	2	1	2
BSLSDA	IOD	BSL I2C data signal (SDA)	33	1	1	24	1
BSLTX	O	BSL UART transmit signal (TXD)	56	18	18	9	14
BSL_INVOKE	I	BSL invoke signal (if BSL is enabled, must be HIGH during BOOTRST for a BSL entry, and LOW during BOOTRST to prevent BSL entry)	11	33	33	14	22

Table 6-5. Clock Module (CKM) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
CLK_OUT	O	CLK_OUT digital clock output from the PMCU	18, 31, 39, 4, 49, 55, 56, 63, 7	13, 17, 18, 26, 29, 40, 47, 5	13, 17, 18, 26, 29, 40, 47, 5	18, 8, 9	11, 13, 14, 18, 21, 26, 31

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Table 6-5. Clock Module (CKM) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
FCC_IN	I	Frequency clock counter (FCC) input signal	2, 27, 28, 33, 45, 49, 5, 9	1, 11, 13, 24, 27, 31	1, 11, 13, 24, 27, 31	12, 24	1, 11, 16, 19, 9
HFCLKIN	I	High frequency clock digital clock input signal	46, 50, 54	12, 14, 16	12, 14, 16		10, 12
HFXIN	A	High frequency crystal oscillator (HFXT) signal	45	11	11		9
HFXOUT	A	High frequency crystal oscillator (HFXT) signal	46	12	12		10
LFCLKIN	I	Low frequency clock digital clock input signal	44	10	10	7	8
LFXIN	A	Low frequency crystal oscillator (LFXT) signal	43	9	9	6	7
LFXOUT	A	Low frequency crystal oscillator (LFXT) signal	44	10	10	7	8

Table 6-6. Comparator (COMP) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
COMP0_DAC_OUT	A	COMP0 DAC output	57	19	19	10	15
COMP0_OUT	O	COMP0 output	16, 2, 22, 26, 27, 28, 29, 31, 43, 49, 5, 57, 6, 60, 62, 9	13, 19, 22, 24, 27, 28, 31, 38, 45, 47, 9	13, 19, 22, 24, 27, 28, 31, 38, 45, 47, 9	10, 12, 21, 6	11, 15, 16, 19, 20, 29, 31, 7
COMP0_IN0+	A	COMP0 non-inverting input 0	30	46	46	22	30
COMP0_IN0-	A	COMP0 inversting input 0	31	47	47		31
COMP0_IN1+	A	COMP0 non-inverting input 1	11	33	33	14	22
COMP0_IN1-	A	COMP0 inversting input 1	10	32	32	13	21
COMP0_IN2+	A	COMP0 non-inverting input 2	7	29	29		21
COMP0_IN2-	A	COMP0 inversting input 2	6	28	28		20
COMP0_IN3+	A	COMP0 non-inverting input 3	8	30	30	11	

Table 6-7. General Purpose Input Output Module Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
PA0	IO	GPIO port A input/output 0	33	1	1	24	1
PA1	IO	GPIO port A input/output 1	34	2	2	1	2
PA2	IO	GPIO port A input/output 2	42	8	8	5	6
PA3	IO	GPIO port A input/output 3	43	9	9	6	7
PA4	IO	GPIO port A input/output 4	44	10	10	7	8
PA5	IO	GPIO port A input/output 5	45	11	11		9
PA6	IO	GPIO port A input/output 6	46	12	12		10
PA7	IO	GPIO port A input/output 7	49	13	13		11
PA8	IO	GPIO port A input/output 8	54	16	16		12
PA9	IO	GPIO port A input/output 9	55	17	17	8	13
PA10	IO	GPIO port A input/output 10	56	18	18	9	14

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Table 6-7. General Purpose Input Output Module Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
PA11	IO	GPIO port A input/output 11	57	19	19	10	15
PA12	IO	GPIO port A input/output 12	5	27	27		19
PA13	IO	GPIO port A input/output 13	6	28	28		20
PA14	IO	GPIO port A input/output 14	7	29	29		21
PA15	IO	GPIO port A input/output 15	8	30	30	11	
PA16	IO	GPIO port A input/output 16	9	31	31	12	
PA17	IO	GPIO port A input/output 17	10	32	32	13	21
PA18	IO	GPIO port A input/output 18	11	33	33	14	22
PA19	IO	GPIO port A input/output 19	12	34	34	15	23
PA20	IO	GPIO port A input/output 20	13	35	35	16	24
PA21	IO	GPIO port A input/output 21	17	39	39	17	25
PA22	IO	GPIO port A input/output 22	18	40	40	18	26
PA23	IO	GPIO port A input/output 23	24	43	43	19	27
PA24	IO	GPIO port A input/output 24	25	44	44	20	28
PA25	IO	GPIO port A input/output 25	26	45	45	21	29
PA26	IO	GPIO port A input/output 26	30	46	46	22	30
PA27	IO	GPIO port A input/output 27	31	47	47		31
PA28	IO	GPIO port A input/output 28	35	3	3		
PA29	IO	GPIO port A input/output 29	36				
PA30	IO	GPIO port A input/output 30	37				
PA31	IO	GPIO port A input/output 31	39	5	5		
PB0	IO	GPIO port B input/output 0	47				
PB1	IO	GPIO port B input/output 1	48				
PB2	IO	GPIO port B input/output 2	50	14	14		
PB3	IO	GPIO port B input/output 3	51	15	15		
PB4	IO	GPIO port B input/output 4	52				
PB5	IO	GPIO port B input/output 5	53				
PB6	IO	GPIO port B input/output 6	58	20	20		
PB7	IO	GPIO port B input/output 7	59	21	21		
PB8	IO	GPIO port B input/output 8	60	22	22		
PB9	IO	GPIO port B input/output 9	61	23	23		
PB10	IO	GPIO port B input/output 10	62				
PB11	IO	GPIO port B input/output 11	63				
PB12	IO	GPIO port B input/output 12	64				
PB13	IO	GPIO port B input/output 13	1				
PB14	IO	GPIO port B input/output 14	2	24	24		16
PB15	IO	GPIO port B input/output 15	3	25	25		17
PB16	IO	GPIO port B input/output 16	4	26	26		18
PB17	IO	GPIO port B input/output 17	14	36	36		
PB18	IO	GPIO port B input/output 18	15	37	37		
PB19	IO	GPIO port B input/output 19	16	38	38		
PB20	IO	GPIO port B input/output 20	19	41	41		
PB21	IO	GPIO port B input/output 21	20				
PB22	IO	GPIO port B input/output 22	21				

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Table 6-7. General Purpose Input Output Module Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
PB23	IO	GPIO port B input/output 23	22				
PB24	IO	GPIO port B input/output 24	23	42	42		
PB25	IO	GPIO port B input/output 25	27				
PB26	IO	GPIO port B input/output 26	28				
PB27	IO	GPIO port B input/output 27	29				

Table 6-8. Real-time Clock (RTC) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
RTC_OUT	O	Real-time clock output signal	3, 31, 55, 6	17, 25, 28, 47	17, 25, 28, 47	8	13, 17, 20, 31

Table 6-9. Serial Wire Debug (SWD) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
SWCLK	I	Serial wire debug interface clock input signal	13	35	35	16	24
SWDIO	IO	Serial wire debug interface data input/ output signal	12	34	34	15	23

Table 6-10. System Controller (SYSCTL) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
BEEP	O	Beep output	33	1	1	24	1
NRST	RESET	Active-low reset signal (must be logic high for the device to start)	38	4	4	2	3
VCORE	PWR	VCORE capacitor connection	32	48	48	23	32
VDD	PWR	VDD supply	40	6	6	3	4
VSS	PWR	VSS (ground)	41	7	7	4	5

Table 6-11. Timer (TIMx) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
TIMA0_C0	IO	TIMA0 capture/compare 0 signal	17, 2, 28, 33, 42, 51, 54, 60	1, 15, 16, 22, 24, 39, 8	1, 15, 16, 22, 24, 39, 8	17, 24, 5	1, 12, 16, 25, 6
TIMA0_C1	IO	TIMA0 capture/compare 1 signal	18, 19, 34, 35, 43, 49, 52, 55, 61, 64	13, 17, 2, 23, 3, 40, 41, 9	13, 17, 2, 23, 3, 40, 41, 9	1, 18, 6, 8	11, 13, 2, 26, 7
TIMA0_C2	IO	TIMA0 capture/compare 2 signal	12, 14, 19, 43, 47, 49, 5, 52, 56, 64, 8	13, 18, 27, 30, 34, 36, 41, 9	13, 18, 27, 30, 34, 36, 41, 9	11, 15, 6, 9	11, 14, 19, 23, 7
TIMA0_C3	IO	TIMA0 capture/compare 3 signal	1, 10, 23, 24, 26, 28, 35, 44, 5, 50	10, 14, 27, 3, 32, 42, 43, 45	10, 14, 27, 3, 32, 42, 43, 45	13, 19, 21, 7	19, 21, 27, 29, 8

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Table 6-11. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
TIMA0_C0N	O	TIMA0 capture/compare 0 complementary output	18, 29, 55, 61	17, 23, 40	17, 23, 40	18, 8	13, 26
TIMA0_C1N	O	TIMA0 capture/compare 1 complementary output	1, 23, 26, 44, 53	10, 42, 45	10, 42, 45	21, 7	29, 8
TIMA0_C2N	O	TIMA0 capture/compare 2 complementary output	13, 15, 42, 46, 48, 53, 57, 6, 9	12, 19, 28, 31, 35, 37, 8	12, 19, 28, 31, 35, 37, 8	10, 12, 16, 5	10, 15, 20, 24, 6
TIMA0_C3N	O	TIMA0 capture/compare 3 complementary output	11, 25, 29, 3, 30, 39, 42, 51, 6	15, 25, 28, 33, 44, 46, 5, 8	15, 25, 28, 33, 44, 46, 5, 8	14, 20, 22, 5	17, 20, 22, 28, 30, 6
TIMA_FAL0	I	TIMA fault input 0	22, 27, 30, 35, 42, 46, 54, 57	12, 16, 19, 3, 46, 8	12, 16, 19, 3, 46, 8	10, 22, 5	10, 12, 15, 30, 6
TIMA_FAL1	I	TIMA fault input 1	19, 27, 33, 42, 45, 56, 64	1, 11, 18, 41, 8	1, 11, 18, 41, 8	24, 5, 9	1, 14, 6, 9
TIMA_FAL2	I	TIMA fault input 2	27, 31, 34, 54, 58	16, 2, 20, 47	16, 2, 20, 47	1	12, 2, 31
TIMG14_C0	IO	TIMG14 capture/compare 0 signal	12, 14, 2, 24, 33, 45, 47, 5, 52, 56, 62	1, 11, 18, 24, 27, 34, 36, 43	1, 11, 18, 24, 27, 34, 36, 43	15, 19, 24, 9	1, 14, 16, 19, 23, 27, 9
TIMG14_C1	IO	TIMG14 capture/compare 1 signal	13, 15, 25, 3, 34, 46, 48, 53, 57, 6, 63	12, 19, 2, 25, 28, 35, 37, 44	12, 19, 2, 25, 28, 35, 37, 44	1, 10, 16, 20	10, 15, 17, 2, 20, 24, 28
TIMG14_C2	IO	TIMG14 capture/compare 2 signal	10, 16, 17, 2, 20, 24, 3, 30, 34, 36, 43, 45, 49, 58, 62, 8	11, 13, 2, 20, 24, 25, 30, 32, 38, 39, 43, 46, 9	11, 13, 2, 20, 24, 25, 30, 32, 38, 39, 43, 46, 9	1, 11, 13, 17, 19, 22, 6	11, 16, 17, 2, 21, 25, 27, 30, 7, 9
TIMG14_C3	IO	TIMG14 capture/compare 3 signal	11, 18, 21, 25, 31, 34, 37, 4, 42, 44, 46, 49, 59, 63	10, 12, 13, 2, 21, 26, 33, 40, 44, 47, 8	10, 12, 13, 2, 21, 26, 33, 40, 44, 47, 8	1, 14, 18, 20, 5, 7	10, 11, 18, 2, 22, 26, 28, 31, 6, 8
TIMG1_C0	IO	TIMG1 capture/compare 0 signal	14, 17, 26, 28, 36, 45, 50, 52, 58, 60, 62	11, 14, 20, 22, 36, 39, 45	11, 14, 20, 22, 36, 39, 45	17, 21	25, 29, 9

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Table 6-11. Timer (TIMx) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
TIMG1_C1	IO	TIMG1 capture/compare 1 signal	15, 18, 29, 30, 37, 46, 51, 53, 59, 61, 63	12, 15, 21, 23, 37, 40, 46	12, 15, 21, 23, 37, 40, 46	18, 22	10, 26, 30
TIMG2_C0	IO	TIMG2 capture/compare 0 signal	10, 24, 3, 30, 35, 43, 55	17, 25, 3, 32, 43, 46, 9	17, 25, 3, 32, 43, 46, 9	13, 19, 22, 6, 8	13, 17, 21, 27, 30, 7
TIMG2_C1	IO	TIMG2 capture/compare 1 signal	11, 16, 25, 31, 39, 4, 42, 44, 49, 54	10, 13, 16, 26, 33, 38, 44, 47, 5, 8	10, 13, 16, 26, 33, 38, 44, 47, 5, 8	14, 20, 5, 7	11, 12, 18, 22, 28, 31, 6, 8

Table 6-12. Unified Communication Module (UniComm) Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
UC4_PICO_TX	IO	Unified Communication Module UC4: SPI PICO or UART TX signal	14, 33, 35, 4, 45, 47, 50, 55, 56, 7	1, 11, 14, 17, 18, 26, 29, 3, 36	1, 11, 14, 17, 18, 26, 29, 3, 36	24, 8, 9	1, 13, 14, 18, 21, 9
UC4_POCI_RTS	IO	Unified Communication Module UC4: SPI POCI or UART RTS signal	16, 28, 3, 37, 44, 46, 49, 5, 54, 56, 6, 8	10, 12, 13, 16, 18, 25, 27, 28, 30, 38	10, 12, 13, 16, 18, 25, 27, 28, 30, 38	11, 7, 9	10, 11, 12, 14, 17, 19, 20, 8
UC4_SCLK_RX	IOD	Unified Communication Module UC4: SPI SCLK or UART RX signal	15, 34, 39, 46, 48, 5, 51, 57	12, 15, 19, 2, 27, 37, 5	12, 15, 19, 2, 27, 37, 5	1, 10	10, 15, 19, 2
UC6_SCL	IOD	Unified Communication Module UC6: I2C SCL signal	14, 18, 20, 34, 39, 47, 55, 57	17, 19, 2, 36, 40, 5	17, 19, 2, 36, 40, 5	1, 10, 18, 8	13, 15, 2, 26
UC6_SDA	IOD	Unified Communication Module UC6: I2C SDA signal	15, 19, 21, 33, 35, 48, 54, 56	1, 16, 18, 3, 37, 41	1, 16, 18, 3, 37, 41	24, 9	1, 12, 14
UC7_SCL	IOD	Unified Communication Module UC7: I2C SCL signal	10, 13, 34, 36, 44, 46, 5, 50, 57, 8	10, 12, 14, 19, 2, 27, 30, 32, 35	10, 12, 14, 19, 2, 27, 30, 32, 35	1, 10, 11, 13, 16, 7	10, 15, 19, 2, 21, 24, 8
UC7_SDA	IOD	Unified Communication Module UC7: I2C SDA signal	11, 12, 33, 37, 43, 45, 51, 56, 6, 9	1, 11, 15, 18, 28, 31, 33, 34, 9	1, 11, 15, 18, 28, 31, 33, 34, 9	12, 14, 15, 24, 6, 9	1, 14, 20, 22, 23, 7, 9
UC8_PICO_TX	IO	Unified Communication Module UC8: SPI PICO or UART TX signal	10, 11, 20, 21, 3, 43, 45, 52, 54, 58, 60	11, 16, 20, 22, 25, 32, 33, 9	11, 16, 20, 22, 25, 32, 33, 9	13, 14, 6	12, 17, 21, 22, 7, 9

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Table 6-12. Unified Communication Module (UniComm) Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	PM PIN	PT PIN	RGZ PIN	RGE PIN	RHB PIN
UC8_POCI	IO	Unified Communication Module UC8: SPI POCI signal	12, 2, 20, 59, 6, 9	21, 24, 28, 31, 34	21, 24, 28, 31, 34	12, 15	16, 20, 23
UC8_SCLK_RX	IOD	Unified Communication Module UC8: SPI SCLK or UART RX signal	10, 11, 13, 2, 21, 22, 4, 44, 46, 53, 55, 59, 61	10, 12, 17, 21, 23, 24, 26, 32, 33, 35	10, 12, 17, 21, 23, 24, 26, 32, 33, 35	13, 14, 16, 7, 8	10, 13, 16, 18, 21, 22, 24, 8
UC11_RX	IO	Unified Communication Module UC11: UART RX signal	15, 18, 25, 4, 51, 7	15, 26, 29, 37, 40, 44	15, 26, 29, 37, 40, 44	18, 20	18, 21, 26, 28
UC11_TX	IO	Unified Communication Module UC11: UART TX signal	14, 17, 24, 3, 50, 6	14, 25, 28, 36, 39, 43	14, 25, 28, 36, 39, 43	17, 19	17, 20, 25, 27
UC4_CS0_CTS	IO	Unified Communication Module UC4: SPI CS0 or UART CTS signal	11, 16, 27, 36, 4, 42, 44, 45, 54, 55, 7	10, 11, 16, 17, 26, 29, 33, 38, 8	10, 11, 16, 17, 26, 29, 33, 38, 8	14, 5, 7, 8	12, 13, 18, 21, 22, 6, 8, 9
UC8_CS0	IO	Unified Communication Module UC8: SPI CS0 signal	1, 19, 3, 30, 42, 58, 6	20, 25, 28, 41, 46, 8	20, 25, 28, 41, 46, 8	22, 5	17, 20, 30, 6

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin, with respect to VSS	–0.3	4.1	V
V_I	Input voltage	Applied to any 5-V tolerant open-drain pins	–0.3	V_{DD} + 3.6 (5.5 MAX)	V
V_I	Input voltage	Applied to any common tolerance pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD}	Current into VDD pin (source)	-40°C ≤ Tj ≤ 130°C		80	mA
		-40°C ≤ Tj ≤ 85°C		100	
I_{VSS}	Current out of VSS pin (sink)	-40°C ≤ Tj ≤ 130°C		80	mA
		-40°C ≤ Tj ≤ 85°C		100	
I_{IO}	Current for LDIO pin	Current sunk or sourced by LDIO pin		3	mA
	Current for SDIO pin	Current sunk or sourced by SDIO pin		6	
	Current for HDIO pin	Current sunk or sourced by HDIO pin		20	
	Current for ODIO pin	Current sunk by ODIO pin		20	
I_D	Supported diode current	Diode current on LDIO and HDIO pins	–2	2	mA
		Diode current on SDIO pins	–2	0.05	
Tj	Junction temperature		–40	130	°C
T_{stg}	Storage temperature(2)		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Higher temperatures may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC-Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC-Q100-011 , All pins	±500	V
		Charged device model (CDM), per AEC-Q100-011 , Corner pins	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.62		3.6	V
VCORE	Voltage on VCORE pin (2)		1.35		V
C_{VDD}	Capacitor placed between VDD and VSS (1)		10		uF
C_{VCORE}	Capacitor placed between VCORE and VSS (1) (2)		470		nF
T_A	Ambient temperature	–40		125	°C
T_J	Max junction temperature			130	°C
f_{MCLK}	MCLK, CPUCLK, ULPCLK frequency with 1 flash wait state (3)			32	MHz

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over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
f_{MCLK}	MCLK, CPUCLK, ULPCLK frequency with 0 flash wait states (3)			24	MHz

(1) Connect C_{VDD} and C_{VCORE} between VDD/VSS and VCORE/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD}.
(2) The VCORE pin must only be connected to CVCORE. Do not supply any voltage or apply any external load to the VCORE pin.
(3) Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software.

7.4 Thermal Information

THERMAL METRIC(1)		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-64 (PM)	56.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		24.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		37.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		2.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		37.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LQFP-48 (PT)	63.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		29.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		41.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		3.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		40.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-48 (RGZ)	31.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		14.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		14.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		6.6	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-32 (RHB)	35.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		27.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		16.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		16.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		6.6	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VQFN-24 (RGE)	44.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		37.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		30.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		30.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		6.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		MCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode													
IDD_{RUN}	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	3.1		3.1		3.1		3.2		3.2		mA
IDD_{RUN}, per MHz	MCLK=SYSOSC, While(1), execute from flash	32MHz	52	59	52	59	53	59	53	59	54	60	uA/Mhz
	MCLK=SYSOSC, CoreMark, execute from flash	32MHz	97		98		98		98		99		
SLEEP Mode													
IDD_{SLEEP}	MCLK=SYSOSC, CPU is halted	32MHz	1265	1426	1284	1429	1310	1481	1317	1488	1329	1472	uA
IDD_{SLEEP}	MCLK=LFCLK, CPU is halted	32kHz	262	303	266	304	299	358	307	366	322	381	uA

7.5.2 STOP/STANDBY Modes

VDD=3.3V unless otherwise noted. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode													
IDD_{STOP0}	SYSOSC=32MHz, USE4MHZSTOP=0, DISABLESTOP=0	4MHz	397	447	403	451	411	455	414	458	418	463	uA
IDD_{STOP2}	SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK	32kHz	45	56	47	59	50	82	53	85	62	90	
STANDBY Mode													
IDD_{STBY0}	LFXT and RTC enabled	32kHz	2.14	3.5	2.14	3.5	3.7	24.3	6.3	27.0	15.0	33.1	uA
	LFOSC and IWDT enabled		1.9	2.3	2.0	2.4	3.6	25.6	6.3	28.5	15.0	34.4	uA
	LFXT and RTC enabled, IWDT enabled		2.5	3.5	2.5	3.5	4.0	24.9	6.7	27.6	15.1	33.1	uA
	STOPCLKSTBY=0, TIMG14 enabled		1.9	2.3	2.0	2.4	3.6	25.6	6.3	28.5	15.0	34.4	uA
IDD_{STBY1}	STOPCLKSTBY=1, TIMG14 enabled		1.5	1.8	1.6	1.9	3.2	24.8	5.9	27.7	14.6	34.0	
	STOPCLKSTBY=1, GPIOA enabled		1.5	1.9	1.6	1.9	3.2	24.8	5.9	27.7	14.7	34.0	

7.5.3 SHUTDOWN Mode

All inputs tied to 0V or VDD. Outputs do not source or sink any current. Core regulator is powered down.

PARAMETER		VDD	-40°C		25°C		85°C		105°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDD_{SHDN}	Supply current in SHUTDOWN mode	3.3V	46		81		669		1414		3606		nA

7.6 Power Supply Sequencing

7.6.1 Power Supply Ramp

Figure 7-1 gives the relationship of POR- POR+, BOR0-, and BOR0+ during power-up and power-down.

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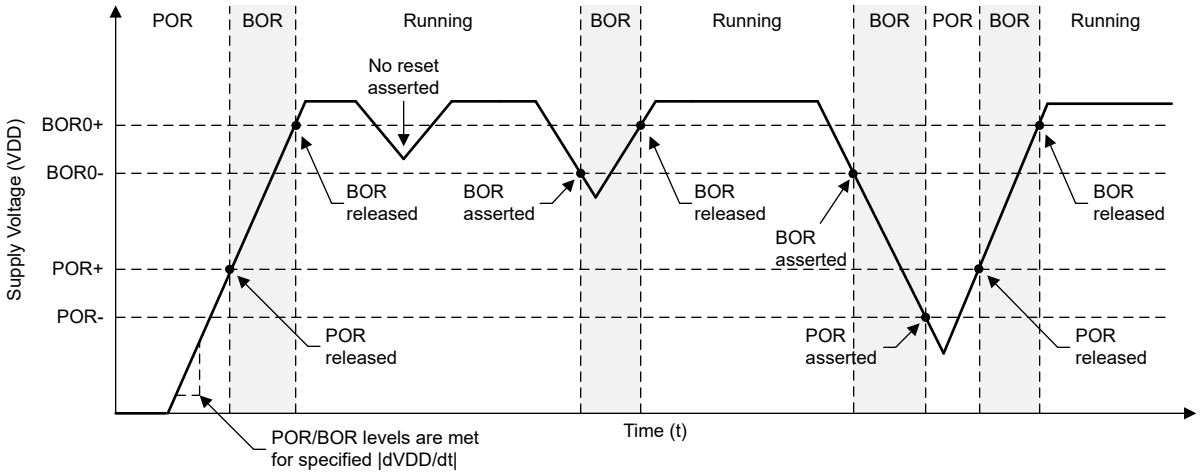


Figure 7-1. Power Cycle POR/BOR Conditions - VDD

7.6.2 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
		Falling (1)			0.01	
dVDD/dt		Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising	0.95	1.30	1.60	V
V_{POR-}		Falling	0.9	1.25	1.55	V
$V_{HYS, POR}$	POR hysteresis		30	58	74	mV
$V_{BOR0+, COLD}$	Brown-out reset voltage level 0 (default level)	-40°C ≤ T_j ≤ 125°C Cold start, rising	1.40	1.48	1.61	V
V_{BOR1+}	Brown-out-reset voltage level 1	Rising (1)	2.13	2.17	2.21	V
V_{BOR1-}		Falling (1)	2.10	2.14	2.18	
$V_{BOR1, STBY}$	Brown-out-reset voltage level 1	STANDBY mode	2.06	2.13	2.20	V
V_{BOR2+}	Brown-out-reset voltage level 2	Rising (1)	2.73	2.77	2.82	V
V_{BOR2-}		Falling (1)	2.7	2.74	2.79	
$V_{BOR2, STBY}$	Brown-out-reset voltage level 2	STANDBY mode	2.62	2.71	2.80	V
V_{BOR3+}	Brown-out-reset voltage level 3	Rising (1)	2.88	2.96	3.04	V
V_{BOR3-}		Falling (1)	2.85	2.93	3.01	
$V_{BOR3, STBY}$	Brown-out-reset voltage level 3	STANDBY mode	2.82	2.92	3.02	V
$V_{HYS,BOR}$	Brown-out reset hysteresis	Level 0		15	21	mV
		Levels 1-3		34	40	
$T_{PD, BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			10	us
		STANDBY mode			100	us

(1) Device operating in RUN, SLEEP, or STOP mode.

7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
$VDD_{PGM/ERASE}$	Program and erase supply voltage		1.62		3.6	V

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta			10	mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta			10	mA
Endurance						
$NWEC_{(HI_ENDURANCE)}$	Erase/program cycle endurance for chosen 32 sectors of flash (1)		100			k cycles
$NWEC_{(NORMAL_ENDURANCE)}$	Erase/program cycle endurance (Flash not used for HI_ENDURANCE) (1)		10			k cycles
$NE_{(MAX)}$	Total erase operations before failure (2)		802			k erase operations
$NW_{(MAX)}$	Write operations per word line before sector erase(3)				83	write operations
Retention						
t_{RET_85}	Flash memory data retention	-40°C ≤T_j ≤ 85°C	60			years
t_{RET_105}	Flash memory data retention	-40°C ≤T_j ≤ 105°C	11.4			years
Program and Erase Timing						
$t_{PROG\ (WORD,\ 64)}$	Program time for flash word (4) (6)			50	275	µs
$t_{PROG\ (SEC,\ 64)}$	Program time for 1kB sector (5) (6)			6.4		ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤2k erase/program cycles, T_j≥25°C		4	20	ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤10k erase/program cycles, T_j≥25°C		20	150	ms
$t_{ERASE\ (SEC)}$	Sector erase time	≤10k erase/program cycles		20	200	ms
$t_{ERASE\ (BANK)}$	Bank erase time	≤10k erase/program cycles		22	220	ms

(1) Up to 32 application-chosen sectors from the main flash bank(s) or data bank can be used as high endurance sectors. This enables applications that frequently update flash data such as EEPROM emulation.
(2) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
(3) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.
(4) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
(5) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
(6) Flash word size is 64 data bits (8 bytes). On devices with ECC, the total flash word size is 72 bits (64 data bits plus 8 ECC bits).

7.8 Timing Characteristics

VDD=3.3V, T_a=25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE,\ SLEEP}$	Wakeup time from SLEEP0 to RUN (1)			2		cycles
	Wakeup time from SLEEP1 to RUN (1)			1.6		us
	Wakeup time from SLEEP2 to RUN (1)			2.2		us
$t_{WAKE,\ STOP}$	Wakeup time from STOP0 to RUN (SYSOSC enabled) (1)			7.2		us
	Wakeup time from STOP2 to RUN (SYSOSC disabled) (1)			8.1		us

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VDD=3.3V, T_a=25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{WAKE, STBY}$	Wakeup time from STANDBY0 to RUN (1)			10		us
	Wakeup time from STANDBY1 to RUN (1)			10		
	Wakeup time from SHUTDOWN to RUN (2)	Fast boot enabled		283		us
		Fast boot disabled		310		us
Asynchronous Fast Clock Request Timing						
t_{DELAY}	Delay time from edge of asynchronous request to first 32MHz MCLK edge	Mode is SLEEP1		0.3		
		Mode is SLEEP2		0.9		us
		Mode is STOP0		0.9		us
		Mode is STOP2		0.9		us
		Mode is STANDBY1		3.1		us
		Mode is STANDBY0		3.1		us
Startup Timing						
$t_{START, RESET}$	Device cold start-up time from reset/ power-up (3)	Fast boot enabled		284		us
		Fast boot disabled		325		us
NRST Timing						
$t_{RST, BOOTRST}$	Minimum pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz		2		us
		ULPCLK=32kHz		100		us
$t_{RST, POR}$	Minimum pulse length on NRST pin to generate POR			1		s

(1) The wake-up time is measured from the edge of an external signal (GPIO wake-up event) to the time that the first CPU instruction is executed, with the GPIO glitch filter disabled (FILTEREN=0x0) and fast wake enabled (FASTWAKEONLY=1)
(2) The wake-up time is measured from the edge of an external wake-up signal (IOMUX wake-up event) to the time that first instruction of the user program is executed.
(3) The start-up time is measured from the time that VDD crosses VBOR0+ (cold start-up) to the time that the first instruction of the user program is executed.

7.9 Clock Specifications

7.9.1 System Oscillator (SYSOSC)

Over operating free-air temperature range (unless otherwise noted). Test conditions indicate lifetime operation under the listed conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		32		MHz
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled (2) (3)	SETUSEFCL=1, T_a = 25 ℃	0		1	%
f_{SYSOSC}		SETUSEFCL=1, -40 ℃ ≤ T_a ≤ 125 ℃	-2.1		1.6	
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, 32MHz	SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 ℃ ≤ T_a ≤ 125 ℃	-2.6		1.8	%
$t_{settle, SYSOSC}$	Settling time to target accuracy (1)	SETUSEFCL=1			30	us

(1) When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency f_{SYSOSC} by an additional error for the time $t_{settle,SYSOSC}$, after which the target accuracy is achieved.
(2) SYSOSC Accuracy is measured in the default power-up state, with MCLK = SYSOSC, and the CPU running a while(1) loop.
(3) SYSOSC is measured with the internal FCC counter using an external 1ms pulse as the measurement trigger.

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7.9.2 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
	LFOSC accuracy	-40 ℃ ≤ T_a ≤ 125 ℃	–5		5	%
		-40 ℃ ≤ T_a ≤ 85 ℃	–3		3	%
I_{LFOSC}	LFOSC current consumption			300		nA
$t_{start, LFOSC}$	LFOSC start-up time			1		ms

7.9.3 Low Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency crystal oscillator (LFXT)						
f_{LFXT}	LFXT frequency			32768		Hz
DC_{LFXT}	LFXT duty cycle		30		70	%
OA_{LFXT}	LFXT crystal oscillation allowance			419		kΩ
$C_{L, eff}$	Integrated effective load capacitance(1)			1		pF
$t_{start, LFXT}$	LFXT start-up time(2)			200		ms
I_{LFXT}	LFXT current consumption	XT1DRIVE=0, LOWCAP=1		200		nA
Low frequency digital clock input (LFCLK_IN)						
f_{LFIN}	LFCLK_IN frequency (3)	SETUSEEXLF=1	29491	32768	36045	Hz
DC_{LFIN}	LFCLK_IN duty cycle (3)	SETUSEEXLF=1	40		60	%
LFCLK Monitor						
$f_{FAULTLF}$	LFCLK monitor fault frequency (4)	MONITOR=1	2800	4200	8400	Hz

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{LFXIN} \times C_{LFXOUT}/(C_{LFXIN}+C_{LFXOUT})$, where C_{LFXIN} and C_{LFXOUT} are the total capacitance at LFXIN and LFXOUT, respectively.
(2) The user must ensure that the crystal is properly rated to support the start-up drive load (e.g. 0.1uW)
(3) The digital clock input (LFCLK_IN) accepts a logic level square wave clock.
(4) The LFCLK monitor may be used to monitor the LFXT or LFCLK_IN. It will always fault below the MIN fault frequency, and will never fault above the MAX fault frequency.

7.9.4 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High frequency crystal oscillator (HFXT)						
f_{HFXT}	HFXT frequency	HFXTRSEL=00	4		8	MHz
f_{HFXT}	HFXT frequency	HFXTRSEL=01	8.01		16	MHz
f_{HFXT}	HFXT frequency	HFXTRSEL=10	16.01		32	MHz
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=00	40		65	%
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=01	40		60	%
DC_{HFXT}	HFXT duty cycle	HFXTRSEL=10	40		60	%
OA_{HFXT}	HFXT crystal oscillation allowance	HFXTRSEL=00 (4 to 8MHz range)		2		kΩ
$C_{L, eff}$	Integrated effective load capacitance (1)			1		pF

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{start, HFXT}$	HFXT start-up time[2]	HFXTRSEL=10, 32MHz crystal		0.5		ms
I_{HFXT}	HFXT current consumption[2]	f_{HFXT}=4MHz, R_m=300Ω, C_L=12pF		100		uA
I_{HFXT}	HFXT current consumption[2]	f_{HFXT}=32MHz, R_m=30Ω, C_L=12pF, C_m=6.26fF, L_m=1.76mH		600		uA
High frequency digital clock input (HFCLK_IN)						
f_{HFIN}	HFCLK_IN frequency [3]	USEEXTHFCLK=1	4		32	MHz
DC_{HFIN}	HFCLK_IN duty cycle [3]	USEEXTHFCLK=1	40		60	%

(1) This includes parasitic bond and package capacitance (≈2pF per pin), calculated as $C_{HFXIN} \times C_{HFXOUT}/(C_{HFXIN}+C_{HFXOUT})$, where C_{HFXIN} and C_{HFXOUT} are the total capacitance at HFXIN and HFXOUT, respectively.
(2) The HFXT startup time ($t_{start, HFXT}$) is measured from the time the HFXT is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Refer to the HFXT section of the MSPM0 H-Series 32-MHz Microcontrollers Technical Reference Manual.Current consumption increases with higher RSEL and start up time is decreases with higher RSEL.
(3) The digital clock input (HFCLK_IN) accepts a logic level square wave clock.

7.10 *Digital IO*

7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	ODIO [1]	VDD≥1.62V	0.7*VDD		5.5	V
			VDD≥2.7V	2		5.5	
		All I/O except ODIO & Reset	VDD≥1.62V	0.7*VDD		VDD+0.3	
V_{IL}	Low level input voltage	ODIO	VDD≥1.62V	-0.3		0.3*VDD	V
			VDD≥2.7V	-0.3		0.8	
		All I/O except ODIO & Reset	VDD≥1.62V	-0.3		0.3*VDD	
V_{HYS}	Hysteresis	ODIO		0.05*VDD			V
		All I/O except ODIO		0.1*VDD			
I_{lkg}	High-Z leakage current	LDIO (except PA12)[2][3]				±100[4]	nA
I_{lkg}	High-Z leakage current	LDIO (PA12 only)				±300[4]	nA
I_{lkg}	High-Z leakage current	SDIO[2][3]	V_pad ≤ VDD			±130[4]	nA
R_{PU}	Pull up resistance	All I/O except ODIO			40		kΩ
R_{PD}	Pull down resistance				40		kΩ

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over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	LDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=3mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=1mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=0.75mA	VDD-0.4			V
		SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA	VDD-0.4			V
		HDIO	VDD ≥ 2.7V, DRV= 1, $\|I_{IO}\|_{,max}$ = 20mA VDD ≥ 2.7V, DRV= 0, $\|I_{IO}\|_{,max}$ = 6mA VDD ≥ 1.71V, DRV= 1, $\|I_{IO}\|_{,max}$ = 10mA VDD ≥ 1.71V, DRV= 0, $\|I_{IO}\|_{,max}$ = 2mA	VDD-0.4			V
V_{OL}	Low level output voltage	ODIO	VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA			0.4	V
		SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=1.5mA			0.4	
		HDIO	VDD ≥ 2.7V, DRV= 1, $\|I_{IO}\|_{,max}$ = 20mA VDD ≥ 2.7V, DRV= 0, $\|I_{IO}\|_{,max}$ = 6mA VDD ≥ 1.71V, DRV= 1, $\|I_{IO}\|_{,max}$ = 10mA VDD ≥ 1.71V, DRV= 0, $\|I_{IO}\|_{,max}$ = 2mA			0.4	
		LDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=3mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=1mA VDD≥1.62V, $\|I_{IO}\|_{,max}$=0.75mA			0.4	

(1) I/O Types: ODIO = 5V Tolerant Open-Drain, LDIO = Low-Drive, SDIO = Standard-Drive, HDIO = High-Drive
(2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(4) This value is for the IO not muxed with any analog inputs. If it is muxed with analog inputs then the leakage can be as high as 100nA.

7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency	ODIO	VDD ≥ 1.71V, FM+, CL= 20pF - 100pF			1	MHz
		LDIO(1)	VDD ≥ 1.71V, C_L= 20pF			8	
			VDD ≥ 2.7V, CL= 20pF			16	
		SDIO (1)	VDD ≥ 1.71V, C_L= 20pF			16	
			VDD ≥ 2.7V, CL= 20pF			32	
		HDIO(1)	VDD ≥ 2.7V, DRV=1, CL= 20pF			20	
			VDD ≥ 2.7V, DRV=0, CL= 20pF			20	
			VDD ≥ 1.7V, DRV=1, CL= 20pF			16	
			VDD ≥ 1.7V, DRV=0, CL= 20pF			16	
t_r,t_f	Output rise/fall time	All output ports except ODIO	VDD ≥ 1.71V			$0.3/f_{max}$	ns
t_f	Output fall time	ODIO	VDD ≥ 1.71V, FM+, CL= 20pF-100pF	20*VDD/5.5		120	ns

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , LDIO = Low-Drive, SDIO = Standard-Drive, HDIO = High-Drive

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7.11 Analog Mux VBOOST

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBST}	VBOOST current adder	MCLK/ULPCLK is LFCLK		0.8		uA
		MCLK/ULPCLK is not LFCLK, SYSOSC frequency is 32MHz		30		
$t_{START,VBST}$	VBOOST startup time			12		us

7.12 *ADC*

7.12.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Vin_{(ADC)}$	Analog input voltage range(1)	Applies to all ADC analog input pins	0		VDD	V
V_{R+}	Positive ADC reference voltage	V_{R+} sourced from VDD		VDD		V
		V_{R+} sourced from external reference pin (VREF+)	1.4		VDD	V
		V_{R+} sourced from internal reference (VREF)		VREF		V
V_{R-}	Negative ADC reference voltage			0		V
F_S	ADC sampling frequency	RES = 0x0 (12-bit mode), External Reference			1.6	Msps
F_S	ADC sampling frequency	RES = 0x1 (10-bit mode), External Reference			1.7	Msps
F_S	ADC sampling frequency	RES = 0x2 (8-bit mode), External Reference			1.9	Msps
$I_{(ADC)}$	Operating supply current into VDD terminal	F_S = 1MSPS, Internal reference OFF, V_{R+} = VDD		350		μA
		F_S = 500ksps, Internal reference ON, V_{R+} = VREF = 2.5V		300		
$C_{S/H}$	ADC sample-and-hold capacitance			0.22		pF
Rin	ADC sampling switch resistance			15		kΩ
ENOB	Effective number of bits	Internal reference, V_{R+} = VREF = 2.5V, F_{in} = 10KHz	9.4	10		bit
		External reference, F_{in} = 10KHz (2)	10	10.6		
ENOB	Effective number of bits	External reference, hardware averaging enabled (16 samples), F_{in} = 10KHz (2)		11.8		bit
SNR	Signal-to-noise ratio	External reference (2)		67		dB
		Internal reference, V_{R+} = VREF = 2.5V		65		
SNR	Signal-to-noise ratio	External reference (2), hardware averaging enabled (16 samples)		75		dB
$PSRR_{DC}$	Power supply rejection ratio, DC	External reference (2), VDD = $VDD_{(min)}$ to $VDD_{(max)}$		68		dB
		VDD = $VDD_{(min)}$ to $VDD_{(max)}$ Internal reference, V_{R+} = VREF = 2.5V		61		
$PSRR_{AC}$	Power supply rejection ratio, AC	External reference (2), ΔVDD = 0.1 V at 1 kHz		61		dB
		ΔVDD = 0.1 V at 1 kHz Internal reference, V_{R+} = VREF = 2.5V		49		
T_{wakeup}	ADC Wakeup Time	Assumes internal reference is active			5	us
$V_{SupplyMon}$	Supply Monitor voltage divider (VDD/3) accuracy	ADC input channel: Supply Monitor(3)	-1.5		+1.5	%
$I_{SupplyMon}$	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		10		uA

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) All external reference specifications are measured with V_{R+} = VREF+ = VDD = 3.3V and V_{R-} = VREF- = VSS = 0V and external 1uF cap on VREF+ pin
(3) Analog power supply monitor. Analog input on channel 31 is disconnected and is internally connected to the voltage divider which is VDD/3.

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7.12.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{ADCCLK}	ADC clock frequency			4		32	MHz
$t_{ADC\ trigger}$	Software trigger minimum width			3			ADCCLK cycles
t_{Sample_step}	Sampling time for step input	12-bit mode, R_S = 50Ω, C_{pext} = 10pF		0.188			µs
t_{Sample_VREF}	Sample time with internal VREF input		ADC CHANNEL=29,12-bit mode, VDD as reference	10			
$t_{Sample_SupplyMon}$	Sample time with Supply Monitor (VDD/3)	12-bit mode		5			µs

7.12.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (INL)	External reference (2)	-2.0		+2.0	LSB
E_D	Differential linearity error (DNL) Guaranteed no missing codes	External reference (2)	-1.0		+1.0	LSB
		External reference (2), HW Averaging Enabled, 16 Samples, effective 14b resolution		1		
E_O	Offset error	External reference (2)	-5		5	mV
E_G	Gain error	External reference (2)	-6		6	LSB

(1) Total Unadjusted Error (TUE) can be calculated from E_I , E_O , and E_G using the following formula: TUE = $\sqrt{(\ E_I^2 + |E_O|^2 + E_G^2\ )}$
Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate

(2) All external reference specifications are measured with VR+ = VREF+ = VDD = 3.3V and VR- = VREF- = VSS = 0V and external 1uF cap on VREF+ pin

7.12.4 Typical Connection Diagram

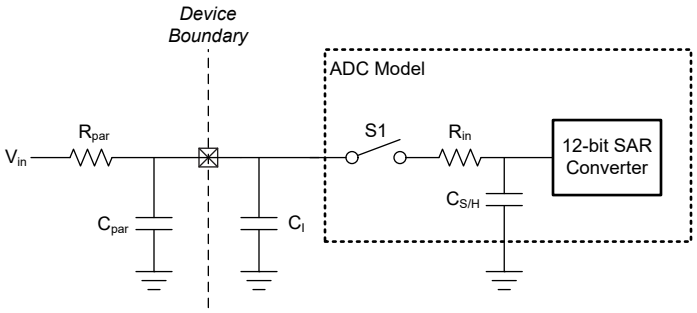


Figure 7-2. ADC Input Network

1. Refer to Section 7.12.1 for the values of R_{in} and $C_{S/H}$
2. Refer to Digital IO Electrical Characteristics for the value of C_I
3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. Tau = $(R_{par} + R_{in})^* C_{S/H} + R_{par}^*(C_{par} + C_I)$
2. K= $\ln(2^n/\text{Settling error}) - \ln((C_{par} + C_I)/C_{S/H})$
3. T (Min sampling time) = K*Tau

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7.13 Temperature Sensor

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{TRIM}	Factory trim temperature (2)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=2h (internal VREF), BUFCONFIG=1h (1.4V VREF), ADC t_{Sample}=10µs	27	30	33	℃
TS_c	Temperature coefficient	-40℃ ≤ T_j ≤ 130℃	-2.05	-1.9	-1.75	mV/℃
$t_{SET, TS}$	Temperature sensor settling time (3)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=2h (internal VREF), BUFCONFIG=1h (1.4V VREF), ADC CHANNEL=28		2.5	10	us

(1) Effective absolute temperature accuracy may be computed by combining the relative temperature accuracy together with the trim accuracy, and accounting for any analog to digital conversion error.
(2) Higher absolute accuracy may be achieved through user calibration.
(3) This is the maximum time required for the temperature sensor to settle when measured by the ADC. It may be used to specify the minimum ADC sample time when measuring the temperature sensor.

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7.14 VREF

7.14.1 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 1	1.62			V
		BUFCONFIG = 0	2.7			
VREF	Voltage reference output voltage	BUFCONFIG = 1	1.38	1.4	1.42	V
		BUFCONFIG = 0	2.46	2.5	2.54	

7.14.2 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current	BUFCONFIG = {0, 1}, No load		80	100	µA
TC_{VREF}	Temperature coefficient of VREF (1)	BUFCONFIG = {0, 1}			80	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C			300	ppm
$PSRR_{DC}$	VREF Power supply rejection ratio, DC	VDD = 1.7 V to VDDmax, BUFCONFIG = 1	60	70		dB
		VDD = 2.7 V to VDDmax, BUFCONFIG = 0	49	60		
ADC F_S	Max supported ADC sampling frequency	Using VREF as ADC reference			515	ksps
$T_{startup}$	VREF startup time	BUFCONFIG = {0, 1} , VDD = 2.8 V			30	us

(1) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.

7.15 *Comparator (COMP)*

7.15.1 Comparator Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator Electrical Characteristics						
Vcm	Common mode input range		0		VDD	V
V_{offset}	Input offset voltage		-20		20	mV
V_{hys}	DC input hysteresis	HYST=00h		0.4		mV
		HYST=01h		10		
		HYST=02h		20		
		HYST=03h		30		
t_{PD_ls}	Propagation delay, response time	Output Filter off, Overdrive = 100 mV, High Speed Mode		32	50	ns
		Output Filter off, Overdrive = 100 mV, Low Power Mode		1.2	4	µs
t_{en}	Comparator enable time	Startup time to reach propagation delay specification, High Speed Mode			5	µs
		Startup time to reach propagation delay specification, Low Power Mode			10	µs
I_{comp}	Comparator current consumption.	Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, High Speed Mode		130	200	µA
		Vcm = VDD/2, 100mV overdrive, DAC output as a voltage reference, VDD is reference for DAC, Low Power Mode		0.85	2.7	µA
		Vcm = VDD/2, 100mV overdrive, comparator only. High Speed Mode		120	180	µA
		Vcm = VDD/2, 100mV overdrive, comparator only, Low Power Mode		0.7	2.1	µA

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over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
8-bit DAC Electrical Characteristics						
V_{dac}	DAC output range		0		VDD	V
$V_{dac-code}$	8-bit DAC output voltage for a given code	VIN = reference voltage into 8-bit DAC, code n = 0 to 255		VIN × (n+1) / 256		V
INL	Integral nonlinearity of 8-bit DAC		-1		1	LSB
DNL	Differential nonlinearity of 8-bit DAC		-1		1	LSB
Gain error	Gain error of 8-bit DAC	Reference voltage = VDD	-2		2	% of FSR
Offset error	Offset error of 8-bit DAC		-5		5	mV
Output Impedance	8-bit DAC output impedance			50		kΩ
t_{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB, DAC output on pin PA11, Cload = 15pF		6		µs
t_{dac_settle}	8-bit DAC settling time in static mode	DACCODE0 = 0 → 255, DAC output accurate to 1 LSB		1.5		µs

7.16 *I2C*

7.16.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain0	2	32	8	32	20	32	MHz
f_{SCL}	SCL clock frequency			0.1		0.4		1	MHz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	Low period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	Bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	Data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	Data valid acknowledge time			3.45		0.9		0.45	us

7.16.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

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7.16.3 I²C Timing Diagram

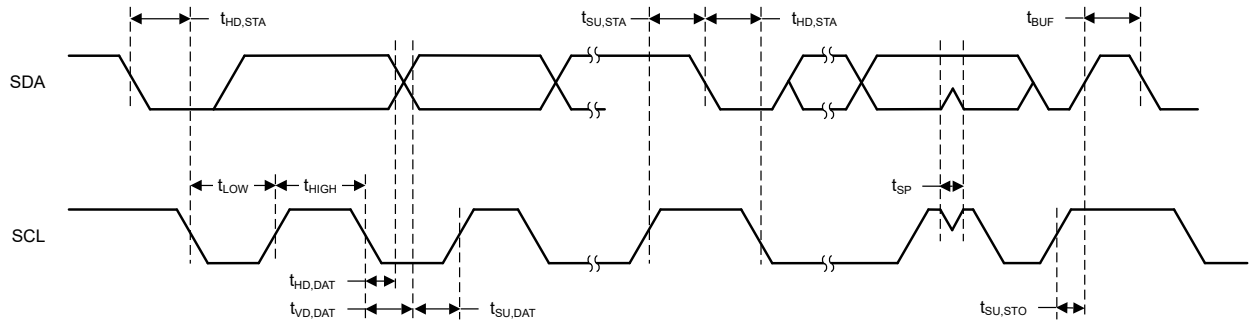


Figure 7-3. I2C Timing Diagram

7.17 SPI

7.17.1 SPI

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
f_{SPI}	SPI clock frequency	Clock max speed = 32MHz 1.62 < VDD < 3.6V Peripheral or Controller mode			16(4)	MHz
DC_{SCK}	SCK Duty Cycle		40	50	60	%
Controller						
$t_{SCLK_H/L}$	SCLK High or Low time		(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock	SPH=0	1 SPI Clock			ns
	CS lead-time, CS active to clock	SPH=1	1/2 SPI Clock			
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive	SPH=0	1/2 SPI Clock			ns
	CS lag time, Last clock to CS inactive	SPH=1	1 SPI Clock			
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1/2 SPI Clock	ns
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high inpedance				1 SPI Clock	ns
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, delayed sampling enabled	1			ns
		1.62 < VDD < 2.7V, delayed sampling enabled	8			
	POCI input data setup time (1)	2.7 < VDD < 3.6V, no delayed sampling	30			
		1.62 < VDD < 2.7V, no delayed sampling	39			
$t_{HD.CI}$	POCI input data hold time		0			ns
$t_{VALID.CO}$	PICO output data valid time (2)				16	ns
$t_{HD.CO}$	PICO output data hold time (3)		1			ns
Peripheral						
$t_{CS.LEAD}$	CS lead-time, CS active to clock		13.5			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			ns

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over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CS.ACC}$	CS access time, CS active to POCI data out				41	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high impedance				41	ns
$t_{SU.PI}$	PICO input data setup time		15			ns
$t_{HD.PI}$	PICO input data hold time		2.9			ns
$t_{VALID.PO}$	POCI output data valid time(2)	2.7 < VDD < 3.6V			31	ns
		1.62 < VDD < 2.7V			41	
$t_{HD.PO}$	POCI output data hold time(3)		5.5			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge
(4) fSPIclk = 1/2tLO/HI with tLO/HI = max(tVALID,CO + tSU,PI, tSU,CI + tVALID,PO).

7.17.2 SPI Timing Diagram

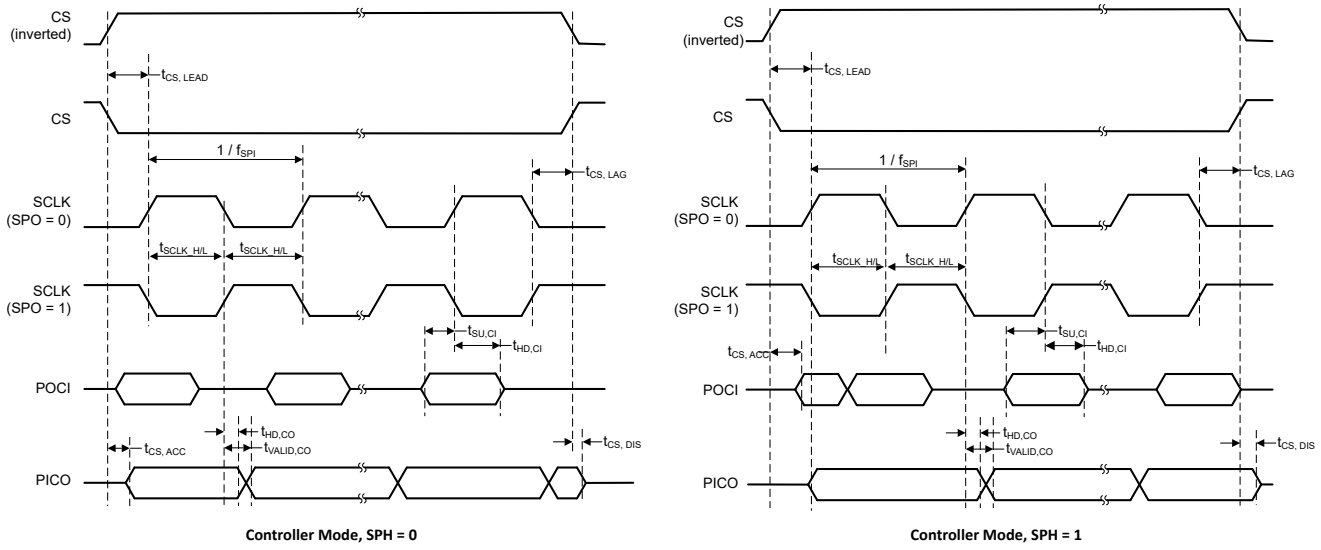


Figure 7-4. SPI Timing Diagram - Controller Mode

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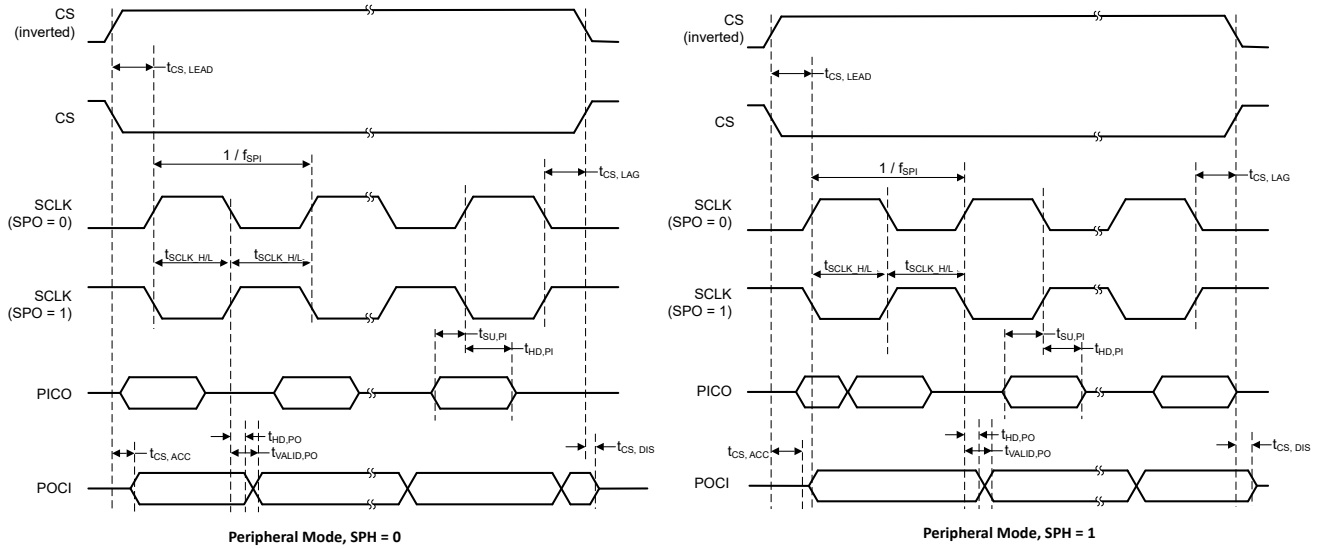


Figure 7-5. SPI Timing Diagram - Peripheral Mode

7.18 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency				32	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)				4	MHz
t_{SP}	Pulse duration of spikes suppressed by input filter (1)	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	
		AGFSELx = 2		22	60	
		AGFSELx = 3		35	90	

(1) Pulses on the UART receive input (RX) that are shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum useable baud rate. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

7.19 TIMx

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{res}	Timer resolution time	$f_{TIMxCLK}$ = 32MHz	31.25			ns
			1			$t_{TIMxCLK}$
t_{res}	Timer resolution time	TIMx with 16bit counter			16	bit
$t_{COUNTER}$	16-bit counter clock period	$f_{TIMxCLK}$ = 32MHz	0.03125		2048	us
			1		65536	$t_{TIMxCLK}$

7.20 Emulation and Debug

7.20.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWD}	SWD frequency				10	MHz

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8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.1 CPU

The CPU subsystem (MCPUSS) implements an Arm Cortex-M0+ CPU, an instruction pre-fetch/cache, a system timer, and interrupt management features. The Arm Cortex-M0+ is a cost-optimized, 32-bit CPU which delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- Arm Cortex-M0+ CPU supporting clock frequencies up to 32kHz
  - ARMv6-M Thumb instruction set (little endian) with 32-cycle 32x32 multiply instruction
- Pre-fetch logic to improve sequential code execution, and I-cache with two 64-bit cache lines
- System timer (SysTick) with 24-bit down counter and automatic reload
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail-chaining

For more details, see the CPU chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.2 Operating Modes

MSPM0 MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD, or a logic level match on certain IOs. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (for example, RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0 devices implement two power domains: **PD1** (for the CPU, memories, and high performance peripherals), and **PD0** (for low speed, low power peripherals).

- **PD1** is always powered in RUN and SLEEP modes, but is disabled in all other modes.
- **PD0** is always powered in RUN, SLEEP, STOP, and STANDBY modes.
- **PD1** and **PD0** are both disabled in SHUTDOWN mode.

8.2.1 Functionality by Operating Mode

Supported functionality in each operating mode is given in Table 8-1.

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode but is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained. When waking up from an OFF state, all module registers must be re-configured to the desired settings by application software.

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Table 8-1. Supported Functionality by Operating Mode

Operating Mode		RUN			SLEEP			STOP		STANDBY		SHUT DOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP2	STANDBY0	STANDBY1	
Oscillators	SYSOSC	EN	EN	DIS	EN	EN	DIS	OPT[1]	DIS	DIS	DIS	OFF
	LFOSC or LFXT	EN										OFF
	HFXT	EN	DIS	DIS	OPT	DIS						OFF
Clocks	CPUCLK	32M	32k	32k	DIS							OFF
	MCLK to PD1	32M	32k	32k	32M	32k	32k	DIS				OFF
	ULPCLK to PD0	32M	32k	32k	32M	32k	32k	4M	32k		DIS	OFF
	ULPCLK to TIMG14,TIMB0, TIMB1, TIMB2, TIMB3	32M	32k	32k	32M	32k	32k	4M	32k			OFF
	RTCCLK	32k										OFF
	MFCLK	OPT	DIS		OPT	DIS		OPT	DIS			OFF
	LFCLK	32k									DIS	OFF
	LFCLK to TIMG14,TIMB0, TIMB1, TIMB2, TIMB3	32k										OFF
	MCLK Monitor	OPT									DIS	OFF
	LFCLK Monitor	OPT										OFF
PMU	POR Monitor	EN										
	BOR Monitor	EN										OFF
	Core Regulator	Full drive								Low drive		OFF
Core Functions	CPU	EN			DIS							OFF
	DMA	OPT						NS (triggers supported)				OFF
	Flash	EN						OPT		DIS		OFF
	SRAM	EN						OPT		DIS		OFF
PD1 Peripherals	CRC	OPT						DIS				OFF
	TIMA0	OPT						DIS				OFF
	UC8	OPT						DIS				OFF
	UC11	OPT						DIS				OFF
	AESADV	OPT						DIS				OFF
	TRNG	OPT						OFF				OFF
PD0 Peripherals	TIMG14	OPT									OPT[2]	OFF
	TIMG1	OPT									OPT[2]	OFF
	TIMG2	OPT									OPT[2]	OFF
	UC4	OPT									OPT[2]	OFF
	UC6	OPT									OPT[2]	OFF
	UC7	OPT									OPT[2]	OFF
	GPIOA	OPT									OPT[2]	OFF
	GPIOB	OPT									OPT[2]	OFF
	WWDT0	OPT									DIS	OFF
	Keystore	OPT										OFF

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Table 8-1. Supported Functionality by Operating Mode (continued)

Operating Mode		RUN			SLEEP			STOP		STANDBY		SHUT DOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP2	STANDBY0	STANDBY1	
LFSS Peripherals	IWDT	OPT										OFF
	RTC_B	OPT										OFF
Analog	ADC0	OPT							NS (triggers supported)			OFF
	VREF	OPT							NS			OFF
	COMP0	OPT										OFF
	Temperature Sensor	OTP								OFF		OFF
IOMUX and IO Wakeup		EN										DIS w/ WAKE
Wake Sources		N/A			ANY IRQ			PD0 IRQ				IOMUX, NRST, SWD

(1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as it was in RUN1, and ULPCLK remains at 32kHz as it was in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as it was in RUN2, and ULPCLK remains at 32kHz as it was in RUN2.
(2) When using the STANDBY1 policy for STANDBY, only TIMG14 and TIMB0/1/2/3 are clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.

8.3 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brown-out reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY mode to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted
- 4 bytes of shutdown memory

For more details, see the PMU chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.4 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32kHz)
- **SYSOSC**: Internal high-frequency oscillator (32MHz with factory trim)
- **LFXT/LFCKIN** : low-frequency external crystal oscillator or digital clock input (32kHz)
- **HFXT/HFCKIN**: high-frequency external crystal oscillator or digital clock input (4MHz to 32MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC, LFCLK, or HSCLK, active in RUN and SLEEP modes
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes

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- **LFCLK**: 32kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes
- **RTCCLK**: fixed 32kHz clock direct to RTC
- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes
- **HFCLK**: High frequency clock derived from HFXT or HFCLK_IN, available in RUN and SLEEP mode
- **HSCLK**: High speed clock derived from HFCLK, available in RUN and SLEEP mode

For more details, see the CKM chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.5 DMA Trigger Mapping

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA in these devices support the following key features:

- 3 DMA transfer channel
  - 2 full-feature channels, supporting repeated transfer modes
  - 1 basic channel, supporting single transfer mode
- Configurable DMA channel priorities
- Direct peripheral to DMA trigger is supported from ADC, UART, SPI or timer triggers.
- Byte (8-bit), short word (16-bit) and word (32-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization, such as 3-phase metering applications
- Gather mode

Table 8-2 shows the DMA features that are supported and the corresponding DMA channel numbers.

Table 8-2. DMA_B Channel Features

DMA Feature	DMA_B	
	Full-Feature Channel	Basic Channel
Channel Number	0	1, 2
Repeated mode	✓	–
Table & fill mode	✓	–
Gather mode	✓	–
Early IRQ notification	✓	–
Auto enable	✓	✓
Long long (128-bit) transfer	✓	✓
Stride mode	✓	✓
Cascading channel support	✓	✓

Table 8-3 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Table 8-3. DMA Trigger Mapping

DMACTL.DMATSEL	TRIGGER SOURCE
0	Software
1	Generic Subscriber 0 (FSUB_0)

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Table 8-3. DMA Trigger Mapping (continued)

DMACTL.DMATSEL	TRIGGER SOURCE
2	Generic Subscriber 0 (FSUB_1)
3	AESADV PUBLISHER 1
4	AESADV PUBLISHER 2
5	UC4.PUBLISHER_1
6	UC4.PUBLISHER_2
7	UC6.PUBLISHER_1
8	UC6.PUBLISHER_2
9	UC7.PUBLISHER_1
10	UC7.PUBLISHER_2
11	UC8.PUBLISHER_1
12	UC8.PUBLISHER_2
13	ADC0 DMA Trigger

For more details, see the DMA chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.6 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA, or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) which are interconnected through an event fabric containing a combination of static and programmable routes.

Events which are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
  - Example: RTC interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
  - Example: UART data receive trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)
  - Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

For more details, see the EVENT chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

Table 8-4. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish its event to another entity (or entities, in the case of a splitter route), where an entity may be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A
1	Generic event channel 1 selected	1 : 1
2	Generic event channel 2 selected	1 : 1
3	Generic event channel 3 selected	1 : 1
4	Generic event channel 4 selected	1 : 1
5	Generic event channel 5 selected	1 : 1
6	Generic event channel 6 selected	1 : 1
7	Generic event channel 7 selected	1 : 1
8	Generic event channel 8 selected	1 : 1
9	Generic event channel 9 selected	1 : 1

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Table 8-4. Generic Event Channels (continued)

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish its event to another entity (or entities, in the case of a splitter route), where an entity may be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
10	Generic event channel 10 selected	1 : 1
11	Generic event channel 11 selected	1 : 1
12	Generic event channel 12 selected	1 : 2 (splitter)
13	Generic event channel 13 selected	1 : 2 (splitter)
14	Generic event channel 14 selected	1 : 2 (splitter)
15	Generic event channel 15 selected	1 : 2 (splitter)

8.7 Memory

8.7.1 Memory Organization

Table 8-5 summarizes the memory map of the devices. For more information about the memory region detail, see the *Platform Memory Map* section in the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

Table 8-5. Memory Organization Summary

Memory Region	Subregion	MSPM0L1127	MSPM0L1126
Code (Flash Bank 0)	FLASH Main ECC Corrected	128KB	64KB
		0x00000000 to 0x0001FFFF	0x00000000 to 0x0000FFFF
	FLASH Main ECC Uncorrected	0x00400000 to 0x0041FFFF	0x00400000 to 0x0040FFFF
	FLASH Main ECC Code	0x41800000 to 0x4181FFFF	0x41800000 to 0x4180FFFF
SRAM (SRAM)	SRAM Default	12KB	12KB
		0x20000000 to 0x20002FFF	0x20000000 to 0x20002FFF
	SRAM Parity Checked	0x20100000 to 0x20102FFF	0x20100000 to 0x20102FFF
	SRAM Unchecked	0x20200000 to 0x20202FFF	0x20200000 to 0x20202FFF
	SRAM Parity ECC Code	0x20300000 to 0x20302FFF	0x20300000 to 0x20302FFF
Peripheral	NONMAIN[(2)]	2KB	2KB
		0x41C00000 to 0x41C007FF	0x41C00000 to 0x41C007FF
	FACTORY	1KB	1KB
		0x41C40000 to 0x41C403FF	0x41C40000 to 0x41C403FF
Subsystem		0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF

8.7.2 Peripherals Summary

Table 8-6. Peripherals Summary

Peripheral name	Base Address	Size
ADC0	0x40004000	0x00002000
COMP0	0x40008000	0x00001F00
VREF	0x40030000	0x00001F00
WWDT0	0x40080000	0x00001500
TIMG14	0x40084000	0x00001F00
TIMG1	0x40086000	0x00001F00
TIMG2	0x40088000	0x00001F00
LFSS	0x40094000	0x00001600
GPIOA	0x400A0000	0x00001F00

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Table 8-6. Peripherals Summary (continued)

Peripheral name	Base Address	Size
GPIOB	0x400A2000	0x00001F00
KEYSTORECTL	0x400AC000	0x00002000
SYSCTL	0x400AF000	0x00003100
TIMB0	0x400B8000	0x00001C00
TIMB1	0x400BA000	0x00001C00
TIMB2	0x400BC000	0x00001C00
TIMB3	0x400BE000	0x00001C00
DEBUGSS	0x400C7000	0x00001F00
EVENTLP	0x400C9000	0x00003000
FLASHCTL	0x400CD000	0x00002000
CPUSS	0x40400000	0x00001F00
WUC	0x40424000	0x00000500
IOMUX	0x40428000	0x00002000
DMA	0x4042A000	0x00001F00
CRC0	0x40440000	0x00002000
AESADV	0x40442000	0x00001200
ADC0_SVT	0x4055A000	0x00001000
TIMA0	0x40860000	0x00001F00
UC4_UART	0x40A00000	0x00001500
UC6_I2CC	0x40A22000	0x00023500
UC7_I2CT	0x40A44000	0x00045500
UC4_SPI	0x40A60000	0x00061200
UC4	0x40A80000	0x00081C00
UC6	0x40A82000	0x00082A00
UC7	0x40A84000	0x00084A00
SPG0	0x40A9F000	0x000A0C00
UC8_UART	0x40B00000	0x00001500
UC11_UART	0x40B02000	0x00003500
UC8_SPI	0x40B60000	0x00061200
UC8	0x40B80000	0x00081C00
UC11	0x40B82000	0x00082A00

8.7.3 Interrupt Vector Number

Table 8-7. Interrupt Vector Number

Peripheral name	NVIC IRQ
SYSCTL	0
DEBUGSS	1
UC6	3
ADC0	4
TIMB0	5
TIMB1	6
COMP0	7
UC7	8
UC8	9
TIMB2	13

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Table 8-7. Interrupt Vector Number (continued)

Peripheral name	NVIC IRQ
TIMB3	14
UC4	15
TIMG14	16
TIMG2	17
TIMA0	18
TIMG1	19
GPIOA	22
GPIOB	23
UC11	24
AESADV	26
FLASHCTL	27
WWDT0	29
LFSS	30
DMA	31

8.8 Flash Memory

A single bank of nonvolatile flash memory is provided for storing executable program code and application data.

Key features of the flash include:

- Hardware ECC protection (encode and decode) with single bit error correction and double-bit error detection
- In-circuit program and erase operations supported across the entire recommended supply range
- Small 1KB sector sizes (minimum erase resolution of 1KB)
- Up to 100,000 program/erase cycles on 32 selected sectors of the flash memory, with up to 10,000 program/erase cycles on the remaining flash memory (devices with 32kB support 100,000 cycles on the entire flash memory)

For more details, see the NVM chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.9 SRAM

MSPM0Lxx MCUs include a low-power high-performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. MSPM0Lxx MCUs also provide up to 128KB of ECC protected SRAM with hardware parity. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in RUN, SLEEP, STOP, and STANDBY operating modes and is lost in SHUTDOWN mode. A write protection mechanism is provided to allow the application to dynamically write protect the SRAM memory with 1KB resolution. Write protection is useful when placing executable code into SRAM to provide a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

8.10 GPIO

The general purpose input/output (GPIO) peripheral lets the application write data out and read data in through the device pins. Through the use of the Port A and Port B GPIO peripheral, these devices support up to 60 GPIO pins.

The key features of the GPIO module include:

- Set/Clear/Toggle multiple bits without the need of a read-modify-write construct in software
- GPIOs with "Standard with Wake" drive functionality able to wake the device from SHUTDOWN mode
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

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For more details, see the GPIO chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.11 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO Pad configuration registers allow for programmable drive strength, speed, pullup-down, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.12 ADC

The 12-bit analog-to-digital converter (ADC) module in these devices support fast 12-bit conversions with single-ended inputs.

ADC features include:

- 12-bit output resolution at up to 1.6Msps with 10.6-bit ENOB
- Up to 26 external input channels
- Internal channels for temperature sensing, supply monitoring, and analog signal chain
- Software selectable reference:
  - Configurable internal dedicated ADC reference voltage of 1.4V or 2.5V (VREF)
  - MCU supply voltage (VDD)
  - Support for bringing in an external reference on VREF+/- device pins
  - Requires a decpoupling capacitor placed on VREF+/- pins for proper operation.
- Operates in RUN, SLEEP, and STOP modes and supports triggers from STANDBY mode

Table 8-8. ADC0 Channel Mapping

CHANNEL[0:7]	SIGNAL NAME	CHANNEL[8:15]	SIGNAL NAME
0	A0	16	A16
1	A1	17	A17
2	A2	18	A18
3	A3	19	A19
4	A4	20	A20
5	A5	21	A21
6	A6	22	A22
7	A7	23	A23
8	A8	24	A24
9	A9	25	A25
10	A10	26	-
11	A11	27	Reserved
12	A12	28	*Temperature Sensor*
13	A13	29	VREFINT
14	A14	30	Reserved
15	A15	31	*Supply/Battery Monitor*

Italicized signal names are internal to the SoC. These signals are used for internal peripheral interconnections.

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For more details, see the ADC chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.13 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 1.4V internal VREF at the factory trim temperature (TS_{TRIM}). This calibration value can be used with the temperature sensor temperature coefficient (TS_c) to estimate the device temperature. See the temperature sensor section of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual for guidance on estimating the device temperature with the factory trim value.

8.14 LFSS

The Low-Frequency Subsystem (LFSS) combines several functional peripherals under one shared subsystem. These peripherals are clocked by the low-frequency clock (LFCLK) or need to be active during low-power modes. The low-frequency clock has a typical frequency of 32kHz and is mainly intended for long-term timekeeping.

LFSS in this device contains following components:

- Real-time clock (RTC_B) with additional prescalar extension and timestamp captures
- An asynchronous Independent Watchdog Timer (IWDT)

For more details, see the LFSS chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.15 IWDT

The independent watchdog timer (IWDT) in the LFSS is a device-independent supervisor which monitors code execution and overall hang up scenarios of the device. Due to the nature of LFSS, this IWDT has its own system independent clock source. If the application software does not successfully reset the watchdog within the programmed time, the watchdog generates a POR reset to the device.

Key features of the IWDT include:

- A 25-bit counter with closed and open window
- Counter driven from LFOSC (fixed 32kHz clock path) with a programmable clock divider
- Eight selectable watchdog timer periods

For more details, see the IWDT chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.16 RTC_B

The RTC_B instance of the real-time clock operates off of a 32kHz input clock source (typically a low frequency crystal) and provides a time base to the application with multiple options for interrupts to the CPU. The RTC_B provides common key features in relation to the Low-Frequency Sub System (LFSS).

Common key features of the RTC_B include:

- Counters for seconds, minutes, hours, day of the week, day of the month, month, and year
- Binary or BCD format
- Leap-year handling
- One customizable alarm interrupt based on minute, hour, day of the week, and day of the month
- Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon
- Interval alarm interrupt providing periodic wake-up at 4096, 2048, 1024, 512, 256, or 128Hz

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- Interval alarm interrupt providing periodic wake-up at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz
- Calibration for crystal offset error (up to +/- 240ppm)
- Compensation for temperature drift (up to +/- 240ppm)
- RTC clock output to pin for calibration

Table 8-9 shows the RTC features supported in this device.

Table 8-9. RTC_B Key Features

RTC Features	RTC_B
Power enable register	-
Real-time clock and calendar mode providing seconds, minutes, hours, day of week, day of month, and year	Yes
Selectable binary or binary-coded decimal (BCD) format	Yes
Leap-year correction (valid for year 1901 through 2099)	Yes
Two customizable calendar alarm interrupts based on minute, hour, day of the week, and day of the month	Yes
Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon	Yes
Periodic interrupt to wake at 4096, 2048, 1024, 512, 256, or 128Hz	Yes
Periodic interrupt to wake at 64, 32, 16, 8, 4, 2, 1, and 0.5Hz	Yes
Interrupt capability down to STANDBY mode with STOPCLKSTBY	Yes
Calibration for crystal offset error and crystal temperature drift (up to ±240ppm total)	Yes
RTC clock output to pin for calibration (GPIO)	Yes
RTC clock output to pin for calibration (TIO)	-
Three -bit prescaler for heartbeat function with interrupt generation	-
RTC external clock selection of untrimmed 32kHz, trimmed 512Hz, 256Hz or 1Hz	-
RTC time stamp capture upon detection of a timer stamp event, including: • TIO event • VDD fail event	-
RTC counter lock function	-

For more details, see the RTC chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.17 VREF

The voltage reference module (VREF) contains a configurable voltage reference buffer dedicated for the on-board ADC. The devices also support connection of an external reference for applications in which higher accuracy is required.

VREF features include:

- 1.4V and 2.5V user-selectable internal references.
- Internal reference supports ADC operation up to 515ksps
- Support for bringing in an external reference on VREF+ and VREF- device pins
- No decoupling capacitor is required for proper operation. See Figure 8-1 for more details

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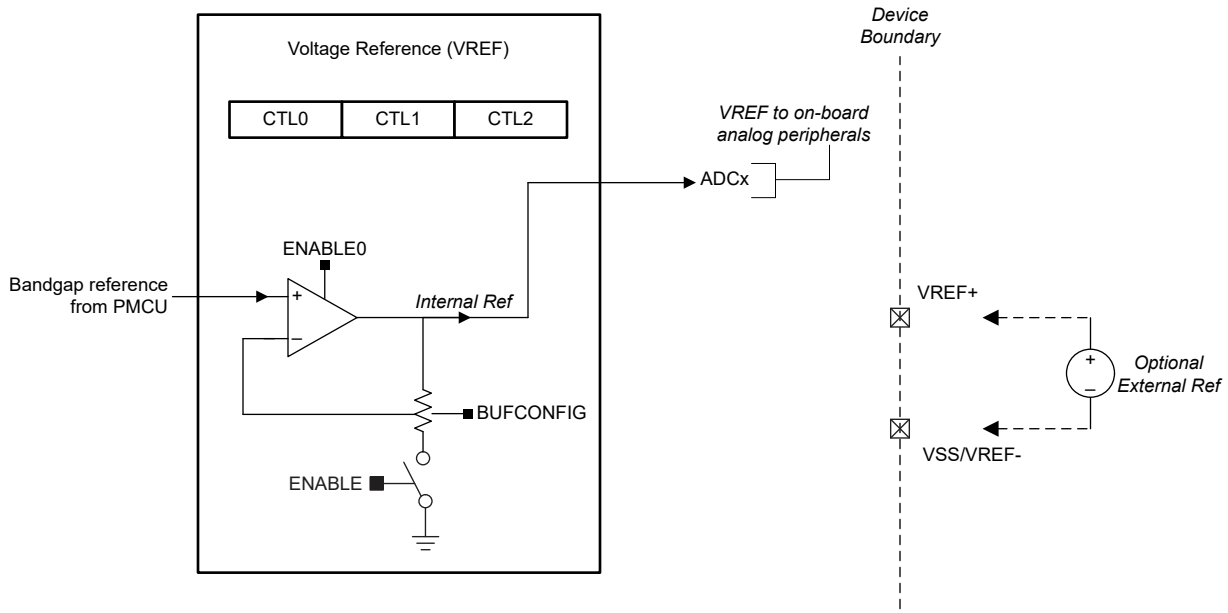


Figure 8-1. VREF module

For more details, see the VREF chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.18 COMP

The comparator peripheral in the device compares the voltage levels on two inputs terminals and provides a digital output based on this comparison. It supports the following key features:

- Programmable hysteresis
- Programmable reference voltage:
  - External reference voltage (VREF IO)
  - Integrated 8-bit reference DAC
- Configurable operation modes:
  - High speed mode
  - Lower power mode
- Programmable output glitch filter delay
- Supports 6 blanking sources from TIMx instances (see Table 8-10)
- Support output wake up device from all low power modes
- Output connected to advanced timer fault handling mechanism
- The IPSEL and IMSEL bits in comparator registers can be used to select the comparator channel inputs from device pins
- 8-bit reference DAC can be used to output to device pins

Table 8-10. COMP0 Input Channel Selection

IPSEL / IMSEL BITS	POSITIVE TERMINAL INPUT	NEGATIVE TERMINAL INPUT
0x0	COMP0_IN0+	COMP0_IN0-
0x1	COMP0_IN1+	COMP0_IN1-
0x2	COMP0_IN2+	COMP0_IN2-
0x3	COMP0_IN3+	-
0x5	-	Temperature Sensor

Table 8-11. COMP0 Blanking Source Table

CTL2.BLANKSRC	Blanking Source Selected
1	TIMA0.CC2

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Table 8-11. COMP0 Blanking Source Table (continued)

CTL2.BLANKSRC	Blanking Source Selected
2	TIMA0.CC3
3	TIMA0.CC1
4	TIMG14.CC1
5	TIMG1.CC1
6	TIMG2.CC1

For more information about device analog connections, refer to Analog Connections.

For more details, see the COMP chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.19 Security

This device offers several security features, including:

- Debug security
- Device identify
- AES-128/256 accelerator with support for GCM/GMAC, CCM/CBC-MAC, CBC, CTR
- Flexible firewalls for protecting code and data
  - Flash write-erase protection
  - Flash read-execute protection
  - Flash IP protection
  - SRAM write-execute mutual exclusion
- Secure boot
- Secure firmware update
- Secure key storage for up to two 128-bit AES keys
- Customer secure code
- Cyclic Redundancy Checker (CRC-16) with support for custom polynomial

For more details, see the Security chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.20 AESADV

The AES advanced (AESADV) accelerator module performs encryption and decryption of 128-bit data blocks with a 128-bit or 256-bit key in hardware according to the advanced encryption standard (AES). AES is a symmetric-key block cipher algorithm specified in FIPS PUB 197.

The AESADV accelerator features include:

- AES operation with 128-bit and 256-bit keys
- Key scheduling in hardware
- Enc/decrypt only modes: CBC, CFB-1, CFB-8, CFB-128, OFB-128, CTR/ICM
- Authentication only modes: CBC-MAC, CMAC
- AES-CCM (using AES-CTR mode and AES-CBC-MAC)
- AES-GCM (using AES-CTR mode and GHASH, supports basic GHASH operation when selecting no encryption)
- AES-CCM and AES-GCM modes support continuation with hold/resume of payload data
- 32-bit word access to provide key data, input data, and output data
- AESADV ready interrupt
- DMA triggers for input/output data
- Supported in RUN and SLEEP (see the Section 8.2l)

For more details, see the AESADV chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

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8.21 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for bit reversal

For more details, see the CRC chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.22 Keystore

The Keystore controller provides secure management of the Advanced Encryption Engine (AES) keys. The use-model of the keystore controller is to securely deposit keys into it during the execution of customer secure code, and have the AES engine access them subsequently in a secure manner without leaking any key data to observers. Two 128-bit or one 256-bit keys can be stored in the keystore's key slots. The keystore and its interaction with the AES engine are designed for secure operation including thwarting partial key modification attacks.

For more details, see the KEYSTORE chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.23 UNICOMM (UART/I²C/SPI)

UNICOMM is a highly flexible peripheral which can be configured as a UART, SPI, I²C-Controller or I²C-Target function. The user can select one of the serial interfaces before configuration and data transfer. The peripheral uses a common FIFO per instance to maximize the device capability based on the operating state. A serial peripheral group combines one or more UNICOMM for special functions like I²C loopback and is an optional configuration. Table 8-12 describes the grouping of UNICOMM, peripheral serial interfaces available and FIFO depth.

Table 8-12. UNICOMM (UCx) Serial Peripheral

SERIAL PERIPHERAL GROUP	UNICOMM INSTANCE	Local UCx Index	Global UCx Index	UART	I²C Controller	I²C Target	SPI	FIFO depth
SPG0 (PD0)	UC4	0	4	Yes	-	-	Yes	4
	UC6	1	6	-	Yes	-	-	4
	UC7	2	7	-	-	Yes	-	4
SPG1 (PD1)	UC8	0	8	Yes	-	-	Yes	4
	UC11	1	11	Yes	-	-	-	1

8.23.1 UART (UNICOMM)

The UART peripheral function provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7 or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - Line-break detection
  - Programmable baud rate generation with oversampling by 16, 8 or 3
  - Local Interconnect Network (LIN) mode support
- Support transmit and receive loopback mode operation
- See Table 8-13 for detail information on supported protocols

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Table 8-13. UART (UNICOMM) Features

Supported Features	UC4.UART	UC8.UART, UC11.UART
Active in Stop and Standby Mode	Yes	-
Support hardware flow control	Yes	Yes
Support 9-bit configuration	Yes	Yes
Support LIN mode	Yes	-
Support DALI	Yes	-
Support IrDA	Yes	-
Support ISO7816 Smart Card	Yes	-
Support Manchester coding	Yes	-

For more details, see the UART (UNICOMM) chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*

8.23.2 I2C (UNICOMM)

The inter-integrated circuit interface (I^2C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100kbit/s
- Support Fast-mode (Fm), with a bit rate up to 400kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
  - Supported on open drain IOs (ODIO) and high-drive (HDIO) IOs only
- Separated transmit and receive FIFOs support DMA data transfer
- Wakeup from low power mode on address match
- Supportt digital glitch filter for input signal glitch suppression
- See Table 8-14 and Table 8-15 for detailed information on supported features for controller and target functions

Table 8-14. I2C Controller (UNICOMM) Features

Supported Features	UC6.I2C,
Supports standard-mode (Sm)	Yes
Supports Fast-mode (Fm)	Yes
Supports Fast-mode Plus (Fm+)	Yes
Supports analog glitch filter	Yes
Supports digital glitch filter	-
Supports burst mode	Yes
Supports SMBus mode	Yes

Table 8-15. I2C Target (UNICOMM) Features

Supported Features	UC7.I2C
Supports standard-mode (Sm)	Yes
Supports Fast-mode (Fm)	Yes
Supports Fast-mode Plus (Fm+)	Yes
Supports analog glitch filter	Yes
Supports digital glitch filter	-

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Table 8-15. I2C Target (UNICOMM) Features (continued)

Supported Features	UC7.I2C
Supports second target address & mask	Yes
Supports SMBus mode	Yes
Supports low power wakeup	Yes

For more details, see the I2C (UNICOMM) chapter of the *MSPM0 L-Series Technical Reference Manual.*

8.23.3 SPI (UNICOMM)

The serial peripheral interface (SPI) peripherals function support the following key features:

- Support ULPCLK/2 bit rate and up to 16Mbits/s in both controller and peripheral mode
- Configurable as a controller or a peripheral
- Supports single parity for transmit and receive
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode) and 7 bits to 16 bit (peripheral mode)
- Transmit and receive FIFOs (4 entries each with 16 bits per entry) supporting DMA data transfer
- Supports TI mode and Motorola mode
- Support single bit parity in both transmit and receive paths
- See Table 8-16 for detailed information on supported features

Table 8-16. SPI (UNICOMM) Features

Supported Features	UC4.SPI, UC8.SPI
Controller and Peripheral mode	Yes
Supports Parity function	Yes
Supports Repeat mode transfer	-
Supports Receive timeout	-
Supports Command/Data control	-
Supports 4 chip selects	-

For more details, see the SPI (UNICOMM) chapter of the *MSPM0 L-Series Technical Reference Manual.*

8.24 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.25 Timers (TIMx)

There are two timer peripherals in these devices support that following key features: TIMBx (basic timer), TIMGx (general-purpose timer) and TIMAx (advanced timer). TIMGx is a subset of TIMAx, which means these timers share many common features that are compatible in software. For specific configuration, see Table 8-17:

Specific features for the general-purpose timer **(TIMGx)** include:

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- 16-bit and 32-bit timers with up, down or up-down counting modes, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt/DMA trigger generation and cross peripherals (such as ADC) trigger capability

Specific features for the advanced timer **(TIMAx)** include:

- 16-bit timer with up, down or up-down counting modes, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter
- Up to four independent CC channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Two additional capture/compare channels for internal events (CC4/CC5)
- Shadow register for load and CC register available in TIMA0
- Complementary output PWM
- Asymmetric PWM with programmable dead band insertion
- Fault handling mechanism to make sure the output signals in a safe user-defined state when a fault condition is encountered
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt and DMA trigger generation and cross peripherals (such as ADC) trigger capability
- Two additional capture/compare channels for internal events

Specific features for the basic software timer (**TIMBx**) include:

- Support for a counter array containing 4 counters
- Each counter is a 16 bit counter
- Clocked by the bus clock
- Ability to concatenate 2 or more counters to create longer time durations
- Ability to measure timing properties of external events
  - Duration between 2 pulses on an event
  - Counting the number of events
  - Ability to start/stop the counter based on external events or internal events

Table 8-17. TIMx Instance Configuration

Instance	Power Domain	Counter Resolution	Prescaler	Repeat Counter	CCP Channels (External/ Internal)	External PWM Channels	Phase Load	Shadow Load	Shadow CCs	Deadband	Fault Handler	QEI / Hall Input Mode
TIMB3	PD0	16 bit	–	–	–	–	–	–	–	–	–	–
TIMB2	PD0	16 bit	–	–	–	–	–	–	–	–	–	–
TIMB1	PD0	16 bit	–	–	–	–	–	–	–	–	–	–
TIMB0	PD0	16 bit	–	–	–	–	–	–	–	–	–	–
TIMG2	PD0	16 bit	8 bit	–	2	–	–	–	–	–	–	–
TIMG1	PD0	16 bit	8 bit	–	2	–	–	–	–	–	-	–
TIMG14	PD0	16 bit	8bit	–	4	–	–	–	–	–	–	–
TIMA0	PD1	16 bit	8 bit	8-bit	4	Yes	Yes	Yes	Yes	Yes	–	–

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Table 8-18. TIMx Cross Trigger Map

TSEL.ETSEL Selection	TIMA0	TIMG14	TIMG1	TIMG2
0	TIMA0.TRIG0	TIMA0.TRIG0	TIMA0.TRIG0	TIMA0.TRIG0
1	TIMG14.TRIG0	TIMG14.TRIG0	TIMG14.TRIG0	TIMG14.TRIG0
2	TIMG1.TRIG0	TIMG1.TRIG0	TIMG1.TRIG0	TIMG1.TRIG0
3	TIMG2.TRIG0	TIMG2.TRIG0	TIMG2.TRIG0	TIMG2.TRIG0
4 to 31	Reserved			

Table 8-19. TIMBx Clock Source Selection

CTRREGSx.CTL0.CLKSEL	Counter update from event source
0	Bus Clock
1	Overflow from Counter 0
2	Overflow from Counter 1
3	Overflow from Counter 2
4 to 8	Reserved
9	GPIO0 Publisher 1
10	GPIO0 Publisher 2
11	GPIO1 Publisher 1
12	GPIO1 Publisher 2
13 to 15	Reserved

Table 8-20. TIMBx Start/Stop/Reset Source Selection

CTRREGSx.CTL0.STARTSEL CTRREGSx.CTL0.STOPSEL CTRREGSx.CTL0.RESETSEL	Start/Stop/Reset from event source
0	No Action
1	Overflow from Counter 0
2	Overflow from Counter 1
3	Overflow from Counter 2
4 to 8	Reserved
9	GPIO0 Publisher 1
10	GPIO0 Publisher 2
11	GPIO1 Publisher 1
12	GPIO1 Publisher 2
13 to 15	Reserved

For more details, see the TIMx chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

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8.26 Device Analog Connections

Figure 8-2 shows the internal analog connection of the device.

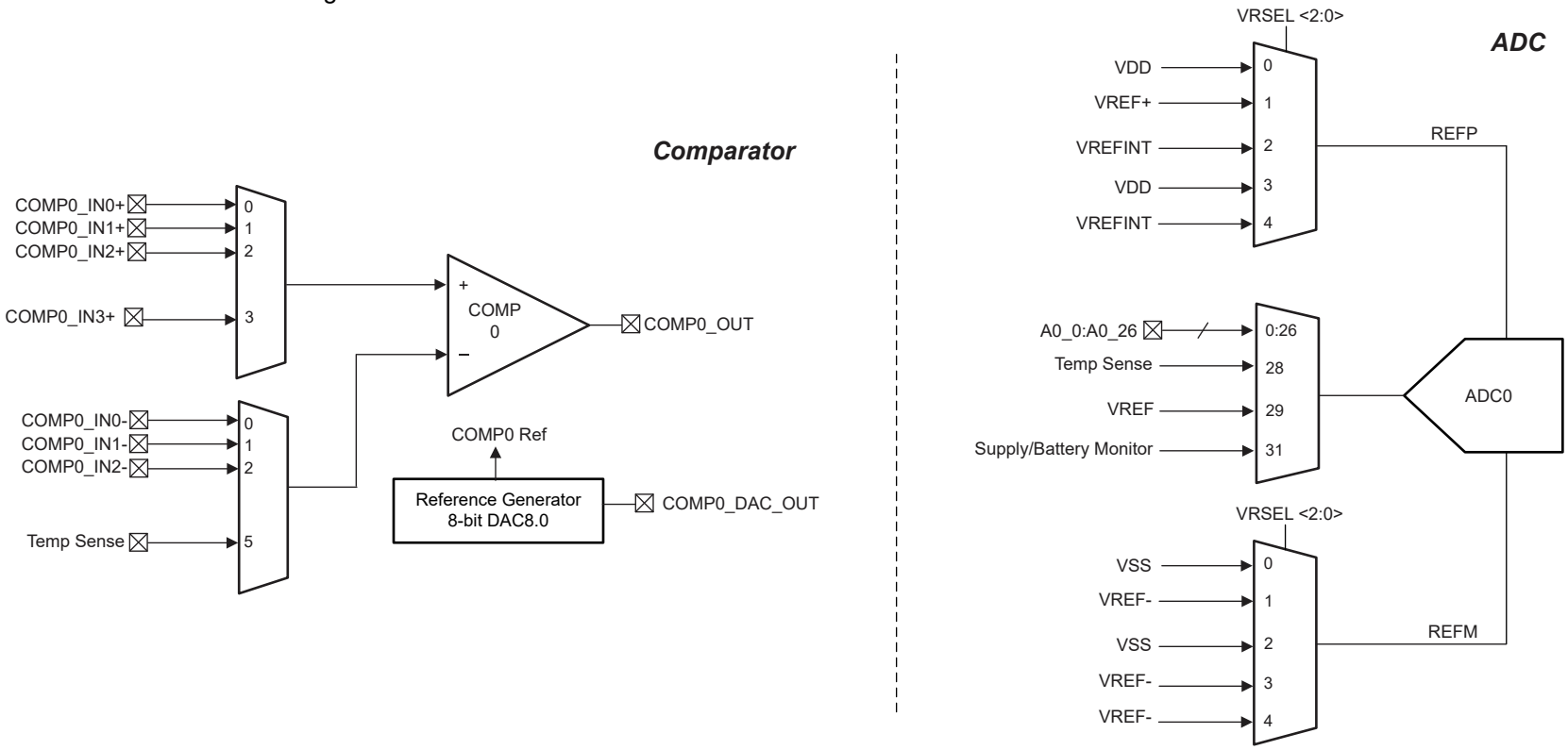


Figure 8-2. Device Analog Connection

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8.27 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. It also provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, refer to the IOMUX section of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-3. Not all pins will have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

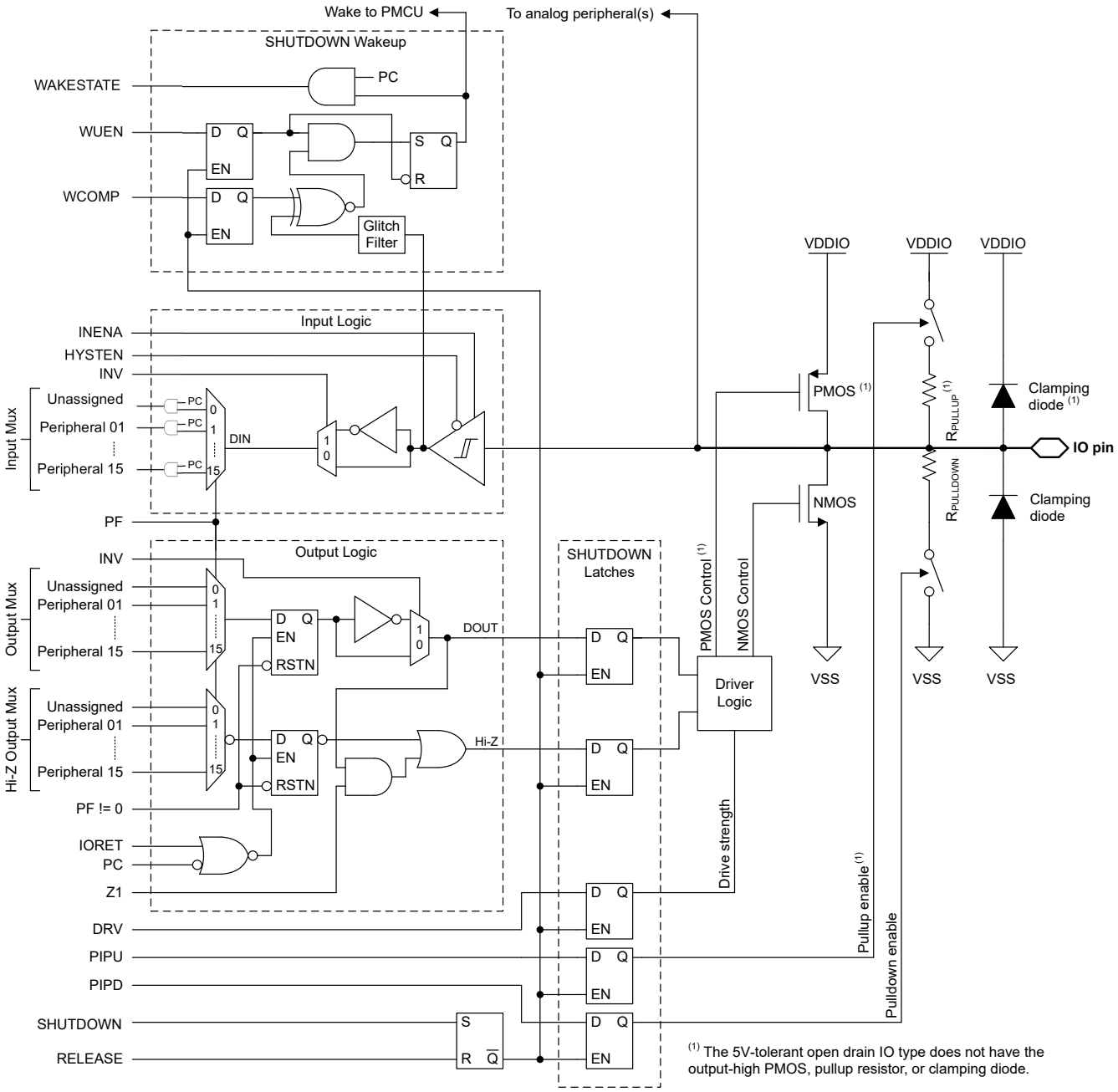


Figure 8-3. Superset Input/Output Diagram

8.28 DEBUGSS

The debug subsystem (DEBUGSS) interfaces the ARM Serial Wire Debug (SWD) two-wire physical interface to multiple debug functions within the device. MSPM0 devices support debugging of processor execution and the device state. The DEBUGSS also provides a mailbox system for communicating with software through SWD.

Key features provided by the debug subsystem include:

- The ARM Serial Wire Debug (SWD) two-wire (SWDIO, SWCLK) debug interface, compatible with both TI and 3rd party debug probes
  - On-chip pullup and pulldown resistors for SWDIO and SWCLK, respectively, enabled by default
  - Support for disabling SWD functions to use SWD pins as general-purpose input/output pins
  - Support for debug on all low power modes
- Debug of the processor
  - Run, halt, and step debug support
  - 2 hardware breakpoints (BPU)
  - 1 hardware watchpoints (DWT)
  - Supporting software breakpoints
- Software-configurable peripheral behavior during processor debug
  - Ability to free run select peripherals through debug halt
  - Ability to halt select peripherals on a debug halt
  - Ability to request reset and mode changes to the PMCU
- Mailbox (DSSM) for passing data and control signals between the SWD interface and boot ROM (as well as application software)
- Support for various security features, including SWD lockout and password authenticated debugging

For more details, see the DEBUGSS chapter of the *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual*.

8.29 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device.

Table 8-21. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

For a complete description of the debug functionality offered on MSPM0 devices, see the Debug chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual.

8.30 Bootstrap Loader (BSL)

The bootstrap loader (BSL) enables configuration of the device as well as programming of the device memory through a UART or I2C serial interface. Access to the device memory and configuration through the BSL is protected by a 256-bit user-defined password, and it is possible to completely disable the BSL in the device configuration, if desired. The BSL is enabled by default from TI to support use of the BSL for production programming.

A minimum of two pins are required to use the BSL: the BSLRX and BSLTX signals (for UART), or the BSLSCL and BSLSDA signals (for I^2C). Additionally, one or two additional pins (BSL_invoke and NRST) may be used for controlled invocation of the bootloader by an external host.

If enabled, the BSL may be invoked (started) in the following ways:

- The BSL is invoked during the boot process if the BSL_invoke pin state matches the defined BSL_invoke logic level. If the device fast boot mode is enabled, this invocation check is skipped. An external host can force the device into the BSL by asserting the invoke condition and applying a reset pulse to the NRST pin to

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trigger a BOOTRST, after which the device will verify the invoke condition during the reboot process and start the BSL if the invoke condition matches the expected logic level.
- The BSL is automatically invoked during the boot process if the reset vector and stack pointer are left unprogrammed. As a result, a blank device from TI will invoke the BSL during the boot process without any need to provide a hardware invoke condition on the BSL_invoke pin. This enables production programming using just the serial interface signals.
- The BSL may be invoked at runtime from application software by issuing a SYSRST with BSL entry command.

Table 8-22. BSL Pin Requirements and Functions

DEVICE SIGNAL	CONNECTION	BSL FUNCTION
BSLRX	Required for UART	UART receive signal (RXD), an input
BSLTX	Required for UART	UART transmit signal (TXD) an output
BSLSCL	Required for I2C	I^2C BSL clock signal (SCL)
BSLSDA	Required for I2C	I^2C BSL data signal (SDA)
BSL_invoke	Optional	Active-high digital input used to start the BSL during boot
NRST	Optional	Active-low reset pin used to trigger a reset and subsequent check of the invoke signal (BSL_invoke)

For a complete description of the BSL functionality and command set, see the MSPM0 boot strap loader user's guide.

8.31 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Please refer to Factory Constants chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual for more information.

Table 8-23. DEVICEID

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Device	PARTNUM	MANUFACTURER
MSPM0L1126	0xBBC7	0x17
MSPM0L1127	0xBBC7	0x17

Table 8-24. USERID

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	Part	Variant
M0L1127QPMQ1	8420	31
M0L1127QPTQ1	8420	33
M0L1127QRGZQ1	8420	34
M0L1127QRHBQ1	8420	35
M0L1127QRGEQ1	8420	38
M0L1126QPMQ1	1893	39
M0L1126QPTQ1	1893	41
M0L1126QRGZQ1	1893	42
M0L1126QRHBQ1	1893	43
M0L1126QRGEQ1	1893	46

8.32 Identification

Revision and Device Identification

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The hardware revision and device identification values are stored in the memory-mapped FACTORY region, refer to Device Factory Constants section, which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to the Factory Constants chapter of the MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual for more information.

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see Section 10.4).

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9 Applications, Implementation, and Layout

9.1 Typical Application

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1.1 Schematic

TI recommends connecting a combination of a 10µF and a 0.1µF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

The NRST reset pin is required to connect an external 47kΩ pullup resistor with a 1000pF pulldown capacitor.

A 0.47-µF tank capacitor is required for the VCORE pin and must be placed close to the device with minimum distance to the device ground. Do not connect other circuits to the VCORE pin.

For devices supporting external crystals, external bypass capacitors for the crystal oscillator pins are required. Refer to *MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual* which explains how to calculate the capacitor value.

For 5V-tolerant open drain IOs (ODIO), a pullup resistor is required to output a logic high signal. This is required for I^{2}C and UART functions if the ODIO are used.

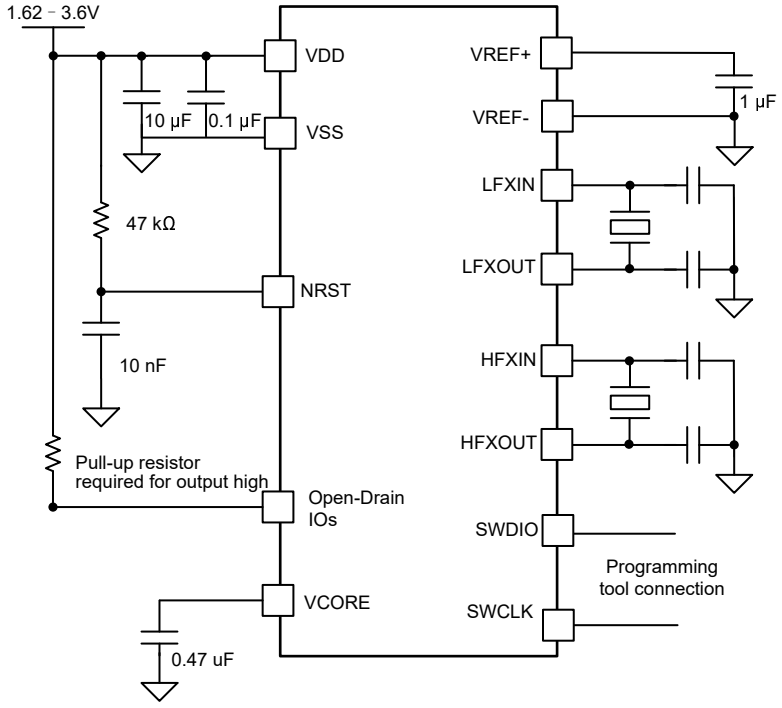


Figure 9-1. Typical Application Schematic

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with development, visit the Texas Instruments *Arm Cortex-M0+ MCUs* page.

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 10-1 provides a legend for reading the complete device name.

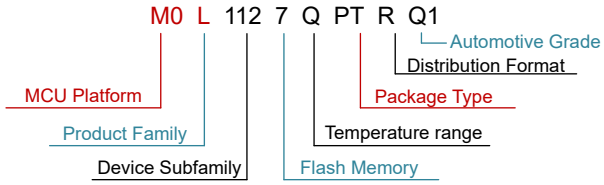


Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

Processor Family	MSP = Mixed-signal processor X= Experimental silicon
MCU Platform	M0 = Arm based 32-bit M0+
Product Family	L = 32MHz frequency
Device Subfamily	1126/7 = 32MHz frequency, ADC, CMP
Flash Memory	6 = 64KB 7= 128KB
Temperature Range	Q = –40°C to 125°C, AEC-Q100 qualified
Package Type	See the *Device Comparison* section and https://www.ti.com/packaging
Distribution Format	R = Large reel No marking = Tube or tray

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

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10.3 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP) Boards: LP-MSPM0L2117	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging/EnergyTrace. The LP ecosystem includes dozens of BoosterPack stackable plug-in modules to extend functionality.

Embedded Software

MSPM0 Software Development Kit (SDK)	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

TI Cloud Tools	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE or in TI Cloud Tools. (offline version)
MSP Academy	Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE & compiler toolchains

Code Composer Studio™ (CCS)	Includes TI Arm-Clang compiler. Supports all TI Arm Cortex MCUs and boasts competitive code size performance advantages, fast compile time, code coverage support, safety certification support, and completely free to use.
IAR Embedded Workbench® IDE	
Keil® MDK IDE	
GNU Arm Embedded Toolchain	

10.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the MSPM0 MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

MSPM0 L-Series 32MHz Microcontrollers Technical Reference Manual	This manual describes the modules and peripherals of the family of devices. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in their exact implementation on different devices.

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Pin functions, internal signal connections, and operational parameters differ from device to device. See the device-specific data sheet for these details.

Errata

MSPM0L112 and MSPM0L211x Microcontroller Errata	This document describes the known exceptions to the functional specifications (advisories).

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.6 Trademarks

LaunchPad™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2026	1.0	Initial Release

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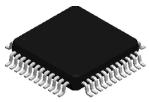
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Mechanical Data

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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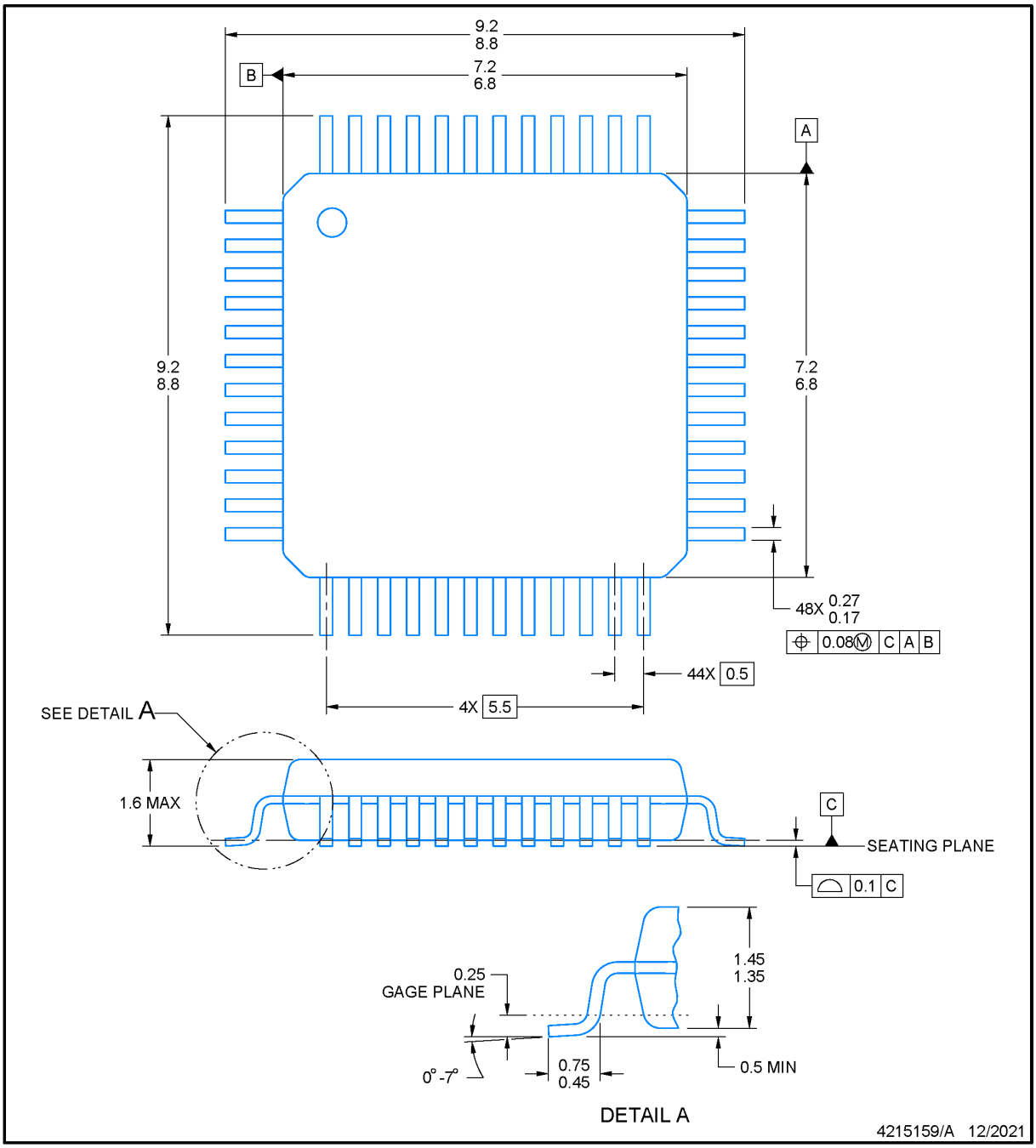


PACKAGE OUTLINE

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.

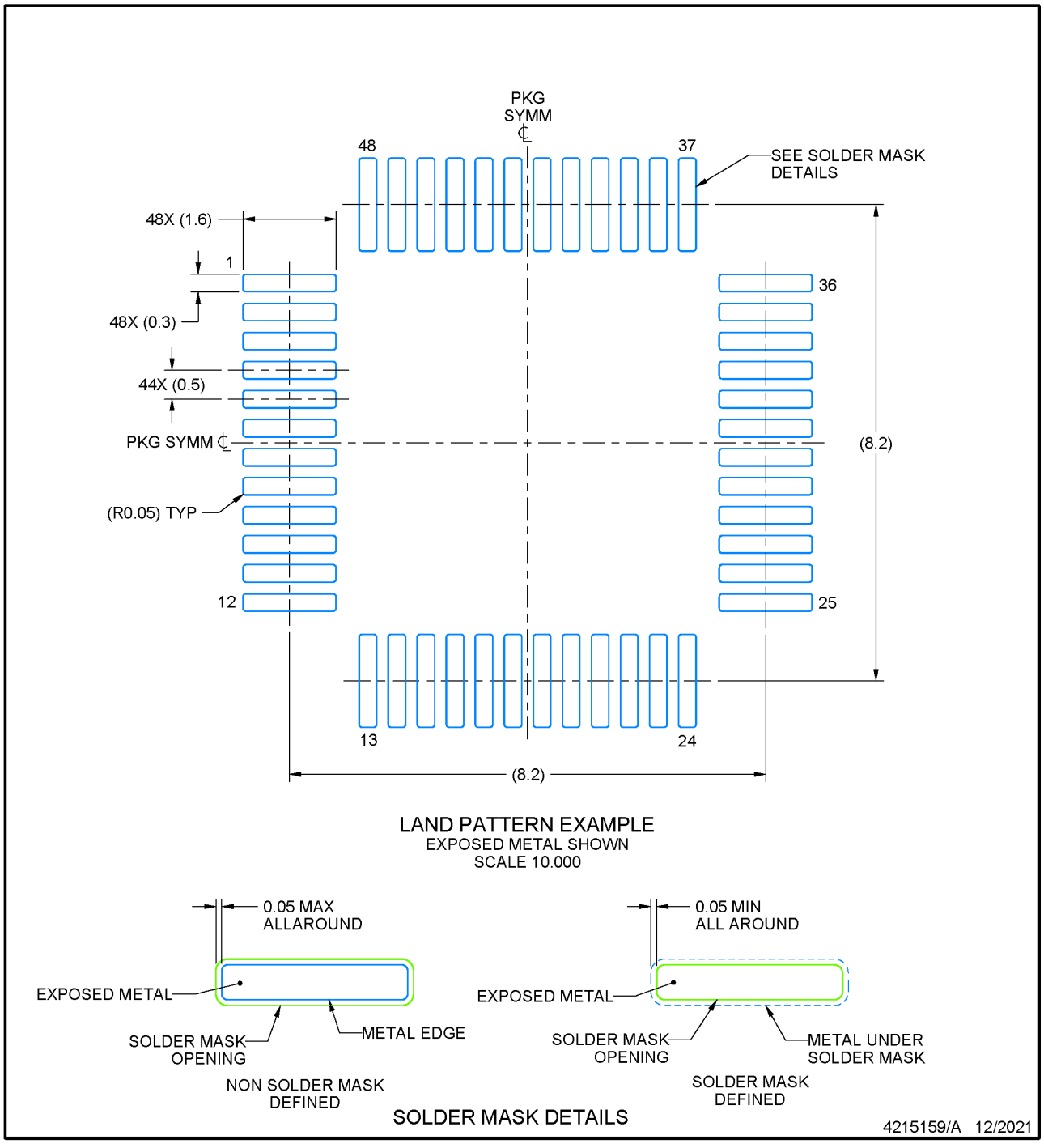
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EXAMPLE BOARD LAYOUT

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

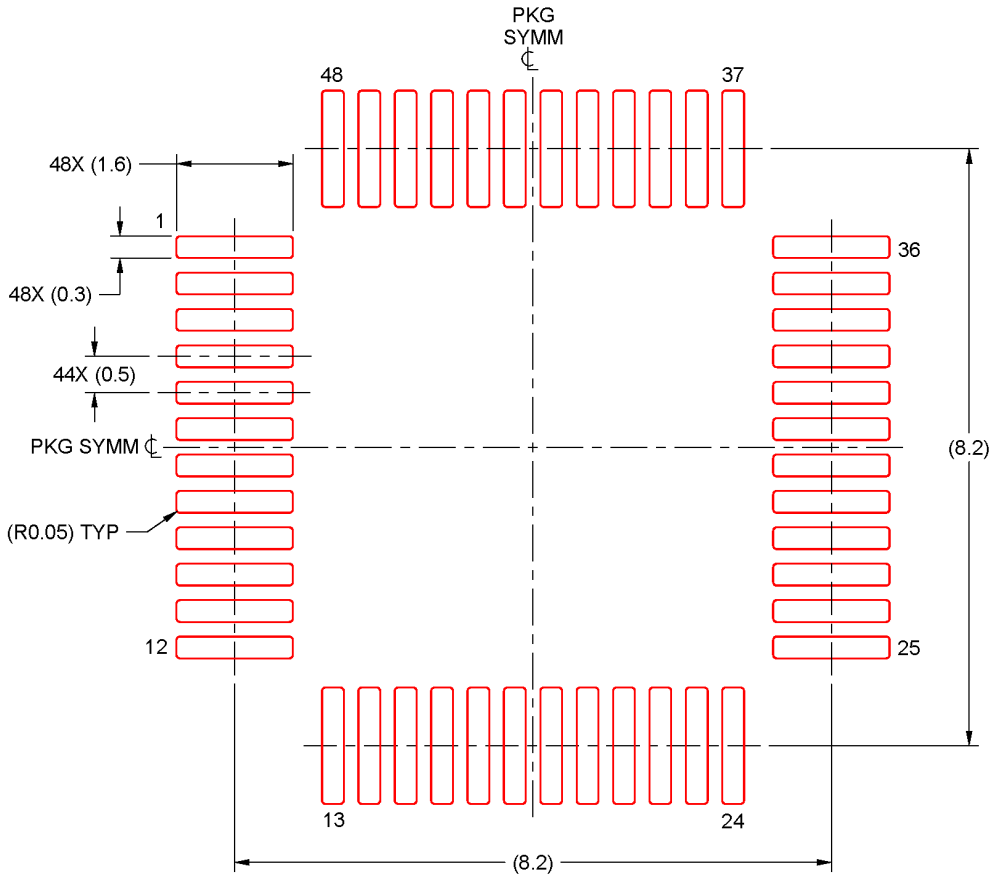
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EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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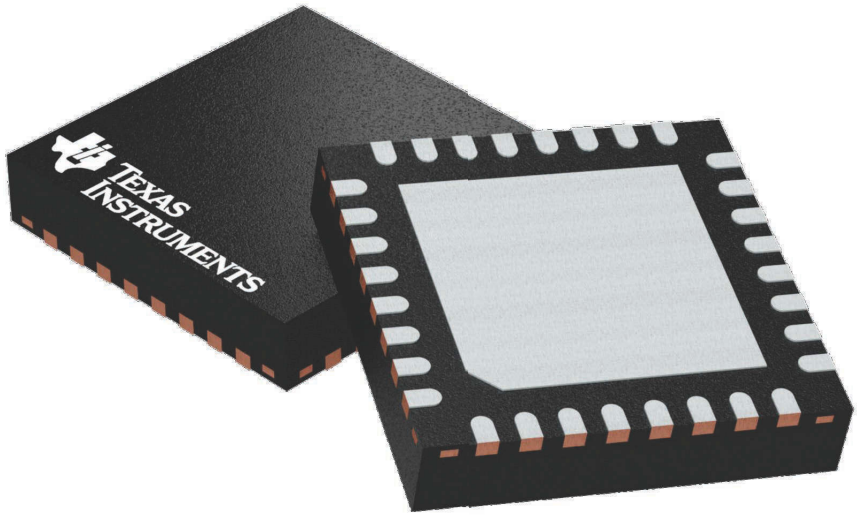
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

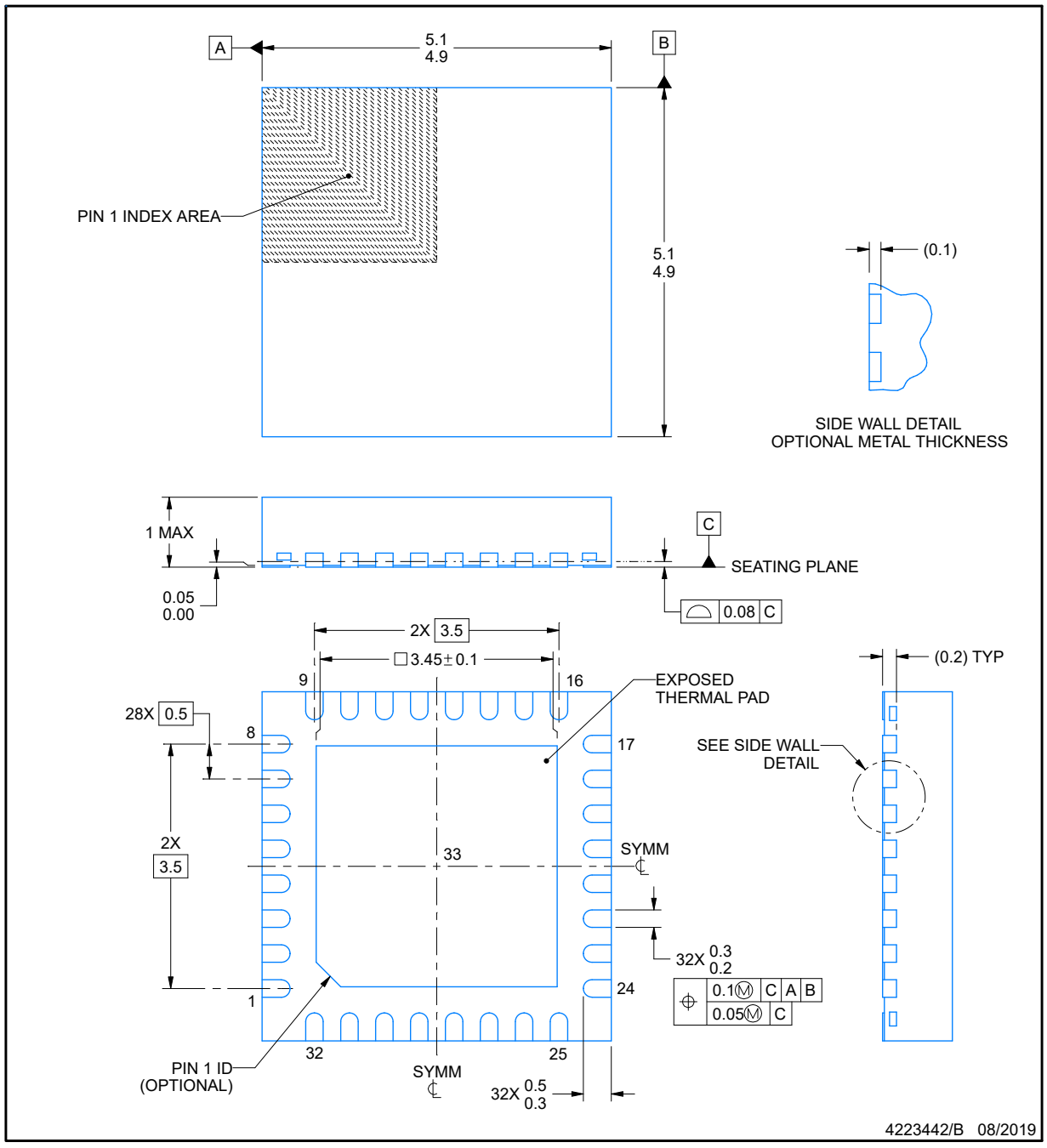
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PACKAGE OUTLINE

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

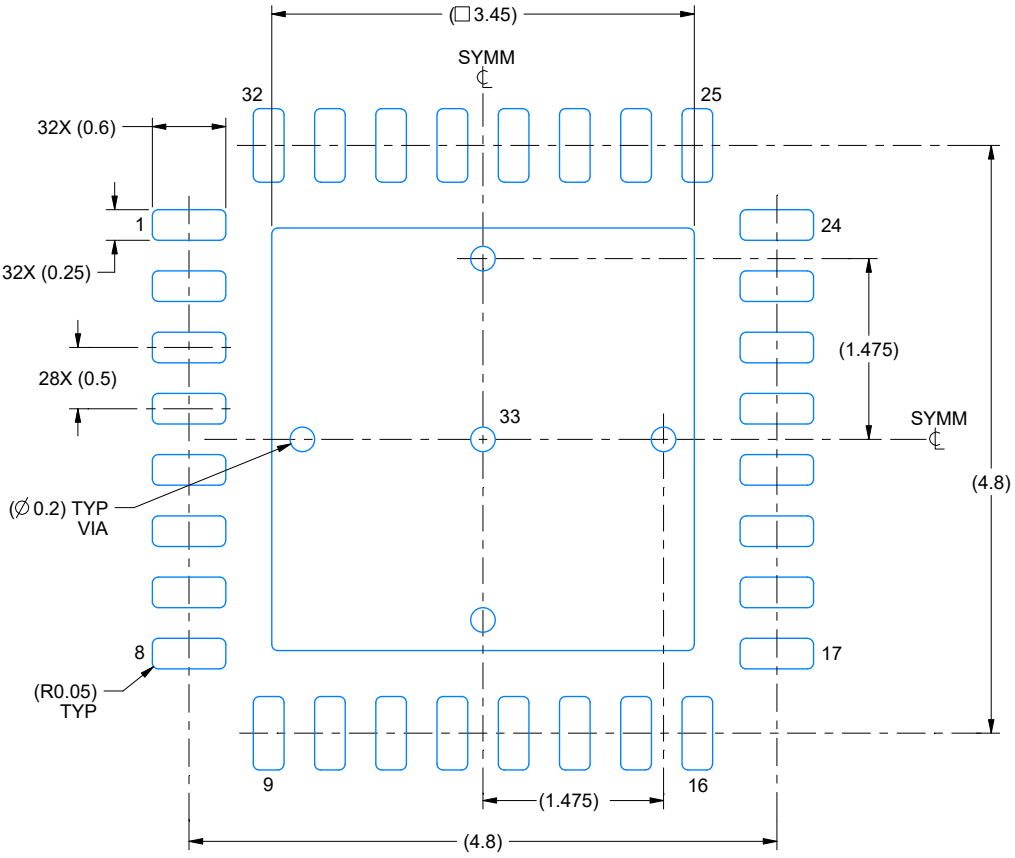
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EXAMPLE BOARD LAYOUT

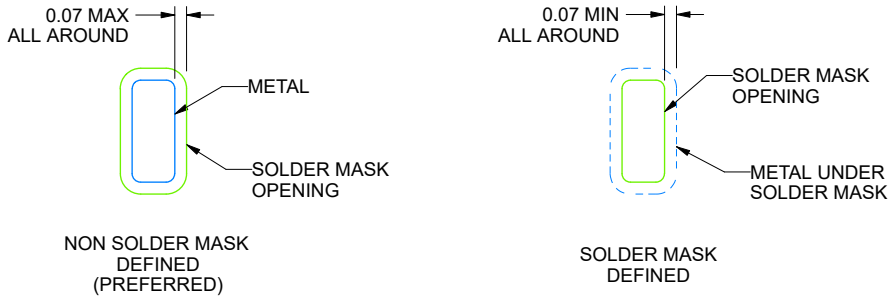
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

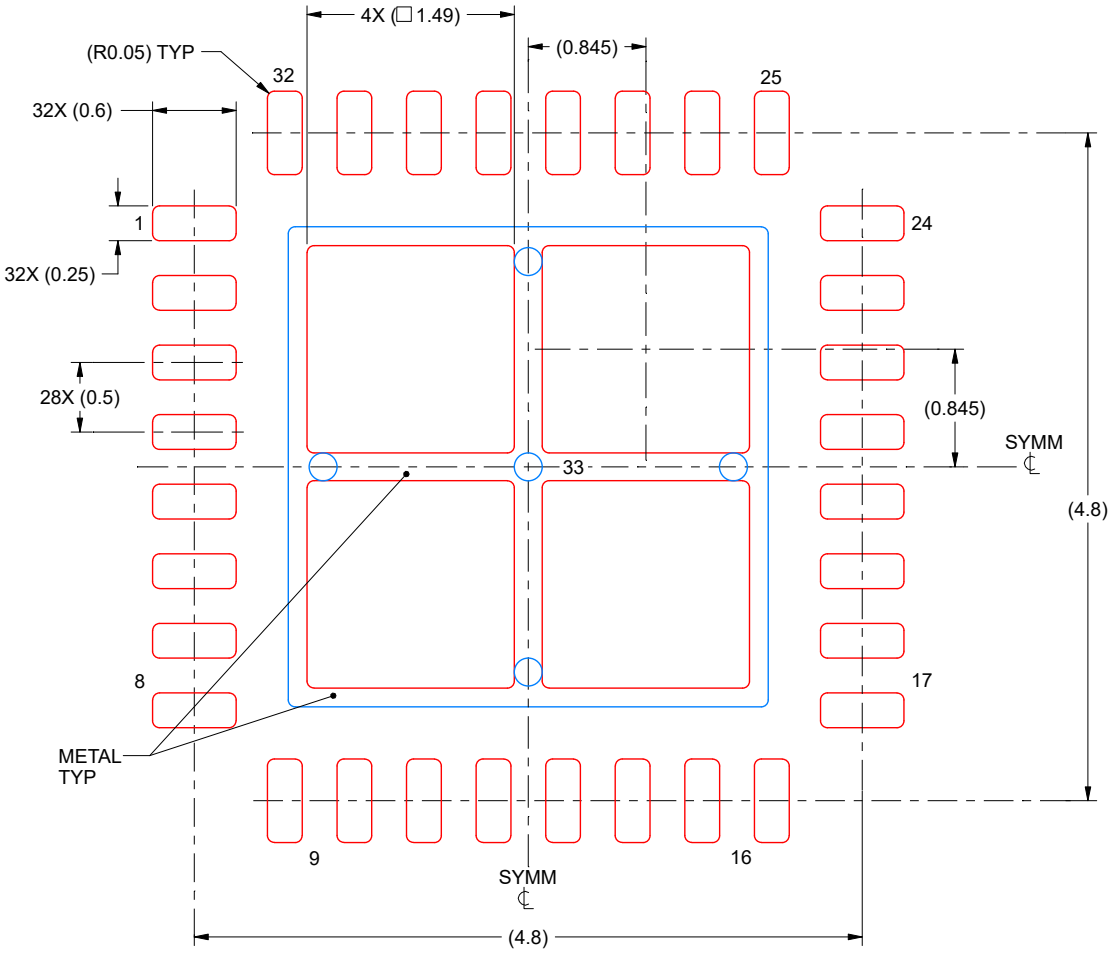
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EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

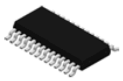
4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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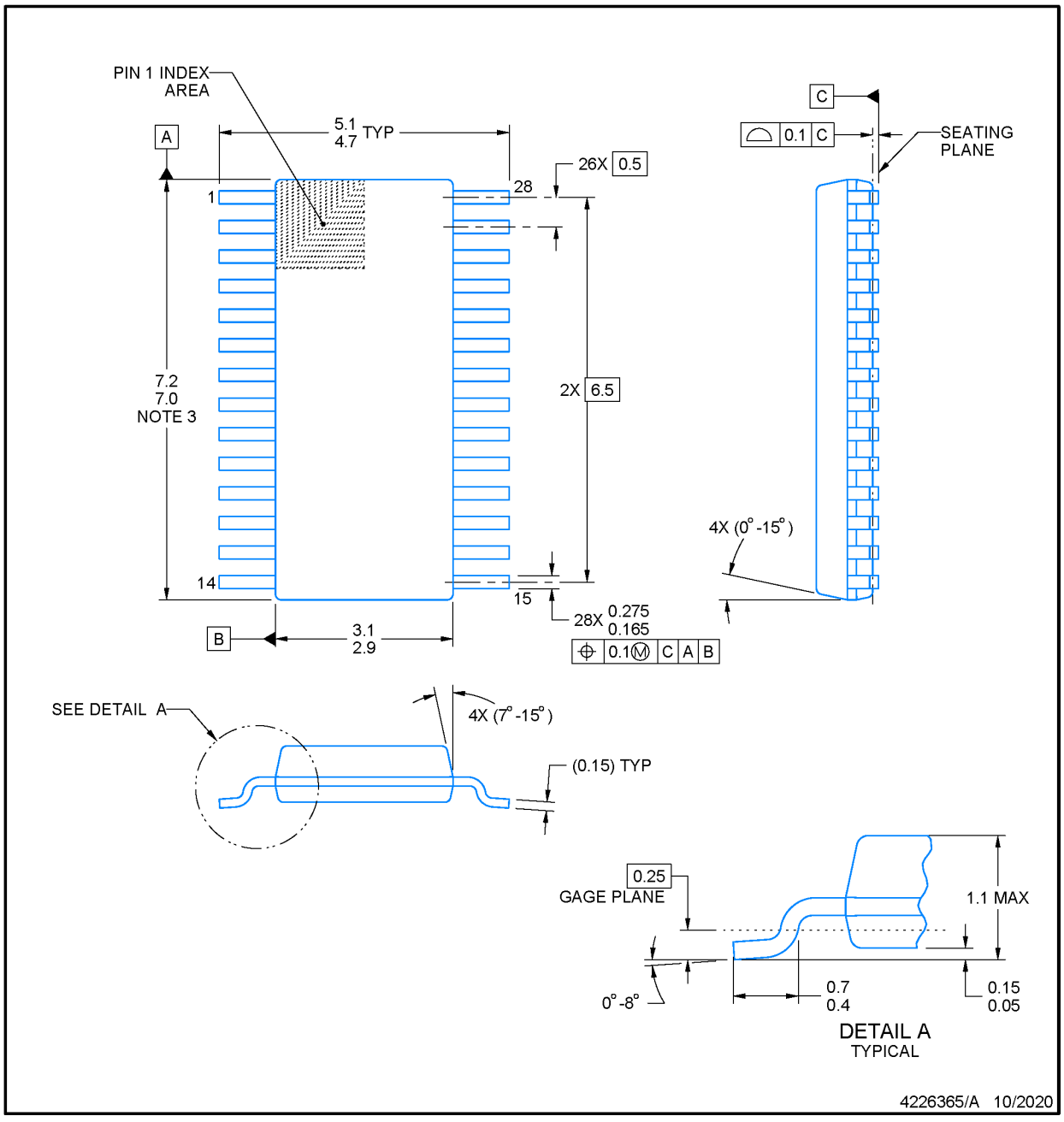
PACKAGE OUTLINE



DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

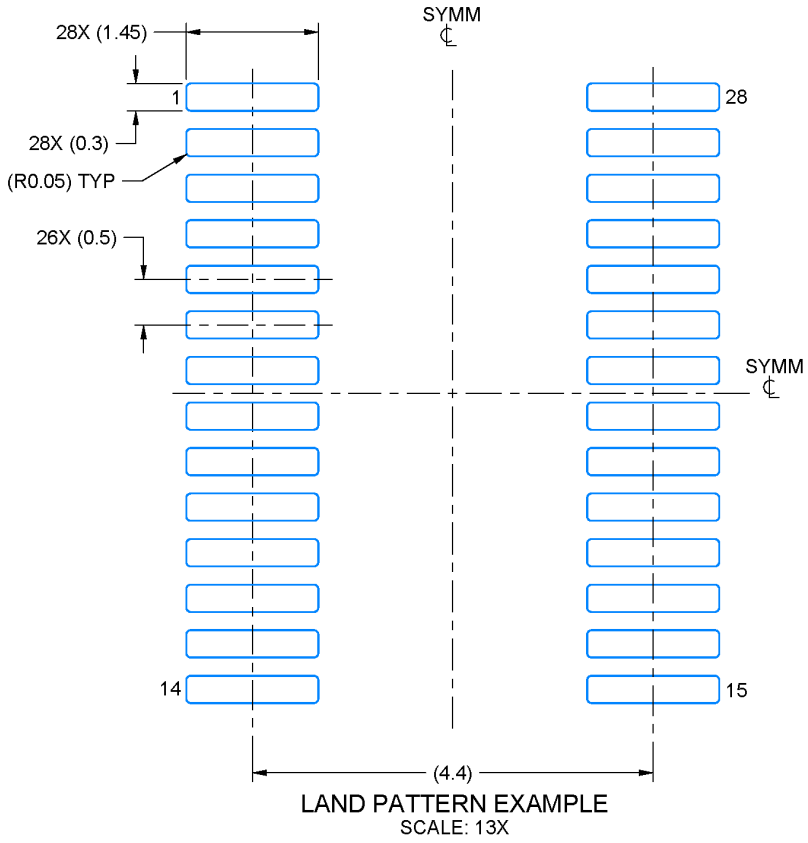
Copyright © 2026 Texas Instruments Incorporated

EXAMPLE BOARD LAYOUT

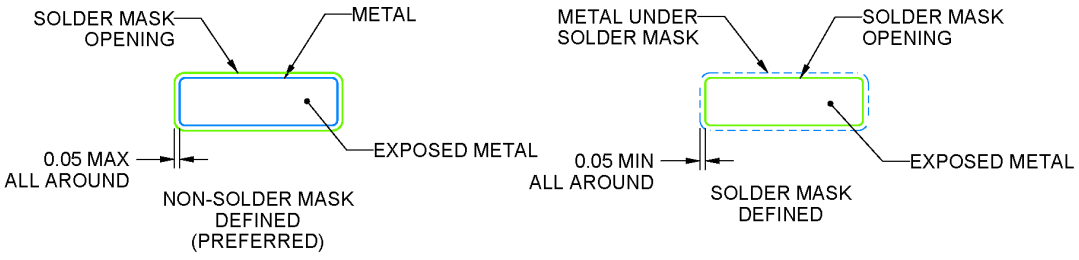
DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE: 13X



SOLDER MASK DETAILS

4226365/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

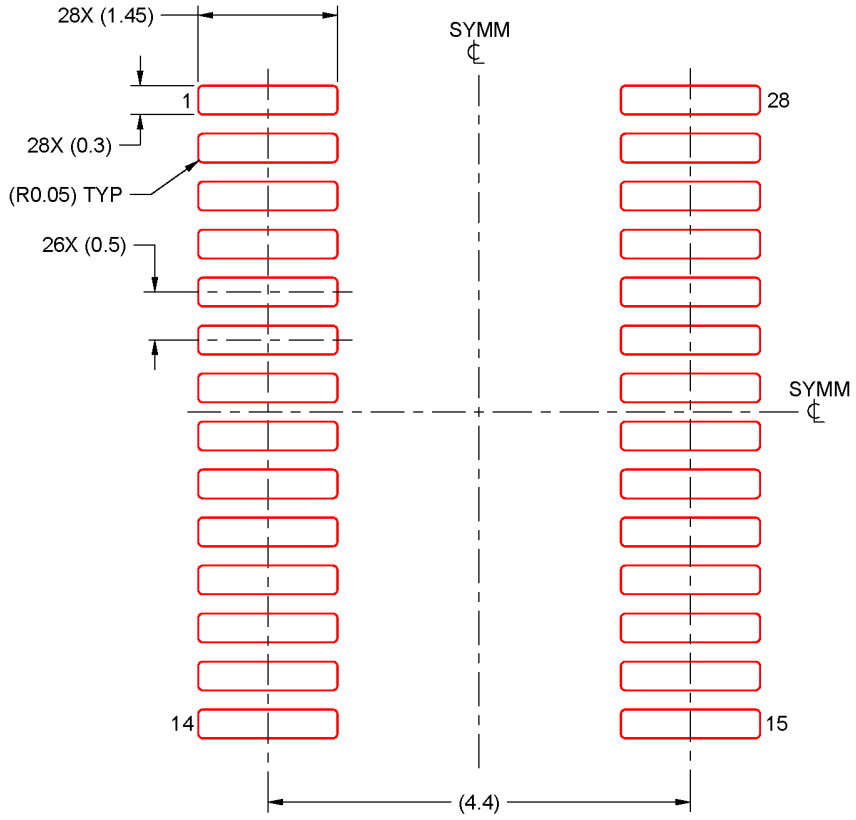
Copyright © 2026 Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 13X

4226365/A 10/2020

NOTES: (continued)

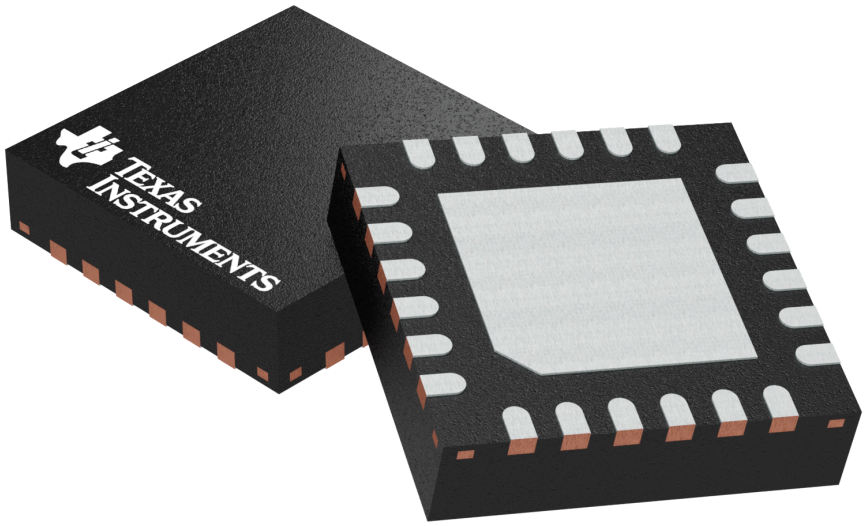
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

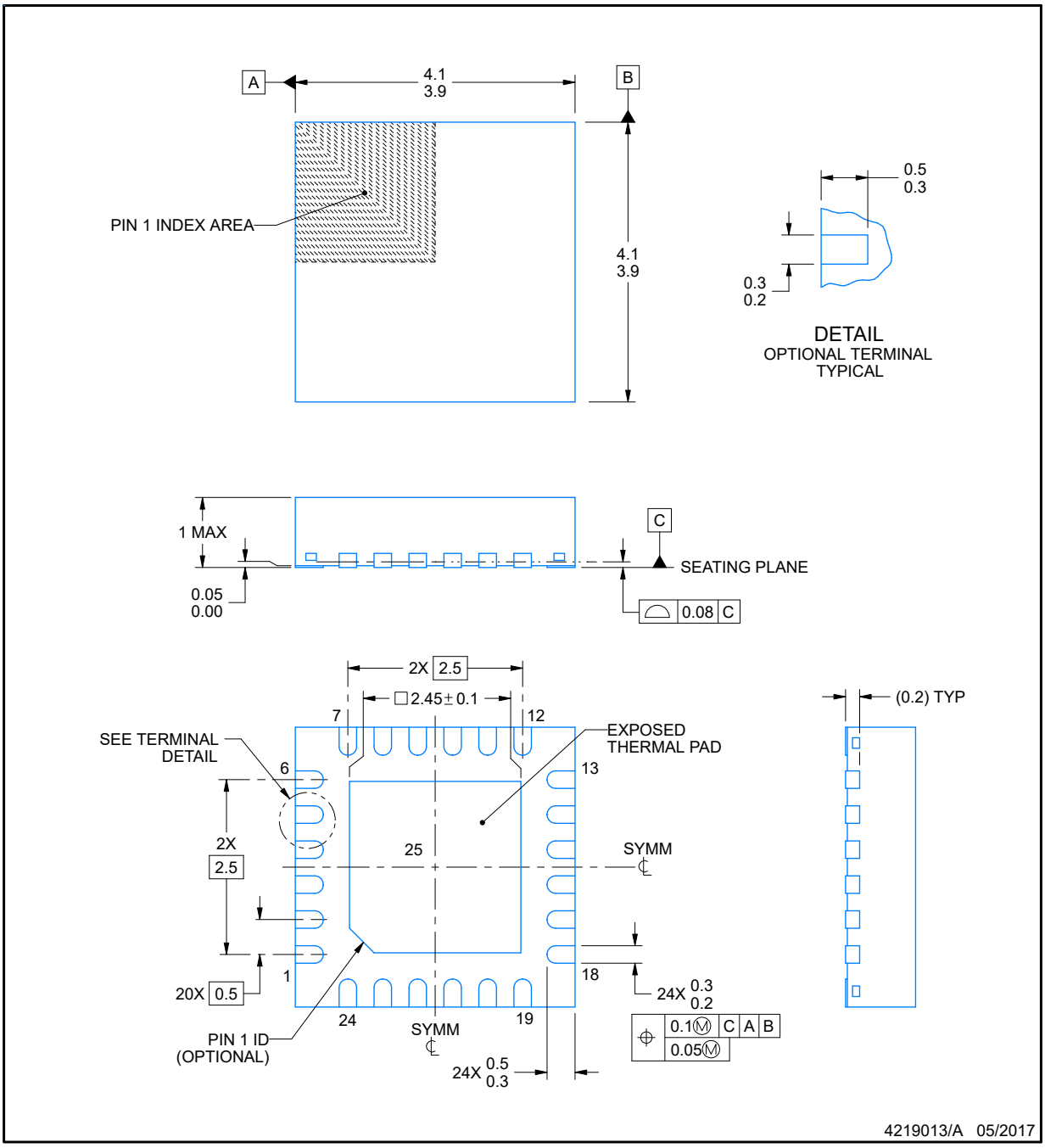
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PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

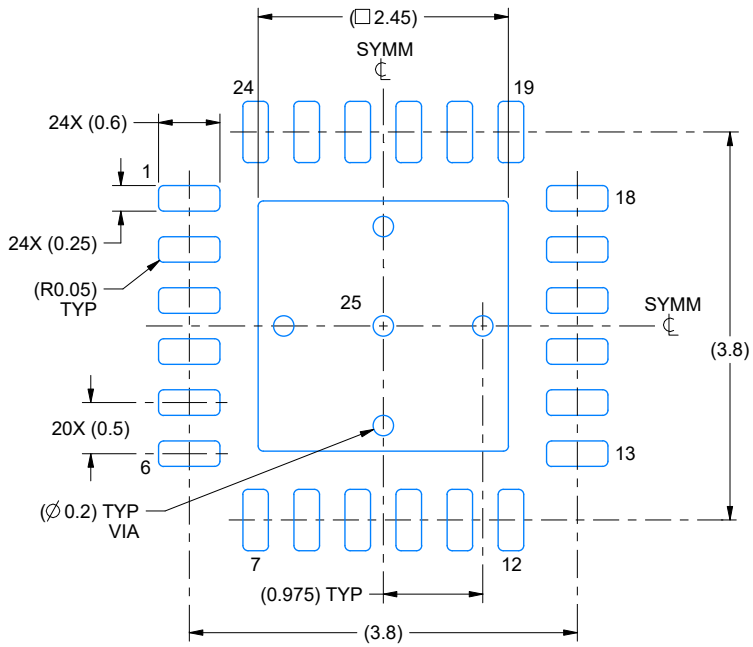
Copyright © 2026 Texas Instruments Incorporated

EXAMPLE BOARD LAYOUT

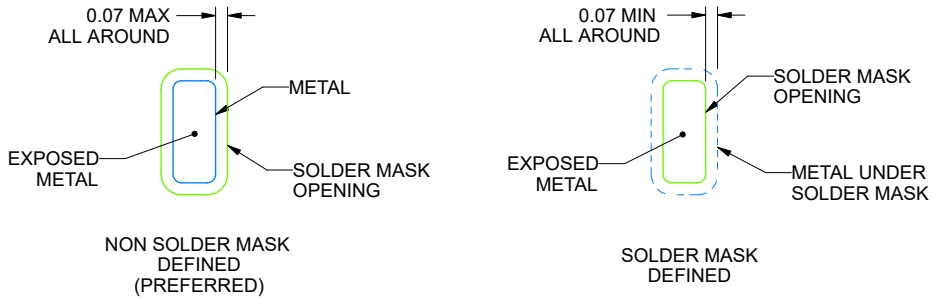
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

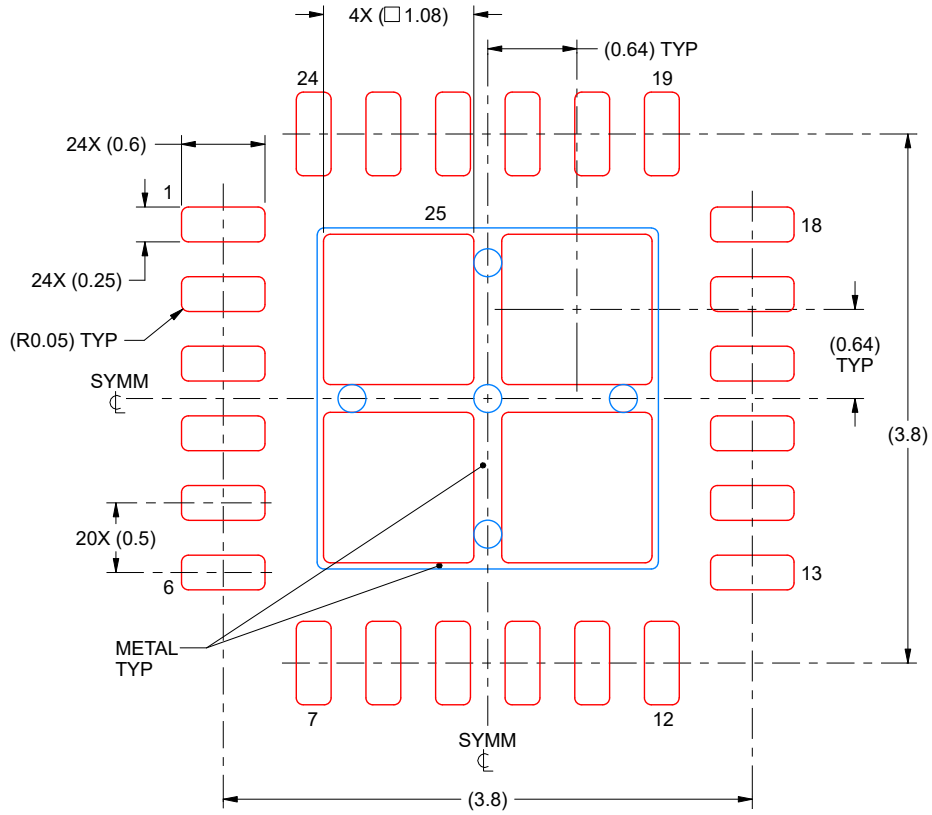
Copyright © 2026 Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

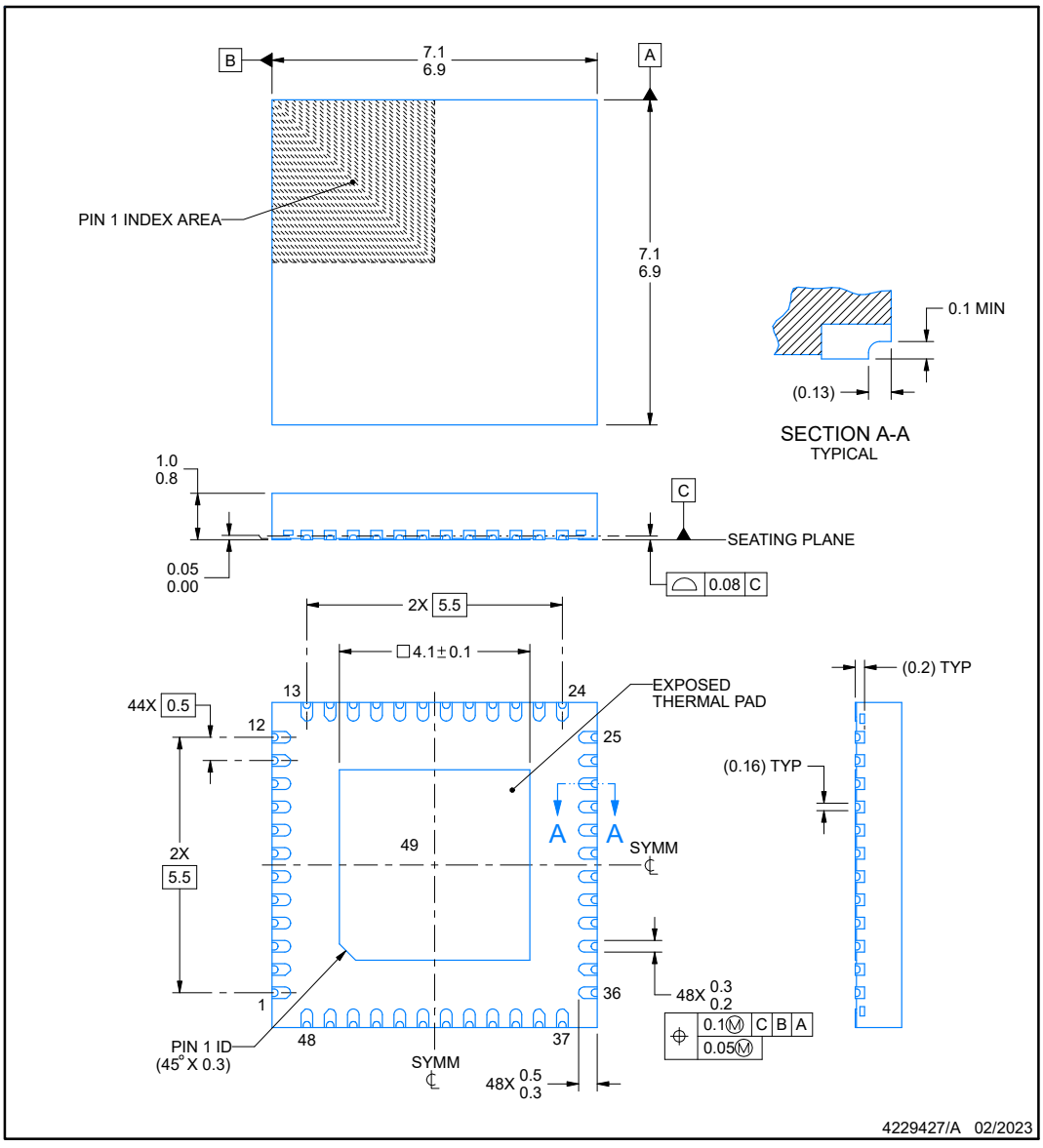
Copyright © 2026 Texas Instruments Incorporated

RGZ0048F

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

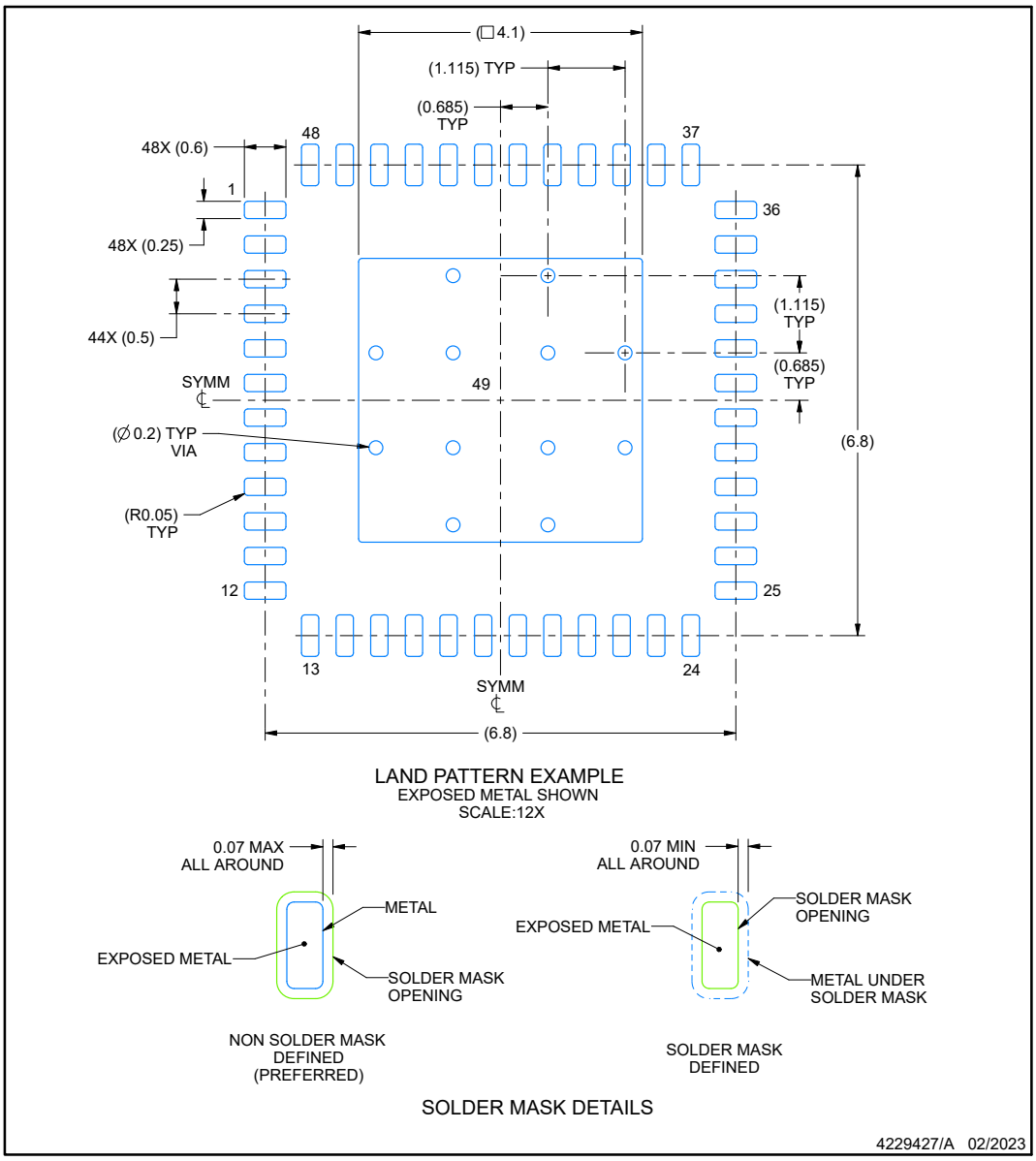
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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EXAMPLE BOARD LAYOUT

RGZ0048F — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

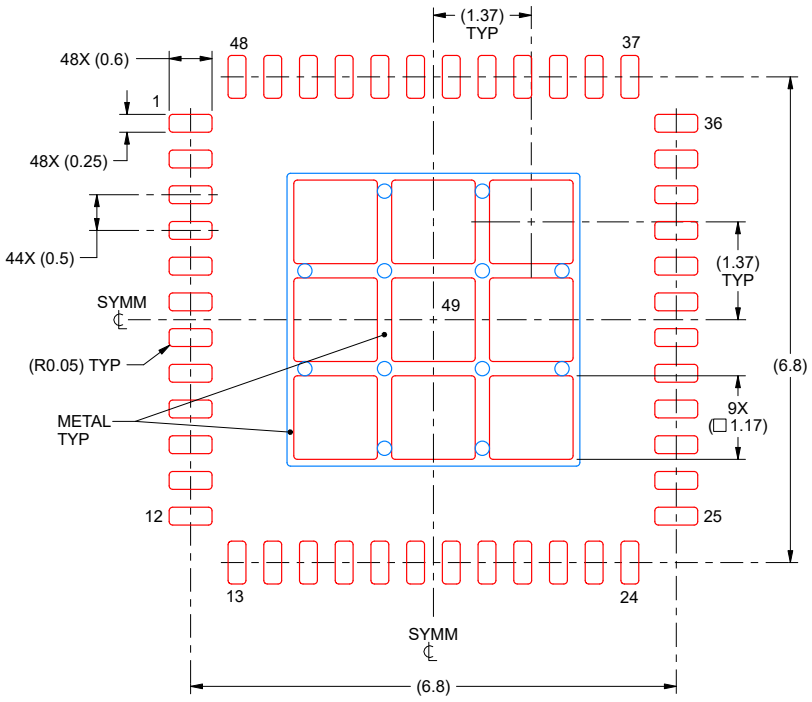
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

RGZ0048F — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4229427/A 02/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M0L1126QPMRQ1	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	M0L1126Q
M0L1126QPTRQ1	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	M0L1126Q
M0L1126QRGERQ1	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	MSPM0 L1126Q
M0L1126QRGZRQ1	Active	Production	VQFN (RGZ) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	MSPM0 L1126Q
M0L1126QRHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	MSPM0 L1126Q
M0L1127QPMRQ1	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	M0L1127Q
M0L1127QPTRQ1	Active	Production	LQFP (PT) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	M0L1127Q
M0L1127QRGERQ1	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	MSPM0 L1127Q
M0L1127QRGZRQ1	Active	Production	VQFN (RGZ) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	MSPM0 L1127Q
M0L1127QRHBRQ1	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	MSPM0 L1127Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSPM0L1126-Q1, MSPM0L1127-Q1 :

- Catalog : MSPM0L1126, MSPM0L1127

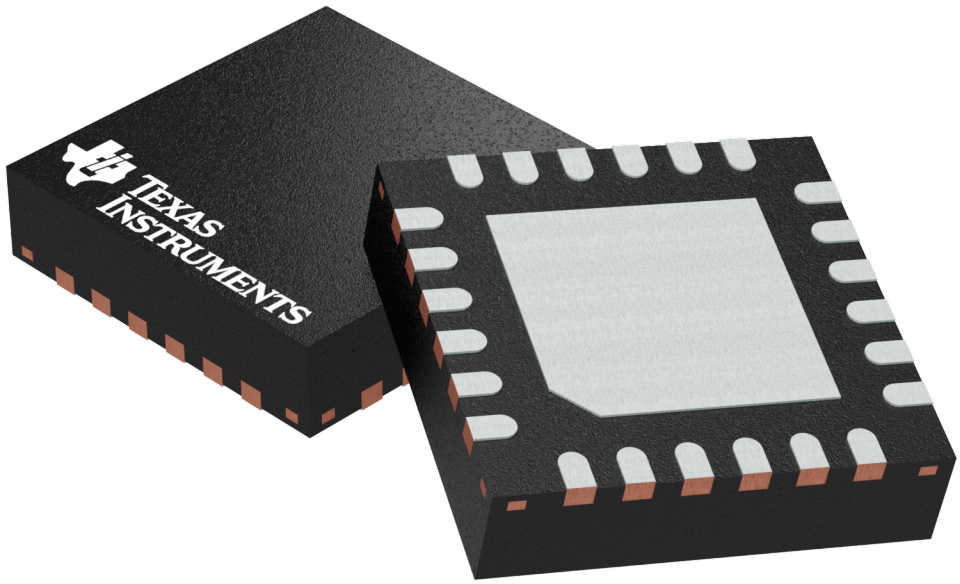
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

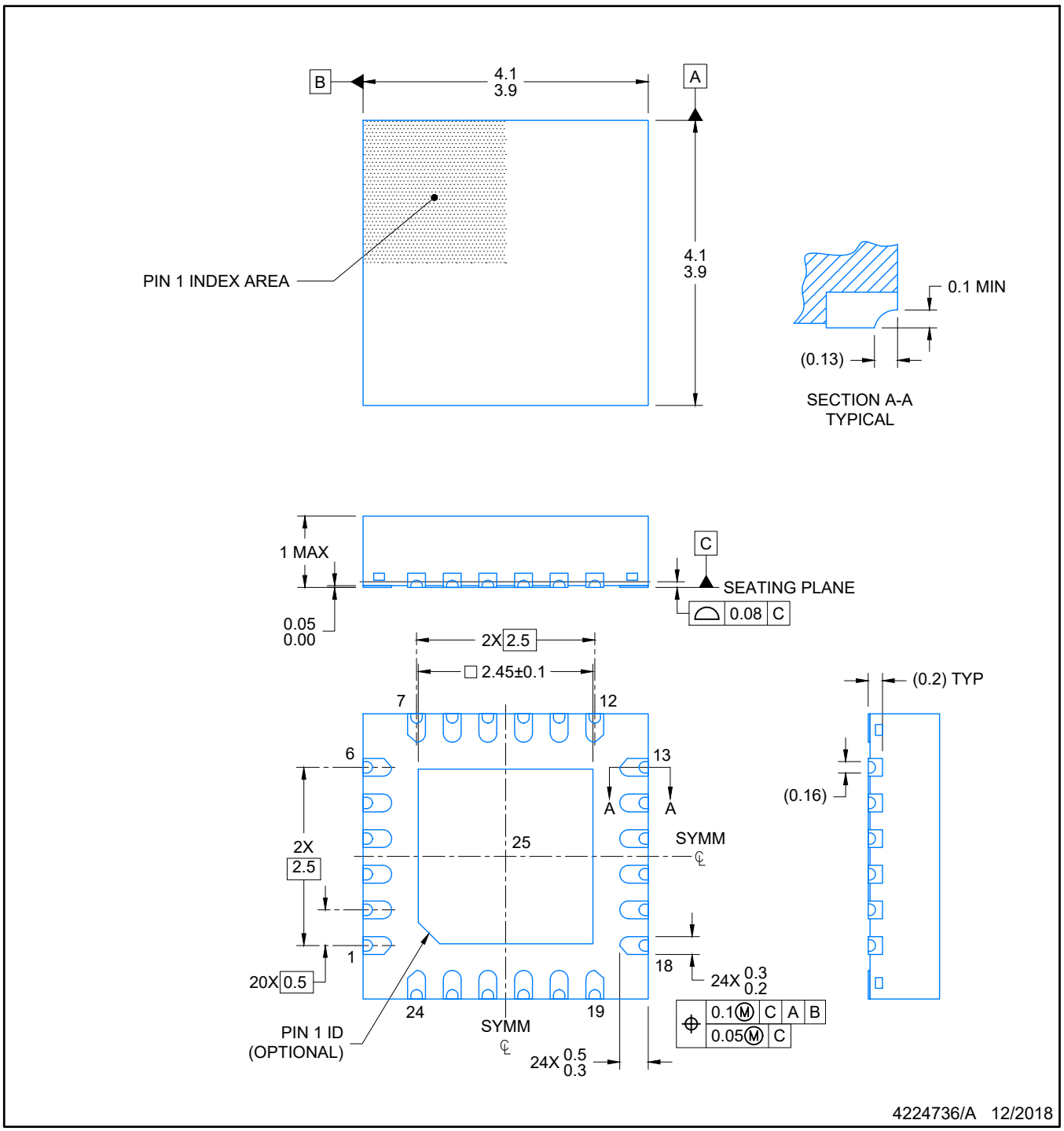
RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



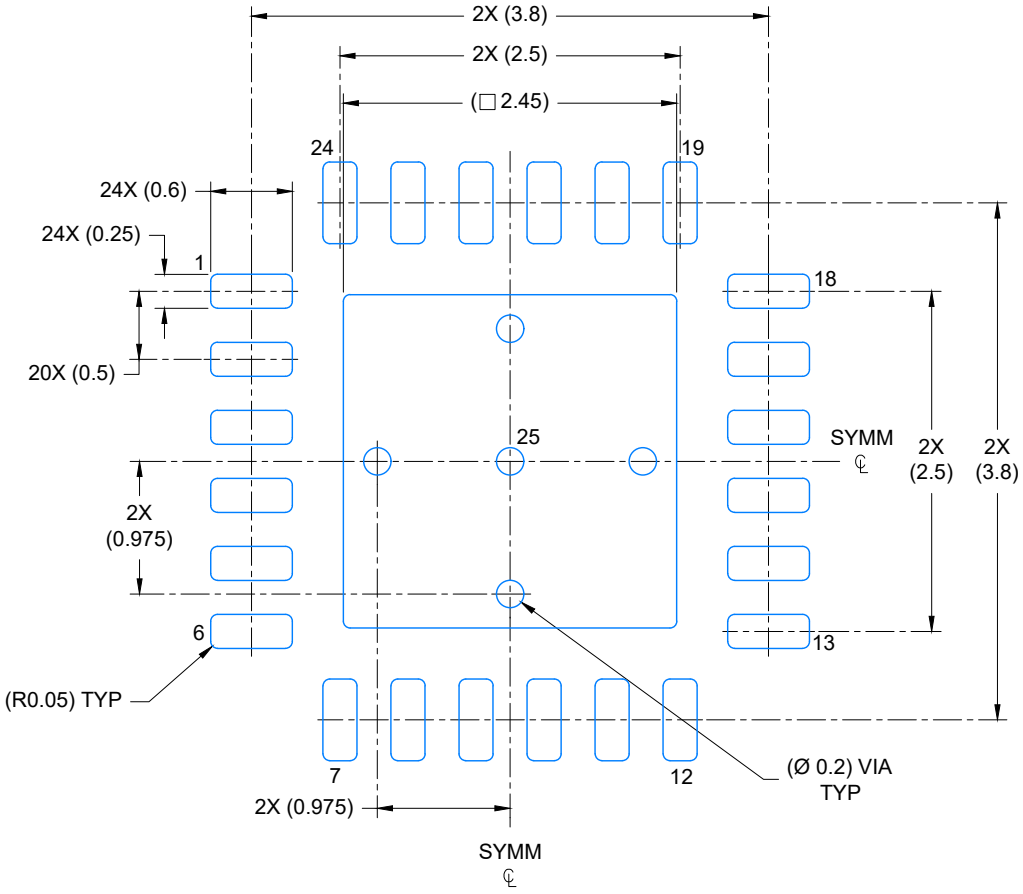
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

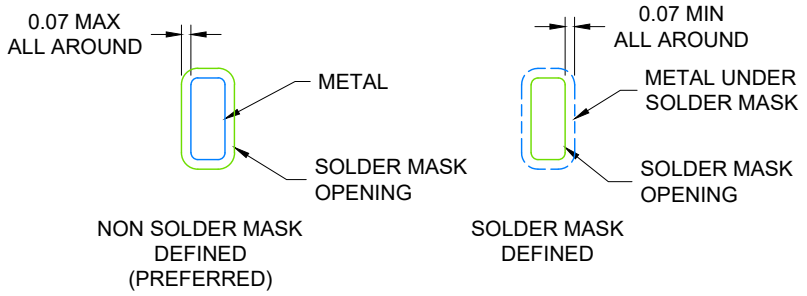


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

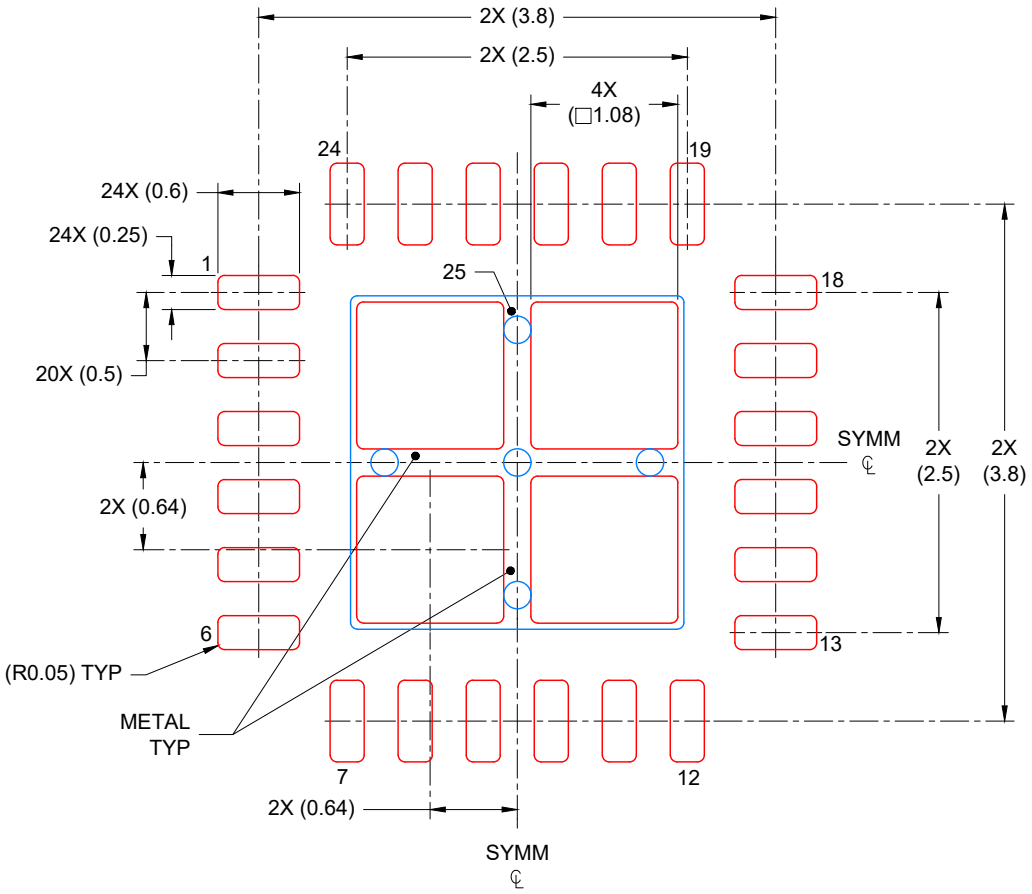


SOLDER MASK DETAILS

4224736/A 12/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 18X

4224736/A 12/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

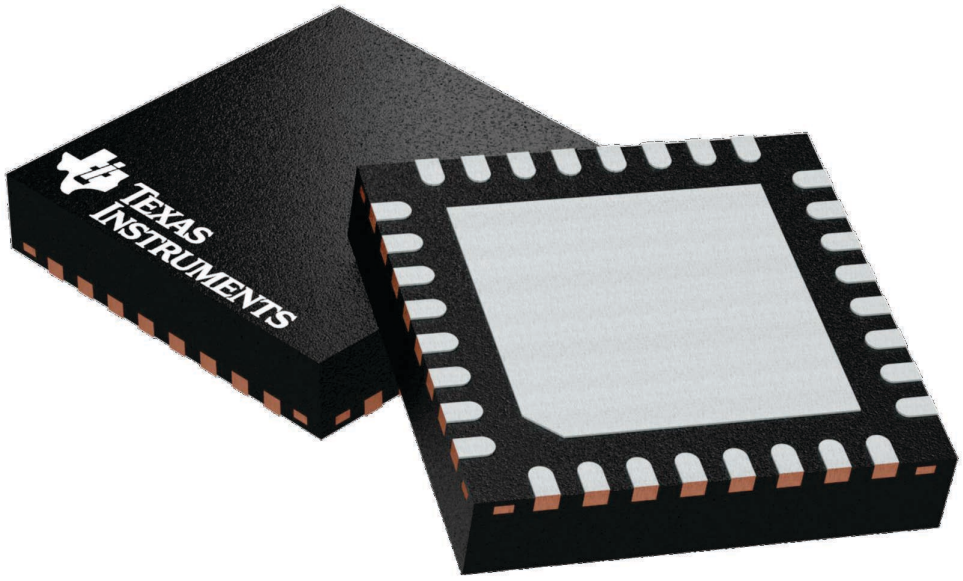
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

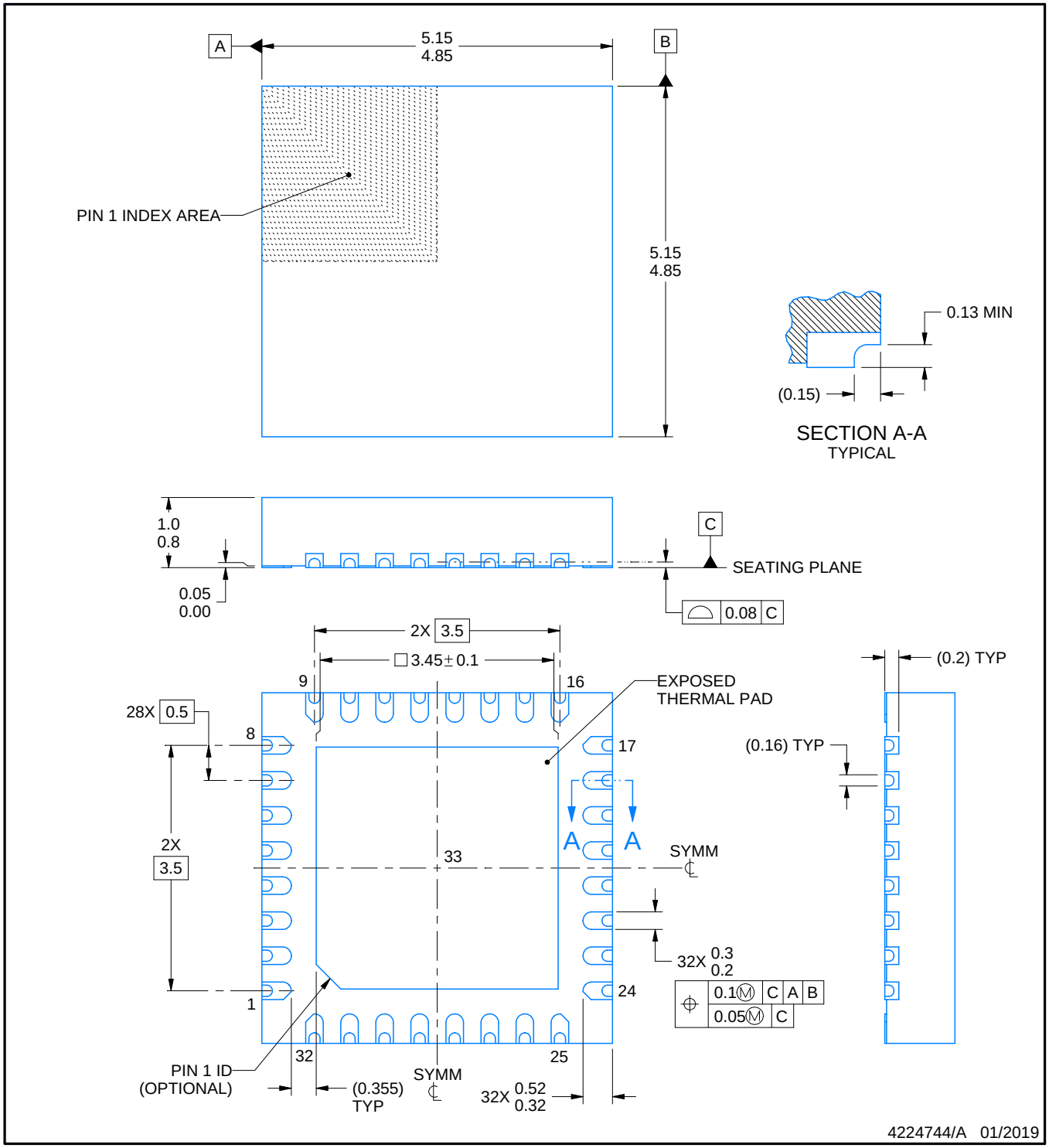
4224745/A

RHB0032T

PACKAGE OUTLINE

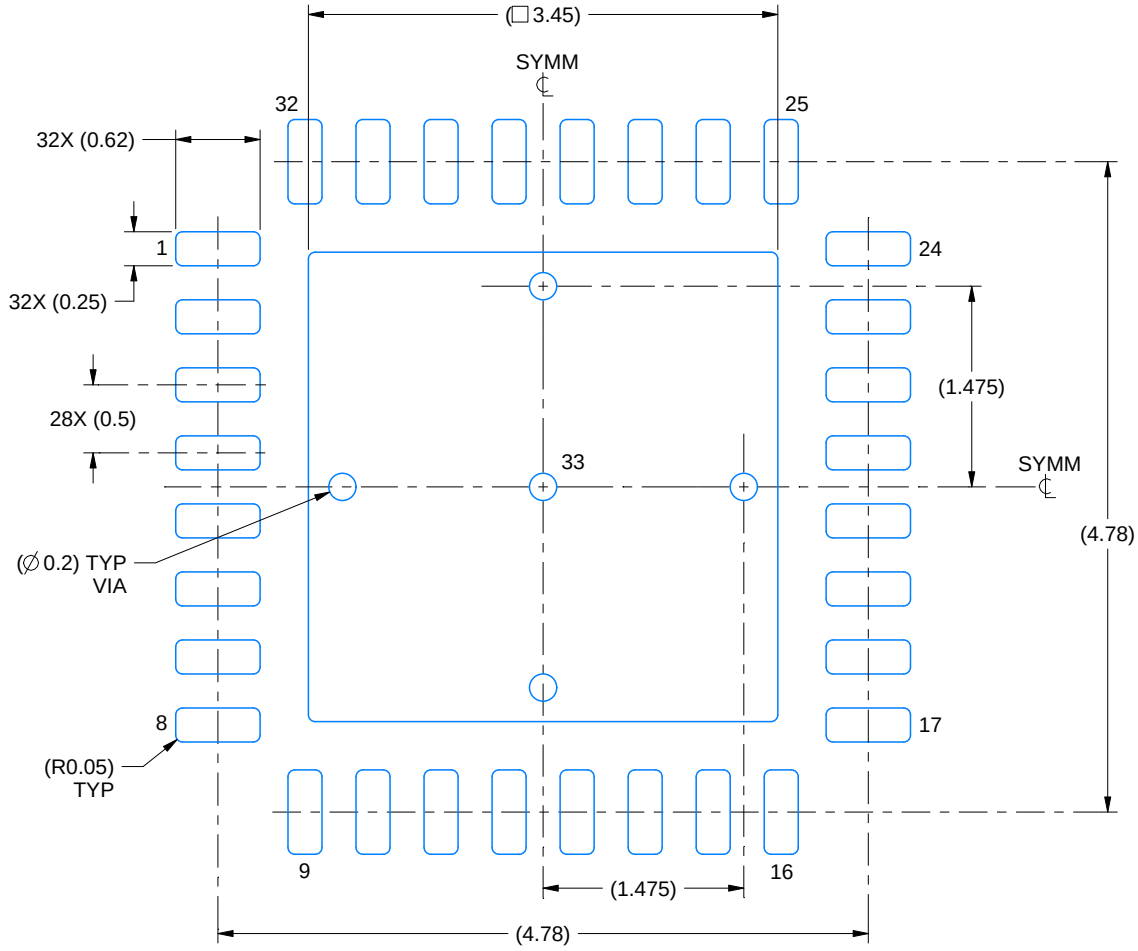
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

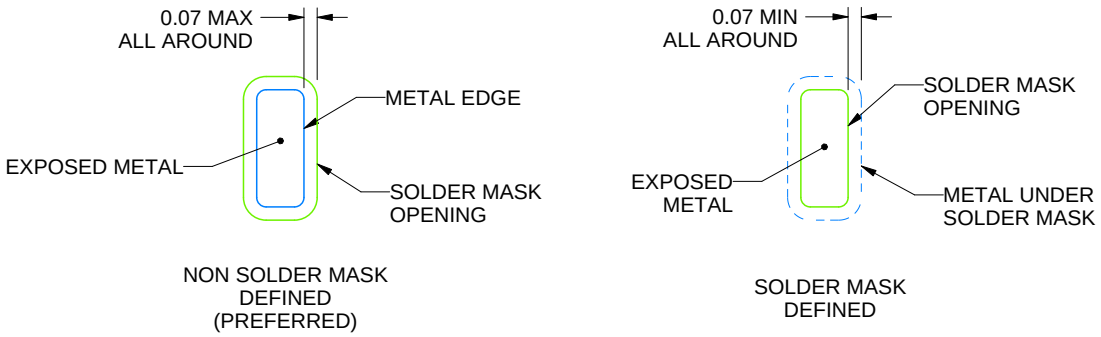
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE:18X

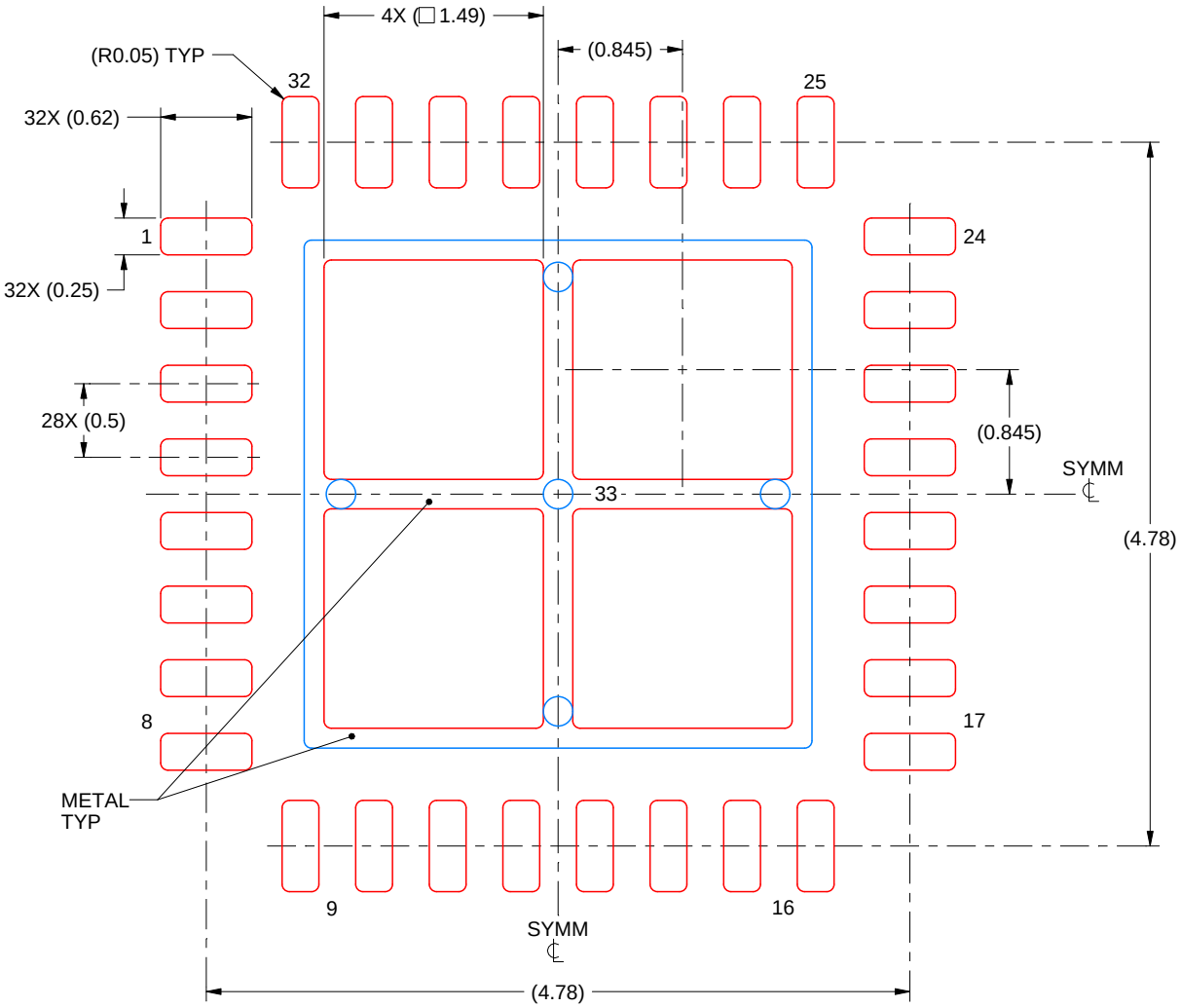


SOLDER MASK DETAILS

4224744/A 01/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4224744/A 01/2019

NOTES: (continued)

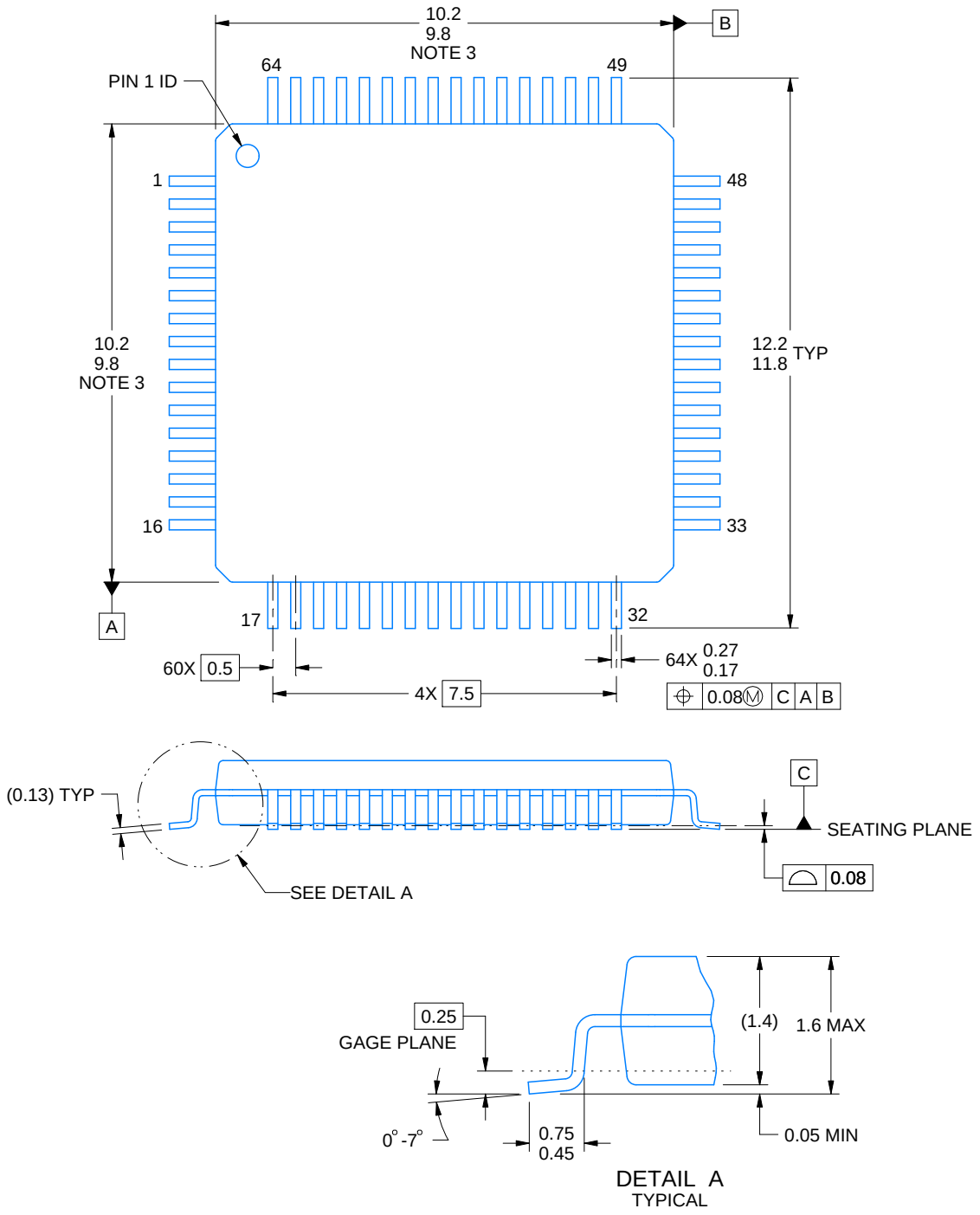
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

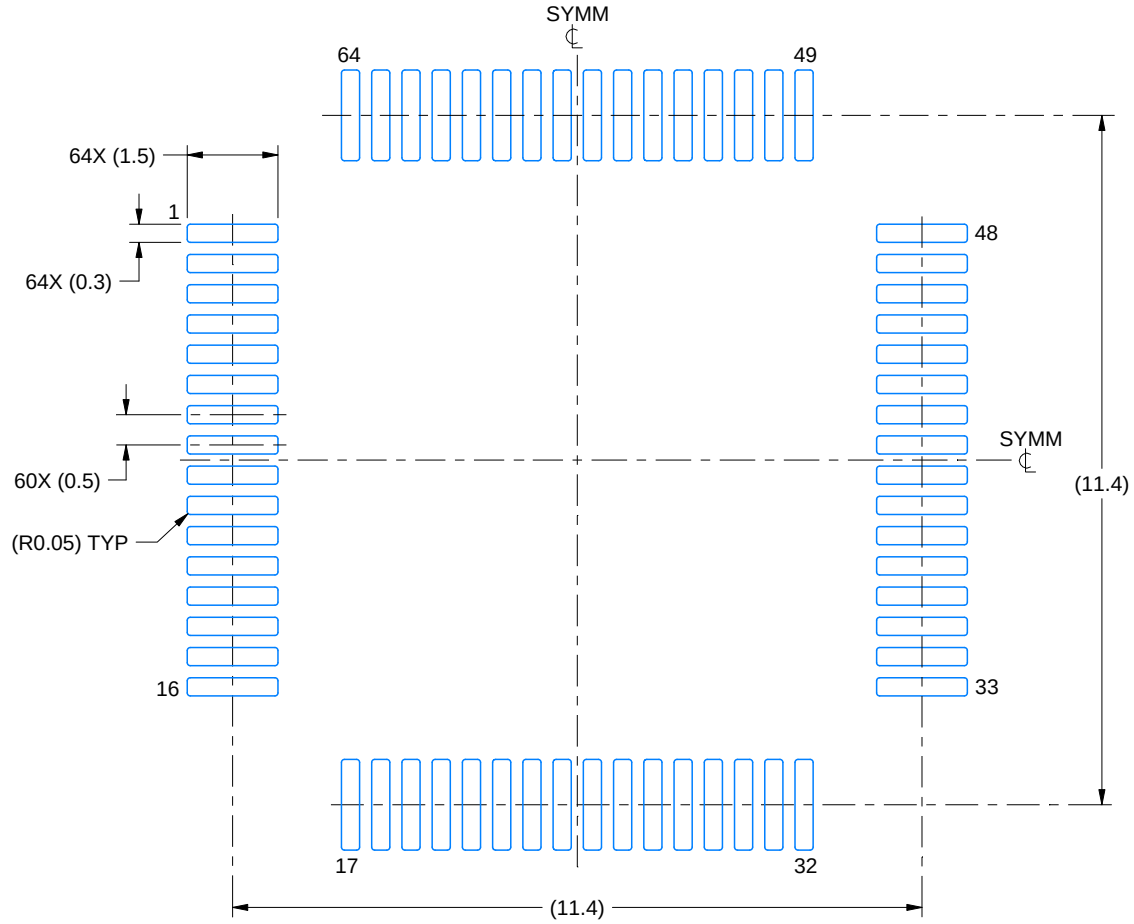
PLASTIC QUAD FLATPACK



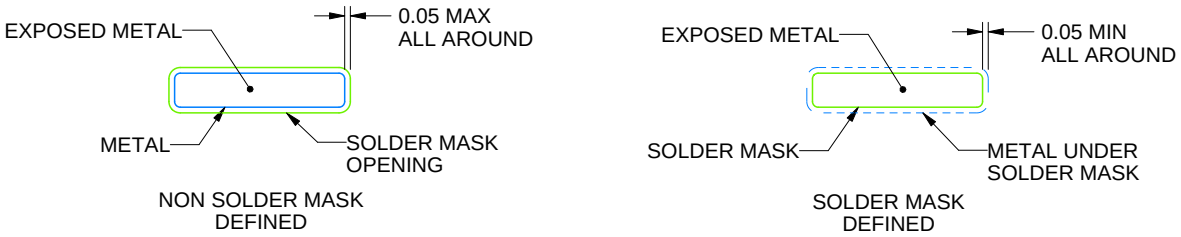
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

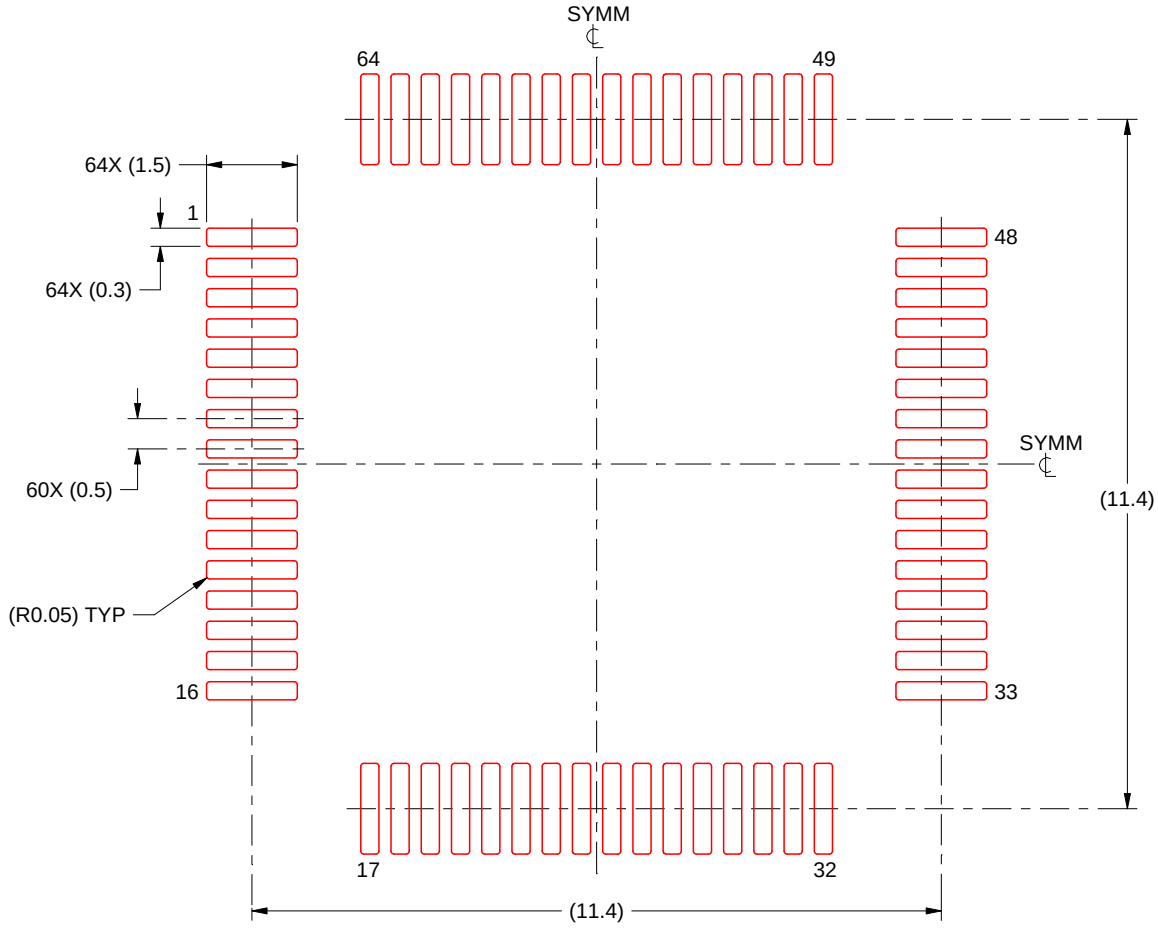


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

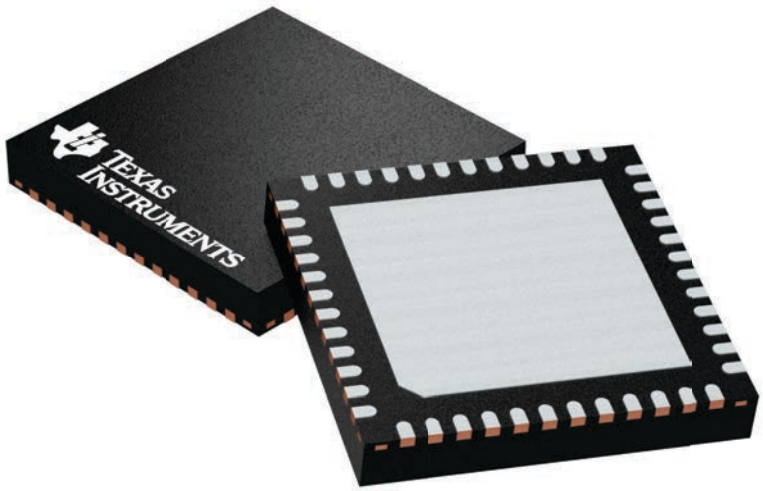
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

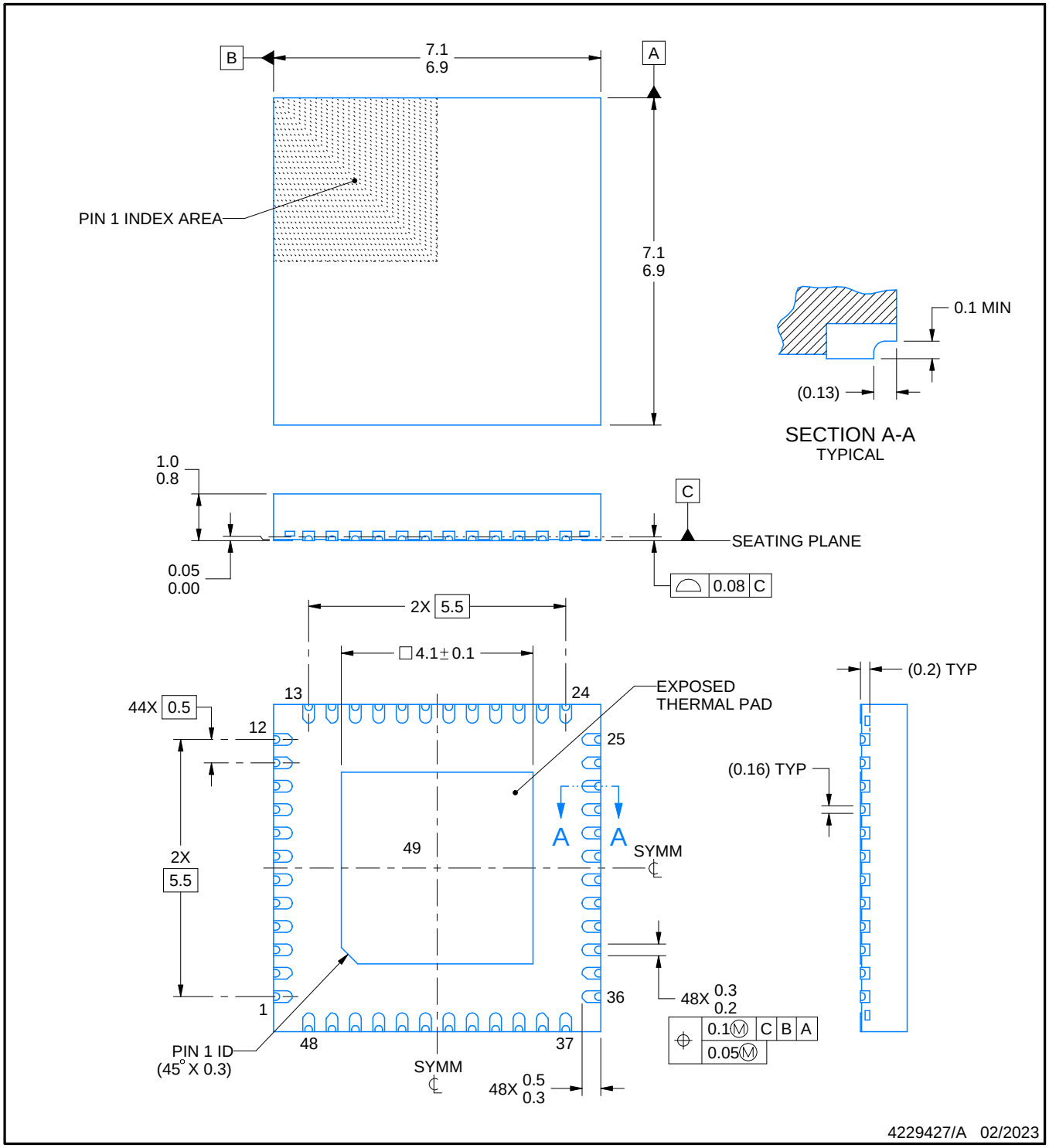
4224671/A

RGZ0048F

PACKAGE OUTLINE

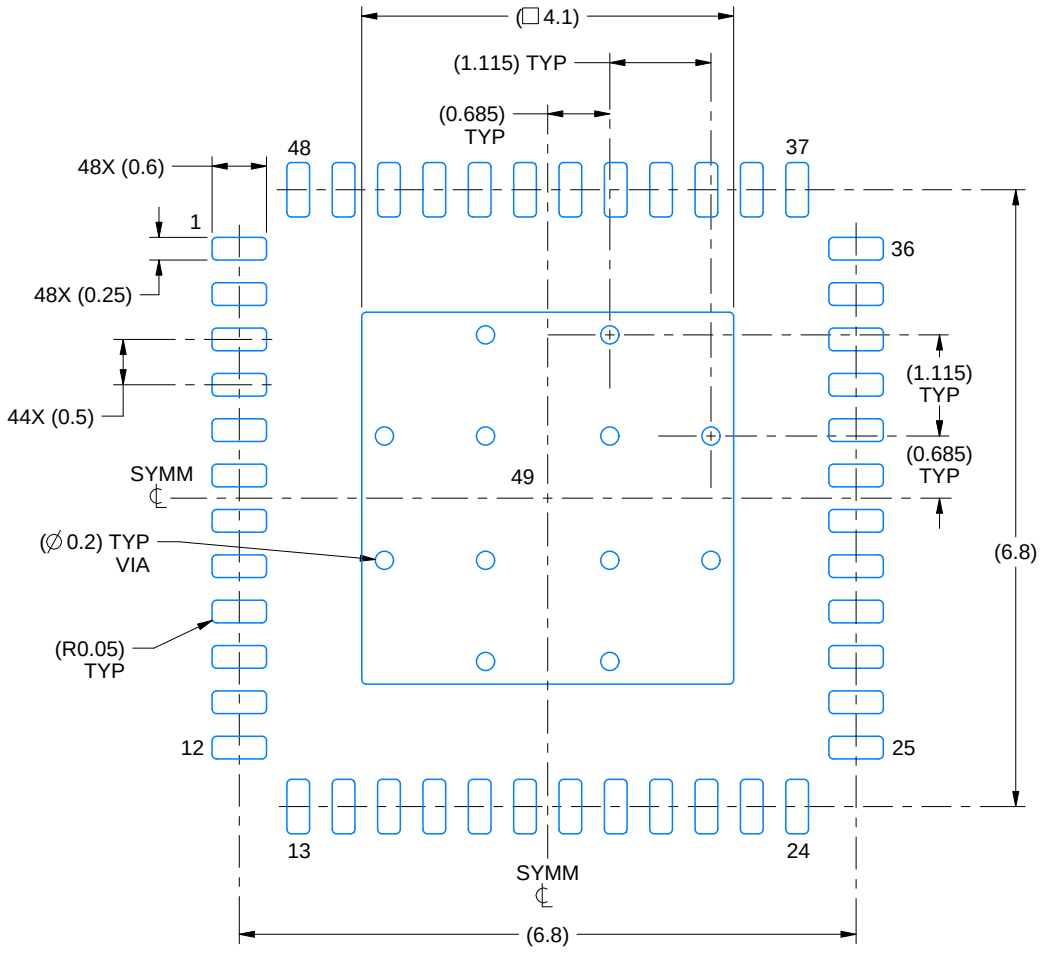
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

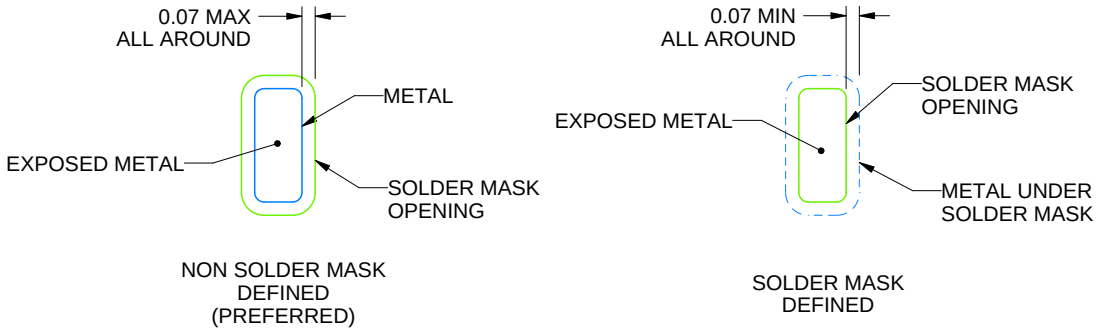


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

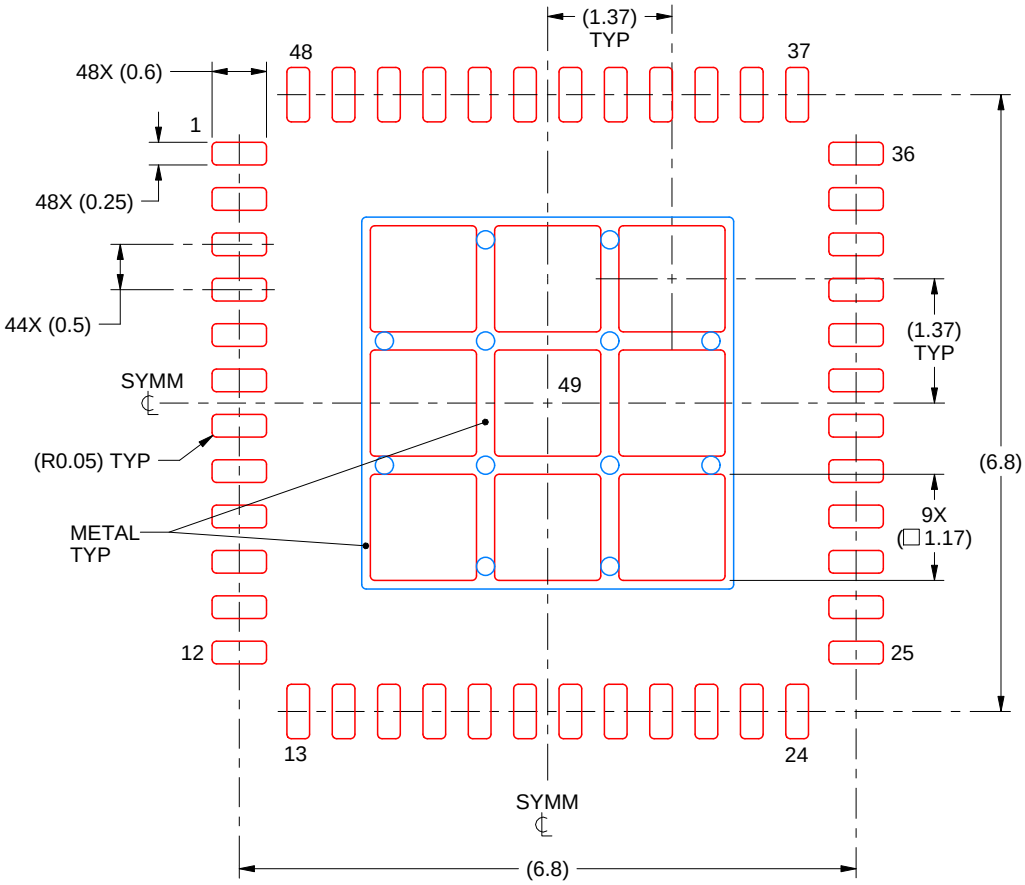


SOLDER MASK DETAILS

4229427/A 02/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4229427/A 02/2023

NOTES: (continued)

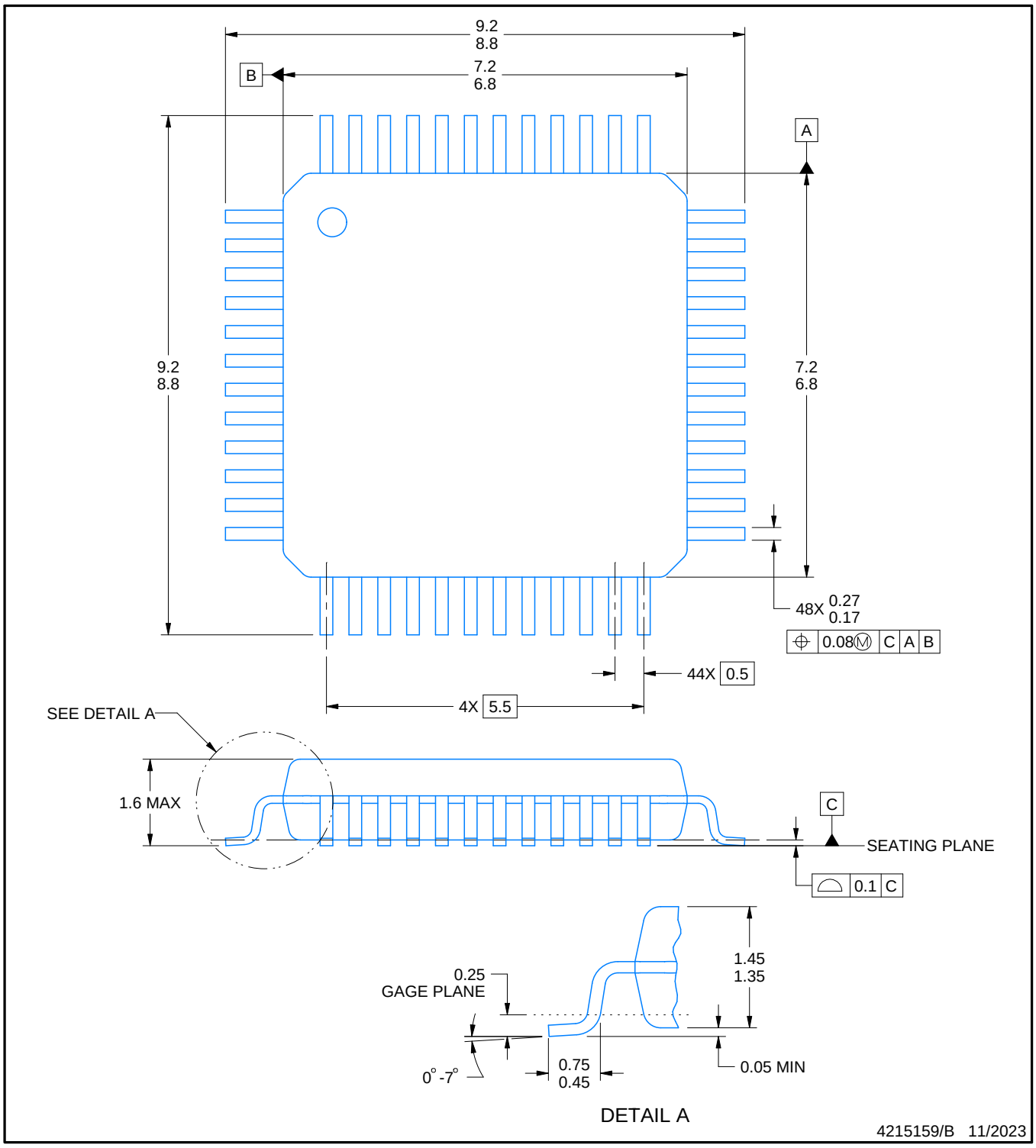
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PT0048A

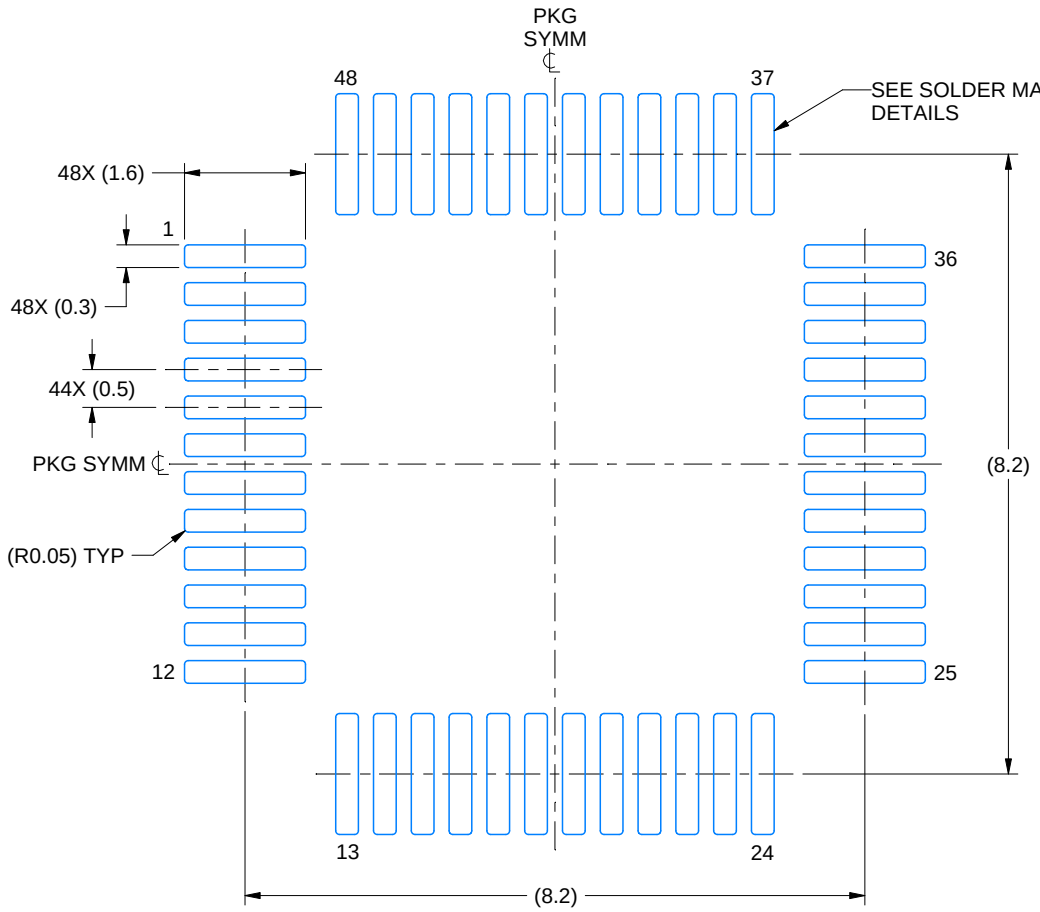
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

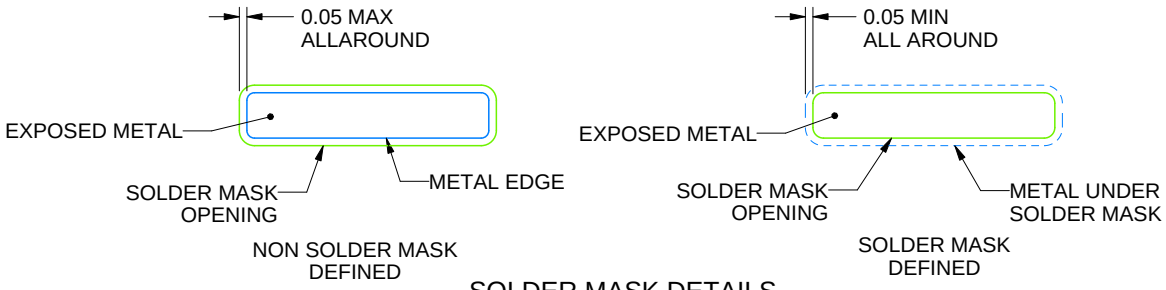


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000

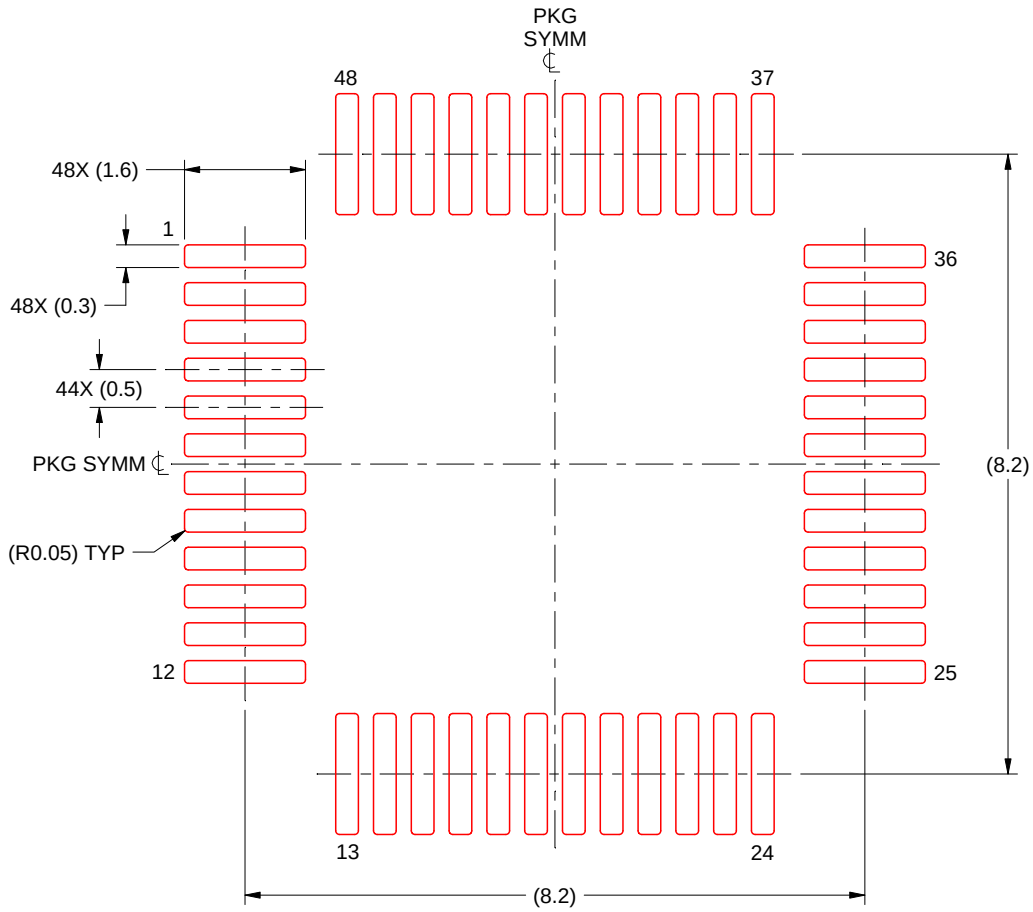


SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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