# MIXED SIGNAL MICROCONTROLLER

## FEATURES

- **Low Supply Voltage Range: 1.8 V to 3.6 V**
- **Ultra-Low Power Consumption**
  - **Active Mode: 220 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.5 µA**
  - **Off Mode (RAM Retention): 0.1 µA**
- **Five Power-Saving Modes**
- **Ultra-Fast Wake-Up From Standby Mode in Less Than 1 µs**
- **16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time**
- **Basic Clock Module Configurations**
  - **Internal Frequencies up to 16 MHz With Four Calibrated Frequencies**
  - **Internal Very-Low-Power Low-Frequency (LF) Oscillator**
  - **32-kHz Crystal**
  - **External Digital Clock Source**
- **One 16-Bit Timer_A With Three Capture/Compare Registers**
- **Up to 16 Capacitive-Touch Enabled I/O Pins**
- **Universal Serial Interface (USI) Supporting SPI and I2C**
- **10-Bit 200-ksps Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan (MSP430G2x52 Only)**
- **On-Chip Comparator for Analog**
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **On-Chip Emulation Logic With Spy-Bi-Wire Interface**
- **Family Members are Summarized in Table 1**
- **Package Options**
  - **TSSOP: 14 Pin, 20 Pin**
  - **PDIP: 20 Pin**
  - **QFN: 16 Pin**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (SLAU144)**

## DESCRIPTION

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430G2x52 and MSP430G2x12 series of microcontrollers are ultra-low-power mixed signal microcontrollers with built-in 16-bit timers, and up to 16 I/O capacitive-touch enabled pins and built-in communication capability using the universal serial communication interface and have a versatile analog comparator. The MSP430G2x52 series have a 10-bit A/D converter. For configuration details see Table 1. Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system.

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**Table 1. Available Options(1)**

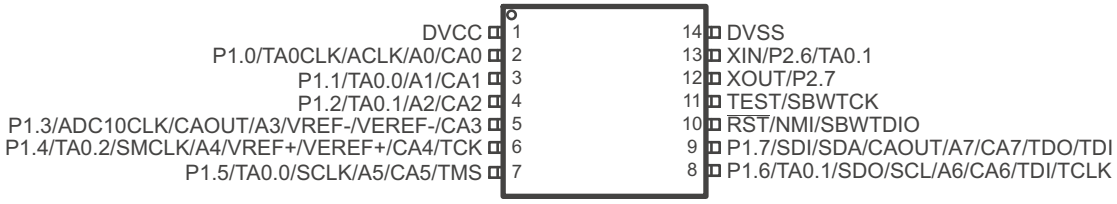
| Device | EEM | Flash (KB) | RAM (B) | Timer_A | Comp_A Channel | ADC10 Channel | USI | Clock | I/O | Package Type(2) |
|---|---|---|---|---|---|---|---|---|---|---|
| MSP430G2452IN20 | 1 | 8 | 256 | 1x TA3 | 8 | 8 | 1 | LF, DCO, VLO | 16 | 20-PDIP |
| MSP430G2452IPW20 | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2452IRSA16 | | | | | | | | | 10 | 16-QFN |
| MSP430G2452IPW14 | | | | | | | | | 10 | 14-TSSOP |
| MSP430G2352IN20 | 1 | 4 | 256 | 1x TA3 | 8 | 8 | 1 | LF, DCO, VLO | 16 | 20-PDIP |
| MSP430G2352IPW20 | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2352IRSA16 | | | | | | | | | 10 | 16-QFN |
| MSP430G2352IPW14 | | | | | | | | | 10 | 14-TSSOP |
| MSP430G2252IN20 | 1 | 2 | 256 | 1x TA3 | 8 | 8 | 1 | LF, DCO, VLO | 16 | 20-PDIP |
| MSP430G2252IPW20 | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2252IRSA16 | | | | | | | | | 10 | 16-QFN |
| MSP430G2252IPW14 | | | | | | | | | 10 | 14-TSSOP |
| MSP430G2152IN20 | 1 | 1 | 128 | 1x TA3 | 8 | 8 | 1 | LF, DCO, VLO | 16 | 20-PDIP |
| MSP430G2152IPW20 | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2152IRSA16 | | | | | | | | | 10 | 16-QFN |
| MSP430G2152IPW14 | | | | | | | | | 10 | 14-TSSOP |
| MSP430G2412IN20 | 1 | 8 | 256 | 1x TA3 | 8 | - | 1 | LF, DCO, VLO | 16 | 20-PDIP |
| MSP430G2412IPW20 | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2412IRSA16 | | | | | | | | | 10 | 16-QFN |
| MSP430G2412IPW14 | | | | | | | | | 10 | 14-TSSOP |
| MSP430G2312IN20 | 1 | 4 | 256 | 1x TA3 | 8 | - | 1 | LF, DCO, VLO | 16 | 20-PDIP |
| MSP430G2312IPW20 | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2312IRSA16 | | | | | | | | | 10 | 16-QFN |
| MSP430G2312IPW14 | | | | | | | | | 10 | 14-TSSOP |
| MSP430G2212IN20 | 1 | 2 | 256 | 1x TA3 | 8 | - | 1 | LF, DCO, VLO | 16 | 20-PDIP |
| MSP430G2212IPW20 | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2212IRSA16 | | | | | | | | | 10 | 16-QFN |
| MSP430G2212IPW14 | | | | | | | | | 10 | 14-TSSOP |
| MSP430G2112IN20 | 1 | 1 | 128 | 1x TA3 | 8 | - | 1 | LF, DCO, VLO | 16 | 20-PDIP |
| MSP430G2112IPW20 | | | | | | | | | 16 | 20-TSSOP |
| MSP430G2112IRSA16 | | | | | | | | | 10 | 16-QFN |
| MSP430G2112IPW14 | | | | | | | | | 10 | 14-TSSOP |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.


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## DEVICE PINOUTS

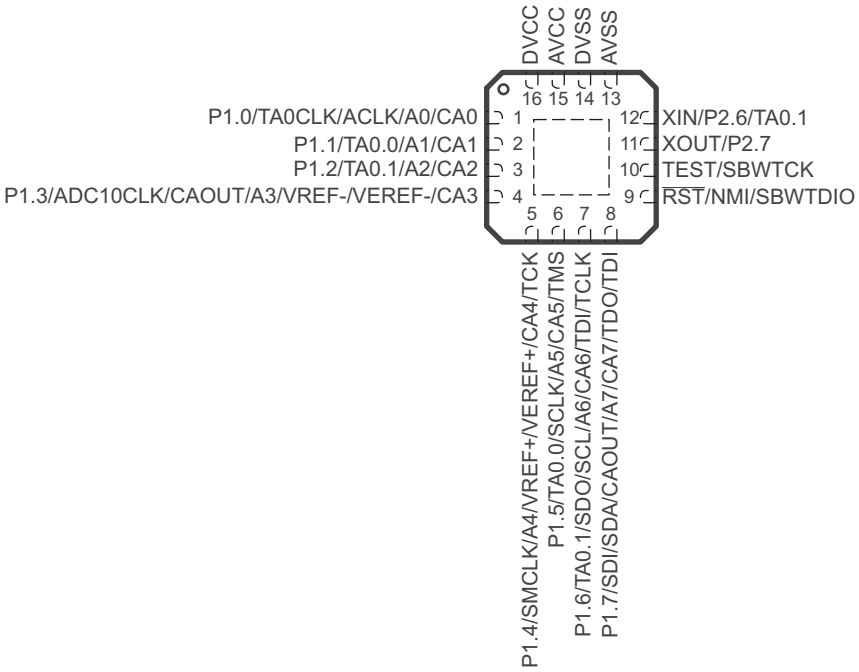
**PW PACKAGE**
**(TOP VIEW)**




NOTE: ADC10 pin functions are available only on MSP430G2x52.

NOTE: The pulldown resistors of port pins P2.0, P2.1, P2.2, P2.3, P2.4, and P2.5 should be enabled by setting P2REN.x = 1.

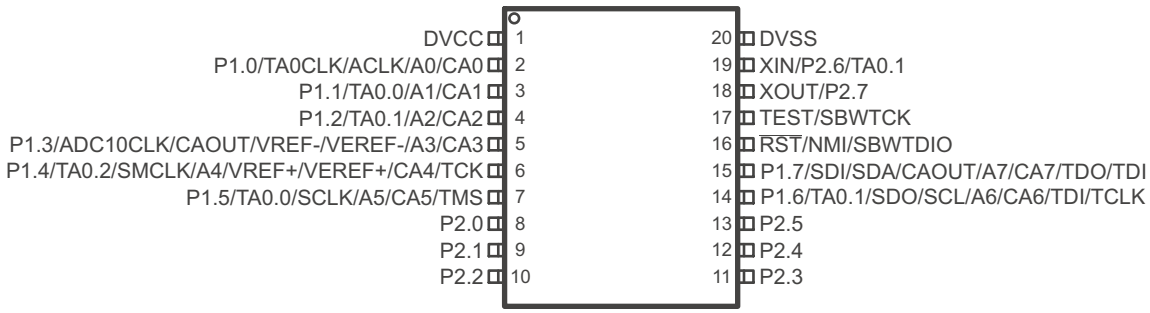
**RSA PACKAGE**
**(TOP VIEW)**




NOTE: ADC10 pin functions are available only on MSP430G2x52.

NOTE: The pulldown resistors of port pins P2.0, P2.1, P2.2, P2.3, P2.4, and P2.5 should be enabled by setting P2REN.x = 1.

**N OR PW PACKAGE**
**(TOP VIEW)**

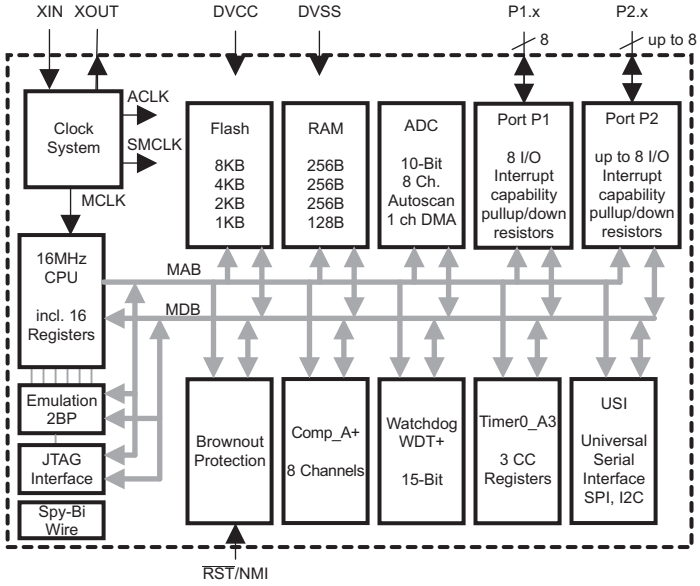



NOTE: ADC10 pin functions are available only on MSP430G2x52.

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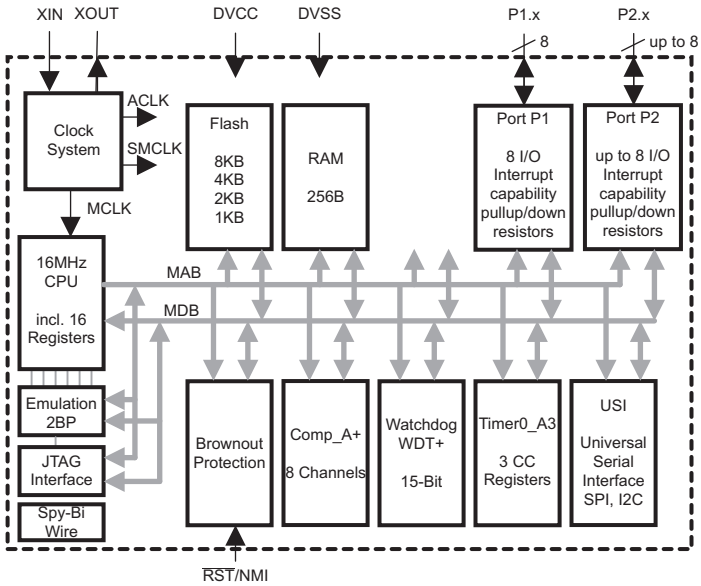
# FUNCTIONAL BLOCK DIAGRAMS

## Functional Block Diagram, MSP430G2x52




NOTE: Port P2. Two pins are available on the 14-pin and 16-pin package options. Eight pins are available on the 20-pin package options.

## Functional Block Diagram, MSP430G2x12




NOTE: Port P2. Two pins are available on the 14-pin and 16-pin package options. Eight pins are available on the 20-pin package options.


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## TERMINAL FUNCTIONS

### Table 2. Terminal Functions

| TERMINAL | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| | 14 PW | 16 RSA | 20 N, PW | | |
| P1.0/ | 2 | 1 | 2 | I/O | General-purpose digital I/O pin |
| TA0CLK/ | | | | | Timer0_A, clock signal TACLK input |
| ACLK/ | | | | | ACLK signal output |
| A0/ | | | | | ADC10 analog input A0(1) |
| CA0 | | | | | Comparator_A+, CA0 input |
| P1.1/ | 3 | 2 | 3 | I/O | General-purpose digital I/O pin |
| TA0.0/ | | | | | Timer0_A, capture: CCI0A input, compare: Out0 output |
| A1/ | | | | | ADC10 analog input A1(1) |
| CA1 | | | | | Comparator_A+, CA1 input |
| P1.2/ | 4 | 3 | 4 | I/O | General-purpose digital I/O pin |
| TA0.1/ | | | | | Timer0_A, capture: CCI1A input, compare: Out1 output |
| A2/ | | | | | ADC10 analog input A2(1) |
| CA2 | | | | | Comparator_A+, CA2 input |
| P1.3/ | 5 | 4 | 5 | I/O | General-purpose digital I/O pin |
| ADC10CLK/ | | | | | ADC10, conversion clock output(1) |
| CAOUT/ | | | | | Comparator_A+, output |
| A3/ | | | | | ADC10 analog input A3(1) |
| VREF-/VEREF-/ | | | | | ADC10 negative reference voltage(1) |
| CA3 | | | | | Comparator_A+, CA3 input |
| P1.4/ | 6 | 5 | 6 | I/O | General-purpose digital I/O pin |
| SMCLK/ | | | | | SMCLK signal output |
| TA0.2/ | | | | | Timer0_A, capture: CCI2A input, compare: Out2 output |
| A4/ | | | | | ADC10 analog input A4(1) |
| VREF+/VEREF+/ | | | | | ADC10 positive reference voltage(1) |
| CA4/ | | | | | Comparator_A+, CA4 input |
| TCK | | | | | JTAG test clock, input terminal for device programming and test |
| P1.5/ | 7 | 6 | 7 | I/O | General-purpose digital I/O pin |
| TA0.0/ | | | | | Timer0_A, compare: Out0 output |
| SCLK/ | | | | | USI: clk input in I2C mode; clk in/output in SPI mode |
| A5/ | | | | | ADC10 analog input A5(1) |
| CA5/ | | | | | Comparator_A+, CA5 input |
| TMS | | | | | JTAG test mode select, input terminal for device programming and test |
| P1.6/ | 8 | 7 | 14 | I/O | General-purpose digital I/O pin |
| TA0.1/ | | | | | Timer0_A, compare: Out1 output |
| SDO/ | | | | | USI: Data output in SPI mode |
| SCL/ | | | | | USI: I2C clock in I2C mode |
| A6/ | | | | | ADC10 analog input A6(1) |
| CA6/ | | | | | Comparator_A+, CA6 input |
| TDI/TCLK | | | | | JTAG test data input or test clock input during programming and test |

(1) Available only on MSP430G2x52 devices.

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**Table 2. Terminal Functions (continued)**

| TERMINAL | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| | 14 PW | 16 RSA | 20 N, PW | | |
| P1.7/<br>CAOUT/<br>SDI/<br>SDA/<br>A7/<br>CA7/<br>TDO/TDI(2) | 9 | 8 | 15 | I/O | General-purpose digital I/O pin<br>Comparator_A+, output<br>USI: Data input in SPI mode<br>USI: I2C data in I2C mode<br>ADC10 analog input A7(1)<br>Comparator_A+, CA7 input<br>JTAG test data output terminal or test data input during programming and test |
| P2.0 | - | - | 8 | I/O | General-purpose digital I/O pin |
| P2.1 | - | - | 9 | I/O | General-purpose digital I/O pin |
| P2.2 | - | - | 10 | I/O | General-purpose digital I/O pin |
| P2.3 | - | - | 11 | I/O | General-purpose digital I/O pin |
| P2.4 | - | - | 12 | I/O | General-purpose digital I/O pin |
| P2.5 | - | - | 13 | I/O | General-purpose digital I/O pin |
| XIN/<br>P2.6/<br>TA0.1 | 13 | 12 | 19 | I/O | Input terminal of crystal oscillator<br>General-purpose digital I/O pin<br>Timer0_A, compare: Out1 output |
| XOUT/<br>P2.7 | 12 | 11 | 18 | I/O | Output terminal of crystal oscillator(3)<br>General-purpose digital I/O pin |
| $\overline{\text{RST}}$/<br>NMI/<br>SBWTDIO | 10 | 9 | 16 | I | Reset<br>Nonmaskable interrupt input<br>Spy-Bi-Wire test data input/output during programming and test |
| TEST/<br><br>SBWTCK | 11 | 10 | 17 | I | Selects test mode for JTAG pins on port 1. The device protection fuse is connected to TEST.<br>Spy-Bi-Wire test clock input during programming and test |
| DVCC | 1 | 16 | 1 | NA | Supply voltage |
| AVCC | - | 15 | - | NA | Supply voltage |
| DVSS | 14 | 14 | 20 | NA | Ground reference |
| AVSS | - | 13 | - | NA | Ground reference |
| NC | - | - | - | NA | Not connected |
| QFN Pad | - | Pad | - | NA | QFN package pad connection to $V_{SS}$ recommended. |

(2) TDO or TDI is selected via JTAG instruction.
(3) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.


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# SHORT-FORM DESCRIPTION

## CPU

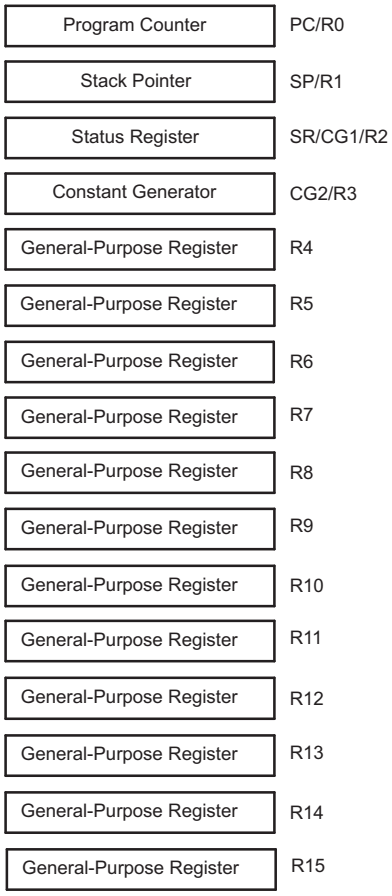
The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.




## Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 3 shows examples of the three types of instruction formats; Table 4 shows the address modes.

**Table 3. Instruction Word Formats**

| FORMAT | EXAMPLE | OPERATION |
|---|---|---|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 –> R5 |
| Single operands, destination only | CALL R8 | PC –>(TOS), R8–> PC |
| Relative jump, un/conditional | JNE | Jump-on-equal bit = 0 |

**Table 4. Address Mode Descriptions(1)**

| ADDRESS MODE | S | D | SYNTAX | EXAMPLE | OPERATION |
|---|---|---|---|---|---|
| Register | ✓ | ✓ | MOV Rs,Rd | MOV R10,R11 | R10 – –> R11 |
| Indexed | ✓ | ✓ | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5) – –> M(6+R6) |
| Symbolic (PC relative) | ✓ | ✓ | MOV EDE,TONI | | M(EDE) – –> M(TONI) |
| Absolute | ✓ | ✓ | MOV &MEM,&TCDAT | | M(MEM) – –> M(TCDAT) |
| Indirect | ✓ | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) – –> M(Tab+R6) |
| Indirect autoincrement | ✓ | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) – –> R11<br>R10 + 2– –> R10 |
| Immediate | ✓ | | MOV #X,TONI | MOV #45,TONI | #45 – –> M(TONI) |

(1) S = source, D = destination

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## Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - DCO's dc generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped


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## Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, if flash is not programmed) the CPU goes into LPM4 immediately after power-up.

**Table 5. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| Power-Up<br>External Reset<br>Watchdog Timer+<br>Flash key violation<br>PC out-of-range(1) | PORIFG<br>RSTIFG<br>WDTIFG<br>KEYV(2) | Reset | 0FFFEh | 31, highest |
| NMI<br>Oscillator fault<br>Flash memory access violation | NMIIFG<br>OFIFG<br>ACCVIFG(2)(3) | (non)-maskable<br>(non)-maskable<br>(non)-maskable | 0FFFCh | 30 |
| | | | 0FFFAh | 29 |
| | | | 0FFF8h | 28 |
| Comparator_A+ | CAIFG(4) | maskable | 0FFF6h | 27 |
| Watchdog Timer+ | WDTIFG | maskable | 0FFF4h | 26 |
| Timer0_A3 | TACCR0 CCIFG(4) | maskable | 0FFF2h | 25 |
| Timer0_A3 | TACCR2 TACCR1 CCIFG. TAIFG(2)(4) | maskable | 0FFF0h | 24 |
| | | | 0FFEEh | 23 |
| | | | 0FFECh | 22 |
| ADC10(5) | ADC10IFG(4)(5) | maskable | 0FFEAh | 21 |
| USI | USIIFG, USISTTIFG(2)(4) | maskable | 0FFE8h | 20 |
| I/O Port P2 (up to eight flags) | P2IFG.0 to P2IFG.7(2)(4) | maskable | 0FFE6h | 19 |
| I/O Port P1 (up to eight flags) | P1IFG.0 to P1IFG.7(2)(4) | maskable | 0FFE4h | 18 |
| | | | 0FFE2h | 17 |
| | | | 0FFE0h | 16 |
| See (6) | | | 0FFDEh to 0FFC0h | 15 to 0, lowest |

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) MSP430G2x52 only
(6) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

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## Special Function Registers (SFRs)

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

| Legend | | |
|---|---|---|
| | **rw:** | Bit can be read and written. |
| | **rw-0,1:** | Bit can be read and written. It is reset or set by PUC. |
| | **rw-(0,1):** | Bit can be read and written. It is reset or set by POR. |
| | | SFR bit is not present in device. |

**Table 6. Interrupt Enable Register 1 and 2**

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **00h** | | | **ACCVIE** | **NMIIE** | | | **OFIE** | **WDTIE** |
| | | | rw-0 | rw-0 | | | rw-0 | rw-0 |

| | |
|---|---|
| **WDTIE** | Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode. |
| **OFIE** | Oscillator fault interrupt enable |
| **NMIIE** | (Non)maskable interrupt enable |
| **ACCVIE** | Flash access violation interrupt enable |

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **01h** | | | | | | | | |

**Table 7. Interrupt Flag Register 1 and 2**

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **02h** | | | | **NMIIFG** | **RSTIFG** | **PORIFG** | **OFIFG** | **WDTIFG** |
| | | | | rw-0 | rw-(0) | rw-(1) | rw-1 | rw-(0) |

| | |
|---|---|
| **WDTIFG** | Set on watchdog timer overflow (in watchdog mode) or security key violation.<br>Reset on $V_{CC}$ power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode. |
| **OFIFG** | Flag set on oscillator fault. |
| **PORIFG** | Power-On Reset interrupt flag. Set on $V_{CC}$ power-up. |
| **RSTIFG** | External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on $V_{CC}$ power-up. |
| **NMIIFG** | Set via $\overline{RST}$/NMI pin |

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **03h** | | | | | | | | |


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## Memory Organization

**Table 8. Memory Organization**

| | | MSP430G2112 MSP430G2152 | MSP430G2212 MSP430G2252 | MSP430G2312 MSP430G2352 | MSP430G2412 MSP430G2452 |
|---|---|---|---|---|---|
| Memory | Size | 1kB | 2kB | 4kB | 8kB |
| Main: interrupt vector | Flash | 0xFFFF to 0xFFC0 | 0xFFFF to 0xFFC0 | 0xFFFF to 0xFFC0 | 0xFFFF to 0xFFC0 |
| Main: code memory | Flash | 0xFFFF to 0xFC00 | 0xFFFF to 0xF800 | 0xFFFF to 0xF000 | 0xFFFF to 0xE000 |
| Information memory | Size | 256 Byte | 256 Byte | 256 Byte | 256 Byte |
| | Flash | 010FFh to 01000h | 010FFh to 01000h | 010FFh to 01000h | 010FFh to 01000h |
| RAM | Size | 128 B | 256 B | 256 B | 256 B |
| | | 0x027F to 0x0200 | 0x02FF to 0x0200 | 0x02FF to 0x0200 | 0x02FF to 0x0200 |
| Peripherals | 16-bit | 01FFh to 0100h | 01FFh to 0100h | 01FFh to 0100h | 01FFh to 0100h |
| | 8-bit | 0FFh to 010h | 0FFh to 010h | 0FFh to 010h | 0FFh to 010h |
| | 8-bit SFR | 0Fh to 00h | 0Fh to 00h | 0Fh to 00h | 0Fh to 00h |

## Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset, segment A is protected against programming and erasing. It can be unlocked, but care should be taken not to erase this segment if the device-specific calibration data is required.

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## Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

### Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

### Calibration Data Stored in Information Memory Segment A

Calibration data is stored for both the DCO and for ADC10 organized in a tag-length-value structure.

**Table 9. Tags Used by the ADC Calibration Tags**

| NAME | ADDRESS | VALUE | DESCRIPTION |
|---|---|---|---|
| TAG_DCO_30 | 0x10F6 | 0x01 | DCO frequency calibration at $V_{CC}$ = 3 V and $T_A$ = 30°C at calibration |
| TAG_ADC10_1 | 0x10DA | 0x10 | ADC10_1 calibration tag |
| TAG_EMPTY | - | 0xFE | Identifier for empty memory areas |

**Table 10. Labels Used by the ADC Calibration Tags**

| LABEL | CONDITION AT CALIBRATION / DESCRIPTION | SIZE | ADDRESS OFFSET |
|---|---|---|---|
| CAL_ADC_25T85 | INCHx = 0x1010, REF2_5 = 1, $T_A$ = 85°C | word | 0x0010 |
| CAL_ADC_25T30 | INCHx = 0x1010, REF2_5 = 1, $T_A$ = 30°C | word | 0x000E |
| CAL_ADC_25VREF_FACTOR | REF2_5 = 1, $T_A$ = 30°C, $I_{(VREF+)}$ = 1 mA | word | 0x000C |
| CAL_ADC_15T85 | INCHx = 0x1010, REF2_5 = 0, $T_A$ = 85°C | word | 0x000A |
| CAL_ADC_15T30 | INCHx = 0x1010, REF2_5 = 0, $T_A$ = 30°C | word | 0x0008 |
| CAL_ADC_15VREF_FACTOR | REF2_5 = 0, $T_A$ = 30°C, $I_{(VREF+)}$ = 0.5 mA | word | 0x0006 |
| CAL_ADC_OFFSET | External VREF = 1.5 V, $f_{(ADC10CLK)}$ = 5 MHz | word | 0x0004 |
| CAL_ADC_GAIN_FACTOR | External VREF = 1.5 V, $f_{(ADC10CLK)}$ = 5 MHz | word | 0x0002 |
| CAL_BC1_1MHz | - | byte | 0x0009 |
| CAL_DCO_1MHz | - | byte | 0x00008 |
| CAL_BC1_8MHz | - | byte | 0x0007 |
| CAL_DCO_8MHz | - | byte | 0x0006 |
| CAL_BC1_12MHz | - | byte | 0x0005 |
| CAL_DCO_12MHz | - | byte | 0x0004 |
| CAL_BC1_16MHz | - | byte | 0x0003 |
| CAL_DCO_16MHz | - | byte | 0x0002 |


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### Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ..., RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter $S_{DCO}$.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

### Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

### Digital I/O

There are two 8-bit I/O ports implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition(port P1 and port P2 only) is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and port P2, if available.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.
- Each I/O has an individually programmable pin-oscillator enable bit to enable low-cost capacitive-touch detection.

### WDT+ Watchdog Timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

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### Timer0_A3

Timer0_A3 is a 16-bit timer/counter with three capture/compare registers. Timer0_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer0_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 11. Timer0_A3 Signal Connections(1)**

| INPUT PIN NUMBER | | | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | |
|---|---|---|---|---|---|---|---|---|---|
| N20, PW20 | PW14 | RSA16 | | | | | N20, PW20 | PW14 | RSA16 |
| P1.0-2 | P1.0-2 | P1.0-1 | TACLK | TACLK | Timer | NA | | | |
| | | | ACLK | ACLK | | | | | |
| | | | SMCLK | SMCLK | | | | | |
| PinOsc | PinOsc | PinOsc | | INCLK | | | | | |
| P1.1-3 | P1.1-3 | P1.1-2 | TA0.0 | CCI0A | CCR0 | TA0 | P1.1-3 | P1.1-3 | P1.1-2 |
| | | | ACLK | CCI0B | | | P1.5-7 | P1.5-7 | P1.5-6 |
| | | | $V_{SS}$ | GND | | | | | |
| | | | $V_{CC}$ | $V_{CC}$ | | | | | |
| P1.2-4 | P1.2-4 | P1.2-3 | TA0.1 | CCI1A | CCR1 | TA1 | P1.2-4 | P1.2-4 | P1.2-3 |
| | | | CAOUT | CCI1B | | | P1.6-14 | P1.6-8 | P1.6-7 |
| | | | $V_{SS}$ | GND | | | P2.6-19 | P2.6-12 | P2.6-12 |
| | | | $V_{CC}$ | $V_{CC}$ | | | | | |
| P1.4-6 | P1.4-6 | P1.4-5 | TA0.2 | CCI2A | CCR2 | TA2 | P1.4-6 | P1.4-6 | P1.4-5 |
| PinOsc | PinOsc | PinOsc | TA0.2 | CCI2B | | | | | |
| | | | $V_{SS}$ | GND | | | | | |
| | | | $V_{CC}$ | $V_{CC}$ | | | | | |

(1) Only one pin-oscillator must be enabled at a time.

### USI

The universal serial interface (USI) module is used for serial data communication and provides the basic hardware for synchronous communication protocols like SPI and I2C.

### Comparator_A+

The primary function of the Comparator_A+module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

### ADC10 (MSP430G2x52 only)

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.


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## Peripheral File Map

**Table 12. Peripherals With Word Access**

| MODULE | REGISTER DESCRIPTION | REGISTER NAME | OFFSET |
|---|---|---|---|
| **ADC10 (MSP430G2x52 devices only)** | ADC data transfer start address | ADC10SA | 01BCh |
| | ADC memory | ADC10MEM | 01B4h |
| | ADC control register 1 | ADC10CTL1 | 01B2h |
| | ADC control register 0 | ADC10CTL0 | 01B0h |
| **Timer0_A3** | Capture/compare register | TACCR2 | 0176h |
| | Capture/compare register | TACCR1 | 0174h |
| | Capture/compare register | TACCR0 | 0172h |
| | Timer_A register | TAR | 0170h |
| | Capture/compare control | TACCTL2 | 0166h |
| | Capture/compare control | TACCTL1 | 0164h |
| | Capture/compare control | TACCTL0 | 0162h |
| | Timer_A control | TACTL | 0160h |
| | Timer_A interrupt vector | TAIV | 012Eh |
| **Flash Memory** | Flash control 3 | FCTL3 | 012Ch |
| | Flash control 2 | FCTL2 | 012Ah |
| | Flash control 1 | FCTL1 | 0128h |
| **Watchdog Timer+** | Watchdog/timer control | WDTCTL | 0120h |

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**Table 13. Peripherals With Byte Access**

| MODULE | REGISTER DESCRIPTION | REGISTER NAME | OFFSET |
|---|---|---|---|
| **ADC10 (MSP430G2x52 devices only)** | Analog enable 1 | ADC10AE1 | 04Bh |
| | Analog enable 0 | ADC10AE0 | 04Ah |
| | ADC data transfer control register 1 | ADC10DTC1 | 049h |
| | ADC data transfer control register 0 | ADC10DTC0 | 048h |
| **USI** | USI control 0 | USICTL0 | 078h |
| | USI control 1 | USICTL1 | 079h |
| | USI clock control | USICKCTL | 07Ah |
| | USI bit counter | USICNT | 07Bh |
| | USI shift register | USISR | 07Ch |
| **Comparator_A+** | Comparator_A+ port disable | CAPD | 05Bh |
| | Comparator_A+ control 2 | CACTL2 | 05Ah |
| | Comparator_A+ control 1 | CACTL1 | 059h |
| **Basic Clock System+** | Basic clock system control 3 | BCSCTL3 | 053h |
| | Basic clock system control 2 | BCSCTL2 | 058h |
| | Basic clock system control 1 | BCSCTL1 | 057h |
| | DCO clock frequency control | DCOCTL | 056h |
| **Port P2** | Port P2 selection 2 | P2SEL2 | 042h |
| | Port P2 resistor enable | P2REN | 02Fh |
| | Port P2 selection | P2SEL | 02Eh |
| | Port P2 interrupt enable | P2IE | 02Dh |
| | Port P2 interrupt edge select | P2IES | 02Ch |
| | Port P2 interrupt flag | P2IFG | 02Bh |
| | Port P2 direction | P2DIR | 02Ah |
| | Port P2 output | P2OUT | 029h |
| | Port P2 input | P2IN | 028h |
| **Port P1** | Port P1 selection 2 | P1SEL2 | 041h |
| | Port P1 resistor enable | P1REN | 027h |
| | Port P1 selection | P1SEL | 026h |
| | Port P1 interrupt enable | P1IE | 025h |
| | Port P1 interrupt edge select | P1IES | 024h |
| | Port P1 interrupt flag | P1IFG | 023h |
| | Port P1 direction | P1DIR | 022h |
| | Port P1 output | P1OUT | 021h |
| | Port P1 input | P1IN | 020h |
| **Special Function** | SFR interrupt flag 2 | IFG2 | 003h |
| | SFR interrupt flag 1 | IFG1 | 002h |
| | SFR interrupt enable 2 | IE2 | 001h |
| | SFR interrupt enable 1 | IE1 | 000h |


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## Absolute Maximum Ratings(1)

| | | |
|---|---|---|
| Voltage applied at $V_{CC}$ to $V_{SS}$ | | –0.3 V to 4.1 V |
| Voltage applied to any pin(2) | | –0.3 V to $V_{CC}$ + 0.3 V |
| Diode current at any device pin | | ±2 mA |
| Storage temperature range, $T_{stg}$ (3) | Unprogrammed device | –55°C to 150°C |
| | Programmed device | –55°C to 150°C |

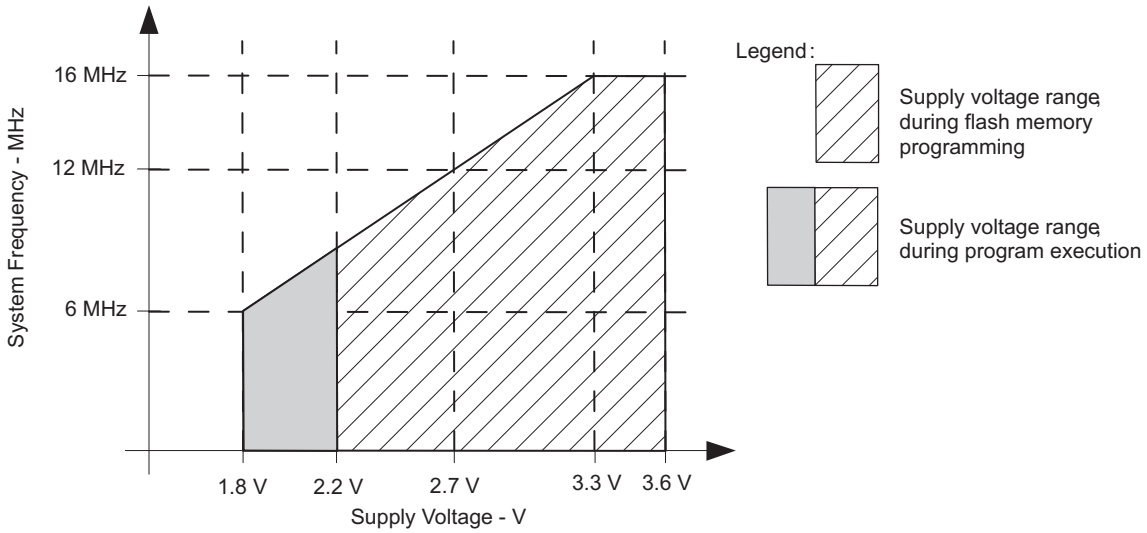
(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to $V_{SS}$. The JTAG fuse-blow voltage, $V_{FB}$, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## Recommended Operating Conditions

Typical values are specified at $V_{CC}$ = 3.3 V and $T_A$ = 25°C (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | During program execution | 1.8 | | 3.6 | V |
| | | During flash programming/erase | 2.2 | | 3.6 | |
| $V_{SS}$ | Supply voltage | | | 0 | | V |
| $T_A$ | Operating free-air temperature | | -40 | | 85 | °C |
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency using the USART module)(1)(2) | $V_{CC}$ = 1.8 V, Duty cycle = 50% ± 10% | dc | | 6 | MHz |
| | | $V_{CC}$ = 2.7 V, Duty cycle = 50% ± 10% | dc | | 12 | |
| | | $V_{CC}$ = 3.3 V, Duty cycle = 50% ± 10% | dc | | 16 | |

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.




Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum $V_{CC}$ of 2.2 V.

**Figure 1. Safe Operating Area**

## Electrical Characteristics

### Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{AM,1MHz}$ | Active mode (AM) current (1 MHz) | $f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, $f_{ACLK}$ = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | 2.2 V | | 220 | | µA |
| | | | 3 V | | 320 | 400 | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

### Typical Characteristics – Active Mode Supply Current (Into $V_{CC}$)

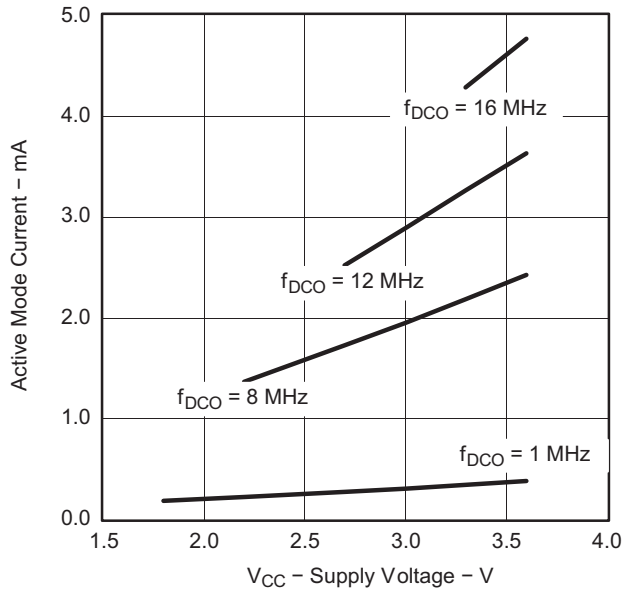



**Figure 2. Active Mode Current vs $V_{CC}$, $T_A$ = 25°C**

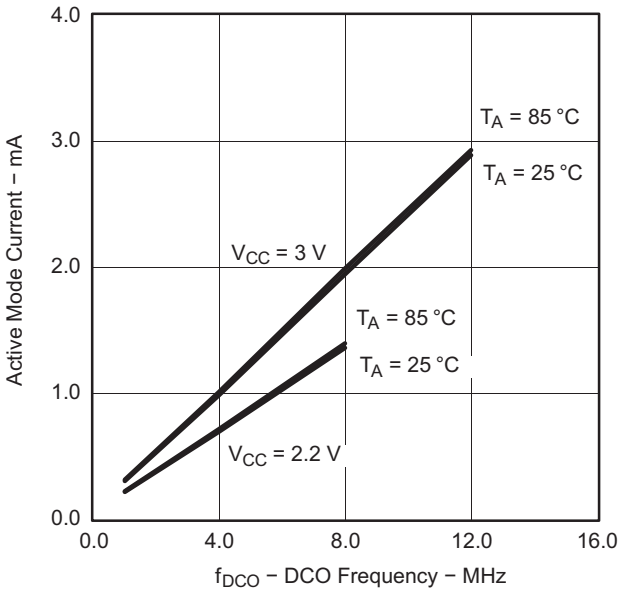



**Figure 3. Active Mode Current vs DCO Frequency**


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## Low-Power Mode Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

| PARAMETER | | TEST CONDITIONS | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{LPM0,1MHz}$ | Low-power mode 0 (LPM0) current(3) | $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = $f_{DCO}$ = 1 MHz, $f_{ACLK}$ = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | 25°C | 2.2 V | | 55 | | µA |
| $I_{LPM2}$ | Low-power mode 2 (LPM2) current(4) | $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{DCO}$ = 1 MHz, $f_{ACLK}$ = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 22 | | µA |
| $I_{LPM3,LFXT1}$ | Low-power mode 3 (LPM3) current(4) | $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 0.7 | 1.0 | µA |
| $I_{LPM3,VLO}$ | Low-power mode 3 current, (LPM3)(4) | $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 | 25°C | 2.2 V | | 0.5 | 0.7 | µA |
| $I_{LPM4}$ | Low-power mode 4 (LPM4) current(5) | $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 | 25°C | 2.2 V | | 0.1 | 0.5 | µA |
| | | | 85°C | | | 0.8 | 1.5 | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.
(5) Current for brownout included.

## Typical Characteristics Low-Power Mode Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

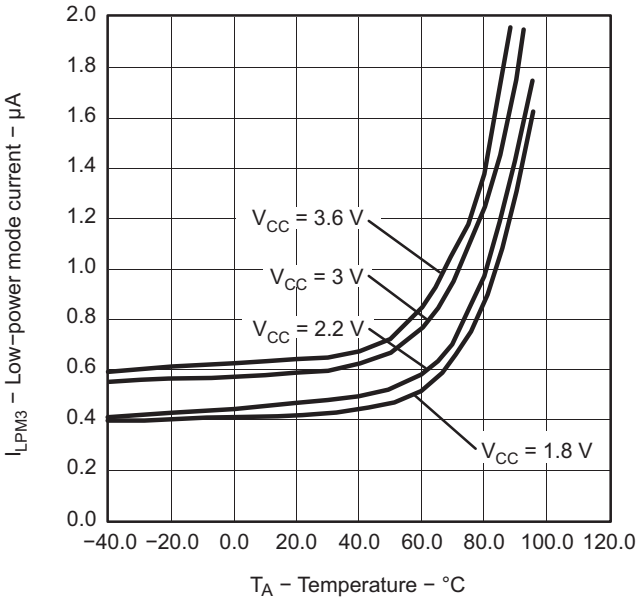



**Figure 4. LPM3 (VLO) Current vs Temperature**

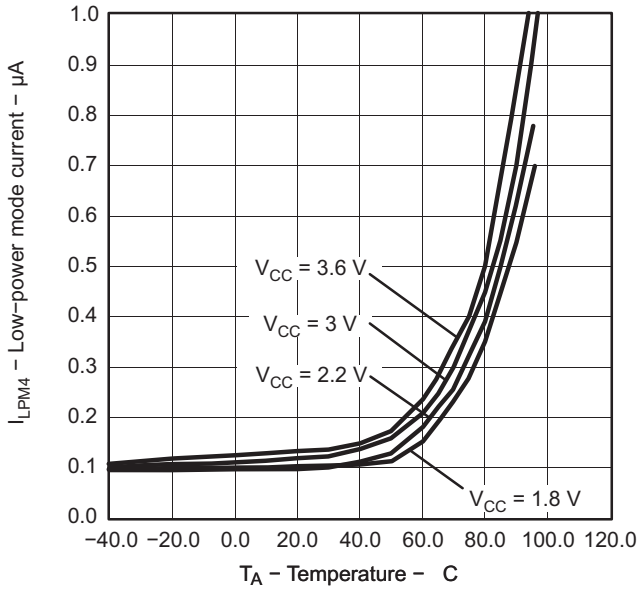



**Figure 5. LPM4 Current vs Temperature**

## Schmitt-Trigger Inputs – Ports Px(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | | 0.45 $V_{CC}$ | | 0.75 $V_{CC}$ | V |
| | | | 3 V | 1.35 | | 2.25 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | | 0.25 $V_{CC}$ | | 0.55 $V_{CC}$ | V |
| | | | 3 V | 0.75 | | 1.65 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | | 3 V | 0.3 | | 1 | V |
| $R_{Pull}$ | Pullup/pulldown resistor | For pullup: $V_{IN} = V_{SS}$<br>For pulldown: $V_{IN} = V_{CC}$ | 3 V | 20 | 35 | 50 | kΩ |
| $C_I$ | Input capacitance | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

## Leakage Current – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{lkg(Px.x)}$ | High-impedance leakage current | (1) (2) | 3 V | | ±50 | nA |

(1) The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input, and the pullup/pulldown resistor is disabled.

## Outputs – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –6 mA(1) | 3 V | | $V_{CC}$ – 0.3 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 6 mA(1) | 3 V | | $V_{SS}$ + 0.3 | | V |

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

## Output Frequency – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{Px.y}$ | Port output frequency (with load) | Px.y, $C_L$ = 20 pF, $R_L$ = 1 kΩ(1) (2) | 3 V | | 12 | | MHz |
| $f_{Port_CLK}$ | Clock output frequency | Px.y, $C_L$ = 20 pF(2) | 3 V | | 16 | | MHz |

(1) A resistive divider with two 0.5-kΩ resistors between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.


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## Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

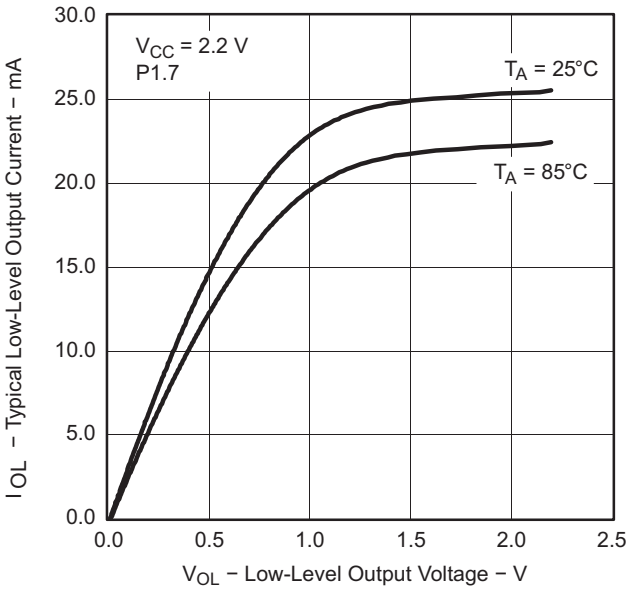



**Figure 6.**

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

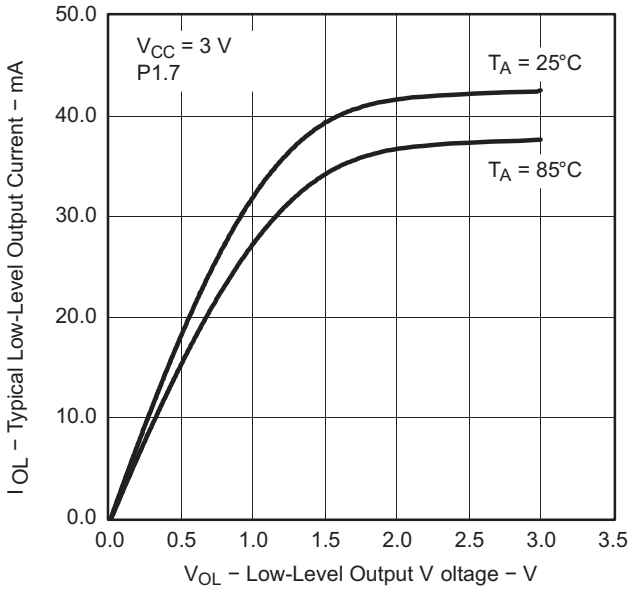



**Figure 7.**

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

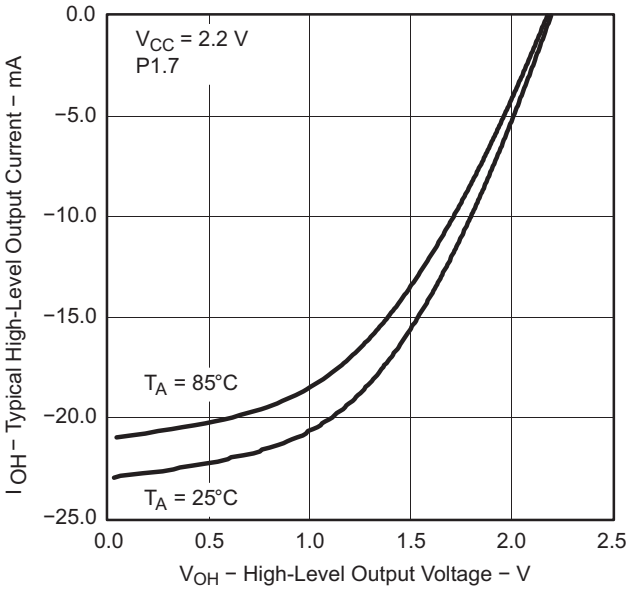



**Figure 8.**

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

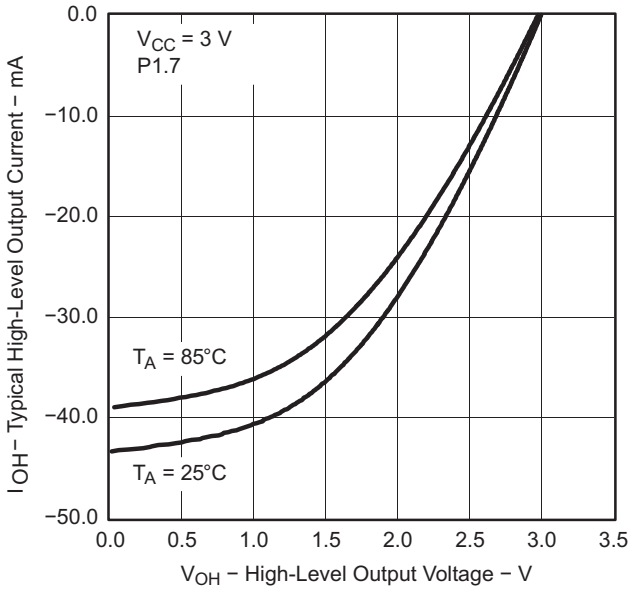



**Figure 9.**

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## Pin-Oscillator Frequency – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $fo_{P1.x}$ | Port output oscillation frequency | P1.y, $C_L$ = 10 pF, $R_L$ = 100 kΩ(1)(2) | 3 V | | 1400 | | kHz |
| | | P1.y, $C_L$ = 20 pF, $R_L$ = 100 kΩ(1)(2) | | | 900 | | |
| $fo_{P2.x}$ | Port output oscillation frequency | P2.0 to P2.5, $C_L$ = 10 pF, $R_L$ = 100 kΩ(1)(2) | 3 V | | 1800 | | kHz |
| | | P2.0 to P2.5, $C_L$ = 20 pF, $R_L$ = 100 kΩ(1)(2) | | | 1000 | | |
| $fo_{P2.6/7}$ | Port output oscillation frequency | P2.6 and P2.7, $C_L$ = 20 pF, $R_L$ = 100 kΩ(1)(2) | 3 V | | 700 | | kHz |

(1) A resistive divider with two 50-kΩ resistors between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider.
(2) The output voltage oscillates with a typical amplitude of 700 mV at the specified toggle frequency.

## Typical Characteristics – Pin-Oscillator Frequency

TYPICAL OSCILLATING FREQUENCY
vs
LOAD CAPACITANCE

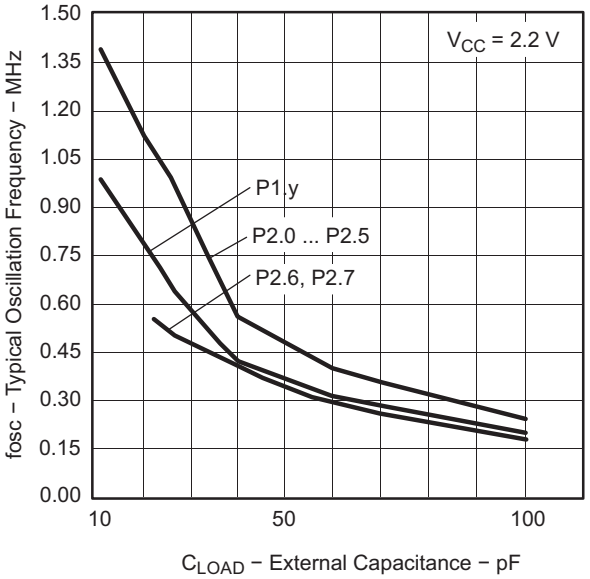



**Figure 10.**

TYPICAL OSCILLATING FREQUENCY
vs
LOAD CAPACITANCE

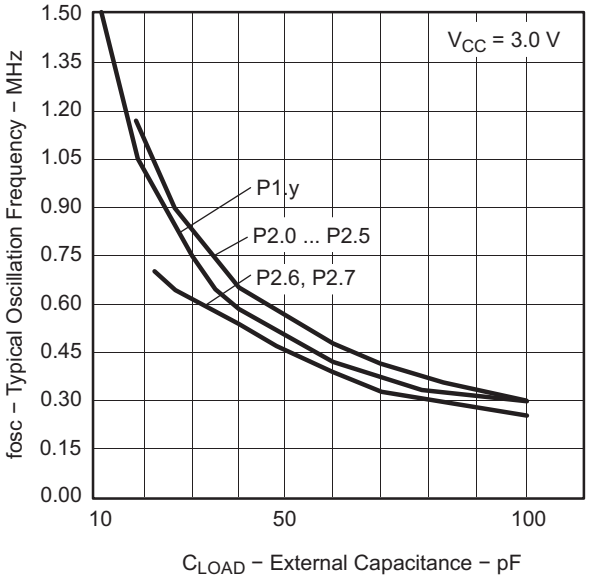



**Figure 11.**


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## POR, BOR(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC(start)}$ | See Figure 12 | $dV_{CC}/dt \le 3$ V/s | | | 0.7 × $V_{(B_IT-)}$ | | V |
| $V_{(B_IT-)}$ | See Figure 12 through Figure 14 | $dV_{CC}/dt \le 3$ V/s | | | 1.40 | | V |
| $V_{hys(B_IT-)}$ | See Figure 12 | $dV_{CC}/dt \le 3$ V/s | | | 140 | | mV |
| $t_{d(BOR)}$ | See Figure 12 | | | | | 2000 | µs |
| $t_{(reset)}$ | Pulse duration needed at $\overline{RST}$/NMI pin to accepted reset internally | | 2.2 V | 2 | | | µs |

(1) The current consumption of the brownout module is already included in the $I_{CC}$ current consumption data. The voltage level $V_{(B_IT-)}$ + $V_{hys(B_IT-)}$is ≤ 1.8 V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B_IT-)} + V_{hys(B_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

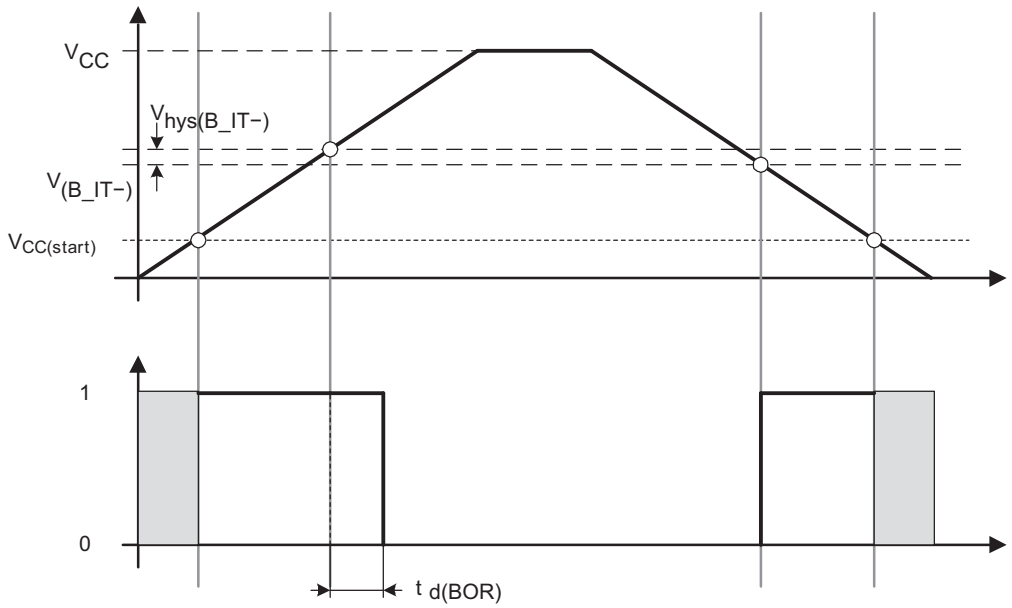



**Figure 12. POR and BOR vs Supply Voltage**

## Typical Characteristics – POR and BOR

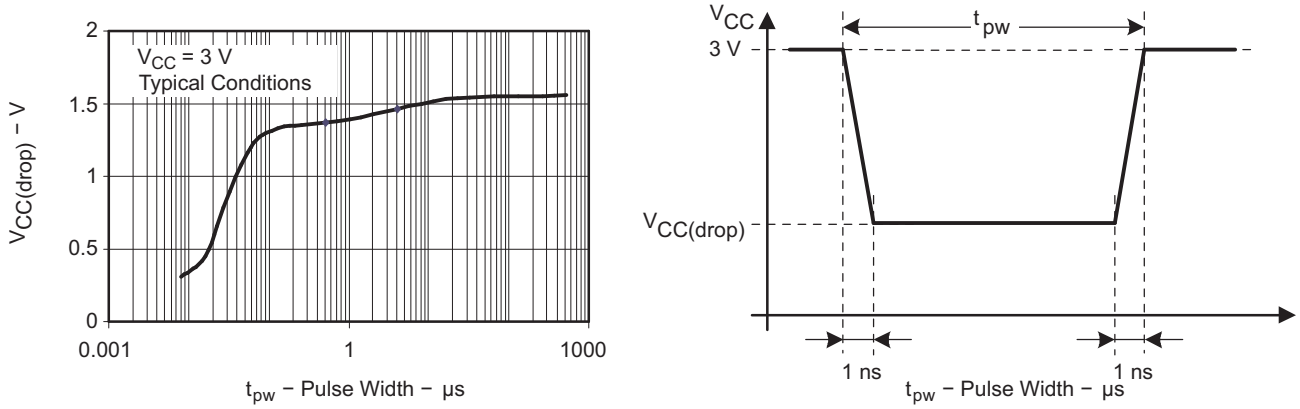



**Figure 13. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal**

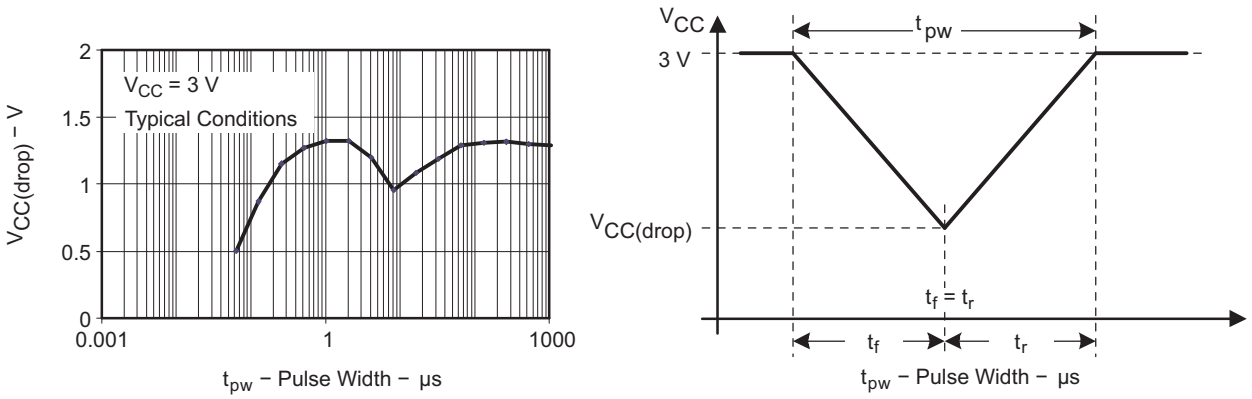



**Figure 14. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal**


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## DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | RSELx < 14 | | 1.8 | | 3.6 | V |
| | | RSELx = 14 | | 2.2 | | 3.6 | V |
| | | RSELx = 15 | | 3 | | 3.6 | V |
| $f_{DCO(0,0)}$ | DCO frequency (0, 0) | RSELx = 0, DCOx = 0, MODx = 0 | 3 V | 0.06 | | 0.14 | MHz |
| $f_{DCO(0,3)}$ | DCO frequency (0, 3) | RSELx = 0, DCOx = 3, MODx = 0 | 3 V | 0.07 | | 0.17 | MHz |
| $f_{DCO(1,3)}$ | DCO frequency (1, 3) | RSELx = 1, DCOx = 3, MODx = 0 | 3 V | | 0.15 | | MHz |
| $f_{DCO(2,3)}$ | DCO frequency (2, 3) | RSELx = 2, DCOx = 3, MODx = 0 | 3 V | | 0.21 | | MHz |
| $f_{DCO(3,3)}$ | DCO frequency (3, 3) | RSELx = 3, DCOx = 3, MODx = 0 | 3 V | | 0.30 | | MHz |
| $f_{DCO(4,3)}$ | DCO frequency (4, 3) | RSELx = 4, DCOx = 3, MODx = 0 | 3 V | | 0.41 | | MHz |
| $f_{DCO(5,3)}$ | DCO frequency (5, 3) | RSELx = 5, DCOx = 3, MODx = 0 | 3 V | | 0.58 | | MHz |
| $f_{DCO(6,3)}$ | DCO frequency (6, 3) | RSELx = 6, DCOx = 3, MODx = 0 | 3 V | 0.54 | | 1.06 | MHz |
| $f_{DCO(7,3)}$ | DCO frequency (7, 3) | RSELx = 7, DCOx = 3, MODx = 0 | 3 V | 0.80 | | 1.50 | MHz |
| $f_{DCO(8,3)}$ | DCO frequency (8, 3) | RSELx = 8, DCOx = 3, MODx = 0 | 3 V | | 1.6 | | MHz |
| $f_{DCO(9,3)}$ | DCO frequency (9, 3) | RSELx = 9, DCOx = 3, MODx = 0 | 3 V | | 2.3 | | MHz |
| $f_{DCO(10,3)}$ | DCO frequency (10, 3) | RSELx = 10, DCOx = 3, MODx = 0 | 3 V | | 3.4 | | MHz |
| $f_{DCO(11,3)}$ | DCO frequency (11, 3) | RSELx = 11, DCOx = 3, MODx = 0 | 3 V | | 4.25 | | MHz |
| $f_{DCO(12,3)}$ | DCO frequency (12, 3) | RSELx = 12, DCOx = 3, MODx = 0 | 3 V | 4.30 | | 7.30 | MHz |
| $f_{DCO(13,3)}$ | DCO frequency (13, 3) | RSELx = 13, DCOx = 3, MODx = 0 | 3 V | 6.00 | | 9.60 | MHz |
| $f_{DCO(14,3)}$ | DCO frequency (14, 3) | RSELx = 14, DCOx = 3, MODx = 0 | 3 V | 8.60 | | 13.9 | MHz |
| $f_{DCO(15,3)}$ | DCO frequency (15, 3) | RSELx = 15, DCOx = 3, MODx = 0 | 3 V | 12.0 | | 18.5 | MHz |
| $f_{DCO(15,7)}$ | DCO frequency (15, 7) | RSELx = 15, DCOx = 7, MODx = 0 | 3 V | 16.0 | | 26.0 | MHz |
| $S_{RSEL}$ | Frequency step between range RSEL and RSEL+1 | $S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$ | 3 V | | 1.35 | | ratio |
| $S_{DCO}$ | Frequency step between tap DCO and DCO+1 | $S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$ | 3 V | | 1.08 | | ratio |
| | Duty cycle | Measured at SMCLK output | 3 V | | 50 | | % |

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## Calibrated DCO Frequencies – Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| 1-MHz tolerance over temperature(1) | BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V | 0°C to 85°C | 3 V | -3 | ±0.5 | +3 | % |
| 1-MHz tolerance over $V_{CC}$ | BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V | 30°C | 1.8 V to 3.6 V | -3 | ±2 | +3 | % |
| 1-MHz tolerance overall | BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 1.8 V to 3.6 V | -6 | ±3 | +6 | % |
| 8-MHz tolerance over temperature(1) | BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V | 0°C to 85°C | 3 V | -3 | ±0.5 | +3 | % |
| 8-MHz tolerance over $V_{CC}$ | BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V | 30°C | 2.2 V to 3.6 V | -3 | ±2 | +3 | % |
| 8-MHz tolerance overall | BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 2.2 V to 3.6 V | -6 | ±3 | +6 | % |
| 12-MHz tolerance over temperature(1) | BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V | 0°C to 85°C | 3 V | -3 | ±0.5 | +3 | % |
| 12-MHz tolerance over $V_{CC}$ | BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V | 30°C | 2.7 V to 3.6 V | -3 | ±2 | +3 | % |
| 12-MHz tolerance overall | BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 2.7 V to 3.6 V | -6 | ±3 | +6 | % |
| 16-MHz tolerance over temperature(1) | BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V | 0°C to 85°C | 3 V | -3 | ±0.5 | +3 | % |
| 16-MHz tolerance over $V_{CC}$ | BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V | 30°C | 3.3 V to 3.6 V | -3 | ±2 | +3 | % |
| 16-MHz tolerance overall | BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V | -40°C to 85°C | 3.3 V to 3.6 V | -6 | ±3 | +6 | % |

(1) This is the frequency change from the measured frequency at 30°C over temperature.


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## Wake-Up From Lower-Power Modes (LPM3 or LPM4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{DCO,LPM3/4}$ | DCO clock wake-up time from LPM3 or LPM4 (1) | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ | 3 V | | 1.5 | | µs |
| $t_{CPU,LPM3/4}$ | CPU wake-up time from LPM3 or LPM4 (2) | | | | $1/f_{MCLK}$ + $t_{Clock,LPM3/4}$ | | |

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

### Typical Characteristics – DCO Clock Wake-Up Time From LPM3 or LPM4

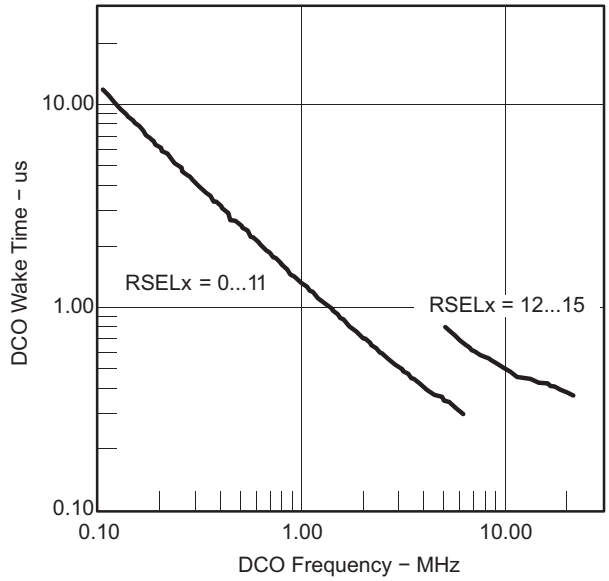



**Figure 15. DCO Wake-Up Time From LPM3 vs DCO Frequency**

## Crystal Oscillator, XT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{LFXT1,LF}$ | LFXT1 oscillator crystal frequency, LF mode 0, 1 | XTS = 0, LFXT1Sx = 0 or 1 | 1.8 V to 3.6 V | | 32768 | | Hz |
| $f_{LFXT1,LF,logic}$ | LFXT1 oscillator logic level square wave input frequency, LF mode | XTS = 0, XCAPx = 0, LFXT1Sx = 3 | 1.8 V to 3.6 V | 10000 | 32768 | 50000 | Hz |
| $OA_{LF}$ | Oscillation allowance for LF crystals | XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF | | | 500 | | kΩ |
| | | XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF | | | 200 | | |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode(2) | XTS = 0, XCAPx = 0 | | | 1 | | pF |
| | | XTS = 0, XCAPx = 1 | | | 5.5 | | |
| | | XTS = 0, XCAPx = 2 | | | 8.5 | | |
| | | XTS = 0, XCAPx = 3 | | | 11 | | |
| Duty cycle | LF mode | XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz | 2.2 V | 30 | 50 | 70 | % |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode(3) | XTS = 0, XCAPx = 0, LFXT1Sx = 3(4) | 2.2 V | 10 | | 10000 | Hz |

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(4) Measured with logic-level input frequency but also applies to operation with crystals.

## Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{VLO}$ | VLO frequency | -40°C to 85°C | 3 V | 4 | 12 | 20 | kHz |
| $df_{VLO}/d_T$ | VLO frequency temperature drift | -40°C to 85°C | 3 V | | 0.5 | | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift | 25°C | 1.8 V to 3.6 V | | 4 | | %/V |

## Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A input clock frequency | SMCLK<br>Duty cycle = 50% ± 10% | | | $f_{SYSTEM}$ | | MHz |
| $t_{TA,cap}$ | Timer_A capture timing | TA0, TA1 | 3 V | 20 | | | ns |


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## USI, Universal Serial Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{USI}$ | USI module clock frequency | External: SCLK, Duty cycle = 50% ± 10% | | | $f_{SYSTEM}$ | | MHz |
| $f_{(SCLK)}$ | Serial clock frequency, slave mode | SPI slave mode | 3 V | | | 6 | MHz |
| $V_{OL,I2C}$ | Low-level output voltage on SDA and SCL | USI module in I2C mode, $I_{(OLmax)}$ = 1.5 mA | 3 V | $V_{SS}$ | | $V_{SS}$ + 0.4 | V |

### Typical Characteristics -- USI Low-Level Output Voltage on SDA and SCL

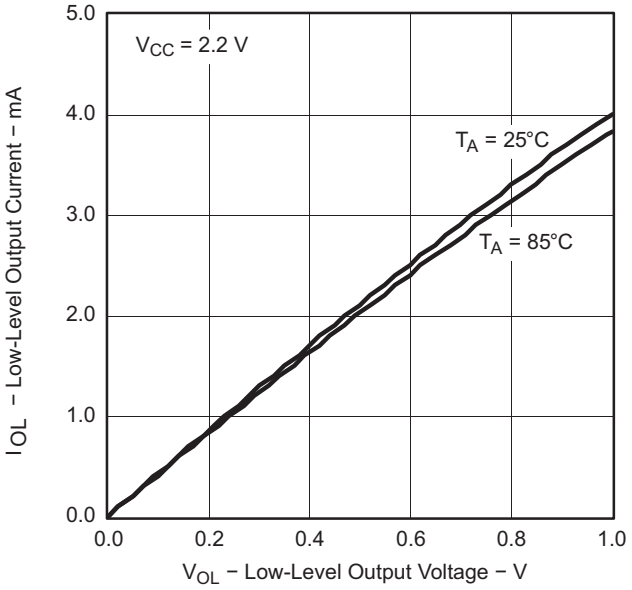



**Figure 16. USI Low-Level Output Voltage vs Output Current**

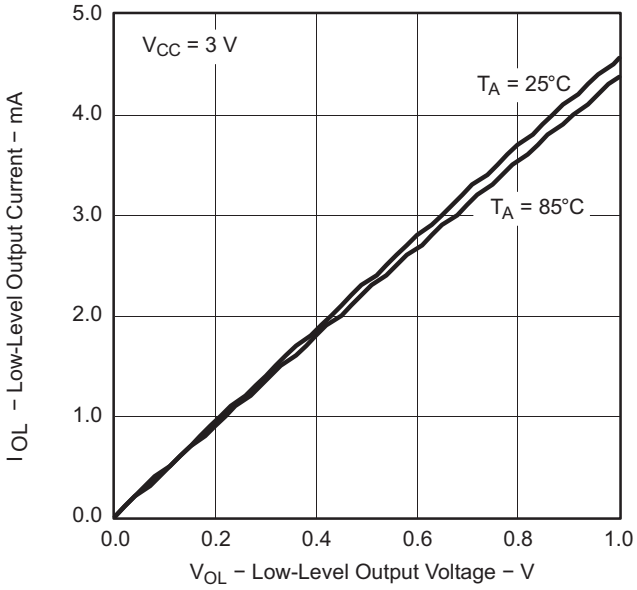



**Figure 17. USI Low-Level Output Voltage vs Output Current**

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## Comparator_A+

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{(DD)}$ | | CAON = 1, CARSEL = 0, CAREF = 0 | 3 V | | 45 | | µA |
| $I_{(Refladder/RefDiode)}$ | | CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at CA0 and CA1 | 3 V | | 45 | | µA |
| $V_{(IC)}$ | Common-mode input voltage | CAON = 1 | 3 V | 0 | | $V_{CC}$ – 1 | V |
| $V_{(Ref025)}$ | (Voltage at 0.25 $V_{CC}$ node) ÷ $V_{CC}$ | PCA0 = 1, CARSEL = 1, CAREF = 1, No load at CA0 and CA1 | 3 V | | 0.24 | | |
| $V_{(Ref050)}$ | (Voltage at 0.5 $V_{CC}$ node) ÷ $V_{CC}$ | PCA0 = 1, CARSEL = 1, CAREF = 2, No load at CA0 and CA1 | 3 V | | 0.48 | | |
| $V_{(RefVT)}$ | See Figure 18 and Figure 19 | PCA0 = 1, CARSEL = 1, CAREF = 3, No load at CA0 and CA1, $T_A$ = 85°C | 3 V | | 490 | | mV |
| $V_{(offset)}$ | Offset voltage(1) | | 3 V | | ±10 | | mV |
| $V_{hys}$ | Input hysteresis | CAON = 1 | 3 V | | 0.7 | | mV |
| $t_{(response)}$ | Response time (low-high and high-low) | $T_A$ = 25°C, Overdrive 10 mV, Without filter: CAF = 0 | 3 V | | 120 | | ns |
| | | $T_A$ = 25°C, Overdrive 10 mV, With filter: CAF = 1 | | | 1.5 | | µs |

(1) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.


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## Typical Characteristics – Comparator_A+

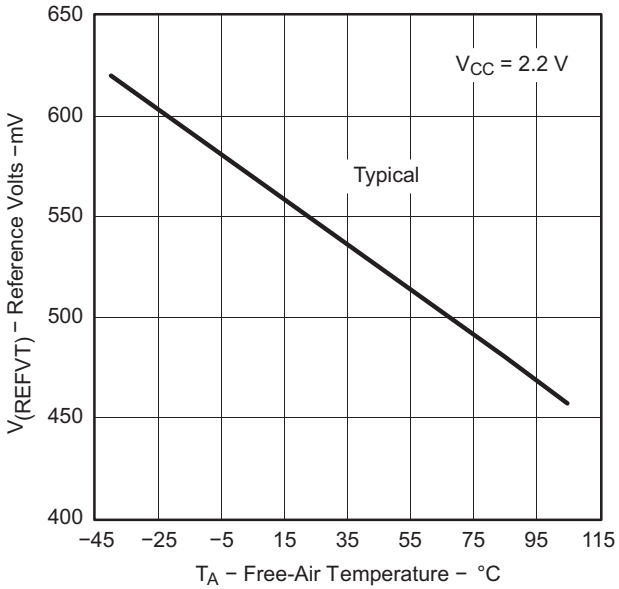



**Figure 18. $V_{(RefVT)}$ vs Temperature, $V_{CC}$ = 2.2 V**

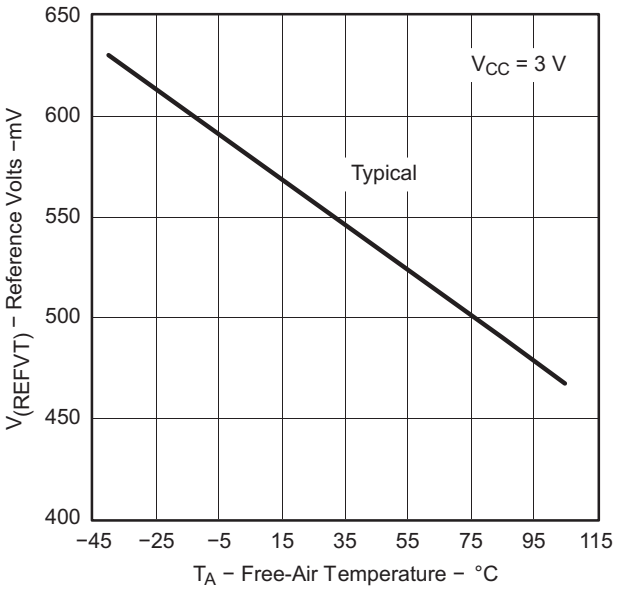



**Figure 19. $V_{(RefVT)}$ vs Temperature, $V_{CC}$ = 3 V**

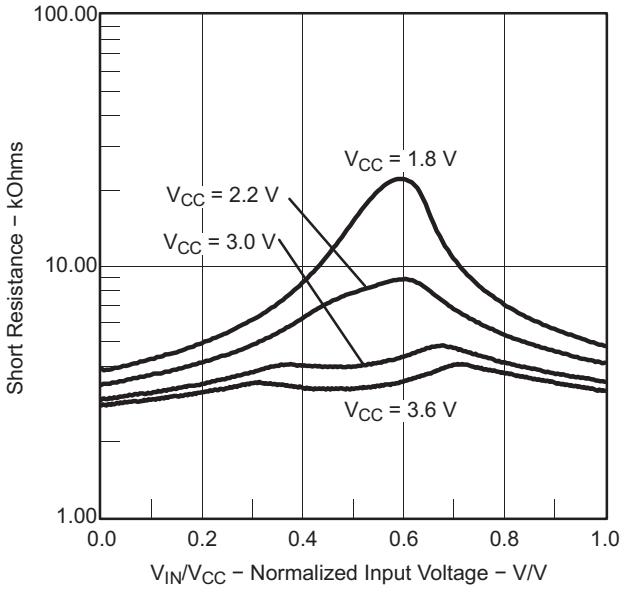



**Figure 20. Short Resistance vs $V_{IN}/V_{CC}$**

## 10-Bit ADC, Power Supply and Input Range Conditions (MSP430G2x52 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Analog supply voltage | $V_{SS}$ = 0 V | | | 2.2 | | 3.6 | V |
| $V_{Ax}$ | Analog input voltage(2) | All Ax terminals, Analog inputs selected in ADC10AE register | | 3 V | 0 | | $V_{CC}$ | V |
| $I_{ADC10}$ | ADC10 supply current(3) | $f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0 | 25°C | 3 V | | 0.6 | | mA |
| $I_{REF+}$ | Reference supply current, reference buffer disabled(4) | $f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0 | 25°C | 3 V | | 0.25 | | mA |
| | | $f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0 | | | | 0.25 | | |
| $I_{REFB,0}$ | Reference buffer supply current with ADC10SR = 0(4) | $f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0 | 25°C | 3 V | | 1.1 | | mA |
| $I_{REFB,1}$ | Reference buffer supply current with ADC10SR = 1(4) | $f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1 | 25°C | 3 V | | 0.5 | | mA |
| $C_I$ | Input capacitance | Only one terminal Ax can be selected at one time | 25°C | 3 V | | | 27 | pF |
| $R_I$ | Input MUX ON resistance | 0 V ≤ $V_{Ax}$ ≤ $V_{CC}$ | 25°C | 3 V | | 1000 | | Ω |

(1) The leakage current is defined in the leakage current table with Px.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range $V_{R+}$ to $V_{R-}$ for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter $I_{ADC10}$.
(4) The internal reference current is supplied via terminal $V_{CC}$. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.


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## 10-Bit ADC, Built-In Voltage Reference (MSP430G2x52 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC,REF+}$ | Positive built-in reference analog supply voltage range | $I_{VREF+} \le 1$ mA, REF2_5V = 0 | | 2.2 | | | V |
| | | $I_{VREF+} \le 1$ mA, REF2_5V = 1 | | 2.9 | | | |
| $V_{REF+}$ | Positive built-in reference voltage | $I_{VREF+} \le I_{VREF+}$max, REF2_5V = 0 | 3 V | 1.41 | 1.5 | 1.59 | V |
| | | $I_{VREF+} \le I_{VREF+}$max, REF2_5V = 1 | | 2.35 | 2.5 | 2.65 | |
| $I_{LD,VREF+}$ | Maximum VREF+ load current | | 3 V | | | ±1 | mA |
| | VREF+ load regulation | $I_{VREF+}$ = 500 µA ± 100 µA, Analog input voltage $V_{Ax} \approx 0.75$ V, REF2_5V = 0 | 3 V | | | ±2 | LSB |
| | | $I_{VREF+}$ = 500 µA ± 100 µA, Analog input voltage $V_{Ax} \approx 1.25$ V, REF2_5V = 1 | | | | ±2 | |
| | $V_{REF+}$ load regulation response time | $I_{VREF+}$ = 100 µA→900 µA, $V_{Ax} \approx 0.5 \times$ VREF+, Error of conversion result ≤ 1 LSB, ADC10SR = 0 | 3 V | | | 400 | ns |
| $C_{VREF+}$ | Maximum capacitance at pin VREF+ | $I_{VREF+} \le$ ±1 mA, REFON = 1, REFOUT = 1 | 3 V | | | 100 | pF |
| $TC_{REF+}$ | Temperature coefficient | $I_{VREF+}$ = const with 0 mA ≤ $I_{VREF+}$ ≤ 1 mA | 3 V | | | ±100 | ppm/°C |
| $t_{REFON}$ | Settling time of internal reference voltage to 99.9% VREF | $I_{VREF+}$ = 0.5 mA, REF2_5V = 0, REFON = 0 → 1 | 3.6 V | | | 30 | µs |
| $t_{REFBURST}$ | Settling time of reference buffer to 99.9% VREF | $I_{VREF+}$ = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1, ADC10SR = 0 | 3 V | | | 2 | µs |

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## 10-Bit ADC, External Reference[1] (MSP430G2x52 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| VEREF+ | Positive external reference input voltage range[2] | VEREF+ > VEREF–, SREF1 = 1, SREF0 = 0 | | 1.4 | | $V_{CC}$ | V |
| | | VEREF– ≤ VEREF+ ≤ $V_{CC}$ – 0.15 V, SREF1 = 1, SREF0 = 1[3] | | 1.4 | | 3 | |
| VEREF– | Negative external reference input voltage range[4] | VEREF+ > VEREF– | | 0 | | 1.2 | V |
| ΔVEREF | Differential external reference input voltage range, ΔVEREF = VEREF+ – VEREF– | VEREF+ > VEREF–[5] | | 1.4 | | $V_{CC}$ | V |
| $I_{VEREF+}$ | Static input current into VEREF+ | 0 V ≤ VEREF+ ≤ $V_{CC}$, SREF1 = 1, SREF0 = 0 | 3 V | | ±1 | | μA |
| | | 0 V ≤ VEREF+ ≤ $V_{CC}$ – 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1[3] | | | 0 | | |
| $I_{VEREF–}$ | Static input current into VEREF– | 0 V ≤ VEREF– ≤ $V_{CC}$ | 3 V | | ±1 | | μA |

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, $C_I$, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current $I_{REFB}$. The current consumption can be limited to the sample and conversion period with REBURST = 1.
(4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

## 10-Bit ADC, Timing Parameters (MSP430G2x52 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{ADC10CLK}$ | ADC10 input clock frequency | For specified performance of ADC10 linearity parameters | ADC10SR = 0 | 3 V | 0.45 | | 6.3 | MHz |
| | | | ADC10SR = 1 | | 0.45 | | 1.5 | |
| $f_{ADC10OSC}$ | ADC10 built-in oscillator frequency | ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$ | | 3 V | 3.7 | | 6.3 | MHz |
| $t_{CONVERT}$ | Conversion time | ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$ | | 3 V | 2.06 | | 3.51 | μs |
| | | $f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0 | | | 13 × ADC10DIV × $1/f_{ADC10CLK}$ | | | |
| $t_{ADC10ON}$ | Turn-on settling time of the ADC | (1) | | | | | 100 | ns |

(1) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

## 10-Bit ADC, Linearity Parameters (MSP430G2x52 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error | | 3 V | | | ±1 | LSB |
| $E_D$ | Differential linearity error | | 3 V | | | ±1 | LSB |
| $E_O$ | Offset error | Source impedance $R_S$ < 100 Ω | 3 V | | | ±1 | LSB |
| $E_G$ | Gain error | | 3 V | | ±1.1 | ±2 | LSB |
| $E_T$ | Total unadjusted error | | 3 V | | ±2 | ±5 | LSB |


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## 10-Bit ADC, Temperature Sensor and Built-In $V_{MID}$ (MSP430G2x52 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{SENSOR}$ | Temperature sensor supply current (1) | REFON = 0, INCHx = 0Ah, $T_A$ = 25°C | 3 V | | 60 | | µA |
| $TC_{SENSOR}$ | | ADC10ON = 1, INCHx = 0Ah (2) | 3 V | | 3.55 | | mV/°C |
| $t_{Sensor(sample)}$ | Sample time required if channel 10 is selected (3) | ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB | 3 V | 30 | | | µs |
| $I_{VMID}$ | Current into divider at channel 11 | ADC10ON = 1, INCHx = 0Bh | 3 V | | | (4) | µA |
| $V_{MID}$ | $V_{CC}$ divider at channel 11 | ADC10ON = 1, INCHx = 0Bh, $V_{MID} \neq 0.5 \times V_{CC}$ | 3 V | | 1.5 | | V |
| $t_{VMID(sample)}$ | Sample time required if channel 11 is selected (5) | ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB | 3 V | 1220 | | | ns |

(1) The sensor current $I_{SENSOR}$ is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, $I_{SENSOR}$ is included in $I_{REF+}$. When REFON = 0, $I_{SENSOR}$ applies during conversion of the temperature sensor input (INCH = 0Ah).
(2) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C] ) + $V_{Offset,sensor}$ [mV] or
$V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A = 0°C)$ [mV]
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) No additional current is needed. The $V_{MID}$ is used during sampling.
(5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

## Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC(PGM/ERASE)}$ | Program and erase supply voltage | | | 2.2 | | 3.6 | V |
| $f_{FTG}$ | Flash timing generator frequency | | | 257 | | 476 | kHz |
| $I_{PGM}$ | Supply current from $V_{CC}$ during program | | 2.2 V/3.6 V | | 1 | 5 | mA |
| $I_{ERASE}$ | Supply current from $V_{CC}$ during erase | | 2.2 V/3.6 V | | 1 | 7 | mA |
| $t_{CPT}$ | Cumulative program time (1) | | 2.2 V/3.6 V | | | 10 | ms |
| $t_{CMErase}$ | Cumulative mass erase time | | 2.2 V/3.6 V | 20 | | | ms |
| | Program/erase endurance | | | $10^4$ | $10^5$ | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J$ = 25°C | | 100 | | | years |
| $t_{Word}$ | Word or byte program time | (2) | | | 30 | | $t_{FTG}$ |
| $t_{Block, 0}$ | Block program time for first byte or word | (2) | | | 25 | | $t_{FTG}$ |
| $t_{Block, 1-63}$ | Block program time for each additional byte or word | (2) | | | 18 | | $t_{FTG}$ |
| $t_{Block, End}$ | Block program end-sequence wait time | (2) | | | 6 | | $t_{FTG}$ |
| $t_{Mass\ Erase}$ | Mass erase time | (2) | | | 10593 | | $t_{FTG}$ |
| $t_{Seg\ Erase}$ | Segment erase time | (2) | | | 4819 | | $t_{FTG}$ |

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

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## RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{(RAMh)}$ | RAM retention supply voltage (1) | CPU halted | 1.6 | | V |

(1) This parameter defines the minimum supply voltage $V_{CC}$ when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

## JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{SBW}$ | Spy-Bi-Wire input frequency | | 2.2 V | 0 | | 20 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse length | | 2.2 V | 0.025 | | 15 | µs |
| $t_{SBW,En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge(1)) | | 2.2 V | | | 1 | µs |
| $t_{SBW,Ret}$ | Spy-Bi-Wire return to normal operation time | | 2.2 V | 15 | | 100 | µs |
| $f_{TCK}$ | TCK input frequency(2) | | 2.2 V | 0 | | 5 | MHz |
| $R_{Internal}$ | Internal pulldown resistance on TEST | | 2.2 V | 25 | 60 | 90 | kΩ |

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
(2) $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.

## JTAG Fuse(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

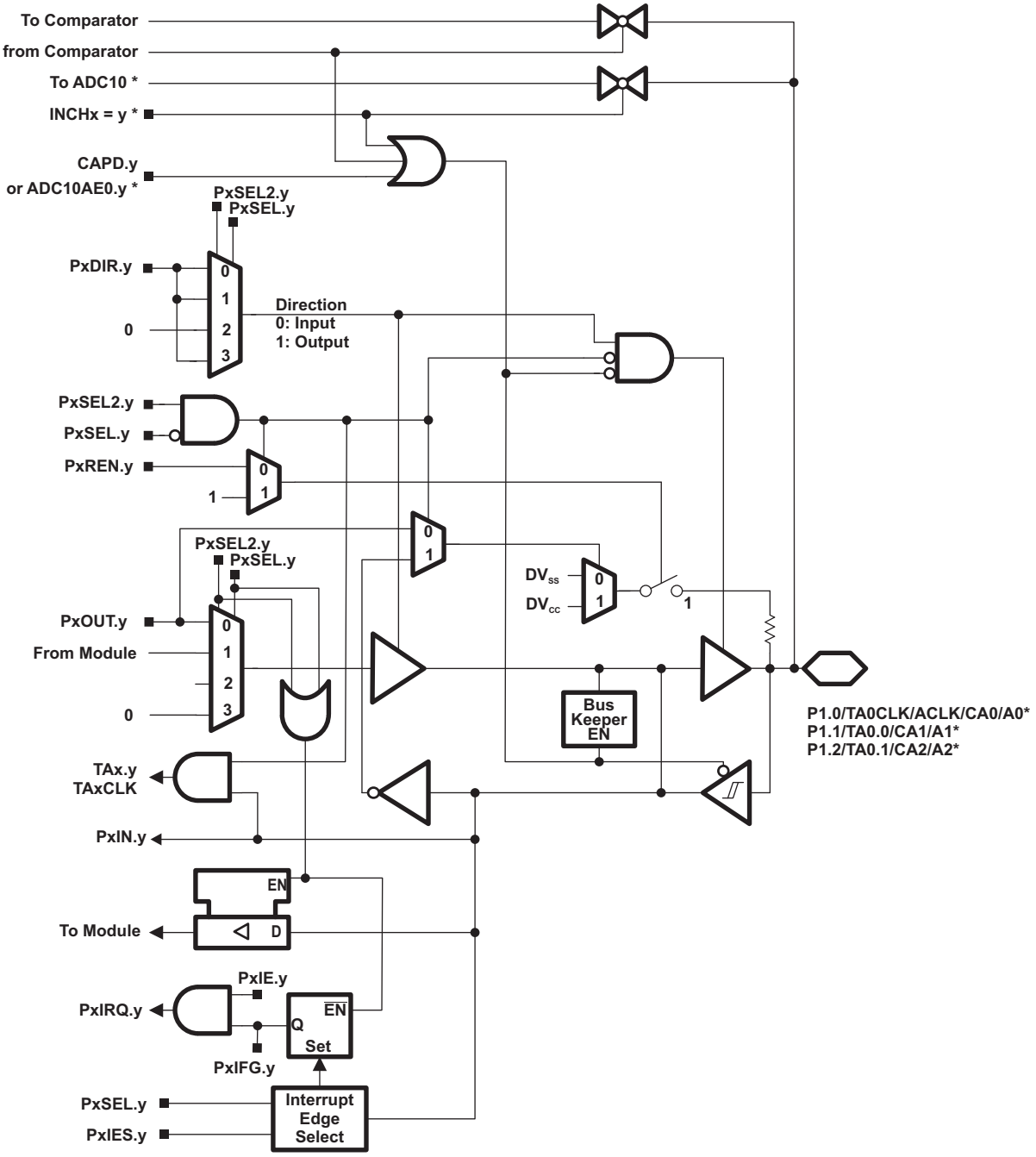
| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC(FB)}$ | Supply voltage during fuse-blow condition | $T_A$ = 25°C | 2.5 | | V |
| $V_{FB}$ | Voltage level on TEST for fuse blow | | 6 | 7 | V |
| $I_{FB}$ | Supply current into TEST during fuse blow | | | 100 | mA |
| $t_{FB}$ | Time to blow fuse | | | 1 | ms |

(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.


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## PIN SCHEMATICS

### Port P1 Pin Schematic: P1.0 to P1.2, Input/Output With Schmitt Trigger




* Note: MSP430G2x32 devices only. MSP430G2x22 devices have no ADC10.

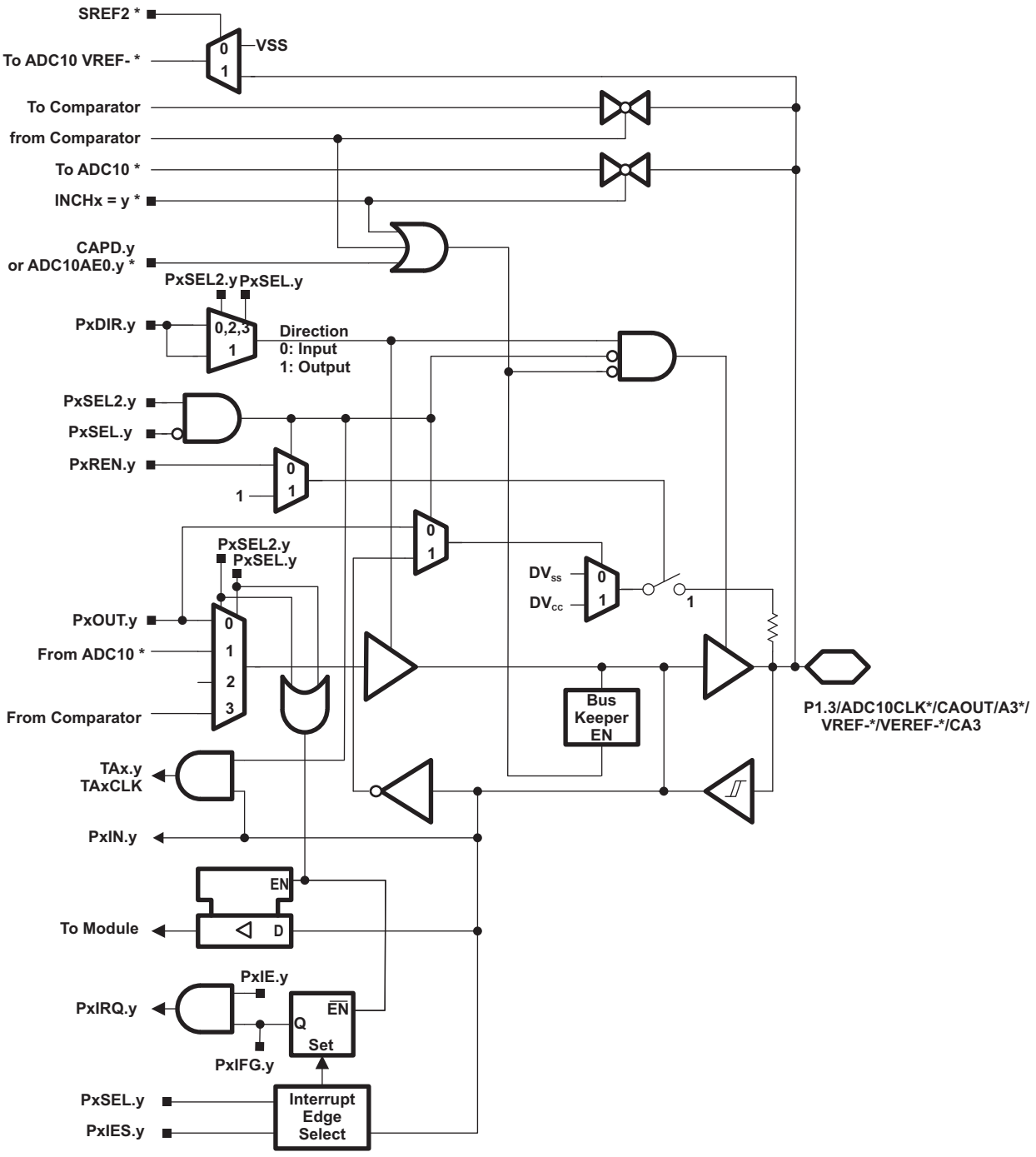
## Table 14. Port P1 (P1.0 to P1.2) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | | | |
|---|---|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x | from Comparator | ADC10AE.x (INCH.y=1)[2] |
| P1.0/ | 0 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 |
| TA0CLK/ | | TA0.TACLK | 0 | 1 | 0 | 0 | 0 |
| ACLK/ | | ACLK | 1 | 1 | 0 | 0 | 0 |
| A0[2]/ | | A0 | X | X | X | 0 | 1 (y = 0) |
| CA0/ | | CA0 | X | X | X | 1 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 | 0 | 0 |
| P1.1/ | 1 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 |
| TA0.0/ | | TA0.0 | 1 | 1 | 0 | 0 | 0 |
| | | TA0.CCI0A | 0 | 1 | 0 | 0 | 0 |
| A1[2]/ | | A1 | X | X | X | 0 | 1 (y = 1) |
| CA1/ | | CA1 | X | X | X | 1 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 | 0 | 0 |
| P1.2/ | 2 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 |
| TA0.1/ | | TA0.1 | 1 | 1 | 0 | 0 | 0 |
| | | TA0.CCI1A | 0 | 1 | 0 | 0 | 0 |
| A2[2]/ | | A2 | X | X | X | 0 | 1 (y = 2) |
| CA2/ | | CA2 | X | X | X | 1 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 | 0 | 0 |

(1) X = don't care
(2) MSP430G2x52 devices only


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## Port P1 Pin Schematic: P1.3, Input/Output With Schmitt Trigger




* Note: MSP430G2x52 devices only. MSP430G2x12 devices have no ADC10.

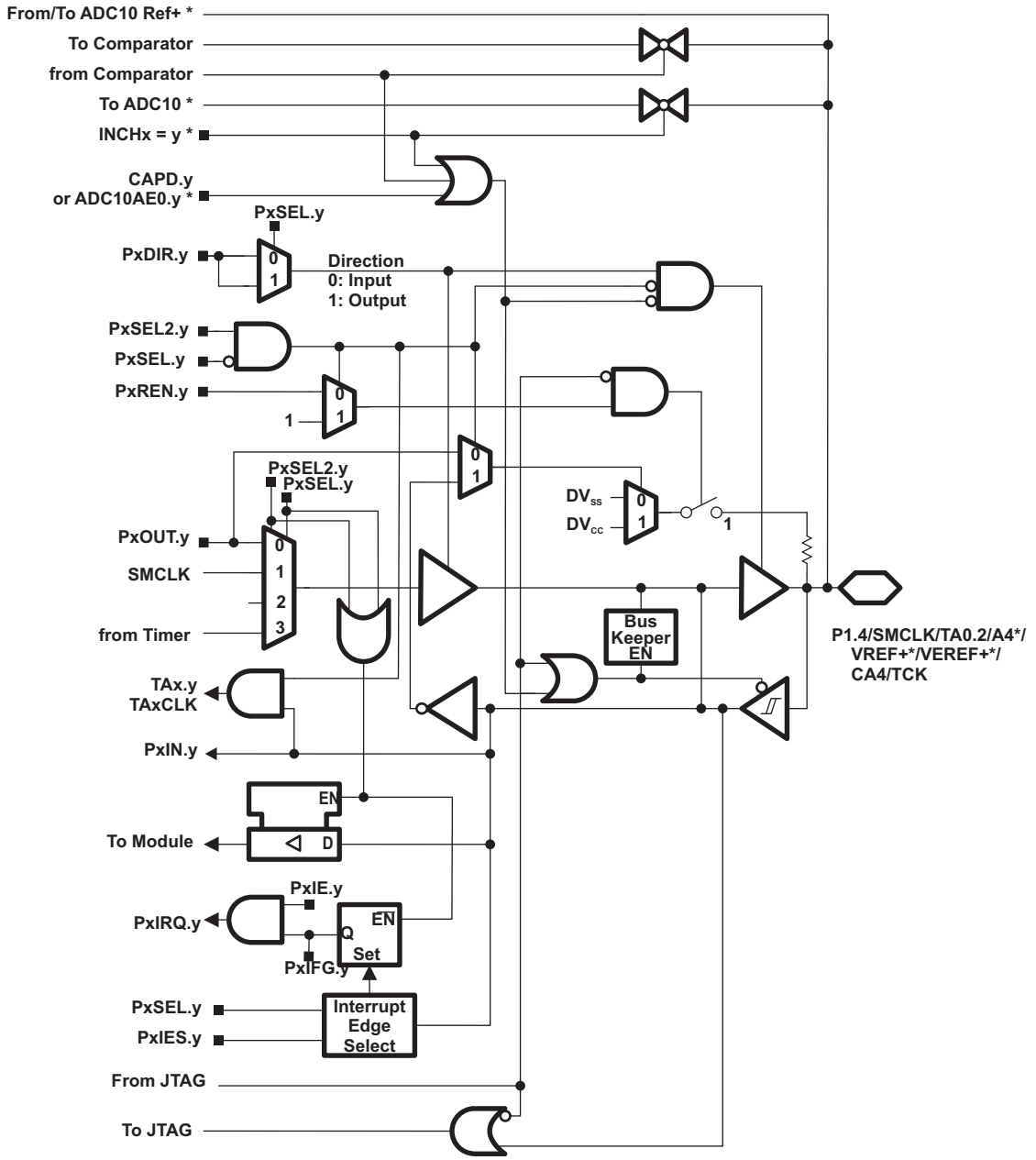
**Table 15. Port P1 (P1.3) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | | | |
|---|---|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x | from Comparator | ADC10AE.x (INCH.x=1)[2] |
| P1.3/ | 3 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 |
| ADC10CLK[2]/ | | ADC10CLK | 1 | 1 | 0 | 0 | 0 |
| CAOUT/ | | CAOUT | 1 | 1 | 1 | 0 | 0 |
| A3[2]/ | | A3 | X | X | X | 0 | 1 (y = 3) |
| VREF-[2]/ | | VREF- | X | X | X | 0 | 1 |
| VEREF-[2]/ | | VEREF- | X | X | X | 0 | 1 |
| CA3/ | | CA3 | X | X | X | 1 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 | 0 | 0 |

(1) X = don't care
(2) MSP430G2x52 devices only


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## Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger




* Note: MSP430G2x52 devices only. MSP430G2x12 devices have no ADC10.

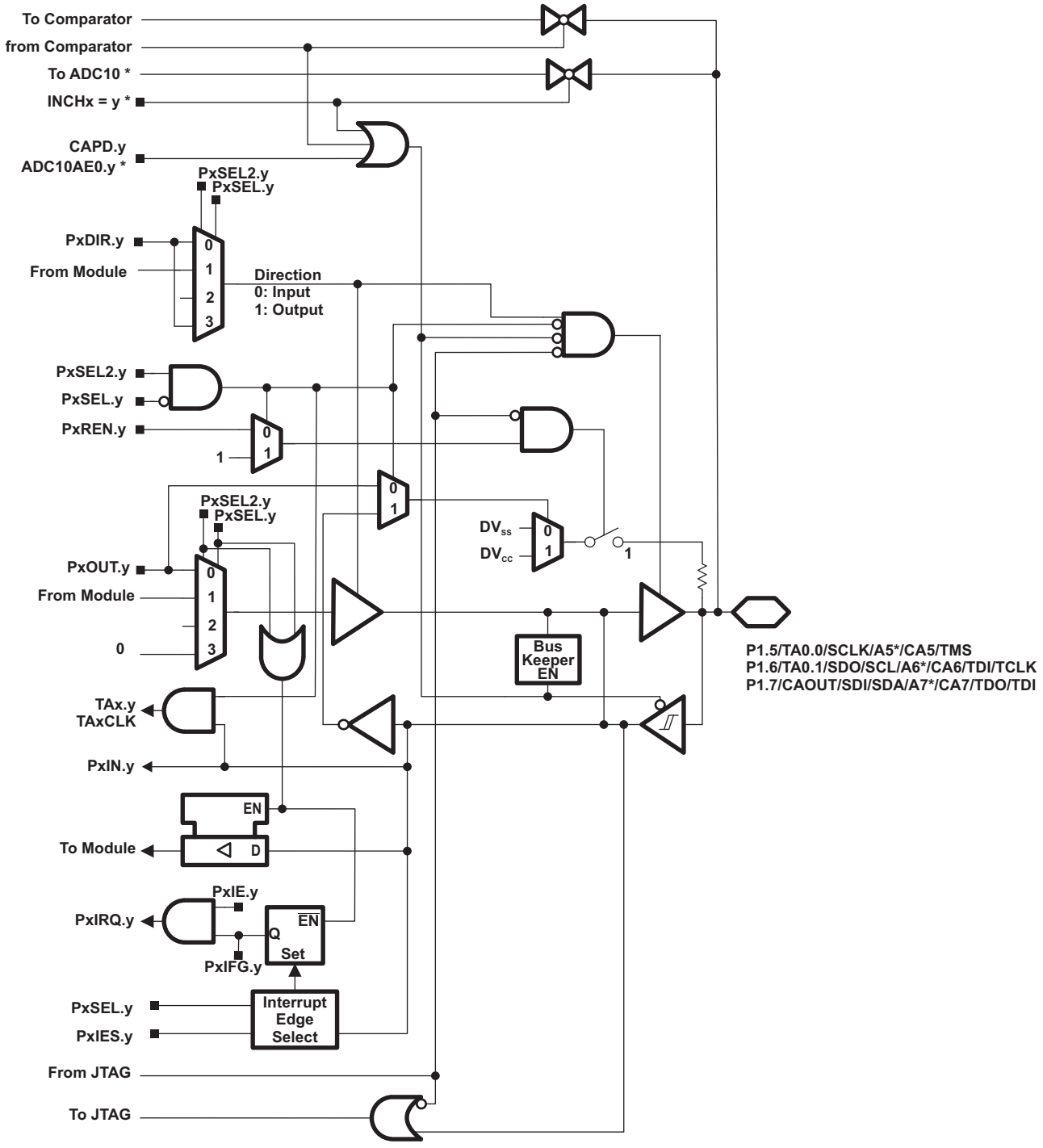
**Table 16. Port P1 (P1.4) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x | ADC10AE.x (INCH.x=1)[2] | JTAG Mode | CAPD.y |
| P1.4/ | 4 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 |
| SMCLK/ | | SMCLK | 1 | 1 | 0 | 0 | 0 | 0 |
| TA0.2/ | | TA0.2 | 1 | 1 | 1 | 0 | 0 | 0 |
| | | TA0.CCI2A | 0 | 1 | 1 | 0 | 0 | 0 |
| VREF+[2]/ | | VREF+ | X | X | X | 1 | 0 | 0 |
| VEREF+[2]/ | | VEREF+ | X | X | X | 1 | 0 | 0 |
| A4[2]/ | | A4 | X | X | X | 1 (y = 4) | 0 | 0 |
| CA4/ | | CA4 | X | X | X | 0 | 0 | 1 (y = 4) |
| TCK/ | | TCK | X | X | X | 0 | 1 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 | 0 | 0 | 0 |

(1) X = don't care
(2) MSP430G2x52 devices only


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## Port P1 Pin Schematic: P1.5 to P1.7, Input/Output With Schmitt Trigger




*** Note: MSP430G2x52 devices only. MSP430G2x12 devices have no ADC10.**

## Table 17. Port P1 (P1.5 to P1.7) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1SEL2.x | USIP.x | JTAG Mode | CAPD.y | ADC10AE.x (INCH.x=1)[2] |
| P1.5/ | 5 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| TA0.0/ | | TA0.0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| SCLK/ | | SPI mode | from USI | 1 | 0 | 1 | 0 | 0 | 0 |
| A5[2]/ | | A5 | X | X | X | X | 0 | 0 | 1 (y = 5) |
| CA5/ | | CA5 | X | X | X | X | 0 | 1 | 0 |
| TMS/ | | TMS | X | X | X | X | 1 | X | X |
| Pin Osc | | Capacitive sensing | X | 0 | 1 | X | 0 | 0 | 0 |
| P1.6/ | 6 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| TA0.1/ | | TA0.1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| SDO/ | | SPI mode | from USI | 1 | 0 | 1 | 0 | 0 | 0 |
| SCL/ | | I2C mode | from USI | 1 | 0 | 1 | 0 | 0 | 0 |
| A6[2]/ | | A6 | X | X | X | X | 0 | 0 | 1 (y = 6) |
| CA6/ | | CA6 | X | X | X | X | 0 | 1 | 0 |
| TDI/TCLK/ | | TDI/TCLK | X | X | X | X | 1 | X | X |
| Pin Osc | | Capacitive sensing | X | 0 | 1 | X | 0 | 0 | 0 |
| P1.7/ | 7 | P1.x (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| CAOUT/ | | CAOUT | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| SDI/ | | SPI mode | from USI | 1 | 0 | 1 | 0 | 0 | 0 |
| SDA/ | | I2C mode | from USI | 1 | 0 | 1 | 0 | 0 | 0 |
| A7[2]/ | | A7 | X | X | X | X | 0 | 0 | 1 (y = 7) |
| CA7/ | | CA7 | X | X | X | X | 0 | 1 | 0 |
| TDO/TDI/ | | TDO/TDI | X | X | X | X | 1 | X | X |
| Pin Osc | | Capacitive sensing | X | 0 | 1 | X | 0 | 0 | 0 |

(1) X = don't care
(2) MSP430G2x52 devices only


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## Port P2 Pin Schematic: P2.0 to P2.5, Input/Output With Schmitt Trigger

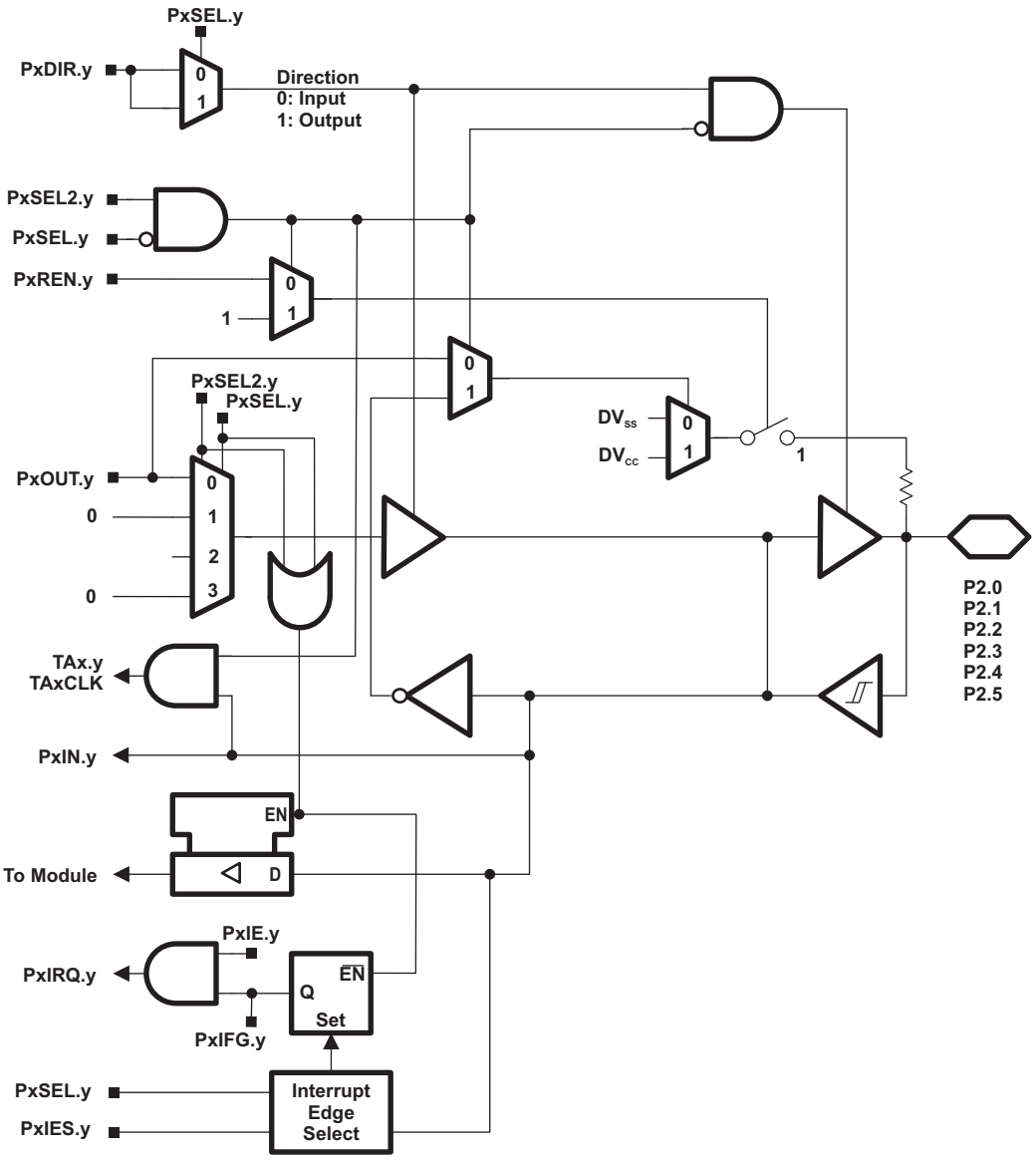


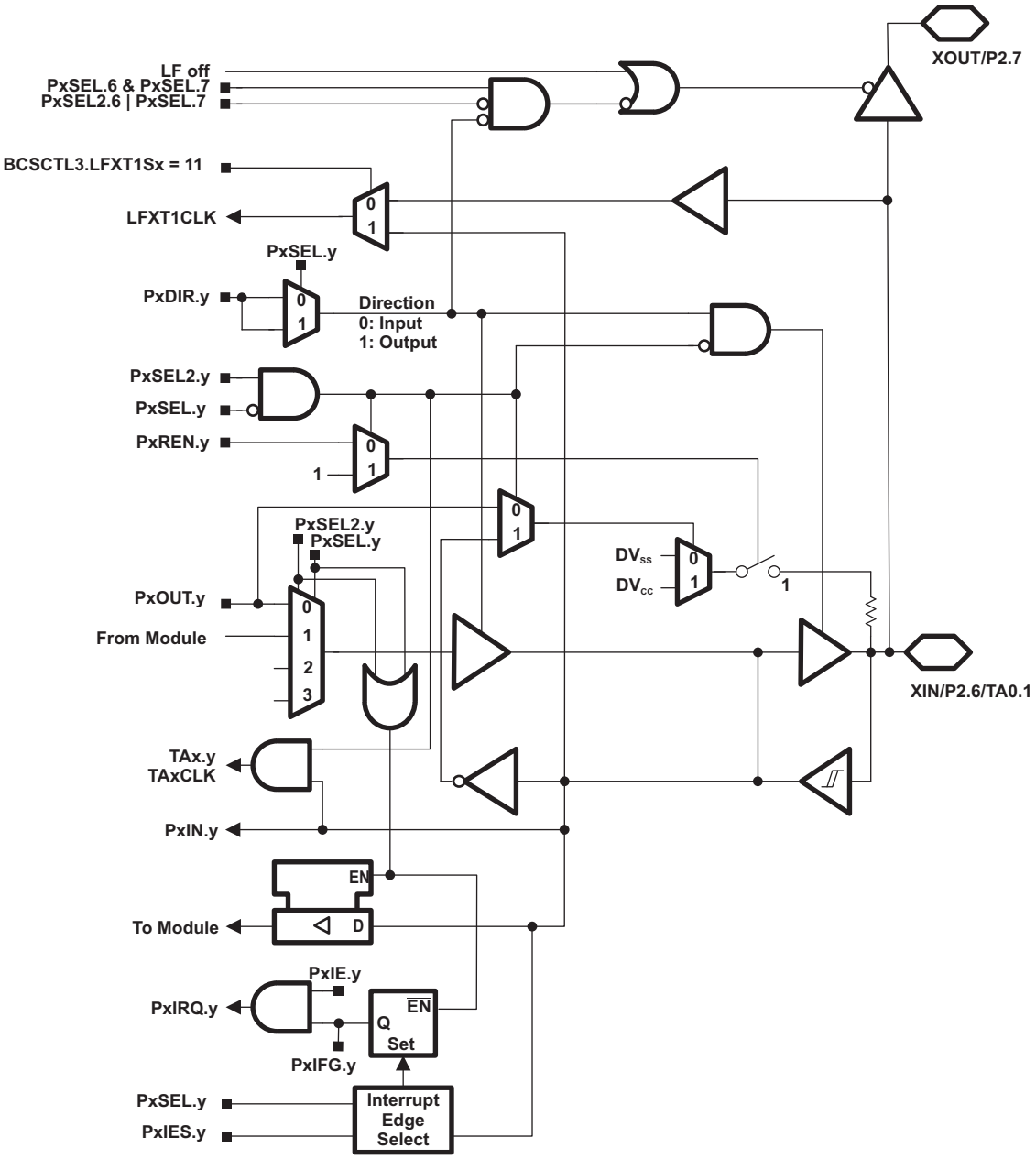
**Table 18. Port P2 (P2.0 to P2.5) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.x | P2SEL2.x |
| P2.0/ | 0 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 |
| P2.1/ | 1 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 |
| P2.2/ | 2 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 |
| P2.3/ | 3 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 |
| P2.4/ | 4 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 |
| P2.5/ | 5 | P2.x (I/O) | I: 0; O: 1 | 0 | 0 |
| Pin Osc | | Capacitive sensing | X | 0 | 1 |

(1) X = don't care


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## Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger



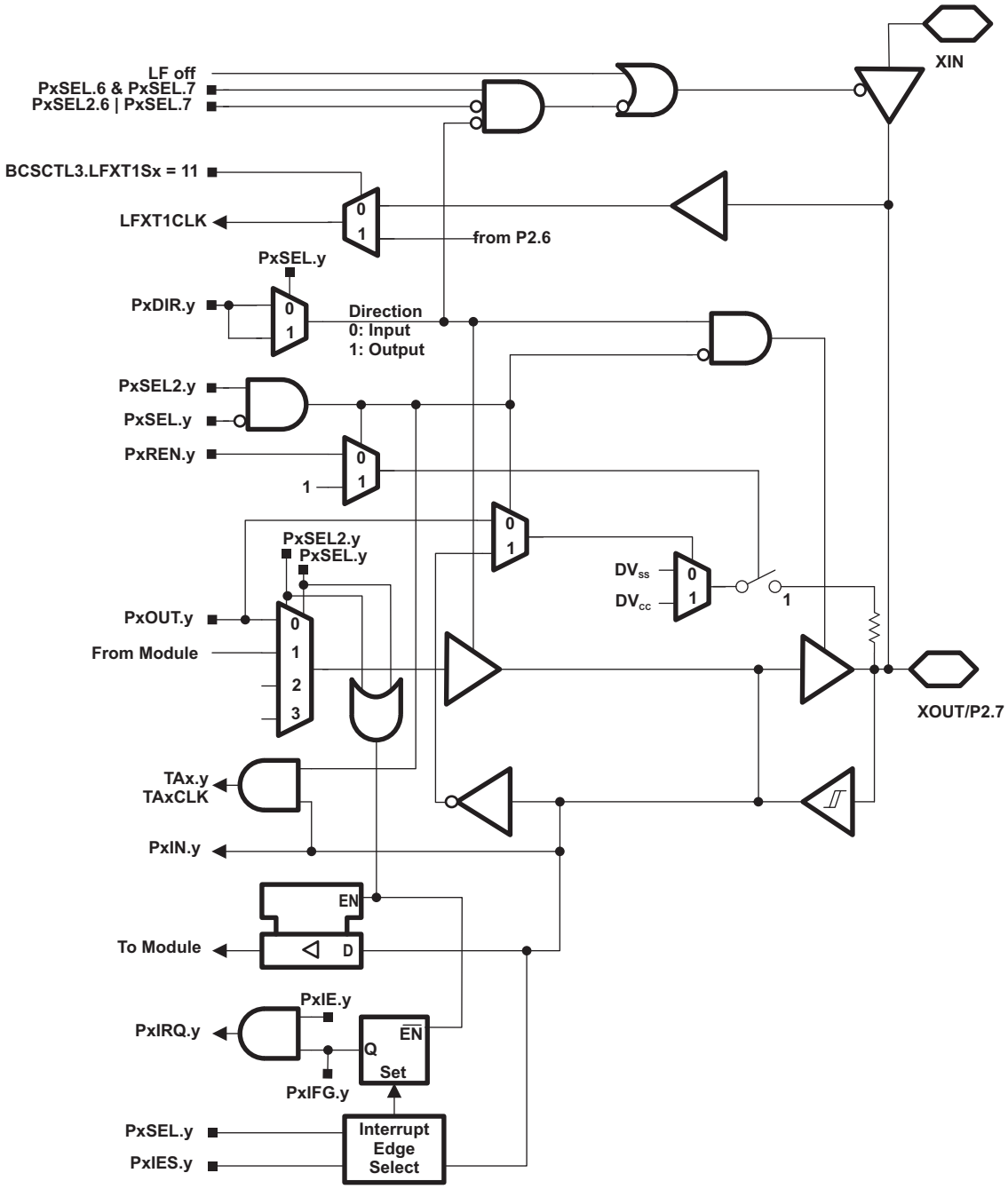

### Table 19. Port P2 (P2.6) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.6<br>P2SEL.7 | P2SEL2.6<br>P2SEL2.7 |
| XIN/ | 6 | XIN | X | 1<br>1 | 0<br>0 |
| P2.6/ | | P2.x (I/O) | I: 0; O: 1 | 0<br>X | 0<br>0 |
| TA0.1/ | | Timer0_A3.TA1 | 1 | 1<br>0 | 0<br>0 |
| Pin Osc | | Capacitive sensing | X | 0<br>X | 1<br>X |

(1) X = don't care

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## Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger




### Table 20. Port P2 (P2.7) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS[1] | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.6<br>P2SEL.7 | P2SEL2.6<br>P2SEL2.7 |
| XOUT/ | 7 | XOUT | X | 1<br>1 | 0<br>0 |
| P2.7/ | | P2.x (I/O) | I: 0; O: 1 | 0<br>X | 0<br>0 |
| Pin Osc | | Capacitive sensing | X | 0<br>X | 1<br>X |

(1) X = don't care


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## REVISION HISTORY

| REVISION | DESCRIPTION |
|---|---|
| SLAS722 | Initial release |
| SLAS722A | Page 1, Changed "Internal Frequencies up to 16 MHz With *One Calibrated Frequency*" to "Internal Frequencies up to 16 MHz With *Four Calibrated Frequencies*" |
| SLAS722B | Added note concerning pulldown resistor to PW14 and RSA16 pinout drawings.<br>Added "N20, PW20" to Input Pin Number and Output Pin Number columns in Table 11.<br>Corrected pin numbers for P1.0 to P1.3 for PW14 package in Table 2.<br>Corrected N20, PW20 Output Pin Number for TA0.0 in Table 11. (June 2011) |
| SLAS722C | Changed Storage temperature range limit in Absolute Maximum Ratings.<br>Corrected SDA pin name in Table 17. |
| SLAS722D | Changed TAG_ADC10_1 value to 0x10 in Table 9.<br>Changed $T_{stg}$, Programmed device, to -55°C to 150°C in Absolute Maximum Ratings. |
| SLAS722E | Changed all port schematics (added buffer after PxOUT.y mux) in Pin Schematics |
| SLAS722F | Table 2, Corrected typo on VEREF- (P1.3) signal name.<br>Recommended Operating Conditions, Added test conditions for typical values.<br>Pin-Oscillator Frequency – Ports Px, Corrected resistor value in note (1).<br>POR, BOR, Added note (2). |
| SLAS722G | Throughout, Changed all variations of touch sense(1) to capacitive touch. |

(1) TouchSense is a trademark of Immersion Corporation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430G2112IN20 | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2112 |
| MSP430G2112IN20.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2112 |
| MSP430G2112IN20.B | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2112 |
| MSP430G2112IPW14 | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2112 |
| MSP430G2112IPW14.A | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2112 |
| MSP430G2112IPW14.B | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2112 |
| MSP430G2112IPW14R | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2112 |
| MSP430G2112IPW14R.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2112 |
| MSP430G2112IPW14R.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2112 |
| MSP430G2112IPW20 | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2112 |
| MSP430G2112IPW20.A | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2112 |
| MSP430G2112IPW20.B | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2112 |
| MSP430G2112IRSA16T | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | M430 G2112 |
| MSP430G2112IRSA16T.A | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2112 |
| MSP430G2112IRSA16T.B | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2112 |
| MSP430G2152IN20 | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2152 |
| MSP430G2152IN20.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2152 |
| MSP430G2152IN20.B | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2152 |
| MSP430G2152IPW14 | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2152 |
| MSP430G2152IPW14.A | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2152 |
| MSP430G2152IPW14.B | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2152 |
| MSP430G2152IPW14R | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2152 |
| MSP430G2152IPW14R.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2152 |
| MSP430G2152IPW14R.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2152 |
| MSP430G2152IPW20 | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2152 |
| MSP430G2152IPW20.A | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2152 |
| MSP430G2152IPW20.B | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2152 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430G2152IPW20R | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2152 |
| MSP430G2152IPW20R.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2152 |
| MSP430G2152IPW20R.B | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2152 |
| MSP430G2152IRSA16R | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | M430 G2152 |
| MSP430G2152IRSA16R.A | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430 G2152 |
| MSP430G2152IRSA16R.B | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430 G2152 |
| MSP430G2152IRSA16T | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | M430 G2152 |
| MSP430G2152IRSA16T.A | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2152 |
| MSP430G2152IRSA16T.B | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2152 |
| MSP430G2212IN20 | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2212 |
| MSP430G2212IN20.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2212 |
| MSP430G2212IN20.B | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2212 |
| MSP430G2212IPW14 | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2212 |
| MSP430G2212IPW14.A | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2212 |
| MSP430G2212IPW14.B | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2212 |
| MSP430G2212IPW14R | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2212 |
| MSP430G2212IPW14R.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2212 |
| MSP430G2212IPW14R.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2212 |
| MSP430G2212IPW20 | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2212 |
| MSP430G2212IPW20.A | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2212 |
| MSP430G2212IPW20.B | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2212 |
| MSP430G2212IPW20R | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2212 |
| MSP430G2212IPW20R.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2212 |
| MSP430G2212IPW20R.B | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2212 |
| MSP430G2212IRSA16R | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | M430 G2212 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430G2212IRSA16R.A | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2212 |
| MSP430G2212IRSA16R.B | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2212 |
| MSP430G2212IRSA16T | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | M430 G2212 |
| MSP430G2212IRSA16T.A | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2212 |
| MSP430G2212IRSA16T.B | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2212 |
| MSP430G2252IN20 | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2252 |
| MSP430G2252IN20.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2252 |
| MSP430G2252IN20.B | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2252 |
| MSP430G2252IPW14 | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2252 |
| MSP430G2252IPW14.A | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2252 |
| MSP430G2252IPW14.B | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2252 |
| MSP430G2252IPW14R | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2252 |
| MSP430G2252IPW14R.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2252 |
| MSP430G2252IPW14R.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2252 |
| MSP430G2252IPW20 | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2252 |
| MSP430G2252IPW20.A | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2252 |
| MSP430G2252IPW20.B | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2252 |
| MSP430G2252IPW20R | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2252 |
| MSP430G2252IPW20R.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2252 |
| MSP430G2252IPW20R.B | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2252 |
| MSP430G2252IRSA16R | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | M430 G2252 |
| MSP430G2252IRSA16R.A | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430 G2252 |
| MSP430G2252IRSA16R.B | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430 G2252 |
| MSP430G2252IRSA16T | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | M430 G2252 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430G2252IRSA16T.A | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2252 |
| MSP430G2252IRSA16T.B | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2252 |
| MSP430G2312IN20 | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2312 |
| MSP430G2312IN20.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2312 |
| MSP430G2312IN20.B | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2312 |
| MSP430G2312IPW14 | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2312 |
| MSP430G2312IPW14.A | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2312 |
| MSP430G2312IPW14.B | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2312 |
| MSP430G2312IPW14R | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2312 |
| MSP430G2312IPW14R.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2312 |
| MSP430G2312IPW14R.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2312 |
| MSP430G2312IPW20 | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2312 |
| MSP430G2312IPW20.A | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2312 |
| MSP430G2312IPW20.B | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2312 |
| MSP430G2312IPW20R | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2312 |
| MSP430G2312IPW20R.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2312 |
| MSP430G2312IPW20R.B | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2312 |
| MSP430G2312IRSA16R | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | M430 G2312 |
| MSP430G2312IRSA16R.A | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430 G2312 |
| MSP430G2312IRSA16R.B | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430 G2312 |
| MSP430G2312IRSA16T | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | M430 G2312 |
| MSP430G2312IRSA16T.A | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2312 |
| MSP430G2312IRSA16T.B | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2312 |
| MSP430G2352IN20 | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2352 |
| MSP430G2352IN20.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2352 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430G2352IN20.B | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2352 |
| MSP430G2352IPW14 | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2352 |
| MSP430G2352IPW14.A | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2352 |
| MSP430G2352IPW14.B | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2352 |
| MSP430G2352IPW14G4 | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2352 |
| MSP430G2352IPW14G4.A | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2352 |
| MSP430G2352IPW14G4.B | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2352 |
| MSP430G2352IPW14R | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2352 |
| MSP430G2352IPW14R.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2352 |
| MSP430G2352IPW14R.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2352 |
| MSP430G2352IPW20 | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2352 |
| MSP430G2352IPW20.A | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2352 |
| MSP430G2352IPW20.B | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2352 |
| MSP430G2352IPW20R | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2352 |
| MSP430G2352IPW20R.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2352 |
| MSP430G2352IPW20R.B | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2352 |
| MSP430G2352IRSA16R | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | M430 G2352 |
| MSP430G2352IRSA16R.A | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2352 |
| MSP430G2352IRSA16R.B | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2352 |
| MSP430G2352IRSA16T | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | M430 G2352 |
| MSP430G2352IRSA16T.A | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2352 |
| MSP430G2352IRSA16T.B | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2352 |
| MSP430G2412IN20 | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2412 |
| MSP430G2412IN20.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2412 |
| MSP430G2412IN20.B | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2412 |
| MSP430G2412IPW14 | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2412 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430G2412IPW14.A | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2412 |
| MSP430G2412IPW14.B | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2412 |
| MSP430G2412IPW14R | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2412 |
| MSP430G2412IPW14R.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2412 |
| MSP430G2412IPW14R.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2412 |
| MSP430G2412IPW20 | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2412 |
| MSP430G2412IPW20.A | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2412 |
| MSP430G2412IPW20.B | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2412 |
| MSP430G2412IPW20R | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2412 |
| MSP430G2412IPW20R.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2412 |
| MSP430G2412IPW20R.B | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2412 |
| MSP430G2412IRSA16T | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | M430 G2412 |
| MSP430G2412IRSA16T.A | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2412 |
| MSP430G2412IRSA16T.B | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2412 |
| MSP430G2452IN20 | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2452 |
| MSP430G2452IN20.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2452 |
| MSP430G2452IN20.B | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430G2452 |
| MSP430G2452IPW14 | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2452 |
| MSP430G2452IPW14.A | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2452 |
| MSP430G2452IPW14.B | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2452 |
| MSP430G2452IPW14R | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2452 |
| MSP430G2452IPW14R.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2452 |
| MSP430G2452IPW14R.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | G2452 |
| MSP430G2452IPW20 | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2452 |
| MSP430G2452IPW20.A | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2452 |
| MSP430G2452IPW20.B | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2452 |
| MSP430G2452IPW20R | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2452 |
| MSP430G2452IPW20R.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2452 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430G2452IPW20R.B | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 430G2452 |
| MSP430G2452IRSA16R | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | M430 G2452 |
| MSP430G2452IRSA16R.A | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430 G2452 |
| MSP430G2452IRSA16R.B | Active | Production | QFN (RSA) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | M430 G2452 |
| MSP430G2452IRSA16T | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 85 | M430 G2452 |
| MSP430G2452IRSA16T.A | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2452 |
| MSP430G2452IRSA16T.B | Active | Production | QFN (RSA) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430 G2452 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

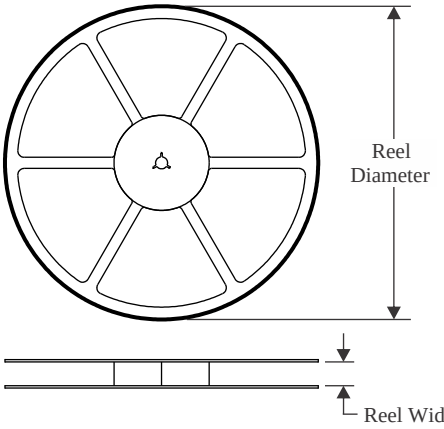
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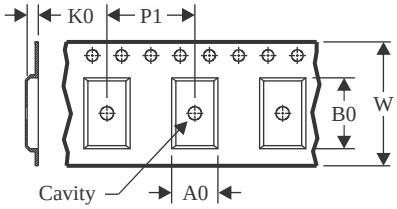
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

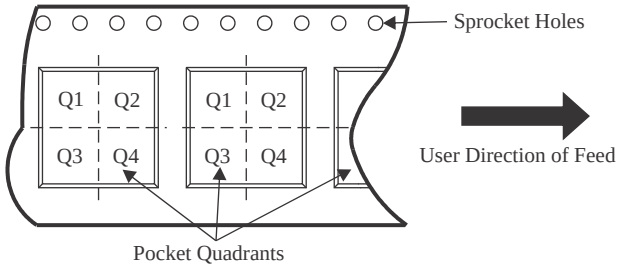



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



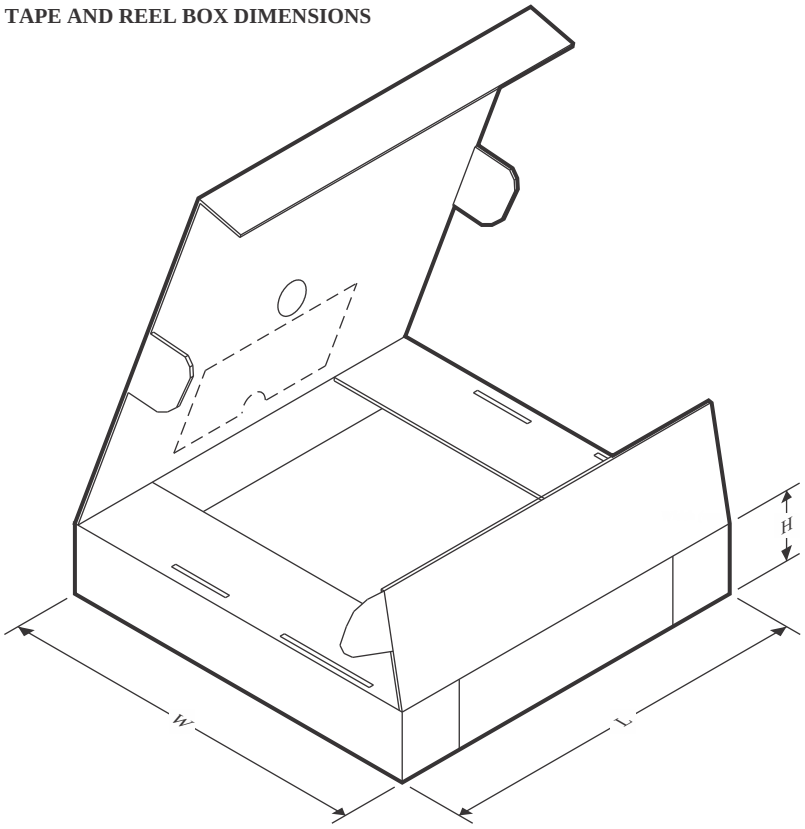

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430G2112IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2112IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2112IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2112IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2152IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2152IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2152IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| MSP430G2152IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| MSP430G2152IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2152IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2152IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2152IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2212IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2212IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2212IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| MSP430G2212IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430G2212IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2212IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2212IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2212IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2252IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2252IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2252IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| MSP430G2252IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| MSP430G2252IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2252IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2252IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2252IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2312IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2312IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2312IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| MSP430G2312IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| MSP430G2312IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2312IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2312IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2312IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2352IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2352IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2352IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| MSP430G2352IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| MSP430G2352IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2352IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2352IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2352IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2412IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2412IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2412IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| MSP430G2412IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| MSP430G2412IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2412IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2452IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2452IPW14R | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430G2452IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| MSP430G2452IPW20R | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| MSP430G2452IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2452IRSA16R | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430G2452IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430G2452IRSA16T | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

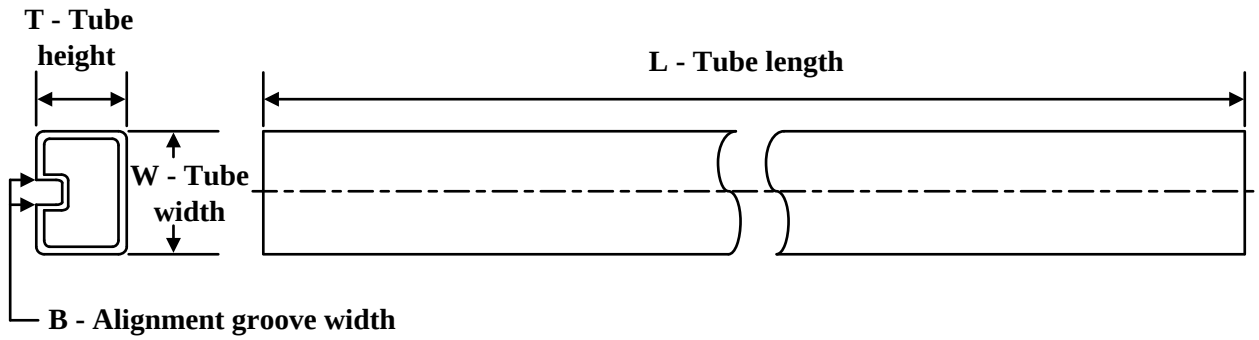



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430G2112IPW14R | TSSOP | PW | 14 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2112IPW14R | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2112IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2112IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2152IPW14R | TSSOP | PW | 14 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2152IPW14R | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2152IPW20R | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2152IPW20R | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2152IRSA16R | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430G2152IRSA16R | QFN | RSA | 16 | 3000 | 360.0 | 360.0 | 36.0 |
| MSP430G2152IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2152IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2212IPW14R | TSSOP | PW | 14 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2212IPW14R | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2212IPW20R | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2212IPW20R | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2212IRSA16R | QFN | RSA | 16 | 3000 | 346.0 | 346.0 | 33.0 |
| MSP430G2212IRSA16R | QFN | RSA | 16 | 3000 | 360.0 | 360.0 | 36.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430G2212IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2212IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2252IPW14R | TSSOP | PW | 14 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2252IPW14R | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2252IPW20R | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2252IPW20R | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2252IRSA16R | QFN | RSA | 16 | 3000 | 360.0 | 360.0 | 36.0 |
| MSP430G2252IRSA16R | QFN | RSA | 16 | 3000 | 346.0 | 346.0 | 33.0 |
| MSP430G2252IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2252IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2312IPW14R | TSSOP | PW | 14 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2312IPW14R | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2312IPW20R | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2312IPW20R | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2312IRSA16R | QFN | RSA | 16 | 3000 | 360.0 | 360.0 | 36.0 |
| MSP430G2312IRSA16R | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430G2312IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2312IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2352IPW14R | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2352IPW14R | TSSOP | PW | 14 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2352IPW20R | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2352IPW20R | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2352IRSA16R | QFN | RSA | 16 | 3000 | 360.0 | 360.0 | 36.0 |
| MSP430G2352IRSA16R | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430G2352IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2352IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2412IPW14R | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2412IPW14R | TSSOP | PW | 14 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2412IPW20R | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2412IPW20R | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2412IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2412IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2452IPW14R | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2452IPW14R | TSSOP | PW | 14 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2452IPW20R | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| MSP430G2452IPW20R | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| MSP430G2452IRSA16R | QFN | RSA | 16 | 3000 | 346.0 | 346.0 | 33.0 |
| MSP430G2452IRSA16R | QFN | RSA | 16 | 3000 | 360.0 | 360.0 | 36.0 |
| MSP430G2452IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430G2452IRSA16T | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| MSP430G2112IN20 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2112IN20.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2112IN20.B | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2112IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2112IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2112IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2112IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2112IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2112IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2112IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2112IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2112IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2112IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2112IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2112IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2152IN20 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2152IN20.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2152IN20.B | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2152IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2152IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2152IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2152IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2152IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2152IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2152IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2152IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2152IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2152IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2152IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| MSP430G2152IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IN20 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2212IN20.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2212IN20.B | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2212IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2212IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IN20 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2252IN20.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2252IN20.B | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2252IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2252IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2312IN20 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2312IN20.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2312IN20.B | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2312IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2312IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2312IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2312IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2312IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2312IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2312IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2312IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2312IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| MSP430G2312IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2312IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2312IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IN20 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2352IN20.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2352IN20.B | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2352IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW14G4 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW14G4.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW14G4.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2352IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IN20 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2412IN20.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2412IN20.B | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2412IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2412IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2452IN20 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2452IN20.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2452IN20.B | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| MSP430G2452IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2452IPW14 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2452IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2452IPW14.A | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |

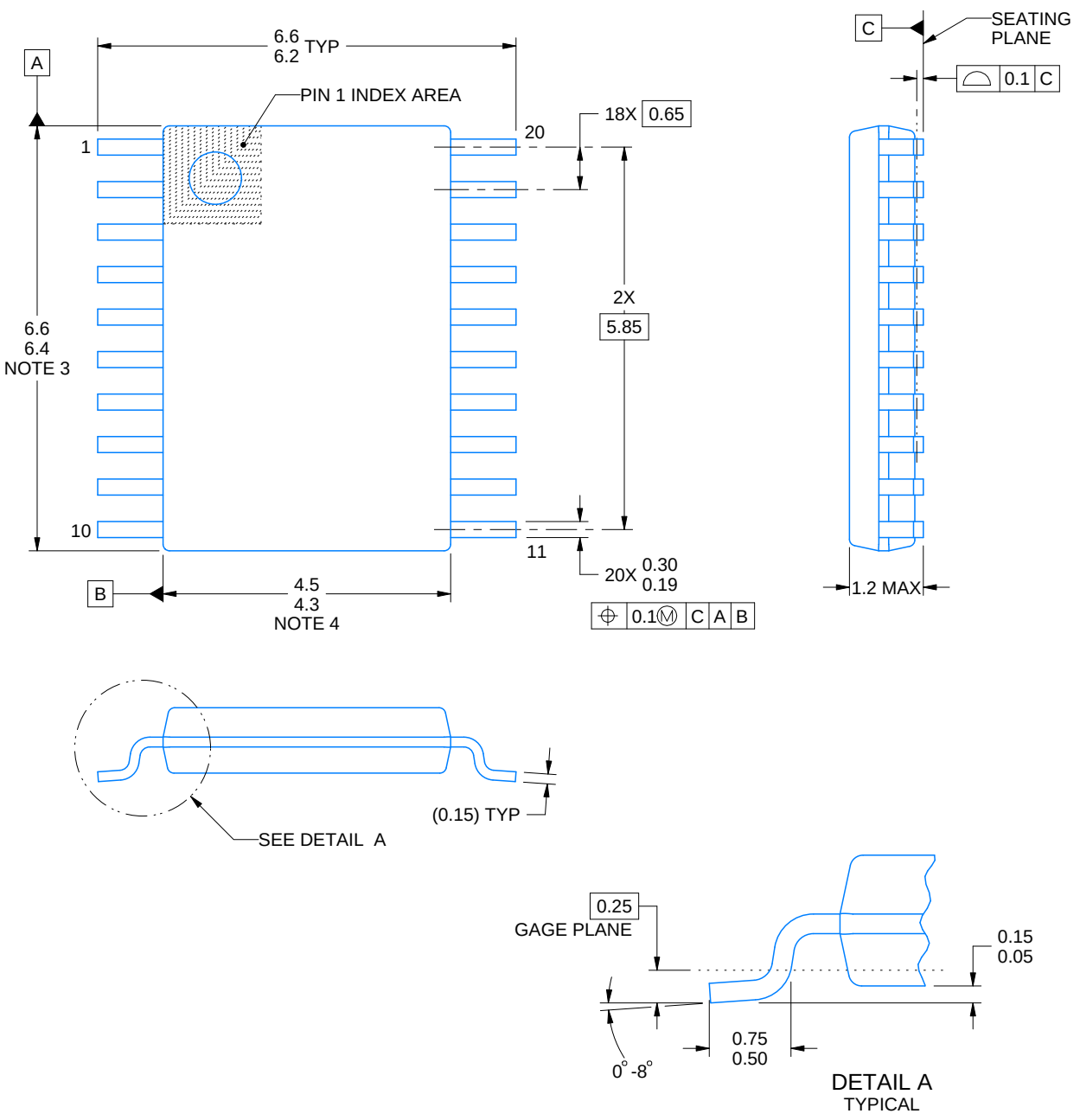
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| MSP430G2452IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2452IPW14.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2452IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2452IPW20 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2452IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2452IPW20.A | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2452IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| MSP430G2452IPW20.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |

# PACKAGE OUTLINE

## PW0020A

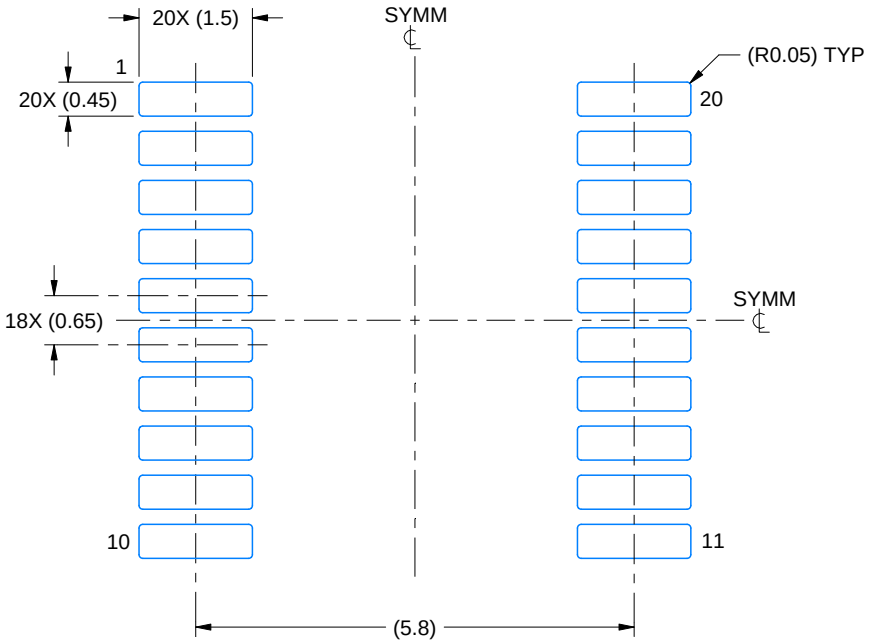
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

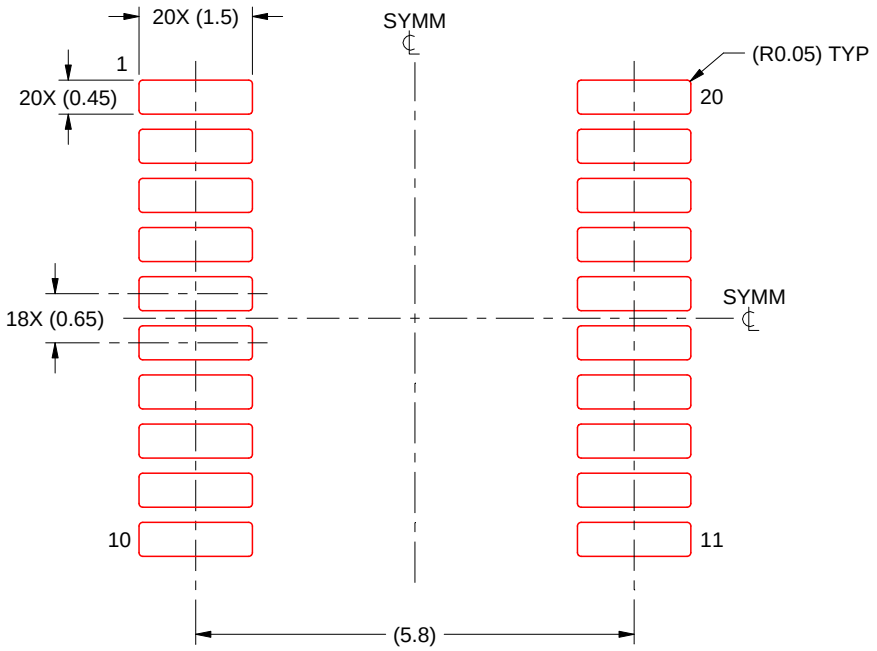



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

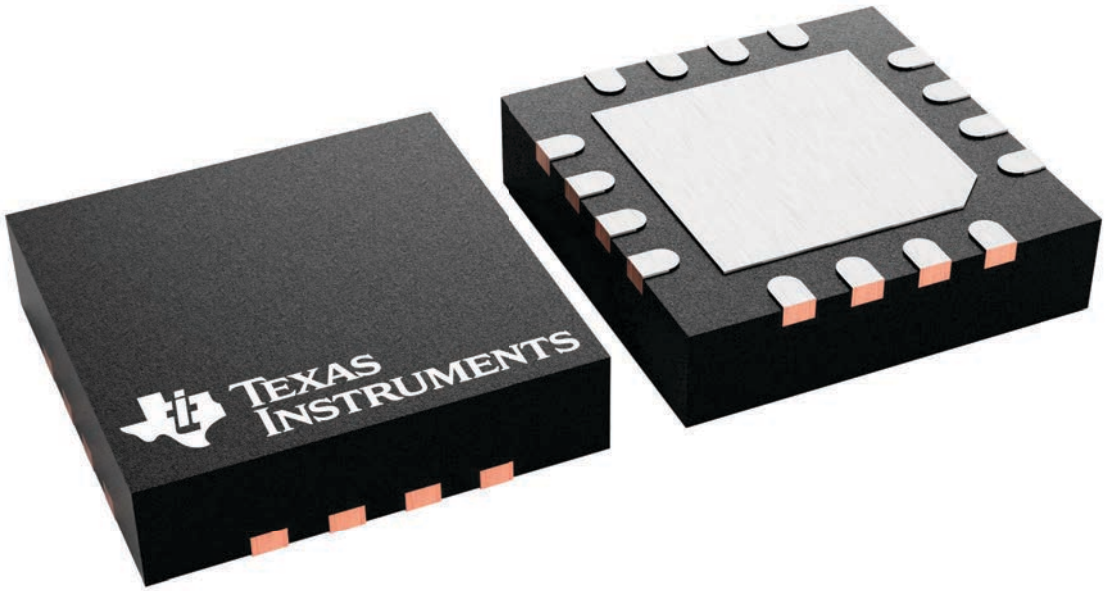
## RSA 16

## VQFN - 1 mm max height

**4 x 4, 0.65 mm pitch**

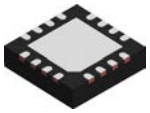
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4230969/A

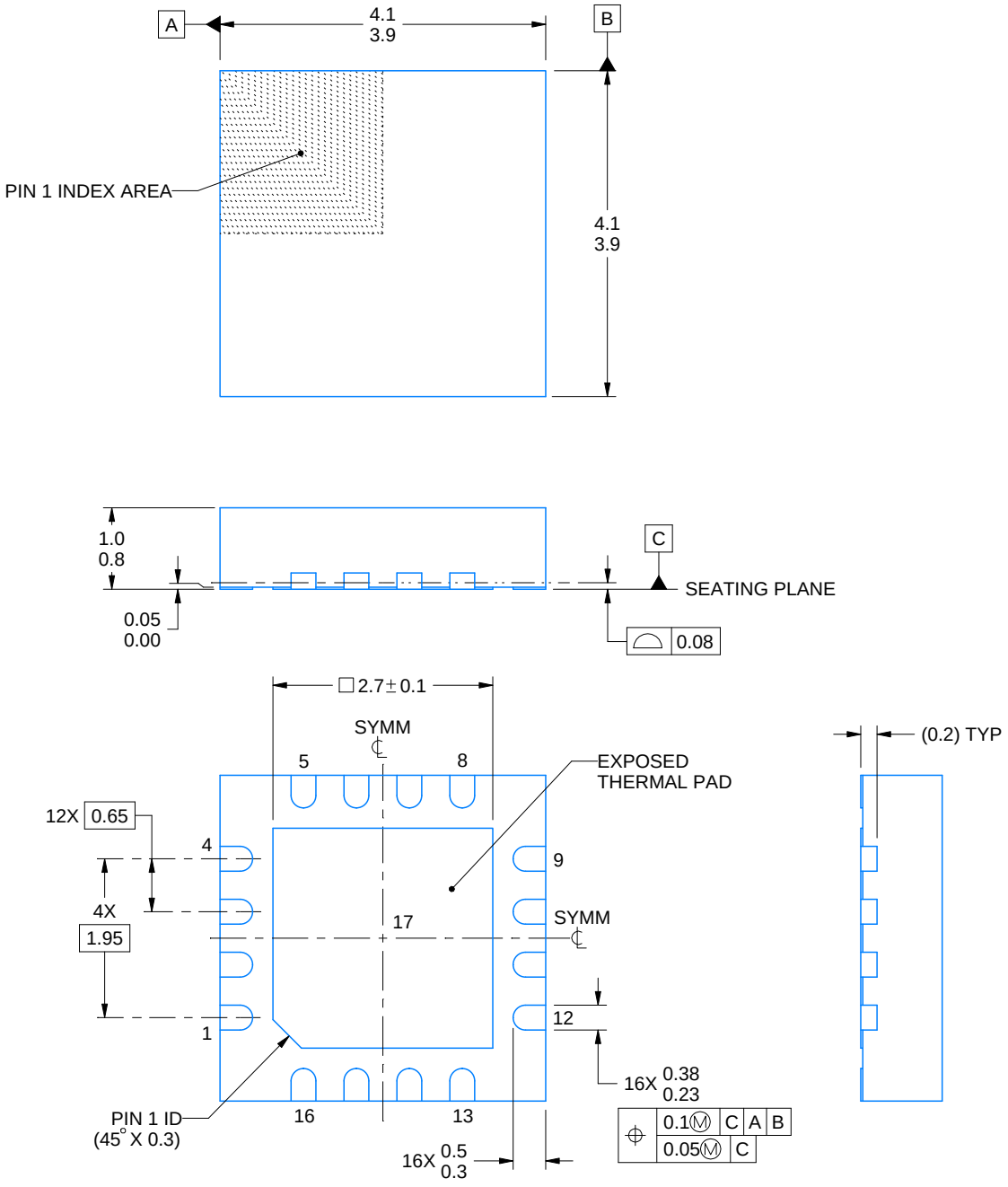
# RSA0016B



# PACKAGE OUTLINE

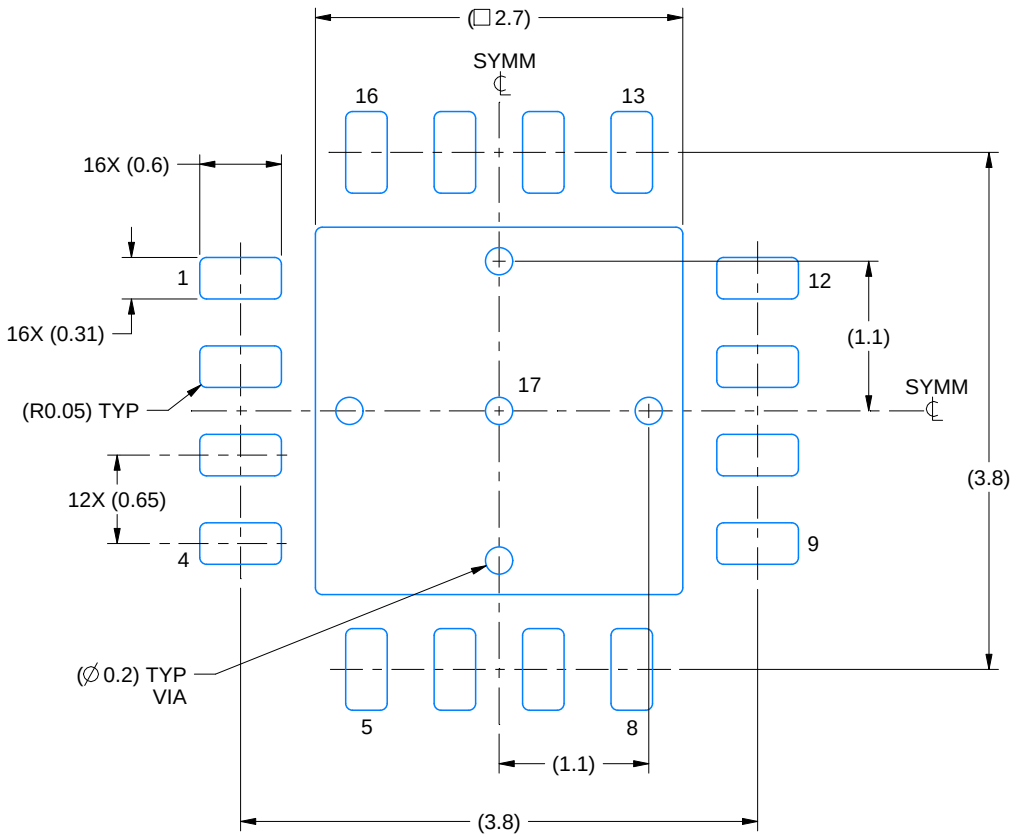
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

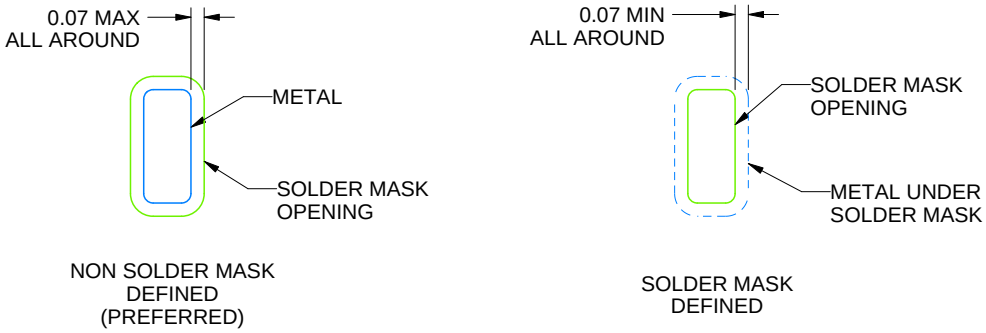



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

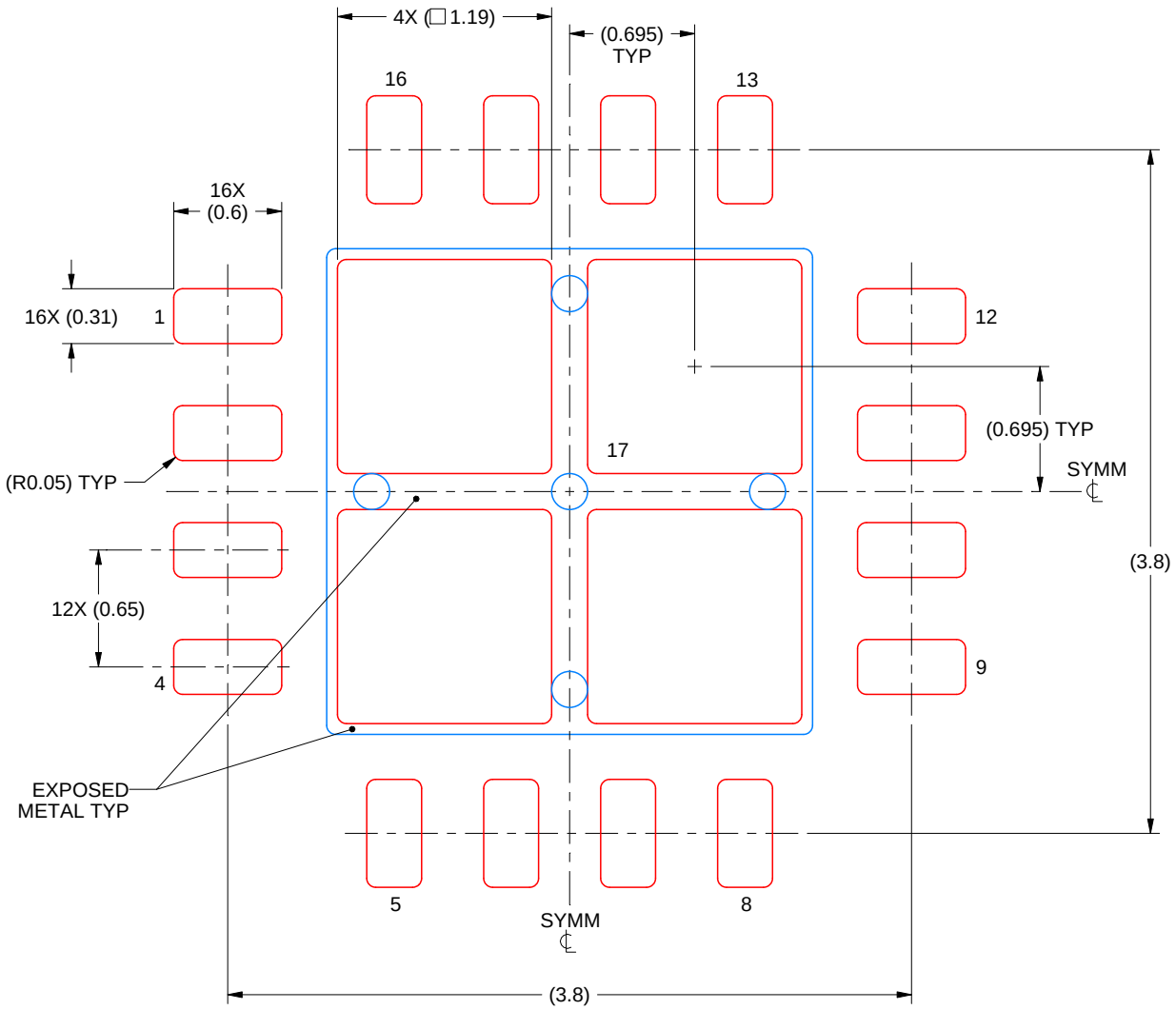



SOLDER MASK DETAILS

4219093/A 08/2021

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4219093/A 08/2021

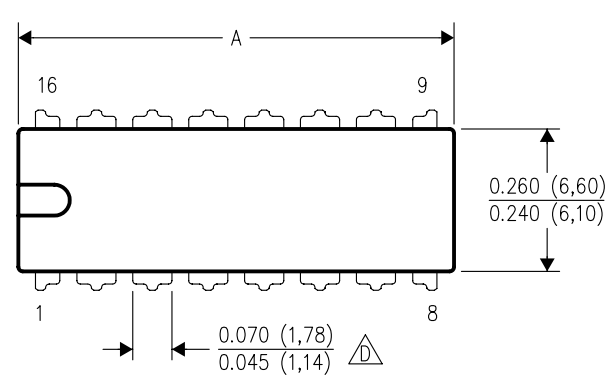
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

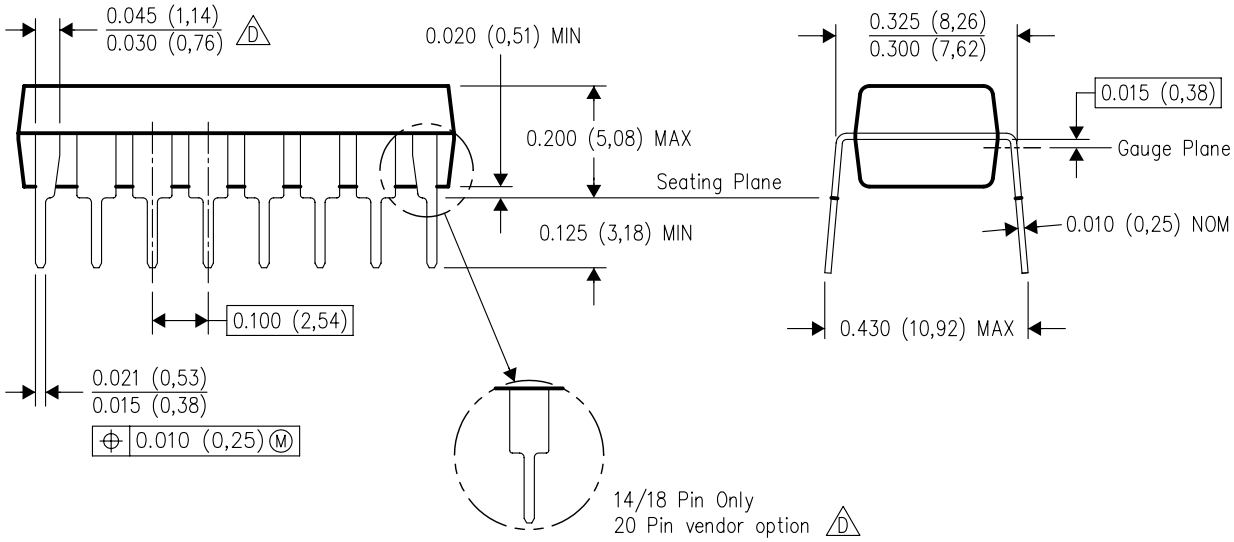
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

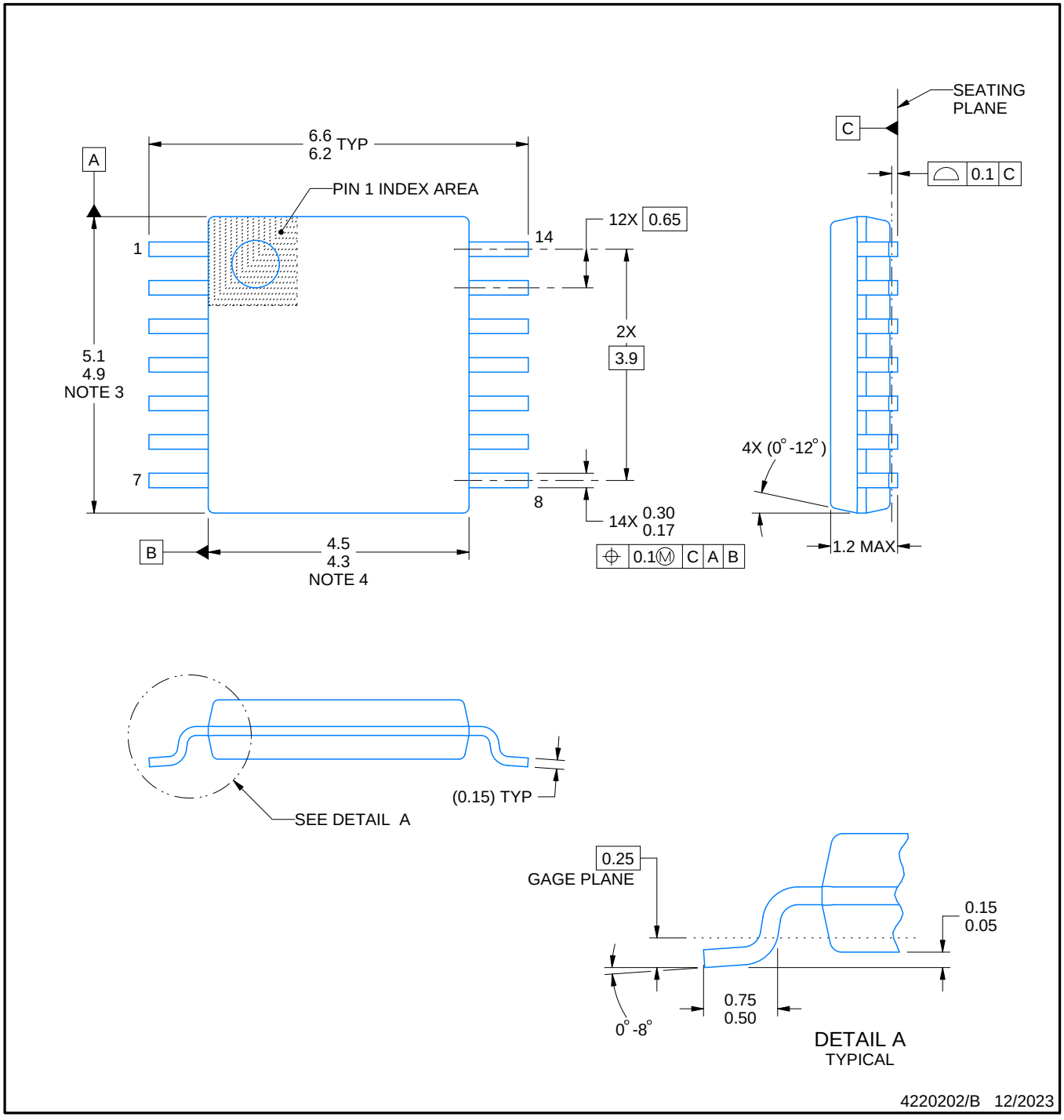
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# PACKAGE OUTLINE

## PW0014A

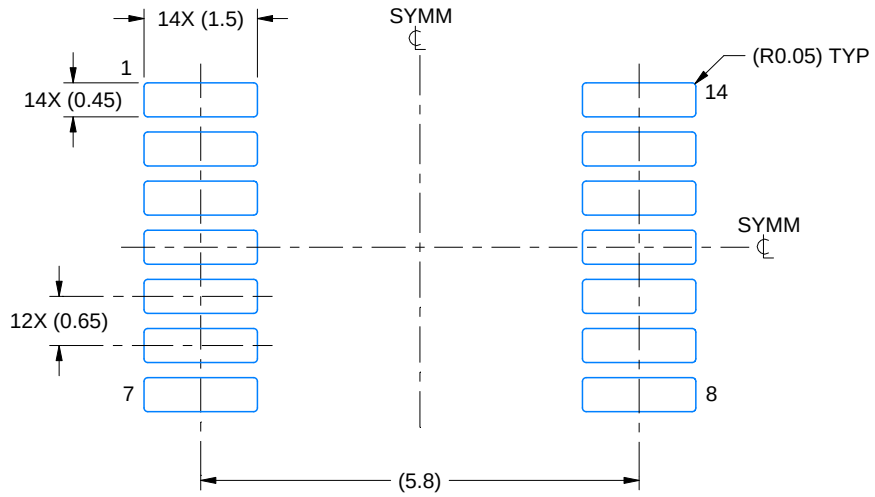
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

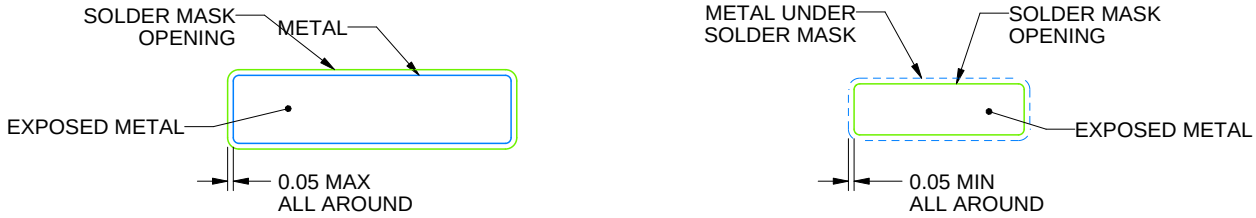



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

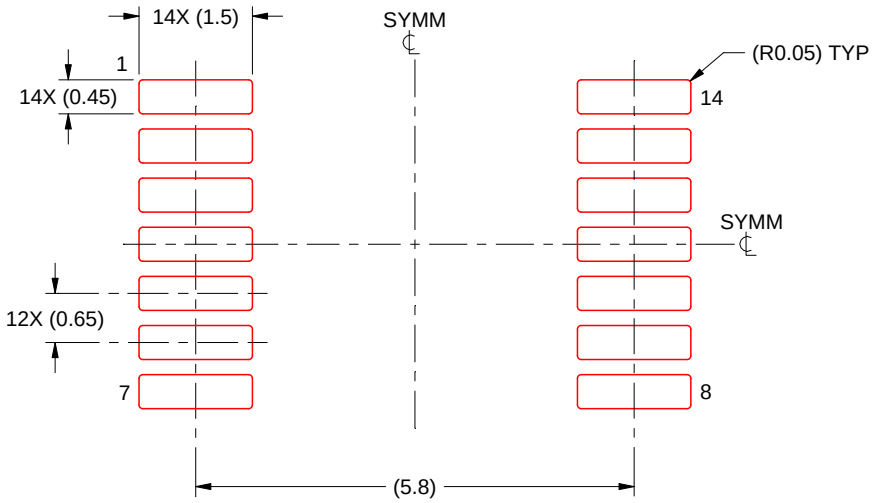



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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