MIXED SIGNAL MICROCONTROLLER

Check for Samples: MSP430F2274-EP

FEATURES

- **Low Supply Voltage Range 1.8 V to 3.6 V**
- **Ultralow-Power Consumption**
  - **Active Mode: 270 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.7 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Ultrafast Wake-Up From Standby Mode in Less than 1 μs**
- **16-Bit RISC Architecture, 62.5 ns Instruction Cycle Time**
- **Basic Clock Module Configurations**
  - **Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to ±1%**
  - **Internal Very Low Power LF Oscillator**
  - **32-kHz Crystal (Available Only from –55°C to 105°C)**
  - **High-Frequency Crystal up to 16 MHz (Available Only from –55°C to 125°C)**
  - **Resonator**
  - **External Digital Clock Source**
  - **External Resistor**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_B With Three Capture/Compare Registers**
- **Universal Serial Communication Interface**
  - **Enhanced UART Supporting Auto-Baud-Rate Detection (LIN)**
  - **IrDA Encoder and Decoder**
  - **Synchronous SPI**
  - **I^2C™**
- **10-Bit, 200-ksps A/D Converter With Internal Reference, Sample-and-Hold, and Autoscan and Data Transfer Controller**
- **Two Configurable Operational Amplifiers**
- **Brownout Detector**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Bootstrap Loader**
- **On-Chip Emulation Logic**
- **Family Members Include the MSP430F2274 With 32KB + 256B Flash Memory, 1KB RAM**
- **Available in 40-Pin QFN Package and 38-Pin Thin Shrink Small-Outline DA Package**
- **For Complete Module Descriptions, Refer to the *MSP430x2xx Family User'sGuide***

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range**[1]
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Custom temperature ranges available

DESCRIPTION

The Texas Instruments MSP430 family of ultralow power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μs.

The MSP430F2274M series is an ultralow-power mixed signal microcontroller with two built-in 16-bit timers, a universal serial communication interface, 10-bit A/D converter with integrated reference and data transfer controller (DTC), two general-purpose operational amplifiers in the MSP430F2274M devices, and 32 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand-alone RF sensor front end is another area of application.

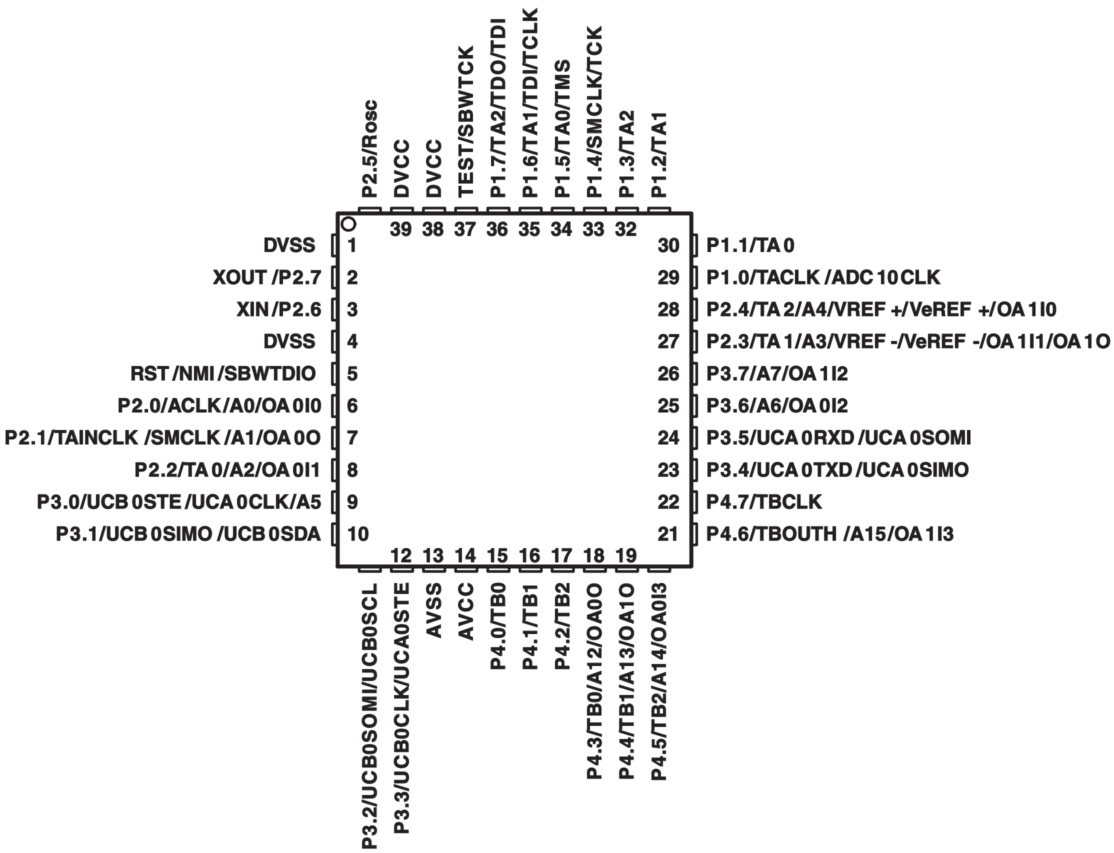
Table 1. ORDERING INFORMATION(1)

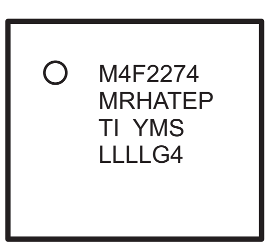
T_A	PACKAGE(2)	ORDERABLE PART NUMBER
–55°C to 125°C	QFN (RHA)	MSP430F2274MRHATEP
	DA (TSSOP)	MSP430F2274MDATEP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DEVICE PINOUTS

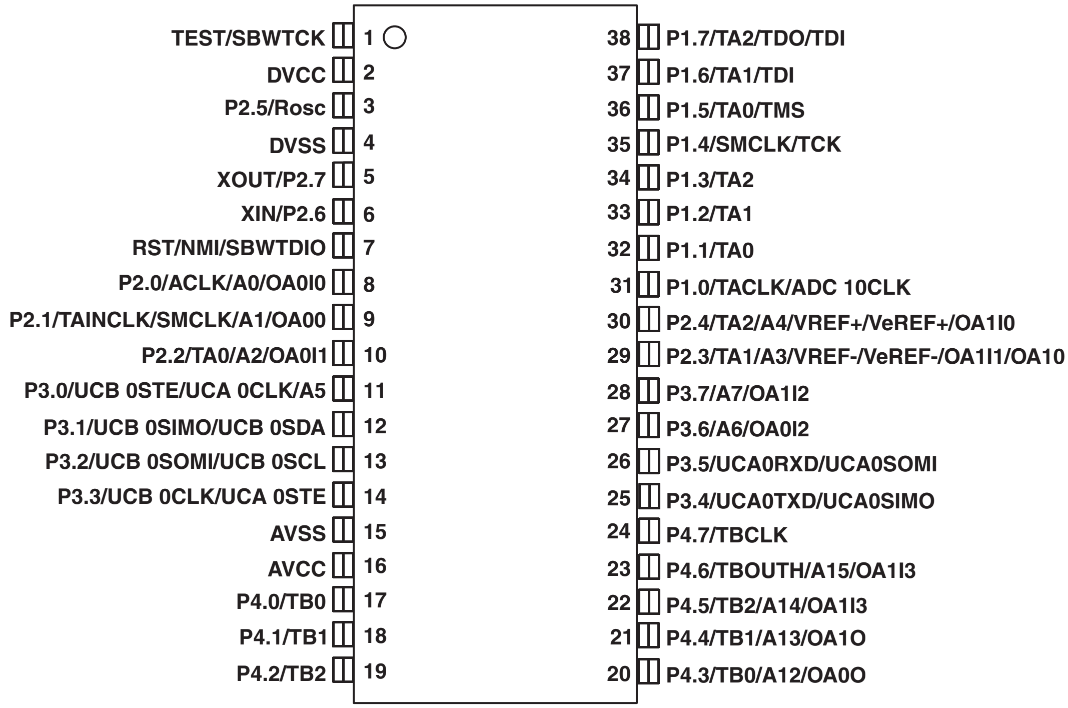
RHA PACKAGE
(TOP VIEW)



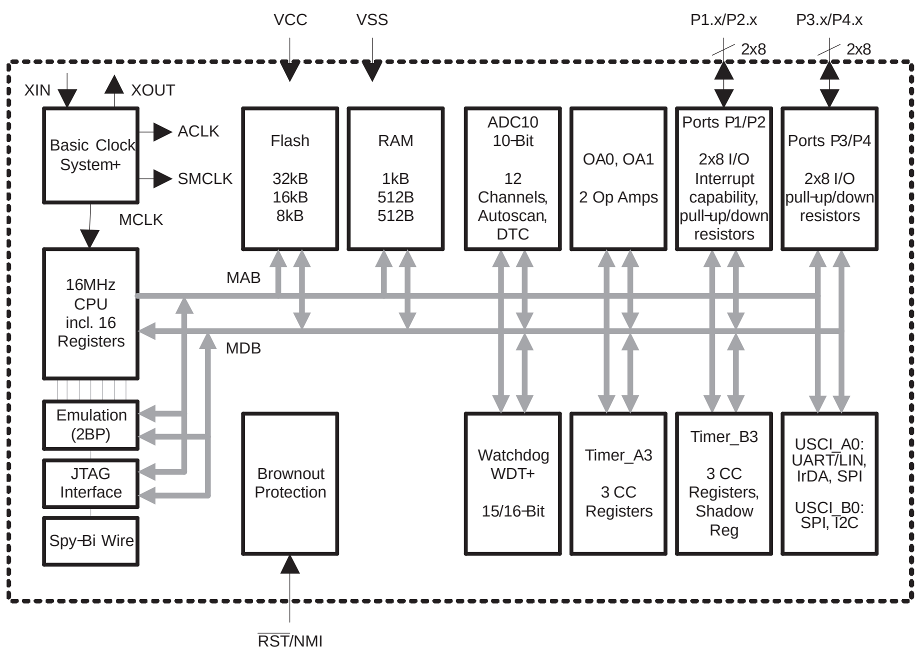


TI = TI
YM = YEAR/MONTH
LLLL = LOT TRACE CODE
S = ASSEMBLY SITE CODE
G4 = RoHS with underscore
O = PIN 1 indicator

DA PACKAGE
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



NOTE: See port schematics section for detailed I/O information.

TERMINAL FUNCTIONS(1)

TERMINAL			I/O	DESCRIPTION
NAME	DA NO.	RHA NO.		
P1.0/TACLK/ADC10CLK	31	29	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ADC10, conversion clock
P1.1/TA0	32	30	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: OUT0 output/BSL transmit
P1.2/TA1	33	31	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: OUT1 output
P1.3/TA2	34	32	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: OUT2 output
P1.4/SMCLK/TCK	35	33	I/O	General-purpose digital I/O pin/SMCLK signal output Test Clock input for device programming and test
P1.5/TA0/TMS	36	34	I/O	General-purpose digital I/O pin/Timer_A, compare: OUT0 output Test Mode Select input for device programming and test
P1.6/TA1/TDI/TCLK	37	35	I/O	General-purpose digital I/O pin/Timer_A, compare: OUT1 output Test Data Input or Test Clock Input for programming and test
P1.7/TA2/TDO/TDI(2)	38	36	I/O	General-purpose digital I/O pin/Timer_A, compare: OUT2 output Test Data Output or Test Data Input for programming and test
P2.0/ACLK/A0/OA0I0	8	6	I/O	General-purpose digital I/O pin/ACLK output ADC10, analog input A0 / OA0, analog input I0
P2.1/TAINCLK/SMCLK/A1/OA0O	9	7	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK SMCLK signal output ADC10, analog input A1/OA0, analog output
P2.2/TA0/A2/OA0I1	10	8	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input/BSL receive, compare: OUT0 output ADC10, analog input A2/OA0, analog input I1
P2.3/TA1/A3/V_{REF-}/V_{eREF-}/OA1I1/OA1O	29	27	I/O	General-purpose digital I/O pin Timer_A, capture CCI1B input, compare: OUT1 output ADC10, analog input A3 / negative reference voltage output/input OA1, analog input I1/OA1, analog output
P2.4/TA2/A4/V_{REF+}/V_{eREF+}/OA1I0	30	28	I/O	General-purpose digital I/O pin/Timer_A, compare: OUT2 output ADC10, analog input A4/positive reference voltage output/input OA1, analog input I0
P2.5/R_{OSC}	3	40	I/O	General-purpose digital I/O pin Input for external DCO resistor to define DCO frequency
XIN/P2.6	6	3	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin
XOUT/P2.7	5	2	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin
P3.0/UCB0STE/UCA0CLK/A5	11	9	I/O	General-purpose digital I/O pin USCI_B0 slave transmit enable/USCI_A0 clock input/output ADC10, analog input A5
P3.1/UCB0SIMO/UCB0SDA	12	10	I/O	General-purpose digital I/O pin USCI_B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode
P3.2/UCB01SOMI/UCB0SCL	13	11	I/O	General-purpose digital I/O pin USCI_B0 slave out/master in SPI mode, SCL I^2C clock in I^2C mode
P3.3/UCB0CLK/UCA0STE	14	12	I/O	General-purpose digital I/O pin USCI_B0 clock input/output/USCI_A0 slave transmit enable
P3.4/UCA0TXD/UCA0SIMO	25	23	I/O	General-purpose digital I/O pin USCI_A0 transmit data output in UART mode, slave in/master out in SPI mode

(1) If XOUT/P2.7ca7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.
(2) TDO or TDI is selected via JTAG instruction.

TERMINAL FUNCTIONS(1) (continued)

TERMINAL			I/O	DESCRIPTION
NAME	DA NO.	RHA NO.		
P3.5/UCA0RXD/UCA0SOMI	26	24	I/O	General-purpose digital I/O pin USCI_A0 receive data input in UART mode, slave out/master in in SPI mode
P3.6/A6/OA0I2	27	25	I/O	General-purpose digital I/O pin ADC10 analog input A6/OA0 analog input I2
P3.7/A7/OA1I2	28	26	I/O	General-purpose digital I/O pin ADC10 analog input A7/OA1 analog input I2
P4.0/TB0	17	15	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A input, compare: OUT0 output
P4.1/TB1	18	16	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A input, compare: OUT1 output
P4.2/TB2	19	17	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A input, compare: OUT2 output
P4.3/TB0/A12/OA0O	20	18	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0B input, compare: OUT0 output ADC10 analog input A12/OA0 analog output
P4.4/TB1A13/OA1O	21	19	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1B input, compare: OUT1 output ADC10 analog input A13/OA1 analog output
P4.5/TB2A14/OA0I3	22	20	I/O	General-purpose digital I/O pin Timer_B, compare: OUT2 output ADC10 analog input A14/OA0 analog input I3
P4.6/TBOUTHA15/OA1I3	23	21	I/O	General-purpose digital I/O pin Timer_B, switch all TB0 to TB3 outputs to high impedance ADC10 analog input A15/OA1 analog input I3
P4.7/TBCLK	24	22	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input
RST/NMI/SBWTDIO	7	5	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	1	37	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DV_{CC}	2	38, 39		Digital supply voltage
AV_{CC}	16	14		Analog supply voltage
DV_{SS}	4	1, 4		Digital ground reference
AV_{SS}	15	13		Analog ground reference
QFN Pad	NA	Package Pad	NA	QFN package pad connection to DV_{SS} recommended.

SHORT-FORM DESCRIPTION

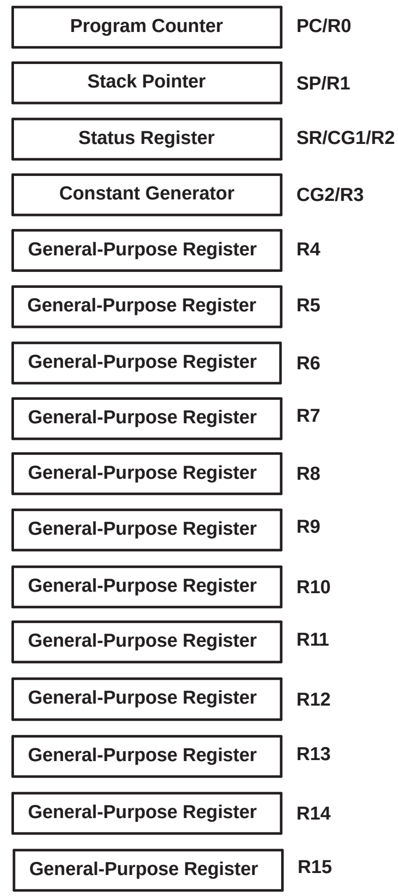
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 2 shows examples of the three types of instruction formats; the address modes are listed in Table 3.

Table 2. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 → R5
Single operands, destination only	e.g., CALL R8	PC → (TOS), R8 → PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 3. Address Mode Descriptions

ADDRESS MODE	S(1)	D(2)	SYNTAX	EXAMPLE	OPERATION
Register	•	•	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	•	•	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	•	•	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	•	•	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	•		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	•		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	•		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source
(2) D = destination

Operating Modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
    ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
  - CPU is disabled ACLK and SMCLK remain active. MCLK is disabled.
    DCO's dc-generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
    MCLK and SMCLK are disabled.
    DCO's dc-generator remains enabled.
    ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
    MCLK and SMCLK are disabled.
    DCO's dc-generator is disabled.
    ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
    ACLK is disabled.
    MCLK and SMCLK are disabled.
    DCO's dc-generator is disabled.
    Crystal oscillator is stopped.

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh–0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (e.g., flash is not programmed), the CPU goes into LPM4 immediately after power up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power up External reset Watchdog Flash key violation PC out-of-range (1)	PORIFG RSTIFG WDTIFG KEYV (2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (2) (3)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	30
Timer_B3	TBCCR0 CCIFG (4)	maskable	0FFFAh	29
Timer_B3	TBCCR1 and TBCCR2 CCIFGs, TBIFG (2) (4)	maskable	0FFF8h	28
			0FFF6h	27
Watchdog Timer	WDTIFG	maskable	0FFF4h	26
Timer_A3	TACCR0 CCIFG (4)	maskable	0FFF2h	25
Timer_A3	TACCR1 CCIFG, TACCR2 CCIFG, TAIFG (2) (4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 Receive	UCA0RXIFG, UCB0RXIFG (2)	maskable	0FFEEh	23
USCI_A0/USCI_B0 Transmit	UCA0TXIFG, UCB0TXIFG (2)	maskable	0FFECh	22
ADC10	ADC10IFG (4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (eight flags)	P2IFG.6 to P2IFG.7 (2) (4)	maskable	0FFE6h	19
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (2) (4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
(5)			0FFDEh	15
(6)			0FFDCh ... 0FFC0h	14 ... 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h–01FFh) or from within unused address range.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot. Nonmaskable: neither the individual nor the general interrupt-enable bit disables an interrupt event.
(4) Interrupt flags are located in the module.
(5) This location is used as bootstrap loader security key (BSLSKEY). A 0AA55h at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.
(6) The interrupt vectors at addresses 0FFDCh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Interrupt Enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.

OFIE: Oscillator fault enable

NMIIE: (Non)maskable interrupt enable

ACCVIE: Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE USCI_A0 receive-interrupt enable

UCA0TXIE USCI_A0 transmit-interrupt enable

UCB0RXIE USCI_B0 receive-interrupt enable

UCB0TXIE USCI_B0 transmit-interrupt enable

Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-up or a reset condition at $\overline{\text{RST}}$/NMI pin in reset mode.

OFIFG: Flag set on oscillator fault

RSTIFG: External reset interrupt flag. Set on a reset condition at $\overline{\text{RST}}$/NMI pin in reset mode. Reset on V_{CC} power up.

PORIFG: Power-On Reset interrupt flag. Set on V_{CC} power up.

NMIIFG: Set via $\overline{\text{RST}}$/NMI-pin

Address	7	6	5	4	3	2	1	0
03h					UCB0 TXIFG	UCB0 RXIFG	UCA0 TXIFG	UCA0 RXIFG
					rw-1	rw-0	rw-1	rw-0

UCA0RXIFG USCI_A0 receive-interrupt flag

UCA0TXIFG USCI_A0 transmit-interrupt flag

UCB0RXIFG USCI_B0 receive-interrupt flag

UCB0TXIFG USCI_B0 transmit-interrupt flag

Legend:

rw:	Bit can be read and written.
rw-0, 1:	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), (1):	Bit can be read and written. It is Reset or Set by POR.
(shaded box)	SFR bit is not present in device.

Memory Organization

		MSP430F223x	MSP430F225x	MSP430F227x
Memory Main: interrupt vector Main: code memory	Size Flash Flash	8KB Flash 0FFFFh–0FFC0h 0FFFFh–0E000h	16KB Flash 0FFFFh–0FFC0h 0FFFFh–0C000h	32KB Flash 0FFFFh–0FFC0h 0FFFFh–08000h
Information memory	Size Flash	256 Byte 010FFh–01000h	256 Byte 010FFh–01000h	256 Byte 010FFh–01000h
Boot memory	Size ROM	1KB 0FFFh–0C00h	1KB 0FFFh–0C00h	1KB 0FFFh–0C00h
RAM	Size	512 Byte 03FFh–0200h	512 Byte 03FFh–0200h	1KB 05FFh–0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh–0100h 0FFh–010h 0Fh–00h	01FFh–0100h 0FFh–010h 0Fh–00h	01FFh–0100h 0FFh–010h 0Fh–00h

Bootstrap Loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the application report, *Features of the MSP430 Bootstrap Loader*, TI literature number SLAA089.

BSL Function	DA Package Pins	RHA Package Pins
Data Transmit	32 - P1.1	30 – P1.1
Data Receive	10 - P2.2	8 – P2.2

Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0–n.
  Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

Peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x2xx Family User's Guide*.

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very low power, low frequency oscillator and an internal digitally-controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator for –55°C to 105°C operation. For > 105°C, use external clock source.
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules

DCO Calibration Data (provided from factory in flash info memory segment A)			
DCO Frequency	**Calibration Register**	**Size**	**Address**
1 MHz	CALBC1_1MHZ	byte	010FFh
	CALDCO_1MHZ	byte	010FEh
8 MHz	CALBC1_8MHZ	byte	010FDh
	CALDCO_8MHZ	byte	010FCh
12 MHz	CALBC1_12MHZ	byte	010FBh
	CALDCO_12MHZ	byte	010FAh
16 MHz	CALBC1_16MHZ	byte	010F9h
	CALDCO_16MHZ	byte	010F8h

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

There are four 8-bit I/O ports implemented – ports P1, P2, P3, and P4:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.

WDT+ Watchdog Timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections

Input Pin Number		Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number	
DA	RHA					DA	RHA
31 - P1.0	29 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
9 - P2.1	7 - P2.1	TAINCLK	INCLK				
32 - P1.1	30 - P1.1	TA0	CCI0A	CCR0	TA0	32 - P1.1	30 - P1.1
10 - P2.2	8 - P2.2	TA0	CCI0B			10 - P2.2	8 - P2.2
		V_{SS}	GND			36 - P1.5	34 - P1.5
		V_{CC}	V_{CC}				
33 - P1.2	31 - P1.2	TA1	CCI1A	CCR1	TA1	33 - P1.2	31 - P1.2
29 - P2.3	27 - P2.3	TA1	CCI1B			29 - P2.3	27 - P2.3
		V_{SS}	GND			37 - P1.6	35 - P1.6
		V_{CC}	V_{CC}				
34 - P1.3	32 - P1.3	TA2	CCI2A	CCR2	TA2	34 - P1.3	32 - P1.3
		ACLK (internal)	CCI2B			30 - P2.4	28 - P2.4
		V_{SS}	GND			38 - P1.7	36 - P1.7
		V_{CC}	V_{CC}				

Timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_B3 Signal Connections

Input Pin Number DA	Input Pin Number RHA	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number DA	Output Pin Number RHA
24 - P4.7	22 - P4.7	TBCLK	TBCLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
24 - P4.7	22 - P4.7	$\overline{\text{TBCLK}}$	INCLK				
17 - P4.0	15 - P4.0	TB0	CCI0A	CCR0	TB0	17 - P4.0	15 - P4.0
20 - P4.3	18 - P4.3	TB0	CCI0B			20 - P4.3	18 - P4.3
		V_{SS}	GND				
		V_{CC}	V_{CC}				
18 - P4.1	16 - P4.1	TB1	CCI1A	CCR1	TB1	18 - P4.1	16 - P4.1
21 - P4.4	19 - P4.4	TB1	CCI1B			21 - P4.4	19 - P4.4
		V_{SS}	GND				
		V_{CC}	V_{CC}				
19 - P4.2	17 - P4.2	TB2	CCI2A	CCR2	TB2	19 - P4.2	17 - P4.2
		ACLK (internal)	CCI2B			22 - P4.5	20 - P4.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				

USCI

The universal serial communication interface (USCI) module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols like UART, enhanced UART with automatic baud-rate detection (LIN), and IrDA.

USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART and IrDA.

USCI_B0 provides support for SPI (3 or 4 pin) and I2C.

ADC10

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling allowing ADC samples to be converted and stored without any CPU intervention.

Operational Amplifier (OA)

The MSP430F2274M has two configurable low-current general-purpose operational amplifiers. Each OA input and output terminal is software-selectable and offer a flexible choice of connections for various applications. The OA op amps primarily support front-end analog signal conditioning prior to analog-to-digital conversion.

OA0 Signal Connections

Analog Input Pin Number		Device Input Signal	Module Input Name
DA	RHA		
8 - A0	6 - A0	OA0I0	OAxI0
10 - A2	8 - A2	OA0I1	OA0I1
10 - A2	8 - A2	OA0I1	OAxI1
27 - A6	25 - A6	OA0I2	OAxIA
22 - A14	20 - A14	OA0I3	OAxIB

OA1 Signal Connections

Analog Input Pin Number		Device Input Signal	Module Input Name
DA	RHA		
30 - A4	28 - A4	OA0I0	OAxI0
10 - A2	8 - A2	OA0I1	OA0I1
29 - A3	27 - A3	OA0I1	OAxI1
28 - A7	26 - A7	OA0I2	OAxIA
23 - A15	21 - A15	OA0I3	OAxIB

Peripheral File Map

PERIPHERALS WITH WORD ACCESS			
ADC10	ADC data transfer start address ADC memory ADC control register 1 ADC control register 0 ADC analog enable 0 ADC analog enable 1 ADC data transfer control register 1 ADC data transfer control register 0	ADC10SA ADC10MEM ADC10CTL1 ADC10CTL0 ADC10AE0 ADC10AE1 ADC10DTC1 ADC10DTC0	1BCh 1B4h 1B2h 1B0h 04Ah 04Bh 049h 048h
Timer_B	Capture/compare register Capture/compare register Capture/compare register Timer_B register Capture/compare control Capture/compare control Capture/compare control Timer_B control Timer_B interrupt vector	TBCCR2 TBCCR1 TBCCR0 TBR TBCCTL2 TBCCTL1 TBCCTL0 TBCTL TBIV	0196h 0194h 0192h 0190h 0186h 0184h 0182h 0180h 011Eh
Timer_A	Capture/compare register Capture/compare register Capture/compare register Timer_A register Capture/compare control Capture/compare control Capture/compare control Timer_A control Timer_A interrupt vector	TACCR2 TACCR1 TACCR0 TAR TACCTL2 TACCTL1 TACCTL0 TACTL TAIV	0176h 0174h 0172h 0170h 0166h 0164h 0162h 0160h 012Eh
Flash Memory	Flash control 3 Flash control 2 Flash control 1	FCTL3 FCTL2 FCTL1	012Ch 012Ah 0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

PERIPHERALS WITH BYTE ACCESS			
OA1	Operational Amplifier 1 control register 1 Operational Amplifier 1 control register 1	OA1CTL1 OA1CTL0	0C3h 0C2h
OA0	Operational Amplifier 0 control register 1 Operational Amplifier 0 control register 1	OA0CTL1 OA0CTL0	0C1h 0C0h
USI_B0	USCI_B0 transmit buffer USCI_B0 receive buffer USCI_B0 status USCI_B0 bit rate control 1 USCI_B0 bit rate control 0 USCI_B0 control 1 USCI_B0 control 0 USCI_B0 I2C slave address USCI_B0 I2C own address	UCB0TXBUF UCB0RXBUF UCB0STAT UCB0BR1 UCB0BR0 UCB0CTL1 UCB0CTL0 UCB0SA UCB0OA	06Fh 06Eh 06Dh 06Bh 06Ah 069h 068h 011Ah 0118h
USI_A0	USCI_A0 transmit buffer USCI_A0 receive buffer USCI_A0 status USCI_A0 modulation control USCI_A0 baud rate control 1 USCI_A0 baud rate control 0 USCI_A0 control 1 USCI_A0 control 0 USCI_A0 IrDA receive control USCI_A0 IrDA transmit control USCI_A0 auto baud rate control	UCA0TXBUF UCA0RXBUF UCA0STAT UCA0MCTL UCA0BR1 UCA0BR0 UCA0CTL1 UCA0CTL0 UCA0IRRCTL UCA0IRTCTL UCA0ABCTL	067h 066h 065h 064h 063h 062h 061h 060h 05Fh 05Eh 05Dh
Basic Clock System+	Basic clock system control 3 Basic clock system control 2 Basic clock system control 1 DCO clock frequency control	BCSCTL3 BCSCTL2 BCSCTL1 DCOCTL	053h 058h 057h 056h
Port P4	Port P4 resistor enable Port P4 selection Port P4 direction Port P4 output Port P4 input	P4REN P4SEL P4DIR P4OUT P4IN	011h 01Fh 01Eh 01Dh 01Ch
Port P3	Port P3 resistor enable Port P3 selection Port P3 direction Port P3 output Port P3 input	P3REN P3SEL P3DIR P3OUT P3IN	010h 01Bh 01Ah 019h 018h
Port P2	Port P2 resistor enable Port P2 selection Port P2 interrupt enable Port P2 interrupt edge select Port P2 interrupt flag Port P2 direction Port P2 output Port P2 input	P2REN P2SEL P2IE P2IES P2IFG P2DIR P2OUT P2IN	02Fh 02Eh 02Dh 02Ch 02Bh 02Ah 029h 028h
Port P1	Port P1 resistor enable Port P1 selection Port P1 interrupt enable Port P1 interrupt edge select Port P1 interrupt flag Port P1 direction Port P1 output Port P1 input	P1REN P1SEL P1IE P1IES P1IFG P1DIR P1OUT P1IN	027h 026h 025h 024h 023h 022h 021h 020h
Special Function	SFR interrupt flag 2 SFR interrupt flag 1 SFR interrupt enable 2 SFR interrupt enable 1	IFG2 IFG1 IE2 IE1	003h 002h 001h 000h

Absolute Maximum Ratings(1)

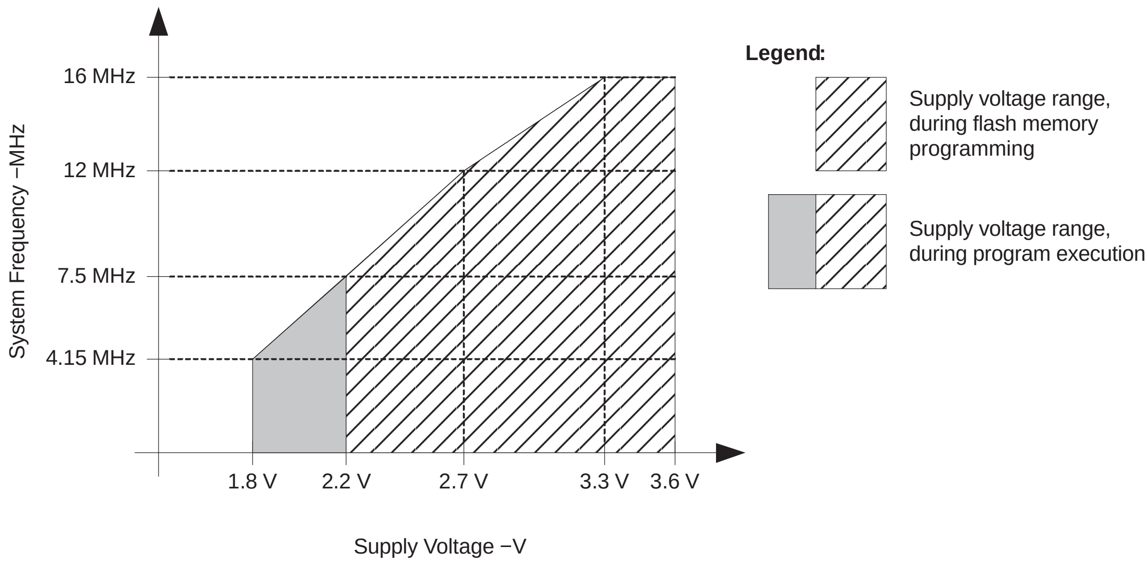
	VALUE	UNIT
Voltage applied at V_{CC} to V_{SS}	–0.3 to 4.1	V
Voltage applied to any pin(2)	–0.3 to V_{CC} + 0.3	V
Diode current at any device terminal	±2	mA
Storage temperature, T_{stg} (unprogrammed device(3))	–55 to 150	°C
Storage temperature, T_{stg} (programmed device (3))	–55 to 125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to VSS. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions[1] [2]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution		1.8		3.6	V
	Supply voltage during program/erase flash memory		2.2		3.6	V
V_{SS}	Supply voltage			0		V
T_A	Operating free-air temperature range		–55		125	°C
	Processor frequency f_{SYSTEM} (Maximum MCLK frequency)[1] [2] (see Figure 1)	V_{CC} = 1.8 V, Duty Cycle = 50% ±10%	dc		4.15	MHz
		V_{CC} = 2.7 V, Duty Cycle = 50% ±10%	dc		12	MHz
		V_{CC} ≥ 3.3 V, Duty Cycle = 50% ±10%	dc		16	MHz

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(2) Modules might have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

Active-Mode Supply Current (Into DV_{CC} + AV_{CC}) Excluding External Current – Electrical Characteristics(1) (2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,\ 1MHz}$	Active-mode (AM) current (1 MHz)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1 MHZ, DCOCTL = CALDCO_1 MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	–55°C to 125°C	2.2 V		270	390	μA
				3 V		390	550	
$I_{AM,\ 1MHz}$	Active-mode (AM) current (1 MHz)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1 MHZ, DCOCTL = CALDCO_1 MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		240		μA
				3 V		340		
$I_{AM,\ 4kHz}$	Active-mode (AM) current (4 kHz)	f_{MCLK} = f_{SMCLK} = f_{ACLK} = 32,768 Hz/8 = 4,096 Hz, f_{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	–55°C to 85°C	2.2 V		5	9	μA
			125°C				18	
			–55°C to 85°C	3 V		6	10	
			125°C				20	
$I_{AM,100kHz}$	Active-mode (AM) current (100 kHz)	f_{MCLK} = f_{SMCLK} = $f_{DCO(0,\ 0)}$ ≉ 100 kHz, f_{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	–55°C to 85°C	2.2 V		60	85	μA
			125°C				95	
			–55°C to 85°C	3 V		72	95	
			125°C				125	

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(2) For T_A < 105°C, the currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF. For T_A > 105°C, the currents are characterized using a 32-kHz external clock source for ACLK..

Typical Characteristics – Active-Mode Supply Current (Into DV_{CC} + AV_{CC})

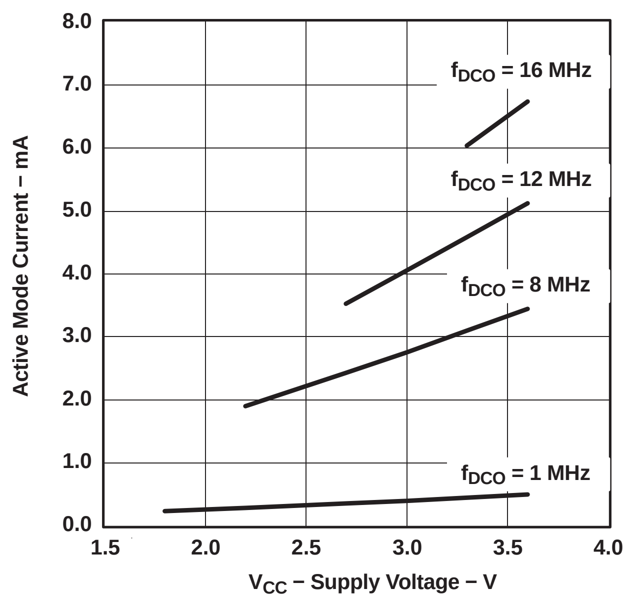


Figure 2. Active-Mode Current vs V_{CC}, T_A = 25°C

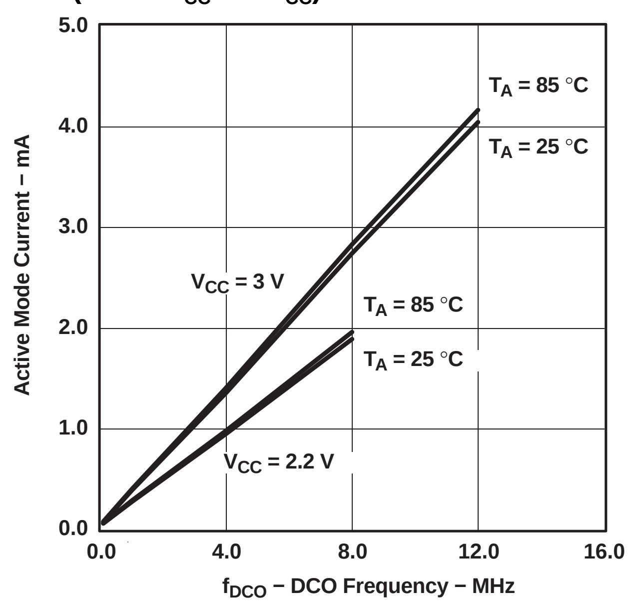


Figure 3. Active-Mode Current vs DCO Frequency

Low-Power-Mode Supply Currents (Into DV_{CC} + AV_{CC}) Excluding External Current – Electrical Characteristics[(1)] [(2)]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,\ 1MHz}$	Low-power mode 0 (LPM0) current[(3)]	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1 MHZ, DCOCTL = CALDCO_1 MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	–55°C to 125°C	2.2 V		75	90	µA
				3 V		90	120	
$I_{LPM0,\ 100kHz}$	Low-power mode 0 (LPM0) current[(3)]	f_{MCLK} = 0 MHz, f_{SMCLK} = $f_{DCO(0,\ 0)}$ $\ncong$ 100 kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1	–55°C to 125°C	2.2 V		37	60	µA
				3 V		41	75	
I_{LPM2}	Low-power mode 2 (LPM2) current[(4)]	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1 MHZ, DCOCTL = CALDCO_1 MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	–55°C to 85°C	2.2 V		22	29	µA
			125°C				40	
			–55°C to 85°C	3 V		25	32	
			125°C				45	
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current[(4)]	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	–55°C	2.2 V		0.7	1.4	µA
			25°C			0.7	1.4	
			85°C			2.8	4.5	
			125°C			6	18	
			–55°C	3 V		0.9	1.5	
			25°C			0.9	1.5	
			85°C			3.0	5.0	
			125°C			6.5	19	
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3) [(4)]	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	–55°C	2.2 V		0.4	1.0	µA
			25°C			0.5	1.0	
			85°C			2.2	4.2	
			125°C			5.7	18	
			–55°C	3 V		0.5	1.2	
			25°C			0.6	1.2	
			85°C			2.5	4.5	
			125°C			6.0	19	
I_{LPM4}	Low-power mode 4 (LPM4) current[(5)]	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	–55°C	2.2 V/ 3 V		0.1	0.5	µA
			25°C			0.1	0.5	
			85°C			1.9	4.0	
			125°C			5.5	16	

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(2) For T_A < 105°C, the currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF. For T_A > 105°C, ACLK was sourced from an external clock source.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.
(5) Current for brownout included.

Schmitt-Trigger Inputs (Ports P1, P2, P3, P4, and RST/NMI[1]) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		–55°C to 125°C	2.2 V	1.00		1.65	V
				3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		–55°C to 125°C	2.2 V	.55		1.20	V
				3 V	.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})		–55°C to 125°C	2.2 V	0.2		1.0	V
				3 V	0.3		1.0	
R_{Pull}	Pullup/pulldown resistor	For pullup: V_{IN} = V_{SS}; For pulldown: V_{IN} = V_{CC}	–55°C to 125°C		20	35	50	kΩ
C_I	Input capacitance	V_{IN} = V_{SS} or V_{CC}				5		pF

(1) RST/NMI limit values specified for -55°C to 125°C.

Inputs (Ports P1 and P2) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag[1]	–55°C to 125°C	2.2 V/3 V	20		ns

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

Leakage Current (Ports P1, P2, P3 and P4) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	[1][2]	–55°C to 125°C	2.2 V/3 V		±100	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs (Ports P1, P2, P3, and P4) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA (1)	–55°C to 125°C	2.2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{OH(max)}$ = –6 mA (2)	–55°C to 125°C		V_{CC} – 0.6	V_{CC}	
		$I_{OH(max)}$ = –1.5 mA (1)	–55°C to 125°C	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{OH(max)}$ = –6 mA (2)	–55°C to 125°C		V_{CC} – 0.6	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA (1)	–55°C to 125°C	2.2 V	V_{SS}	V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA (2)	–55°C to 125°C		V_{SS}	V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA (1)	–55°C to 125°C	3 V	V_{SS}	V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA (2)	–55°C to 125°C		V_{SS}	V_{SS}+0.6	

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency (Ports P1, P2, P3, and P4) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ against $V_{CC}/2$ (1) (2)	–55°C to 125°C	2.2 V		10	MHz
				3 V		12	
f_{Port_CLK}	Clock output frequency	P2.0/ACLK, P1.4/SMCLK, C_L = 20 pF (2)	–55°C to 125°C	2.2 V		12	MHz
				3 V		16	

(1) A resistive divider with 2 times 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics – Outputs

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

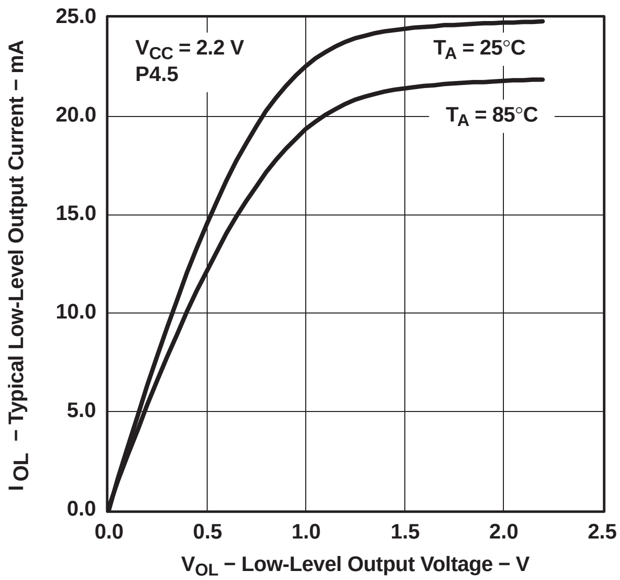


Figure 4.

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

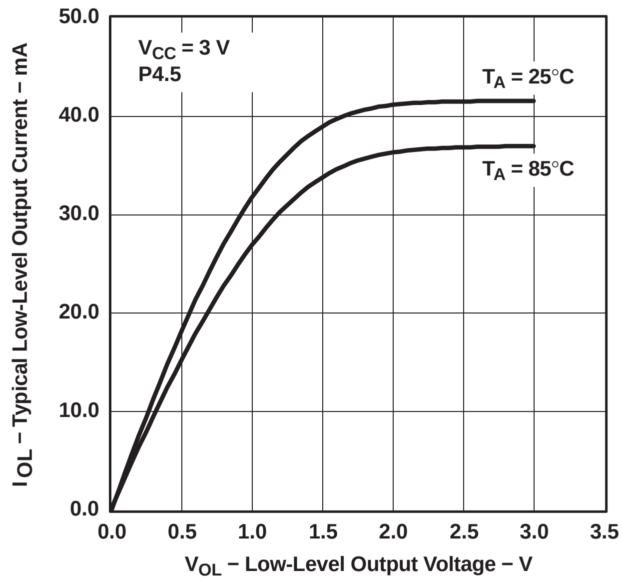


Figure 5.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

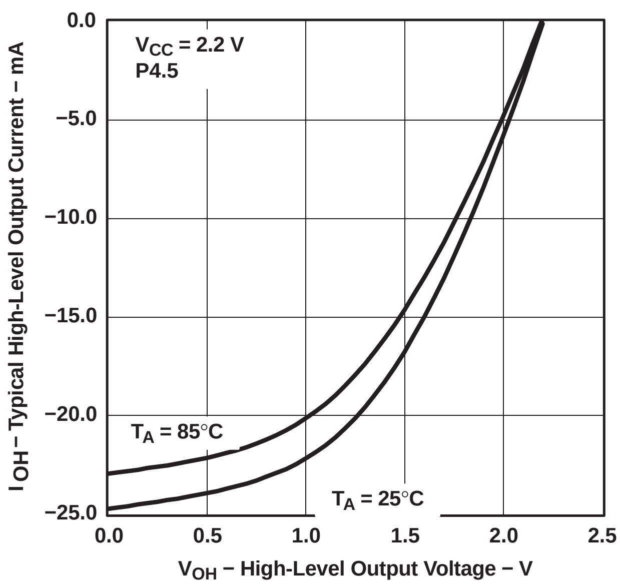


Figure 6.

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

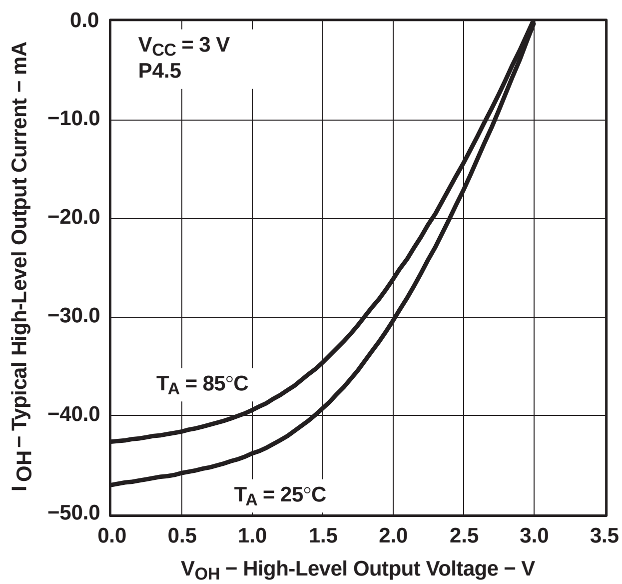


Figure 7.

POR/Brownout Reset (BOR) – Electrical Characteristics(1) (2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 8	$dV_{CC}/dt \le 3$ V/s				0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 8 through Figure 10	$dV_{CC}/dt \le 3$ V/s	–55°C to 125°C				1.71	V
$V_{hys(B\_IT-)}$	See Figure 8	$dV_{CC}/dt \le 3$ V/s	–55°C to 125°C		70	130	210	mV
$t_{d(BOR)}$	See Figure 8		–55°C to 125°C				2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally		–55°C to 125°C	2.2 V/3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.
(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

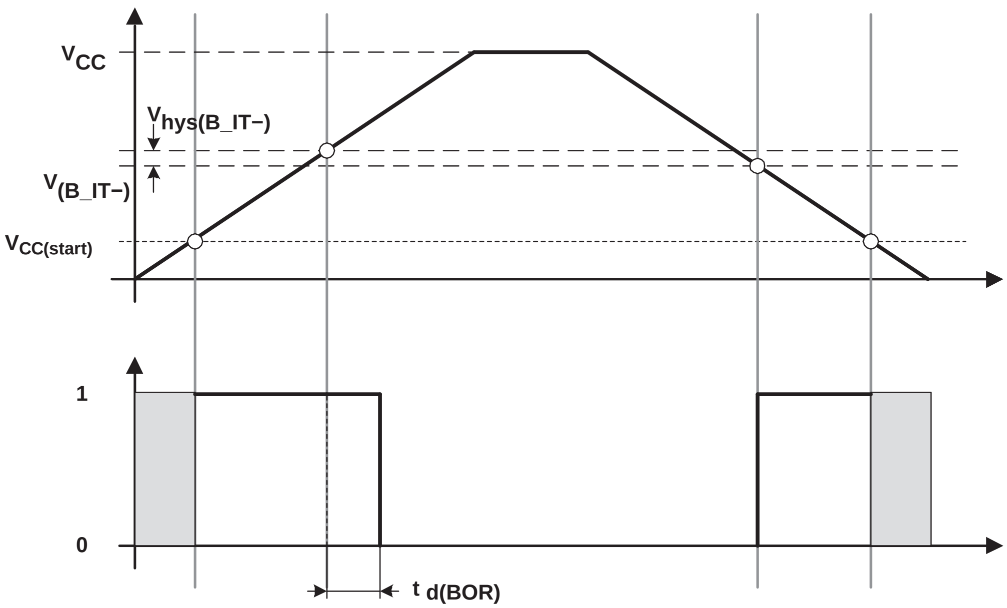


Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage

Typical Characteristics - POR/Brownout Reset (BOR)

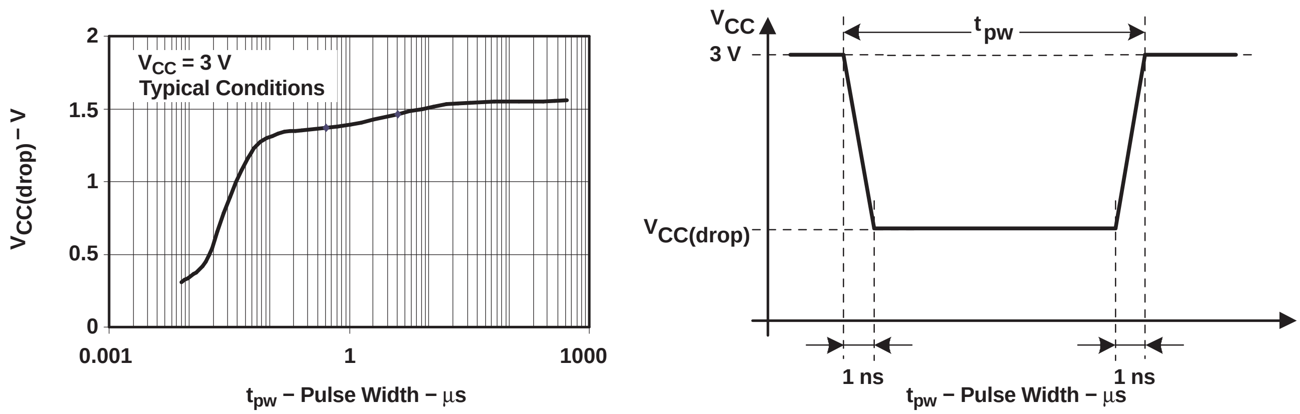


Figure 9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

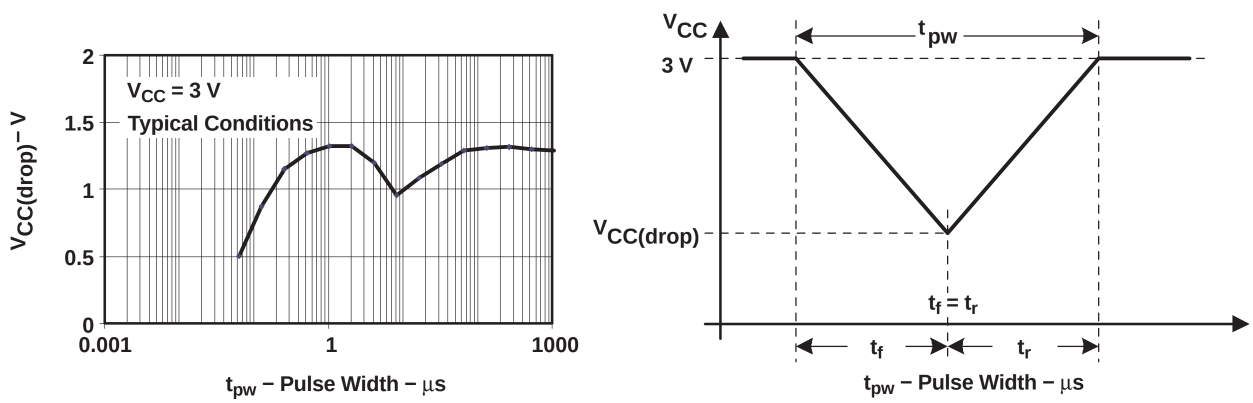


Figure 10. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO} + 1)}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO} + 1)}$$

DCO Frequency – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	RSELx < 14	–55°C to 125°C		1.8		3.6	V
		RSELx = 14	–55°C to 125°C		2.2		3.6	
		RSELx = 15	–55°C to 125°C		3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	–55°C to 125°C	2.2 V/3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	1.60		3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	3.00		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	4.30		7.30	M Hz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	–55°C to 125°C	2.2 V/3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	–55°C to 125°C	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	–55°C to 125°C	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	–55°C to 125°C	2.2 V/3 V			1.55	ratio

DCO Frequency – Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	–55°C to 125°C	2.2 V/3 V	1.05	1.08	1.12	ratio
Duty cycle		Measured at P1.4/SMCLK	–55°C to 125°C	2.2 V/3 V	40	50	60	%

Calibrated DCO Frequencies (Tolerance at Calibration) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
Frequency tolerance at calibration			25°C	3 V	–1	±0.2	1	%
$f_{CAL(1\ MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8\ MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12\ MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16\ MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

Calibrated DCO Frequencies (Tolerance Over Temperature) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature			–55°C to 125°C	3 V	–2.5	±0.5	2.5	%
8-MHz tolerance over temperature			–55°C to 125°C	3 V	–2.5	±1.0	2.5	%
12-MHz tolerance over temperature			–55°C to 125°C	3 V	–2.5	±1.0	2.5	%
16-MHz tolerance over temperature			–55°C to 125°C	3 V	–3.0	±2.0	3.0	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	–55°C to 125°C	2.2 V	0.970	1	1.030	MHz
				3 V	0.975	1	1.025	
				3.6 V	0.970	1	1.030	
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	–55°C to 125°C	2.2 V	7.760	8	8.400	MHz
				3 V	7.800	8	8.200	
				3.6 V	7.600	8	8.240	
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	–55°C to 125°C	2.2 V	11.70	12	12.30	MHz
				3 V	11.70	12	12.30	
				3.6 V	11.70	12	12.30	
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	–55°C to 125°C	3 V	15.52	16	16.48	MHz
				3.6 V	15.00	16	16.48	

Calibrated DCO Frequencies (Tolerance Over Supply Voltage V_{CC}) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over V_{CC}			25°C	1.8 V to 3.6 V	–3	±2	3	%
8-MHz tolerance overV_{CC}			25°C	1.8 V to 3.6 V	–3	±2	3	%
12-MHz tolerance over V_{CC}			25°C	2.2 V to 3.6 V	–3	±2	3	%
16-MHz tolerance over V_{CC}			25°C	3 V to 3.6 V	–6	±2	3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.970	1	1.030	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.760	8	8.240	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V to 3.6 V	15.00	16	16.48	MHz

Calibrated DCO Frequencies (Overall Tolerance) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature			–55°C to 125°C	1.8 V to 3.6 V	-5	±2	+5	%
8-MHz tolerance over temperature			–55°C to 125°C	1.8 V to 3.6 V	-5	±2	+5	%
12-MHz tolerance over temperature			–55°C to 125°C	2.2 V to 3.6 V	-5	±2	+5	%
16-MHz tolerance over temperature			–55°C to 125°C	3 V to 3.6 V	-6	±3	+6	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	–55°C to 125°C	1.8 V to 3.6 V	.950	1	1.050	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	–55°C to 125°C	1.8 V to 3.6 V	7.6	8	8.4	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	–55°C to 125°C	2.2 V to 3.6 V	11.4	12	12.6	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	–55°C to 125°C	3 V to 3.6 V	15.00	16	17.00	MHz

Typical Characteristics – Calibrated 1-MHz DCO Frequency

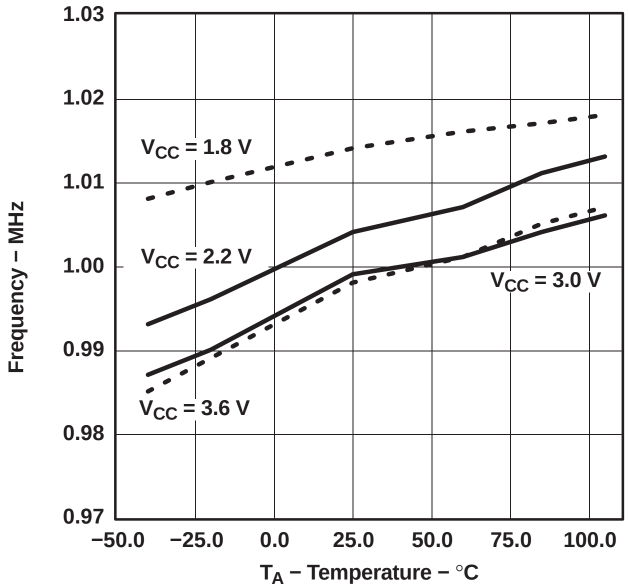


Figure 11. Calibrated 1-MHz Frequency vs Temperature

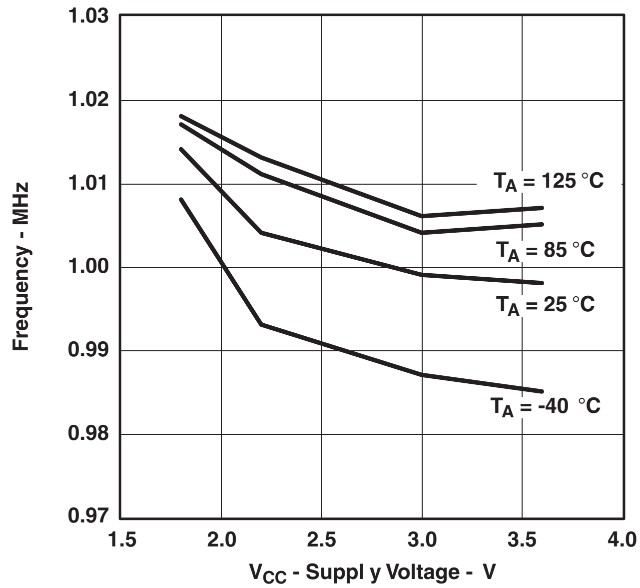


Figure 12. Calibrated 1-MHz Frequency vs V_{CC}

Wake-Up From Lower-Power Modes (LPM3/4) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (1)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ,	–55°C to 125°C	2.2 V/3 V			2	μs
		BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ,	–55°C to 125°C	2.2 V/3 V			1.5	
		BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ,	–55°C to 125°C	3 V			1	
		BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ,	–55°C to 125°C	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (2)					$1/f_{MCLK} + t_{Clock,LPM3/4}$		

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics – DCO Clock Wake-Up Time From LPM3/4

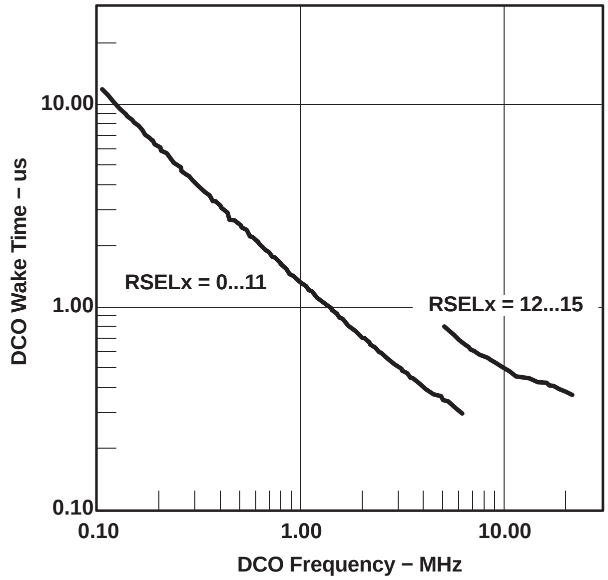


Figure 13. Clock Wake-Up Time From LPM3 vs DCO Frequency

DCO With External Resistor R_{OSC} – Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
$f_{DCO,ROSC}$	DCO output frequency with R_{OSC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T_A = 25°C	2.2 V	1.8	MHz
			3 V	1.95	
D_t	Temperature drift	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	±0.1	%/°C
D_V	Drift with V_{CC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	10	%/V

(1) R_{OSC} = 100kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and T_K = ±50ppm/°C

Typical Characteristics - DCO With External Resistor R_{OSC}

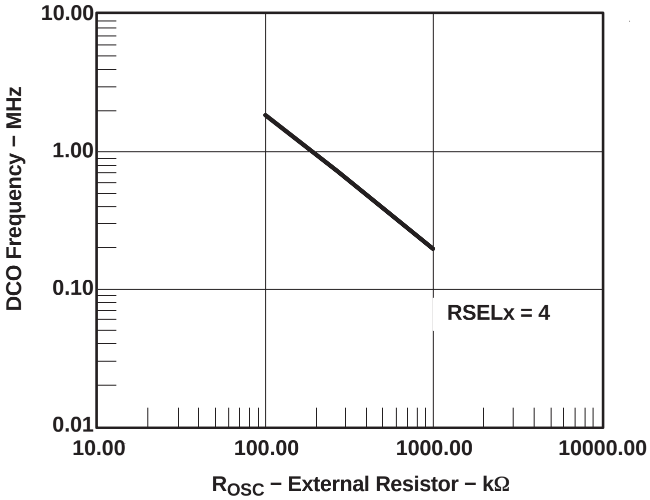


Figure 14. DCO Frequency vs R_{OSC}, V_{CC} = 2.2 V, T_A = 25°C

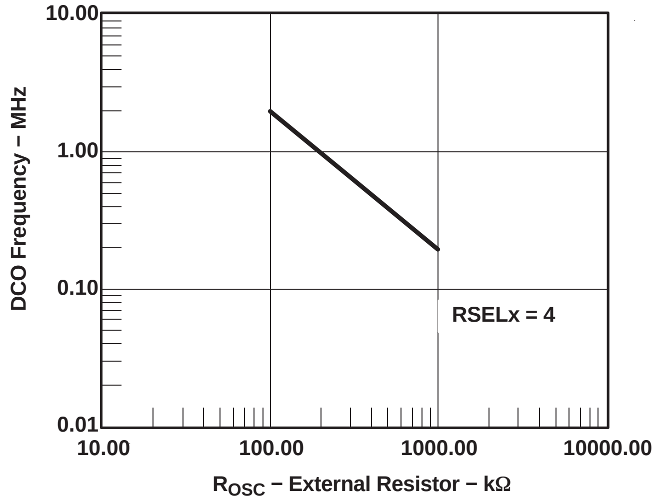


Figure 15. DCO Frequency vs R_{OSC}, V_{CC} = 3.0 V, T_A = 25°C

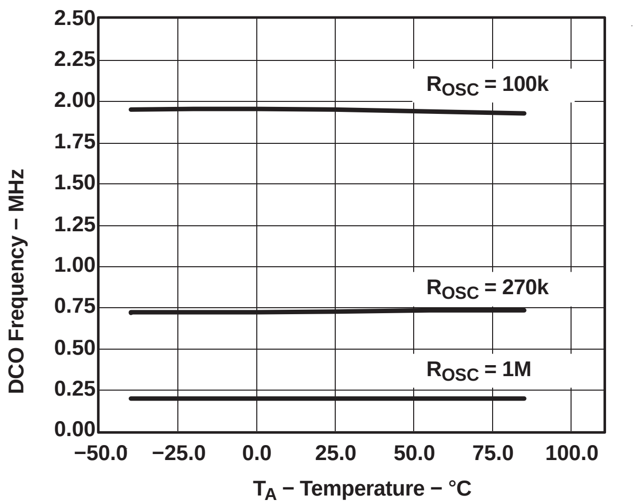


Figure 16. DCO Frequency vs Temperature, V_{CC} = 3.0 V

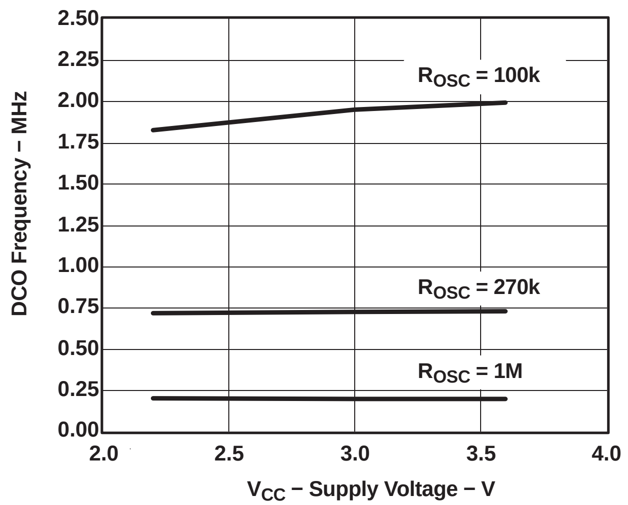


Figure 17. DCO Frequency vs V_{CC}, T_A = 25°C

Crystal Oscillator (LFXT1) Low-Frequency Modes – Electrical Characteristics(1) (2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1		–55°C to 105°C	1.8 V to 3.6 V		32,768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3		–55°C to 125°C	1.8 V to 3.6 V	10,000	32,768	50,000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 6 pF		–55°C to 105°C			500		kΩ
		XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 12 pF		–55°C to 105°C			200		kΩ
$C_{L,eff}$	Integrated effective load capacitance, LF mode(3)	XTS = 0	XCAPx = 0	–55°C to 105°C			1		pF
			XCAPx = 1				5.5		
			XCAPx = 2				8.5		
			XCAPx = 3				11		
Duty Cycle	LF mode	XTS = 0, Measured at P1.4/ACLK, $f_{LFXT1,LF}$ = 32,768 Hz		–55°C to 125°C	2.2 V/3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency threshold, LF mode (4)	XTS = 0, LFXT1Sx = 3(5)		–55°C to 125°C	2.2 V/3 V	10		10,000	Hz

(1) To improve EMI on the LFXT1 oscillator the following guidelines should be observed:
(a) Keep as short of a trace as possible between the device and the crystal.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Use of the LFXT1 Crystal Oscillator with T_A > 105°C is not guaranteed. It is recommended that an external digital clock source or the internal DCO is used to provide clocking.

(3) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.

(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(5) Measured with logic-level input frequency, but also applies to operation with crystals with T_A < 105°C.

Internal Very-Low-Power, Low-Frequency Oscillator (VLO) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency		–55°C to 85°C	2.2 V/3 V	4	12	20	kHz
			125°C	2.2 V/3 V			22	kHz
df_{VLO}/dT	VLO frequency temperature drift	(1)	–55°C to 125°C	2.2 V/3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	(2)	25°C	1.8 V – 3.6V		4		%/V

(1) Calculated using the box method:
I Version: [MAX(–55...85°C) – MIN(–55...85°C)]/MIN(55–...85°C)/[85°C – (–55°C)]
T Version: [MAX(–55...125°C) – MIN(–55...125°C)]/MIN(–55...125°C)/[125°C – (–55°C)]

(2) Calculated using the box method: [MAX(1.8...3.6 V) – MIN(1.8...3.6 V)]/MIN(1.8...3.6 V)/(3.6 V – 1.8 V)

Crystal Oscillator (LFXT1) High Frequency Modes – Electrical Characteristics[(1)] [(2)]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0	–55°C to 125°C	1.8 V to 3.6 V	0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator lcrystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1	–55°C to 125°C	1.8 V to 3.6 V	1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2	–55°C to 125°C	1.8 V to 3.6 V	2		10	MHz
				2.2 V to 3.6 V	2		12	
				3 V to 3.6 V	2		16	
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3	–55°C to 125°C	1.8 V to 3.6 V	0.4		10	MHz
				2.2 V to 3.6 V	0.4		12	
				3 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation allowance for HF crystals (see Figure 18 and Figure 19)	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF	–55°C to 125°C			2700		Ω
		XTS = 0, LFXT1Sx = 1 $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF				800		
		XTS = 0, LFXT1Sx = 2 $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF				300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode[(3)]	XTS = 1[(4)]	–55°C to 125°C			1		pF
Duty Cycle	HF mode	XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 10 MHz	–55°C to 125°C	2.2 V/3 V	40	50	60	%
		XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 16 MHz	–55°C to 125°C		40	50	60	
$f_{Fault,HF}$	Oscillator fault frequency, HF mode[(5)]	XTS = 1, LFXT1Sx = 3[(6)]	–55°C to 125°C	2.2 V/3 V	30		300	kHz

(1) To improve EMI on the LFXT1 oscillator the following guidelines should be observed:
   (a) Keep as short of a trace as possible between the device and the crystal.
   (b) Design a good ground plane around the oscillator pins.
   (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Use of the LFXT1 Crystal Oscillator with T_A > 105°C is not guaranteed. It is recommended that an external digital clock source or the internal DCO is used to provide clocking.

(3) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.

(4) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(5) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(6) Measured with logic-level input frequency, but also applies to operation with crystals

Typical Characteristics – LFXT1 Oscillator in HF Mode (XTS = 1)

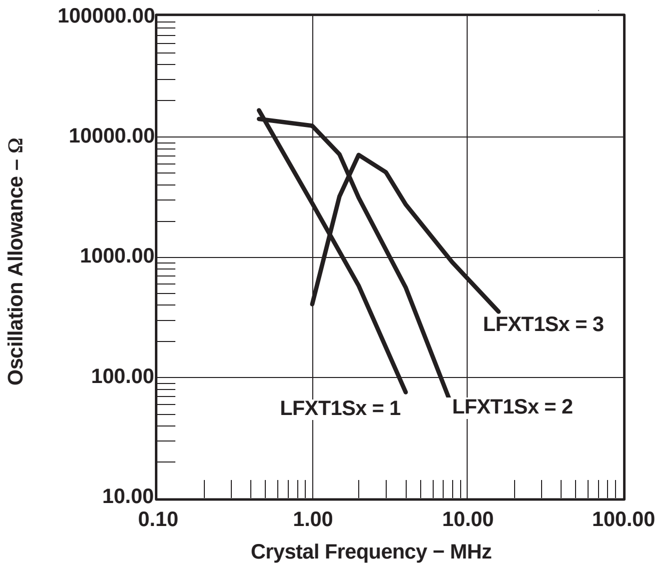


Figure 18. Oscillation Allowance vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

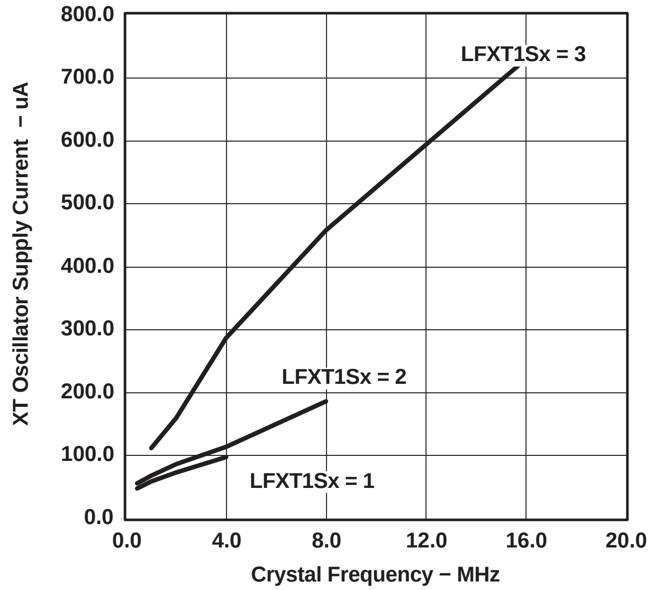


Figure 19. XT Oscillator Supply Current vs Crystal Frequency, $C_{L,eff}$ = 15 pF, T_A = 25°C

Timer_A – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty cycle = 50% ± 10%	–55°C to 125°C	2.2 V		10	MHz
				3 V		16	
$t_{TA,cap}$	Timer_A, capture timing	TA0, TA1, TA2	–55°C to 125°C	2.2 V/3 V	20		ns

Timer_B – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	MAX	UNIT
f_{TB}	Timer_B clock frequency	Internal: SMCLK, ACLK, External: TBCLK, Duty Cycle = 50% ± 10%	–55°C to 125°C	2.2 V		10	MHz
				3 V		16	
$t_{TB,cap}$	Timer_B, capture timing	TB0, TB1, TB2	–55°C to 125°C	2.2 V/3 V	20		ns

USCI (UART Mode) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK, External: UCLK; Duty cycle = 50% ± 10%	–55°C to 125°C				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)		–55°C to 125°C	2.2 V/3 V			1	MHz
$t_τ$	UART receive deglitch time [1]		–55°C to 125°C	2.2 V	50	150	600	ns
				3 V	50	150	600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their width should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 20 and Figure 21)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK, Duty cycle = 50% ± 10%	–55°C to 125°C			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		–55°C to 125°C	2.2 V	110		ns
				3 V	75		
$t_{HD,MI}$	SOMI input data hold time		–55°C to 125°C	2.2 V	0		ns
				3 V	0		
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	–55°C to 125°C	2.2 V		30	ns
				3 V		20	

USCI (SPI Slave Mode) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 22 and Figure 23)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock			2.2 V/3 V		50		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE high		–55°C to 125°C	2.2 V/3 V	10			ns
$t_{STE,ACC}$	STE access time, STE low to SOMI data out			2.2 V/3 V		50		ns
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance			2.2 V/3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		–55°C to 125°C	2.2 V	20			ns
				3 V	15			
$t_{HD,SI}$	SIMO input data hold time		–55°C to 125°C	2.2 V	10			ns
				3 V	10			
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	–55°C to 125°C	2.2 V		75	110	ns
				3 V		50	75	

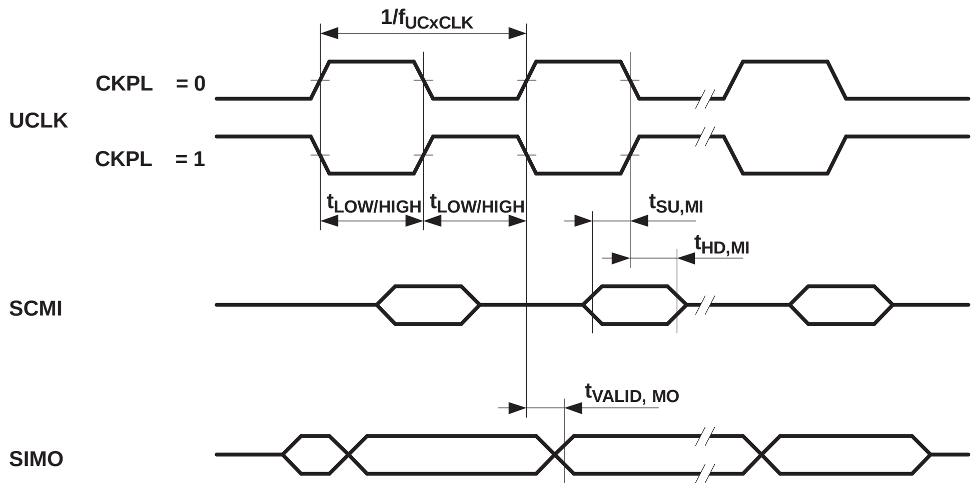


Figure 20. SPI Master Mode, CKPH = 0

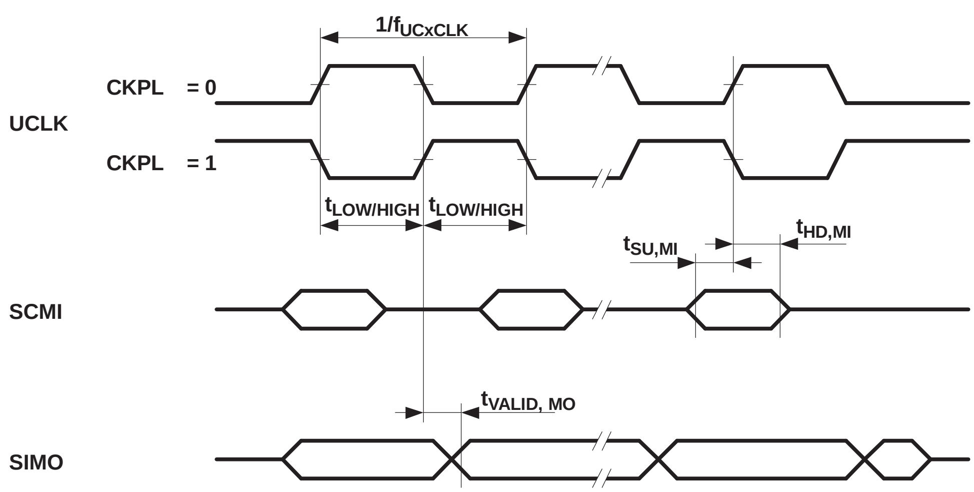


Figure 21. SPI Master Mode, CKPH = 1

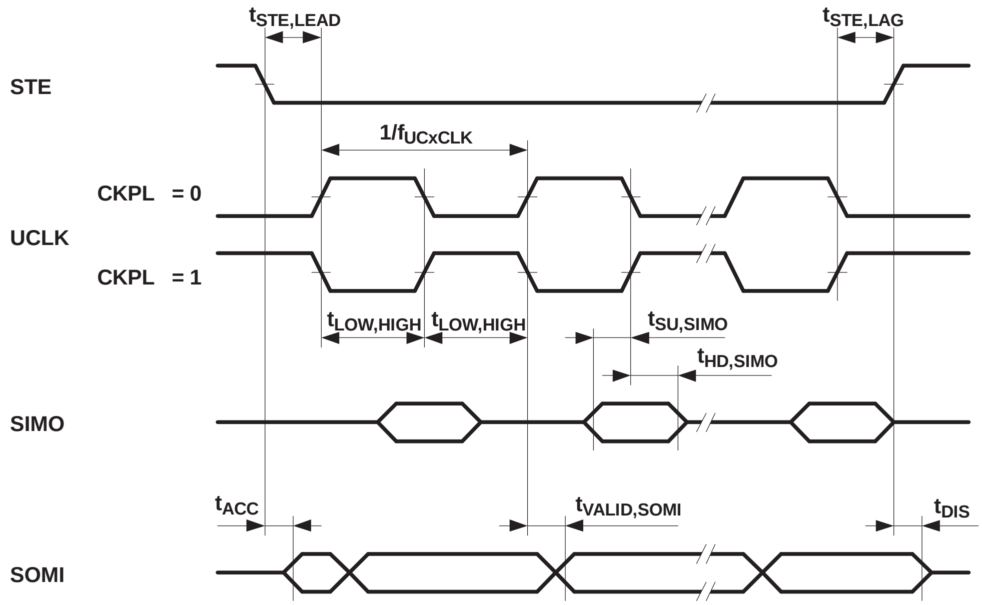


Figure 22. SPI Slave Mode, CKPH = 0

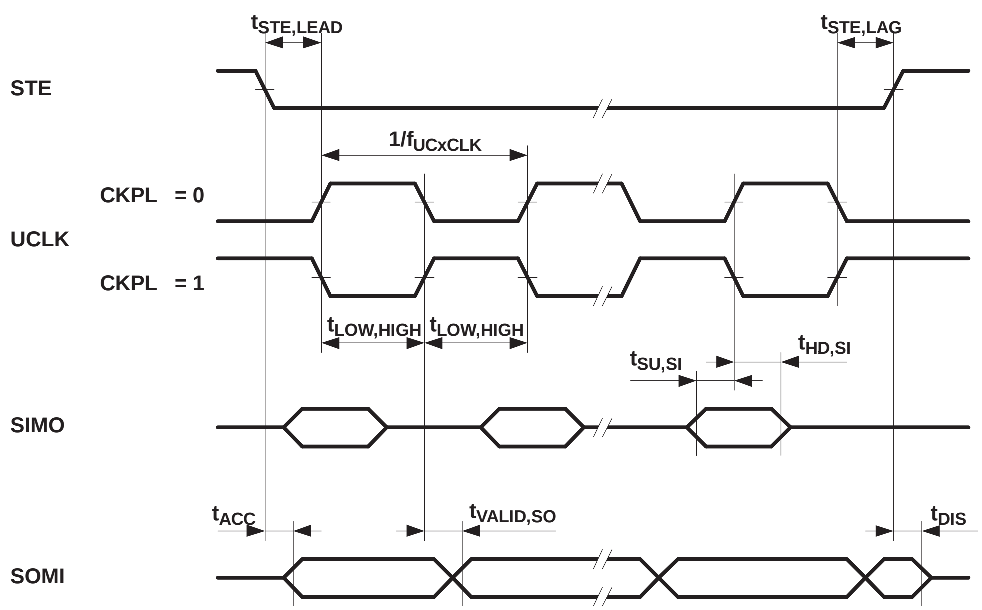


Figure 23. SPI Slave Mode, CKPH = 1

USCI (I2C Mode) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 24)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK, External: UCLK, Duty cycle = 50% ± 10%				f_{SYSTEM}		MHz
f_{SCL}	SCL clock frequency		–55°C to 125°C	2.2 V/3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	–55°C to 125°C	2.2 V/3 V	4.0			µs
		f_{SCL} > 100 kHz	–55°C to 125°C		0.6			
$t_{SU,STA}$	Set-up time for a repeated START	f_{SCL} ≤ 100 kHz	–55°C to 125°C	2.2 V/3 V	4.7			µs
		f_{SCL} > 100 kHz	–55°C to 125°C		0.6			
$t_{HD,DAT}$	Data hold time		–55°C to 125°C	2.2 V/3 V	0			ns
$t_{SU,DAT}$	Data set-up time		–55°C to 125°C	2.2 V/3 V	250			ns
$t_{SU,STO}$	Set-up time for STOP		–55°C to 125°C	2.2 V/3 V	4.0			µs
t_{SP}	Pulse width of spikes suppressed by input filter		–55°C to 125°C	2.2 V	50	150	600	ns
				3 V	50	100	600	

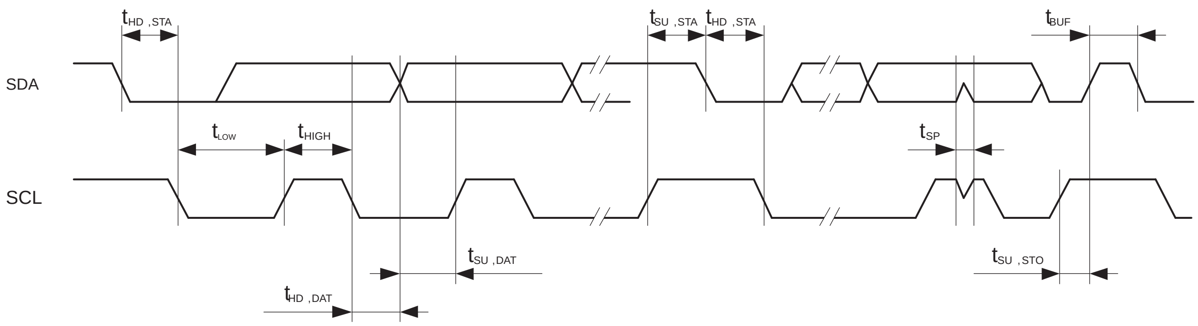


Figure 24. I2C Mode Timing

10-Bit ADC, Power-Supply and Input Range Conditions – Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage range	V_{SS} = 0 V	–55°C to125 °C		2.2		3.6	V
V_{Ax}	Analog input voltage range (2)	All Ax terminals, Analog inputs selected in ADC10AE register	–55°C to 125°C		0		V_{CC}	V
I_{ADC10}	ADC10 supply current(3)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	–55°C to 125°C	2.2 V		0.52	1.05	mA
				3 V		0.6	1.2	
I_{REF+}	Reference supply current, reference buffer disabled(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	–55°C to 125°C	2.2 V/3 V		0.25	.4	mA
		$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0	–55°C to 125°C	3 V				
$I_{REFB,0}$	Reference buffer supply current with ADC10SR = 0(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0	–55°C to 85°C	2.2 V/3 V		1.1	1.4	mA
			125°C	2.2 V/3 V			1.8	
$I_{REFB,1}$	Reference buffer supply current with ADC10SR = 1(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR=1	–55°C to 85°C	2.2 V/3 V		0.5	.7	mA
			125°C	2.2 V/3 V			.8	mA
C_I	Input capacitance	Only one terminal Ax selected at a time				27		pF
R_I	Input MUX ON resistance	0 V ≤ V_{Ax} ≤ V_{CC}		2.2 V/3 V		2000		Ω

(1) The leakage current is defined in the leakage current table with Px.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC10}.
(4) The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

10-Bit ADC, Built-In Voltage Reference – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	I_{VREF+} ≤ 1 mA, REF2_5V = 0		–55°C to 125°C		2.2			V
		I_{VREF+} ≤ 0.5 mA, REF2_5V = 1		–55°C to 125°C		2.8			
		I_{VREF+} ≤ 1 mA, REF2_5V = 1		–55°C to 125°C		2.9			
V_{REF+}	Positive built-in reference voltage	I_{VREF+} ≤ I_{VREF+}max, REF2_5V = 0		–55°C to 125°C	2.2 V/3 V	1.41	1.5	1.59	V
		I_{VREF+} ≤ I_{VREF+}max, REF2_5V = 1		–55°C to 125°C	3 V	2.35	2.5	2.65	
$I_{LD,VREF+}$	Maximum V_{REF+} load current			–55°C to 125°C	2.2 V			±0.5	mA
					3 V			±1	
	V_{REF+} load regulation	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage V_{Ax} ≉ 0.75 V, REF2_5V = 0		–55°C to 125°C	2.2 V/3 V			±2	LSB
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage V_{Ax} ≉ 1.25 V, REF2_5V = 1		–55°C to 125°C	3 V			±2	
	V_{REF+} load regulation response time	I_{VREF+} = 100 µA→900 µA, V_{Ax} ≉ 0.5 × V_{REF+}, Error of conversion result ≤ 1 LSB	ADC10SR = 0	–55°C to 125°C	3 V			400	ns
			ADC10SR = 1	–55°C to 125°C				2000	
C_{VREF+}	Maximum capacitance at pin V_{REF+} (1)	I_{VREF+} ≤ = 1 mA, REFON = 1, REFOUT = 1		–55°C to 125°C	2.2 V/3 V			100	pF
TC_{REF+}	Temperature coefficient	I_{VREF+} = const. with 0 mA ≤ I_{VREF+} ≤ 1 mA		–55°C to 125°C	2.2 V/3 V			±100	ppm/°C
t_{REFON}	Settling time of internal reference voltage (2)	I_{VREF+} = 0.5 mA, REF2_5V = 0 REFON = 0 → 1		–55°C to 125°C	3.6 V			30	µs
$t_{REFBURST}$	Settling time of reference buffer (2)	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 1, REFBURST = 1	ADC10SR = 0	–55°C to 125°C	2.2 V			1	µs
			ADC10SR = 1	–55°C to 125°C				2.5	
		I_{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1	ADC10SR = 0	–55°C to 125°C	3 V			2	
			ADC10SR = 1	–55°C to 125°C				4.5	

(1) The capacitance applied to the internal buffer operational amplifier, if switched to terminal P2.4/TA2/A4/V_{REF+}/V_{eREF+} (REFOUT = 1), must be limited; the reference buffer may become unstable otherwise.
(2) The condition is that the error in a conversion started after t_{REFON} or t_{RefBuf} is less than ±0.5 LSB.

10-Bit ADC, External Reference – Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	MAX	UNIT
V_{eREF+}	Positive external reference input voltage range (2)	$V_{eREF+} > V_{eREF-}$, SREF1 = 1, SREF0 = 0	–55°C to 125°C		1.4	V_{CC}	V
		$V_{eREF-} \le V_{eREF+} \le V_{CC}$ – 0.15 V,SREF1 = 1, SREF0 = 1 (3)	–55°C to 125°C		1.4	3.0	
V_{eREF-}	Negative external reference input voltage range (4)	$V_{eREF+} > V_{eREF-}$	–55°C to 125°C		0	1.2	V
ΔV_{eREF}	Differential external reference input voltage range, $\Delta V_{eREF} = V_{eREF+} - V_{eREF-}$	$V_{eREF+} > V_{eREF-}$ (5)	–55°C to 125°C		1.4	V_{CC}	V
I_{VeREF+}	Static input current into V_{eREF+}	0 V ≤ $V_{eREF+} \le V_{CC}$, SREF1 = 1, SREF0 = 0	–55°C to 125°C	2.2 V/3 V		±1	µA
		0 V ≤ $V_{eREF+} \le V_{CC}$ – 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1(3)	–55°C to 125°C	2.2 V/3 V		0	
I_{VeREF-}	Static input current into V_{eREF-}	0 V ≤ $V_{eREF-} \le V_{CC}$	–55°C to 125°C	2.2 V/3 V		±1	µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
(4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

10-Bit ADC, Timing Parameters – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR=0	–55°C to 125°C	2.2 V/3 V	0.45		6.5	MHz
			ADC10SR=1	–55°C to 125°C	2.2 V/3 V	0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		–55°C to 125°C	2.2 V/3 V	3.25		6.45	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		–55°C to 125°C	2.2 V/3 V	2.06		3.51	µs
		$f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0		–55°C to 125°C			13 = ADC10DIVx 1/$f_{ADC10CLK}$		
$t_{ADC10ON}$	Turn-on settling time of the ADC			(1)–55°C to 125°C				100	ns

(1) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

10-Bit ADC, Linearity Parameters – Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		–55°C to 125°C	2.2 V/3 V			±1	LSB
E_D	Differential linearity error		–55°C to 125°C	2.2 V/3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω	–55°C to 125°C	2.2 V/3 V			±1	LSB
E_G	Gain error	SREFx = 010, un-buffered external reference, V_{eREF+} = 1.5 V	–55°C to 125°C	2.2 V		±1.1	±2	LSB
		SREFx = 010; un-buffered external reference, V_{eREF+} = 2.5 V	–55°C to 125°C	3 V		±1.1	±2	
		SREFx = 011, buffered external reference(2), V_{eREF+} = 1.5 V	–55°C to 125°C	2.2 V		±1.1	±4	
		SREFx = 011, buffered external reference (2), V_{eREF+} = 2.5 V	–55°C to 125°C	3 V		±1.1	±3	
E_T	Total unadjusted error	SREFx = 010, unbuffered external reference, V_{eREF+} = 1.5 V	–55°C to 125°C	2.2 V		±2	±5	LSB
		SREFx = 010, unbuffered external reference, V_{eREF+} = 2.5 V	–55°C to 125°C	3 V		±2	±5	
		SREFx = 011, buffered external reference(2), V_{eREF+} = 1.5 V	–55°C to 125°C	2.2 V		±2	±7	
		SREFx = 011, buffered external reference(2), V_{eREF+} = 2.5 V	–55°C to 125°C	3 V		±2	±6	

(1) 2.2V Not Production Tested.
(2) The reference buffer's offset adds to the gain and total unadjusted error.

10-Bit ADC, Temperature Sensor and Built-In V_{MID} – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Temperature sensor supply current(1)	REFON = 0, INCHx = 0Ah, T_A = 25°C	–55°C to 125°C	2.2 V		40	120	μA
				3 V		60	160	
TC_{SENSOR}		ADC10ON = 1, INCHx = 0Ah(2)	–55°C to 125°C	2.2 V/3 V	3.44	3.55	3.66	mV/°C
$V_{Offset,Sensor}$	Sensor offset voltage	ADC10ON = 1, INCHx = 0Ah(2)	–55°C to 125°C		-100		100	mV
V_{Sensor}	Sensor output voltage(3)	Temperature sensor voltage at T_A = 125°C (T version only)	–55°C to 125°C	2.2 V/3 V	1265	1365	1465	mV
		Temperature sensor voltage at T_A = 85°C	–55°C to 125°C		1195	1295	1395	
		Temperature sensor voltage at T_A = 25°C	–55°C to 125°C		985	1085	1185	
		Temperature sensor voltage at T_A = 0°C	–55°C to 125°C		895	995	1095	
$t_{Sensor(sample)}$	Sample time required if channel 10 is selected(4)	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	–55°C to 125°C	2.2 V/3 V	30			μs
I_{VMID}	Current into divider at channel 11(5)	ADC10ON = 1, INCHx = 0Bh	–55°C to 125°C	2.2 V			NA	μA
				3 V			NA	
V_{MID}	V_{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, V_{MID} is ≉ 0.5 × V_{CC}	–55°C to 125°C	2.2 V	1.06	1.1	1.14	V
				3 V	1.46	1.5	1.54	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected(6)	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	–55°C to 125°C	2.2 V	1400			ns
				3 V	1220			

(1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
(2) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
$V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A = 0°C)$ [mV]
(3) Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offset,sensor}$.
(4) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(5) No additional current is needed. The V_{MID} is used during sampling.
(6) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

Operational Amplifier (OA) Supply Specifications – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range		–55°C to 125°C		2.2		3.6	V
I_{CC}	Supply current(1)	Fast Mode	–55°C to 125°C	2.2 V/3 V		180	290	μA
		Medium Mode	–55°C to 125°C			110	190	
		Slow Mode	–55°C to 125°C			50	80	
PSSR	Power-supply rejection ratio	Noninverting		2.2 V/3 V		70		dB

(1) Corresponding pins configured as OA inputs and outputs, respectively.

Operational Amplifier (OA) Input/Output Specifications – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$V_{I/P}$	Input voltage range		–55°C to 125°C		–0.1		V_{CC} - 1.2	V
I_{lkg}	Input leakage current[1] [2]		–55°C to 55°C	2.2 V/3 V	–15	±0.5	15	nA
			55°C to 85°C		–20	±5	20	
			85°C to 125°C		–100		100	
V_n	Voltage noise density, I/P	Fast Mode, $f_{V(I/P)}$ = 1 kHz				50		nV/√Hz
		Medium Mode, $f_{V(I/P)}$ = 1 kHz				80		
		Slow Mode, $f_{V(I/P)}$ = 1 kHz				140		
		Fast Mode, $f_{V(I/P)}$ = 10 kHz				30		
		Medium Mode, $f_{V(I/P)}$ = 10 kHz				50		
		Slow Mode, $f_{V(I/P)}$ = 10 kHz				65		
V_{IO}	Offset voltage, I/P		–55°C to 125°C	2.2 V/3 V			±10	mV
	Offset temperature drift, I/P	See [3]		2.2 V/3 V		±10		μV/°C
	Offset voltage drift with supply, I/P	0.3 V ≤ V_{IN} ≤ V_{CC} – 1.0 V ΔV_{CC} ≤ ±10%, T_A = 25°C	–55°C to 125°C	2.2 V/3 V			±1.5	mV/V
V_{OH}	High-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ –500 μA	–55°C to 125°C	2.2 V/3 V	V_{CC} – 0.2		V_{CC}	V
		Slow Mode, I_{SOURCE} ≤ –150 μA	–55°C to 125°C		V_{CC} – 0.1		V_{CC}	
V_{OL}	Low-level output voltage, O/P	Fast Mode, I_{SOURCE} ≤ 500 μA	–55°C to 125°C	2.2 V/3 V	V_{SS}		0.2	V
		Slow Mode, I_{SOURCE} ≤ 150 μA	–55°C to 125°C		V_{SS}		0.1	
$R_{O/P(OAx)}$	Output resistance[4] (see Figure 25)	R_{Load} = 3 kΩ, C_{Load} = 50 pF, $V_{O/P(OAx)}$ < 0.2 V		2.2 V/3 V		150		Ω
		R_{Load} = 3 kΩ, C_{Load} = 50 pF, $V_{O/P(OAx)}$ > V_{CC} – 1.2 V				150		
		R_{Load} = 3 kΩ, C_{Load} = 50 pF, 0.2 V ≤ $V_{O/P(OAx)}$ ≤ V_{CC} – 0.2 V				0.1		
CMRR	Common-mode rejection ratio	Noninverting		2.2 V/3 V		70		dB

(1) ESD damage can degrade input current leakage.
(2) The input bias current is overridden by the input leakage current.
(3) Calculated using the box method
(4) Specification valid for voltage-follower OAx configuration

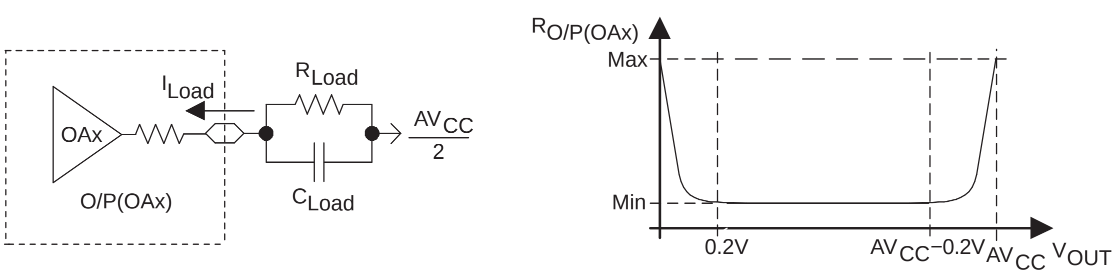


Figure 25. OAx Output Resistance Tests

Operational Amplifier (OA) Dynamic Specifications – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
SR	Slew rate	Fast Mode				1.2		V/μs
		Medium Mode				0.8		
		Slow Mode				0.3		
	Open-loop voltage gain					100		dB
φm	Phase margin	C_L = 50 pF				60		deg
	Gain margin	C_L = 50 pF				20		dB
GBW	Gain-bandwidth product (see Figure 26 and Figure 27)	Noninverting, Fast Mode, R_L = 47 kΩ, C_L = 50 pF		2.2 V/3 V		2.2		MHz
		Noninverting, Medium Mode, R_L = 300 kΩ, C_L = 50 pF				1.4		
		Noninverting, Slow Mode, R_L = 300 kΩ, C_L = 50 pF				0.5		
$t_{en(on)}$	Enable time on	t_{on}, noninverting, Gain = 1	–55°C to 125°C	2.2 V/3 V		10	20	μs
$t_{en(off)}$	Enable time off		–55°C to 125°C	2.2 V/3 V			1	μs

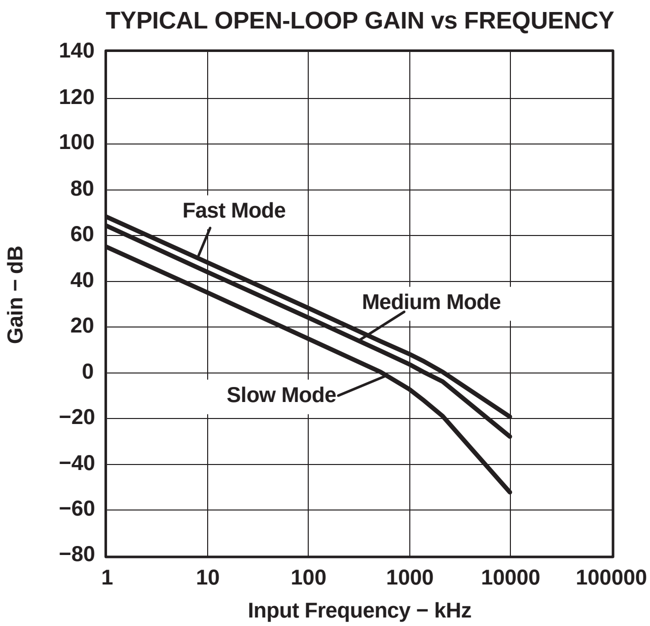


Figure 26.

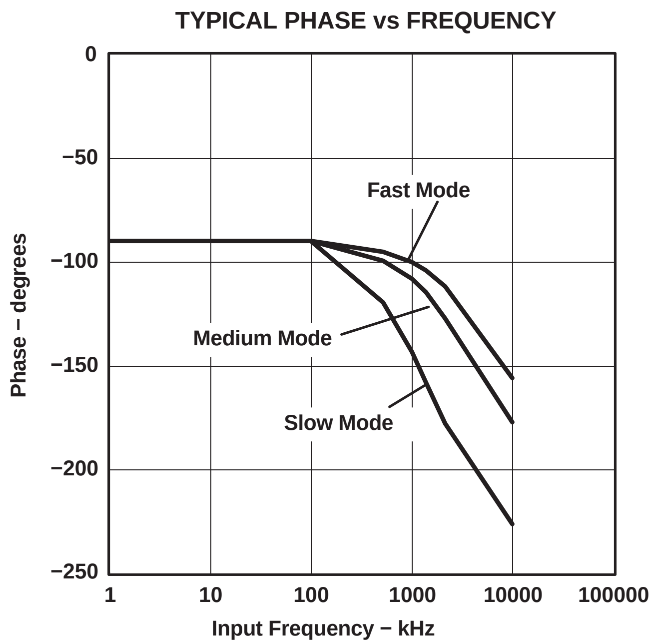


Figure 27.

Operational Amplifier OA Feedback Network, Resistor Network – Electrical Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
R_{total}	Total resistance of resistor string				96		kΩ
R_{unit}	Unit resistor of resistor string(2)				6		kΩ

(1) A single resistor string is composed of 4 R_{unit} + 4 R_{unit} + 2 R_{unit} + 2 R_{unit} + 1 R_{unit} + 1 R_{unit} + 1 R_{unit} + 1 R_{unit} = 16 R_{unit} = R_{total}.
(2) For the matching (i.e., the relative accuracy) of the unit resistors on a device, refer to the gain and level specifications of the respective configurations.

Operational Amplifier (OA) Feedback Network, Comparator Mode (OAFCx = 3) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{Level}	Comparator level	OAFBRx = 1, OARRIP = 0	–55°C to 125°C	2.2 V/3 V	0.242	1/4	0.262	V_{CC}
		OAFBRx = 2, OARRIP = 0	–55°C to 125°C		0.492	½	0.512	
		OAFBRx = 3, OARRIP = 0	–55°C to 125°C		0.619	5/8	0.639	
		OAFBRx = 4, OARRIP = 0				N/A (1)		
		OAFBRx = 5, OARRIP = 0				N/A (1)		
		OAFBRx = 6, OARRIP = 0				N/A (1)		
		OAFBRx = 7, OARRIP = 0				N/A (1)		
		OAFBRx = 1, OARRIP = 1	–55°C to 125°C		0.057	1/16	0.071	
		OAFBRx = 2, OARRIP = 1	–55°C to 125°C		0.122	1/8	0.128	
		OAFBRx = 3, OARRIP = 1	–55°C to 125°C		0.182	3/16	0.197	
		OAFBRx = 4, OARRIP = 1	–55°C to 125°C		0.242	1/4	0.262	
		OAFBRx = 5, OARRIP = 1	–55°C to 125°C		0.367	3/8	0.383	
		OAFBRx = 6, OARRIP = 1	–55°C to 125°C		0.492	½	0.512	
		OAFBRx = 7, OARRIP = 1				N/A (1)		
t_{PLH}, t_{PHL}	Propagation delay (low-high and high-low)	Fast Mode, Overdrive 10 mV		2.2 V/3 V		40		μs
		Fast Mode, Overdrive 100 mV				4		
		Fast Mode, Overdrive 500 mV				3		
		Medium Mode, Overdrive 10 mV				60		
		Medium Mode, Overdrive 100 mV				6		
		Medium Mode, Overdrive 500 mV				5		
		Slow Mode, Overdrive 10 mV				160		
		Slow Mode, Overdrive 100 mV				20		
		Slow Mode, Overdrive 500 mV				15		

(1) The level is not available due to the analog input voltage range of the operational amplifier.

Operational Amplifier (OA) Feedback Network, Noninverting Amplifier Mode (OAFCx = 4) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
G	Gain	OAFBRx = 0	–55°C to 125°C	2.2 V/3 V	0.970	1.00	1.035	
		OAFBRx = 1	–55°C to 125°C		1.325	1.334	1.345	
		OAFBRx = 2	–55°C to 125°C		1.985	2.001	2.017	
		OAFBRx = 3	–55°C to 125°C		2.638	2.667	2.696	
		OAFBRx = 4	–55°C to 125°C		3.94	4.00	4.06	
		OAFBRx = 5	–55°C to 125°C		5.22	5.33	5.44	
		OAFBRx = 6	–55°C to 125°C		7.76	7.97	8.18	
		OAFBRx = 7	–55°C to 125°C		15.0	15.8	16.7	
THD	Total harmonic distortion/nonlinearity	All gains		2.2 V		–60		dB
				3 V		–70		
t_{Settle}	Settling time (1)	All power modes	–55°C to 125°C	2.2 V/3 V		7	12	μs

(1) The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

Operational Amplifier (OA) Feedback Network, Inverting Amplifier Mode (OAFCx = 6) – Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
G	Gain	OAFBRx = 1	–55°C to 125°C	2.2 V/3 V	-0.385	–0.335	-0.305	
		OAFBRx = 2	–55°C to 125°C		-1.023	–1.002	-0.979	
		OAFBRx = 3	–55°C to 125°C		-1.712	–1.668	-1.624	
		OAFBRx = 4	–55°C to 125°C		-3.10	–3.00	-2.90	
		OAFBRx = 5	–55°C to 125°C		-4.51	–4.33	-4.15	
		OAFBRx = 6	–55°C to 125°C		-7.37	–6.97	-6.57	
		OAFBRx = 7	–55°C to 125°C		-16.6	–14.8	-13.1	
THD	Total harmonic distortion/nonlinearity	All gains		2.2 V		–60		dB
				3 V		–70		
t_{Settle}	Settling time[2]	All power modes	–55°C to 125°C	2.2 V/3 V		7	12	µs

(1) This includes the 2 OA configuration "inverting amplifier with input buffer". Both OA needs to be set to the same power mode OAPMx.
(2) The settling time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The settling time of the amplifier itself might be faster.

Flash Memory – Electrical Characteristics[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage		–55°C to 125°C		2.2		3.6	V
f_{FTG}	Flash timing generator frequency		–55°C to 125°C		257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		–55°C to 125°C	2.2 V/3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		–55°C to 125°C	2.2 V/3.6 V		1	10.5	mA
t_{CPT}	Cumulative program time[2]		–55°C to 125°C	2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		–55°C to 125°C	2.2 V/3.6 V	20			ms
	Program/Erase endurance		–55°C to 125°C		10^4	10^5		cycles
$t_{Retention}$	Data retention duration[3]	T_J = 25°C			100			years
t_{Word}	Word or byte program time	[4]				30		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word	[4]				25		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word	[4]				18		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time	[4]				6		t_{FTG}
$t_{Mass Erase}$	Mass erase time	[4]				10593		t_{FTG}
$t_{Seg Erase}$	Segment erase time	[4]				4819		t_{FTG}

(1) Additional Flash retention documentation located in application report (SLAA392).
(2) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(3) To test the flash data retention at various temperatures we make use of accelerated tests on the flash with **500-Hours Baking Time at 250°C**. These tests are wholly based on Arrhenius law and equation.
(4) These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage [1]	CPU halted	–55°C to 125°C	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG and Spy-Bi-Wire Interface – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency		–55°C to 125°C	2.2 V/3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse length		–55°C to 125°C	2.2 V/3 V	0.025		15	µs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge[1])		–55°C to 125°C	2.2 V/3 V			1	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time		–55°C to 125°C	2.2 V/3 V	15		100	µs
f_{TCK}	TCK input frequency[2]		–55°C to 125°C	2.2 V	0		5	MHz
				3 V	0		10	MHz
$R_{Internal}$	Internal pulldown resistance on TEST		–55°C to 125°C	2.2 V/3 V	25	60	90	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse[1] – Electrical Characteristics

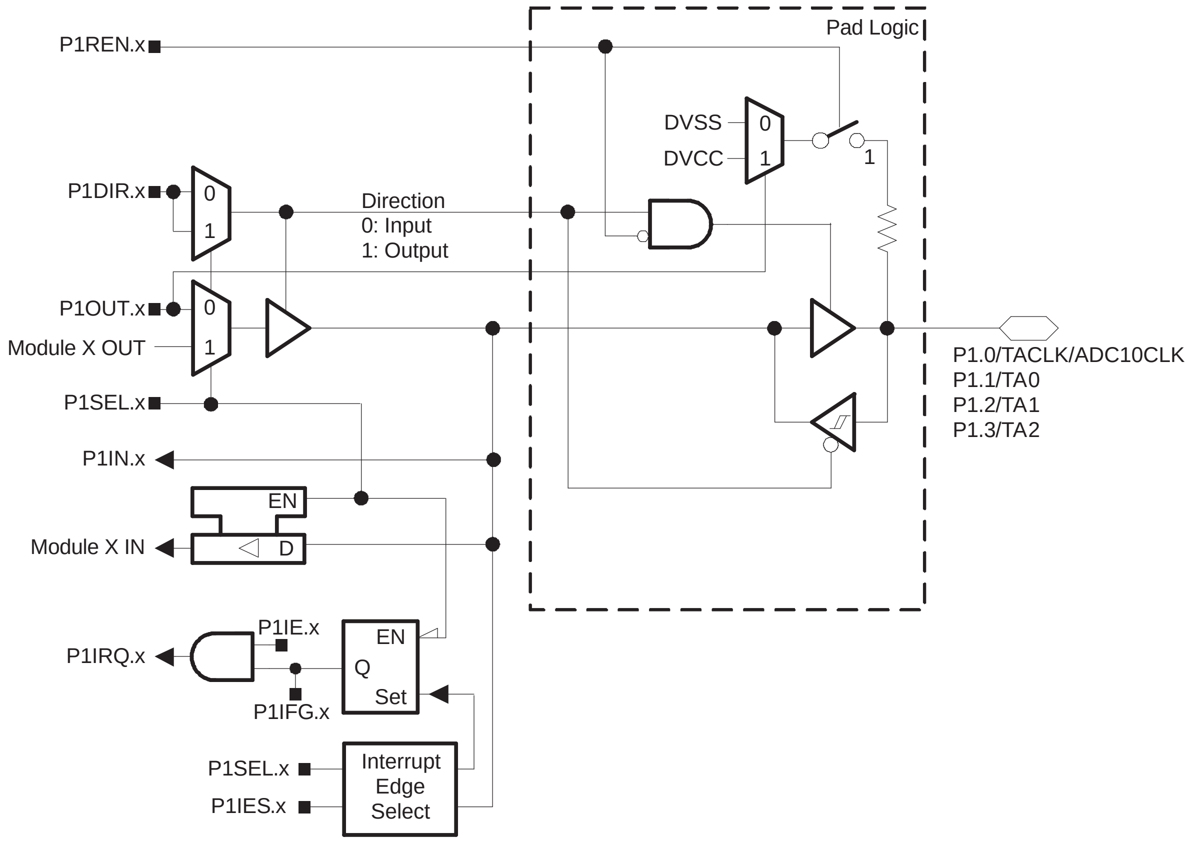
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition		T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		–55°C to 125°C	6	7	V
I_{FB}	Supply current into TEST during fuse blow		–55°C to 125°C		100	mA
t_{FB}	Time to blow fuse		–55°C to 125°C		1	ms

(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

APPLICATION INFORMATION

Port P1 Pin Schematic: P1.0 to P1.3, Input/Output With Schmitt Trigger

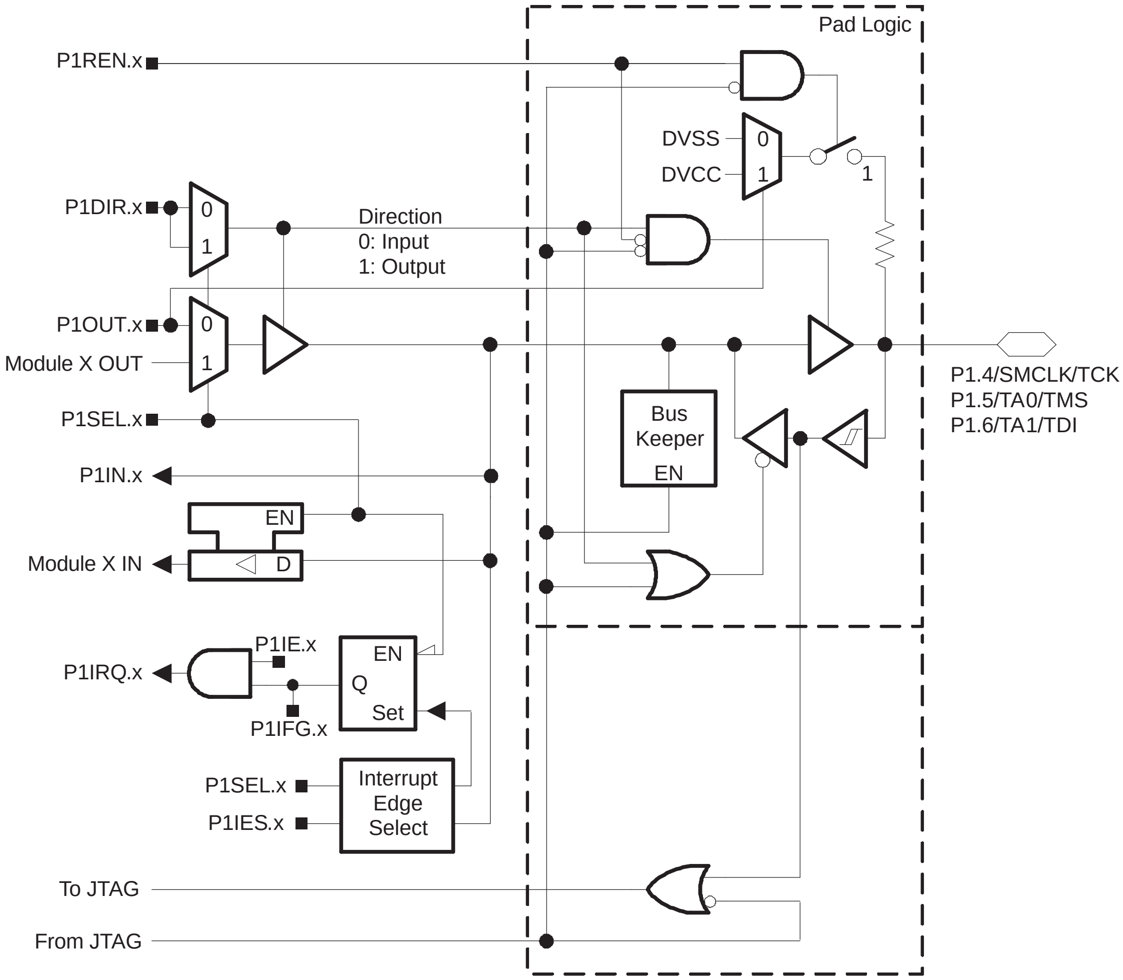


Port P1 (P1.0 to P1.3) Pin Functions

PIN NAME (P1.X)	X	FUNCTION(1)	CONTROL BITS/SIGNALS(2)	
			P1DIR.x	P1SEL.x
P1.0/TACLK/ADC10CLK	0	P1.0(3)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		ADC10CLK	1	1
P1.1/TA0	1	P1.1 (4) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2(4) (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.3/TA2	3	P1.3(4) I/O	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) Default after reset (PUC/POR)

Port P1 Pin Schematic: P1.4 to P1.6, Input/Output With Schmitt Trigger and In-System Access Features

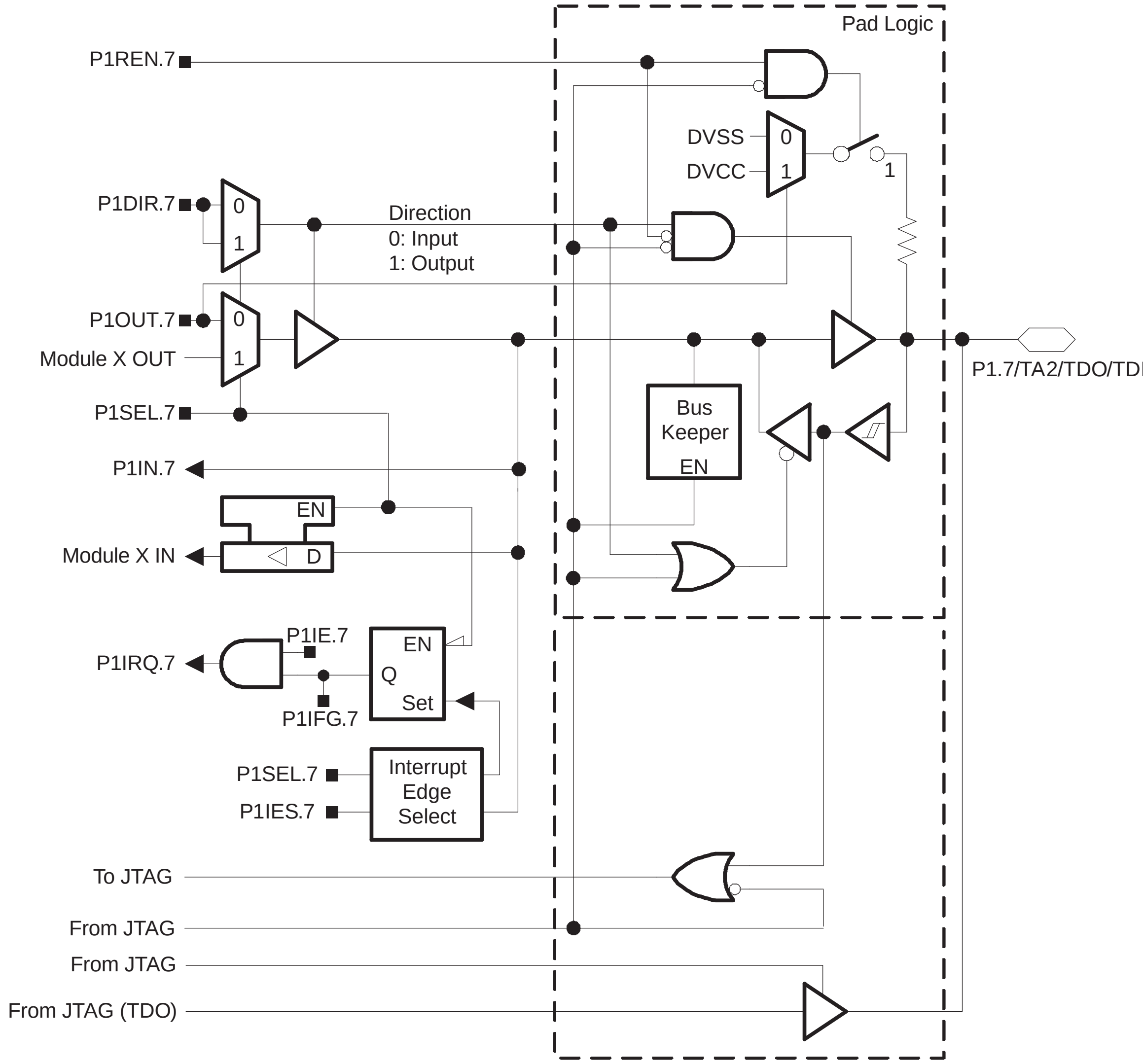


Port P1 (P1.4 to P1.6) Pin Functions

PIN NAME (P1.X)	X	FUNCTION(1)	CONTROL BITS/SIGNALS(2)		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.4/SMCLK/TCK	4	P1.4(3) (I/O)	I: 0; O: 1	0	0
		SMCLK	1	1	0
		TCK	X	X	1
P1.5/TA0/TMS	5	P1.5(3) (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA0	1	1	0
		TMS	X	X	1
P1.6/TA1/TDI/TCLK	6	P1.6(3) (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA1	1	1	0
		TDI/TCLK(4)	X	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) Function controlled by JTAG

Port P1 Pin Schematic: P1.7, Input/Output With Schmitt Trigger and In-System Access Features

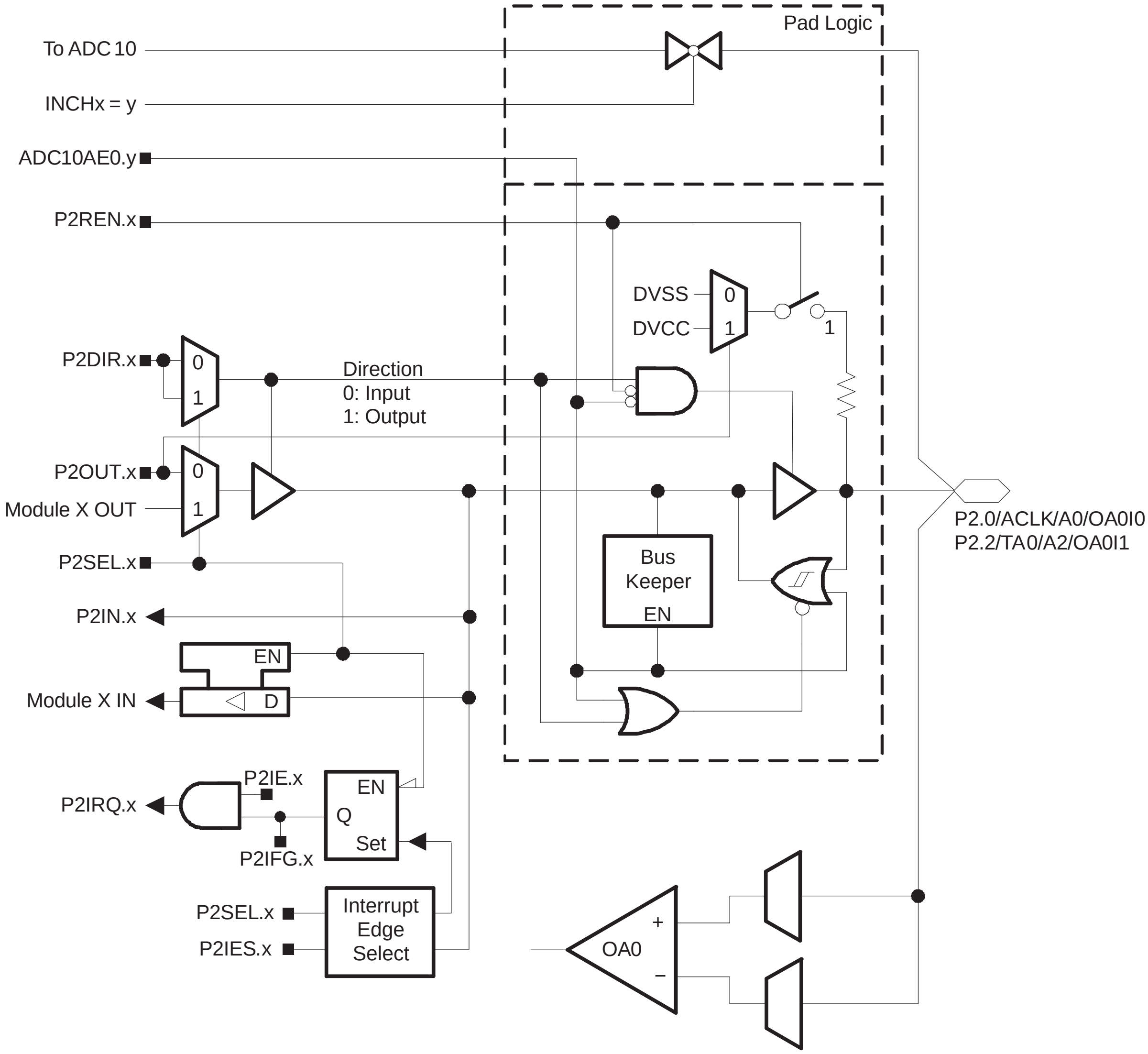


Port P1 (P1.7) Pin Functions

PIN NAME (P1.X)	X	FUNCTION[(1)]	CONTROL BITS/SIGNALS[(2)]		
			P1DIR.x	P1SEL.x	4-Wire JTAG
P1.7/TA2/TDO/TDI	7	P1.7[(3)] (I/O)	I: 0; O: 1	0	0
		Timer_A3.TA2	1	1	0
		TDO/TDI[(4)]	X	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) Function controlled by JTAG

Port P2 Pin Schematic: P2.0, P2.2, Input/Output With Schmitt Trigger

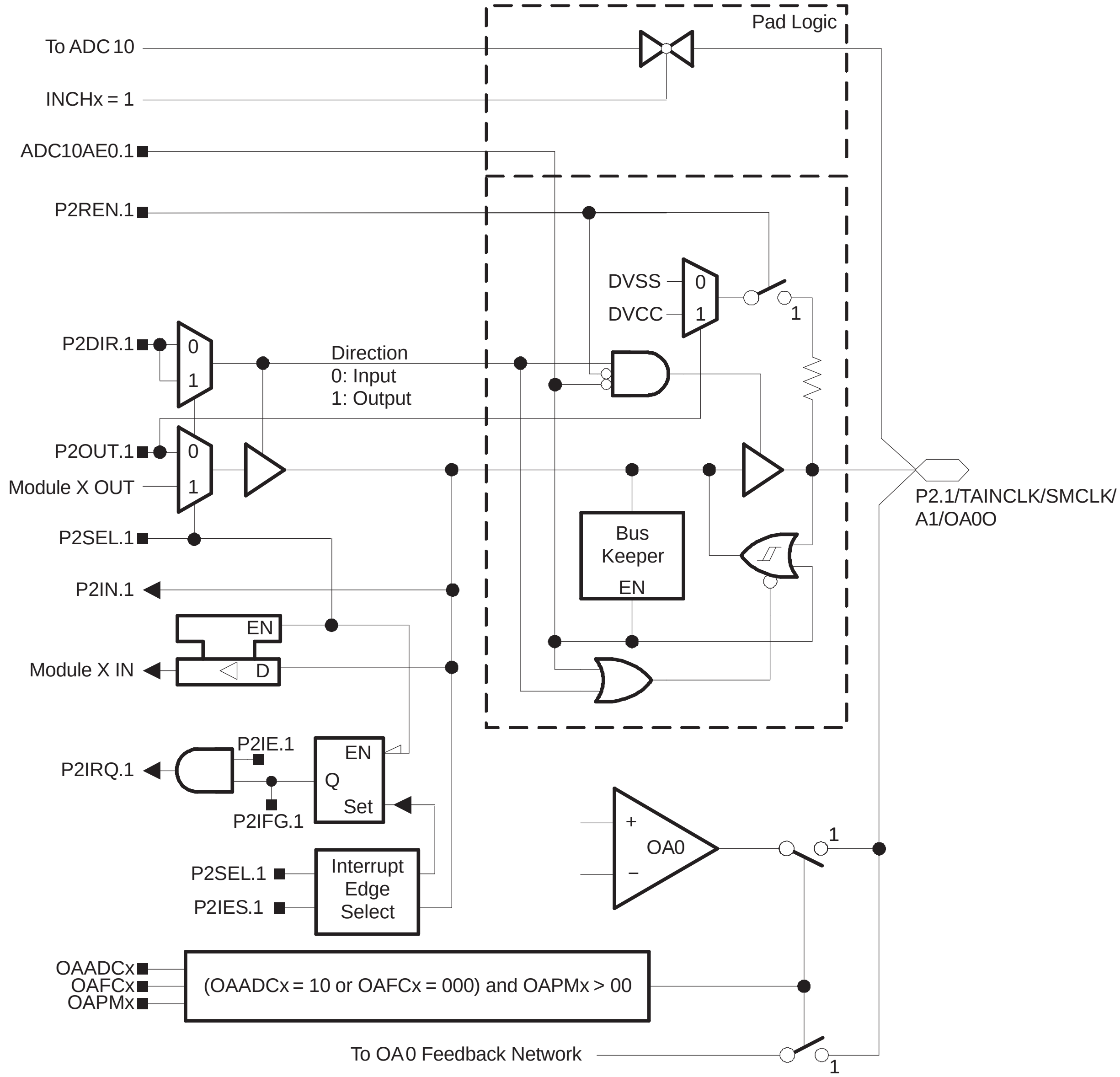


Port P2 (P2.0, P2.2) Pin Functions

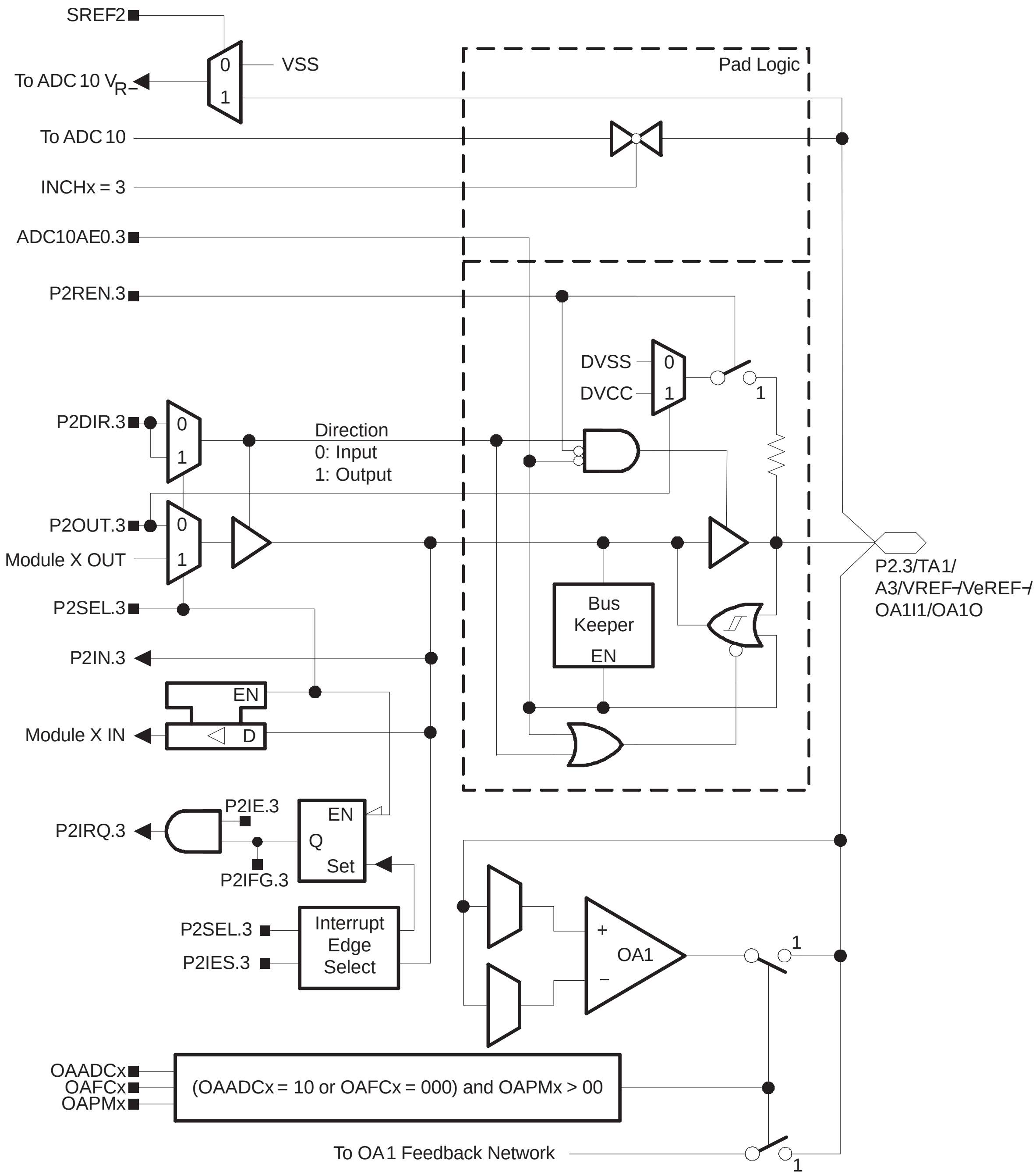
Pin Name (P2.X)	X	Y	FUNCTION[1]	CONTROL BITS/SIGNALS[2]		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.0/ACLK/A0/OA0I0	0	0	P2.0[3] (I/O)	I: 0; O: 1	0	0
			ACLK	1	1	0
			A0/OA0I0[4]	X	X	1
P2.2/TA0/A2/OA0I1	2	2	P2.2[3] (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI0B	0	1	0
			Timer_A3.TA0	1	1	0
			A2/OA0I1[4]	X	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 Pin Schematic: P2.1, Input/Output With Schmitt Trigger



Port P2 Pin Schematic: P2.3, Input/Output With Schmitt Trigger



Port P2 (P2.1) Pin Functions

PIN NAME (P2.X)	X	Y	FUNCTION[1]	CONTROL BITS/SIGNALS[2]		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.1/TAINCLK/SMCLK/A1/OA0O	1	1	P2.1[3] (I/O)	I: 0; O: 1	0	0
			Timer_A3.INCLK	0	1	0
			SMCLK	1	1	0
			A1/OA0O[4]	X	X	1

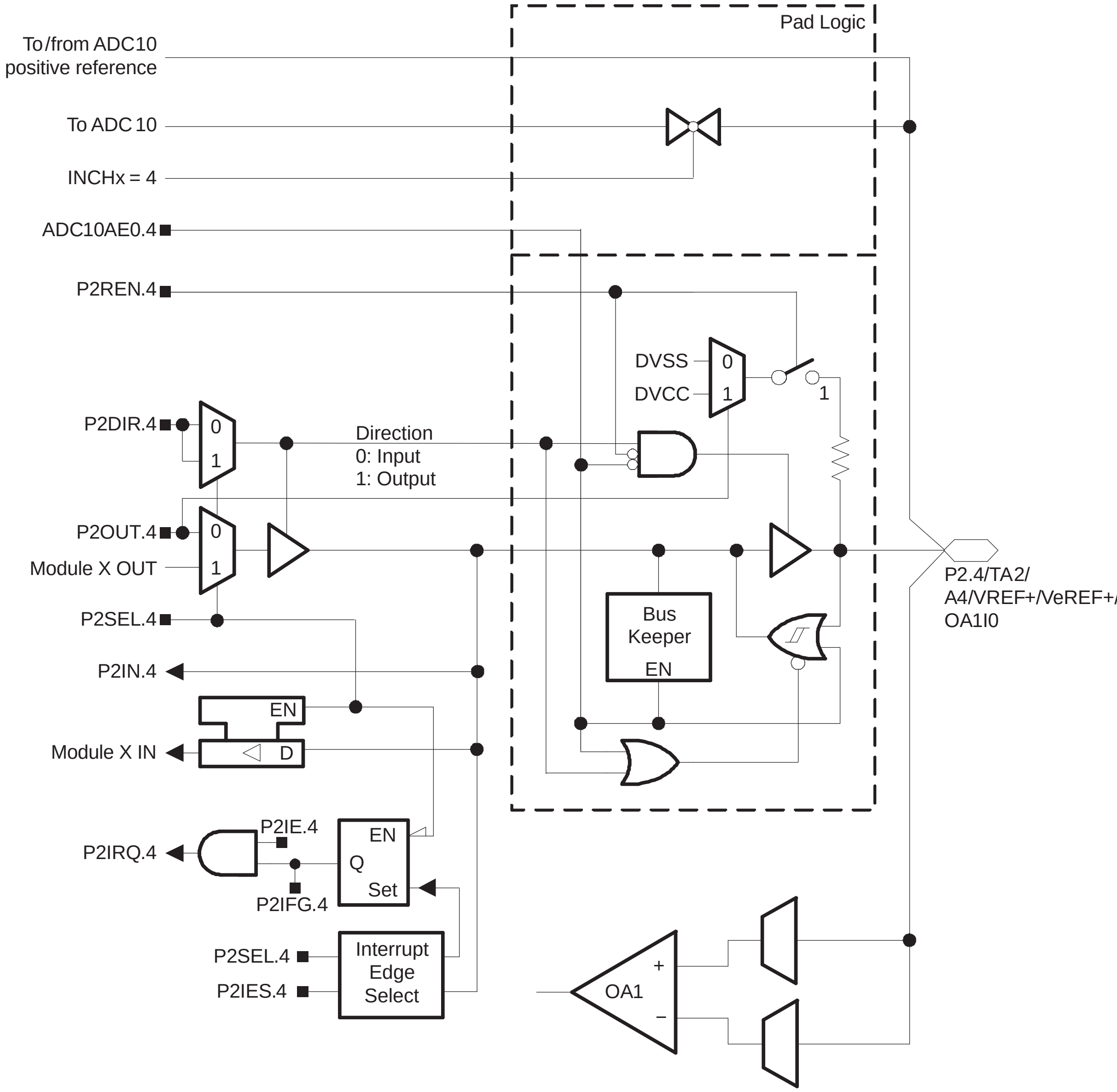
(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 (P2.3) Pin Functions

PIN NAME (P2.X)	X	Y	FUNCTION[1]	CONTROL BITS/SIGNALS[2]		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.3/TA1/A3/V_{REF-}/V_{eREF-}/OA1I1/OA1O	3	3	P2.3[3] (I/O)	I: 0; O: 1	0	0
			Timer_A3.CCI1B	0	1	0
			Timer_A3.TA1	1	1	0
			A3/V_{REF-}/V_{eREF-}/OA1I1/OA1O[4]	X	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 Pin Schematic: P2.4, Input/Output With Schmitt Trigger

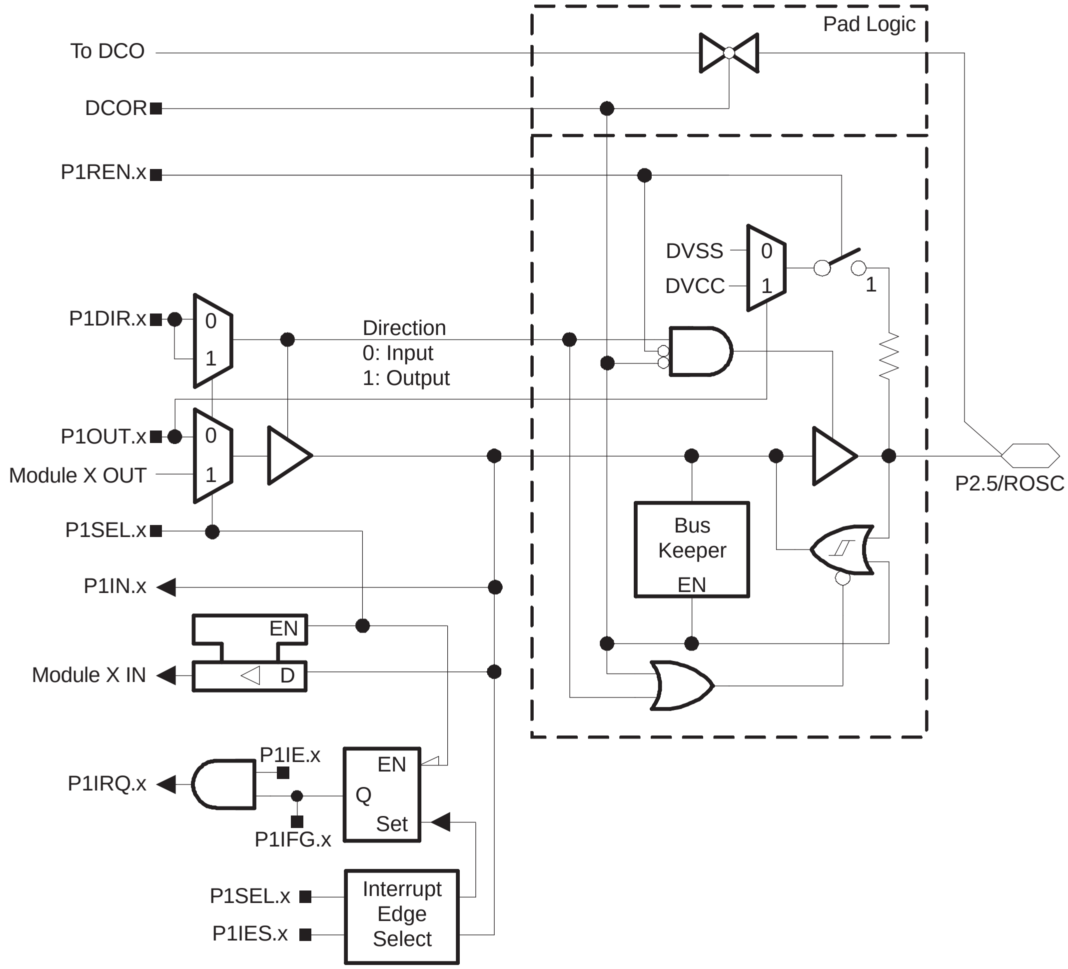


Port P2 (P2.4) Pin Functions

PIN NAME (P2.X)	X	Y	FUNCTION(1)	CONTROL BITS/SIGNALS(2)		
				P2DIR.x	P2SEL.x	ADC10AE0.y
P2.4/TA2/A4/V_{REF+}/V_{eREF+}/OA1I0	4	4	P2.4(3) (I/O)	I: 0; O: 1	0	0
			Timer_A3.TA2	1	1	0
			A4/V_{REF+}/V_{eREF+}/OA1I0(4)	X	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 Pin Schematic: P2.5, Input/Output With Schmitt Trigger and External R_{OSC} for DCO

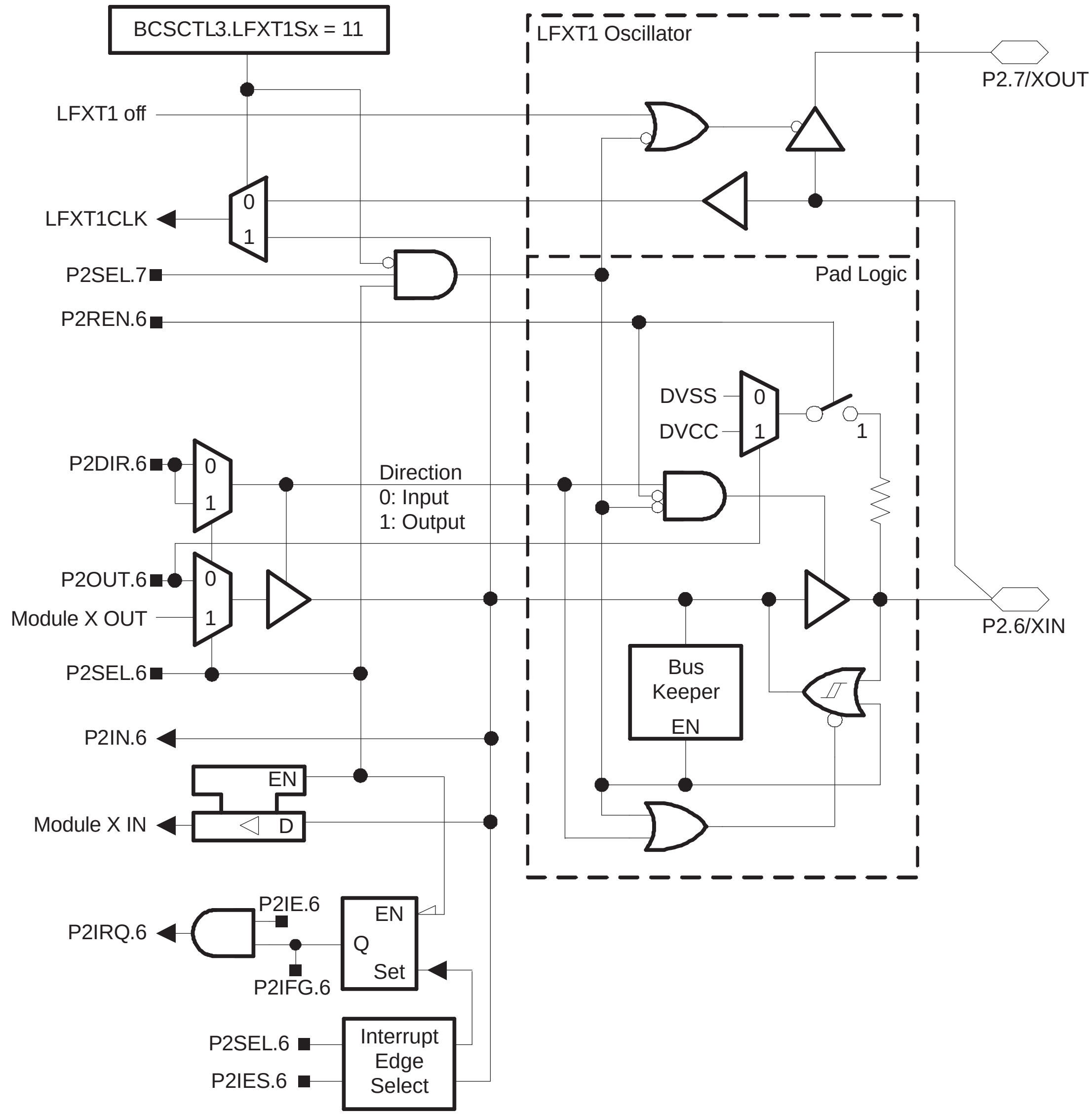


Port P2 (P2.5) Pin Functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS/SIGNALS[(1)]		
			P2DIR.x	P2SEL.x	DCOR
$P2.5/R_{OSC}$	5	P2.5[(2)] (I/O)	0/1	0	0
		N/A[(3)]	0	1	0
		DV_{SS}	1	1	0
		R_{OSC}	X	X	1

(1) X: Don't care
(2) Default after reset (PUC/POR)
(3) N/A: Not available or not applicable

Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger and Crystal Oscillator Input

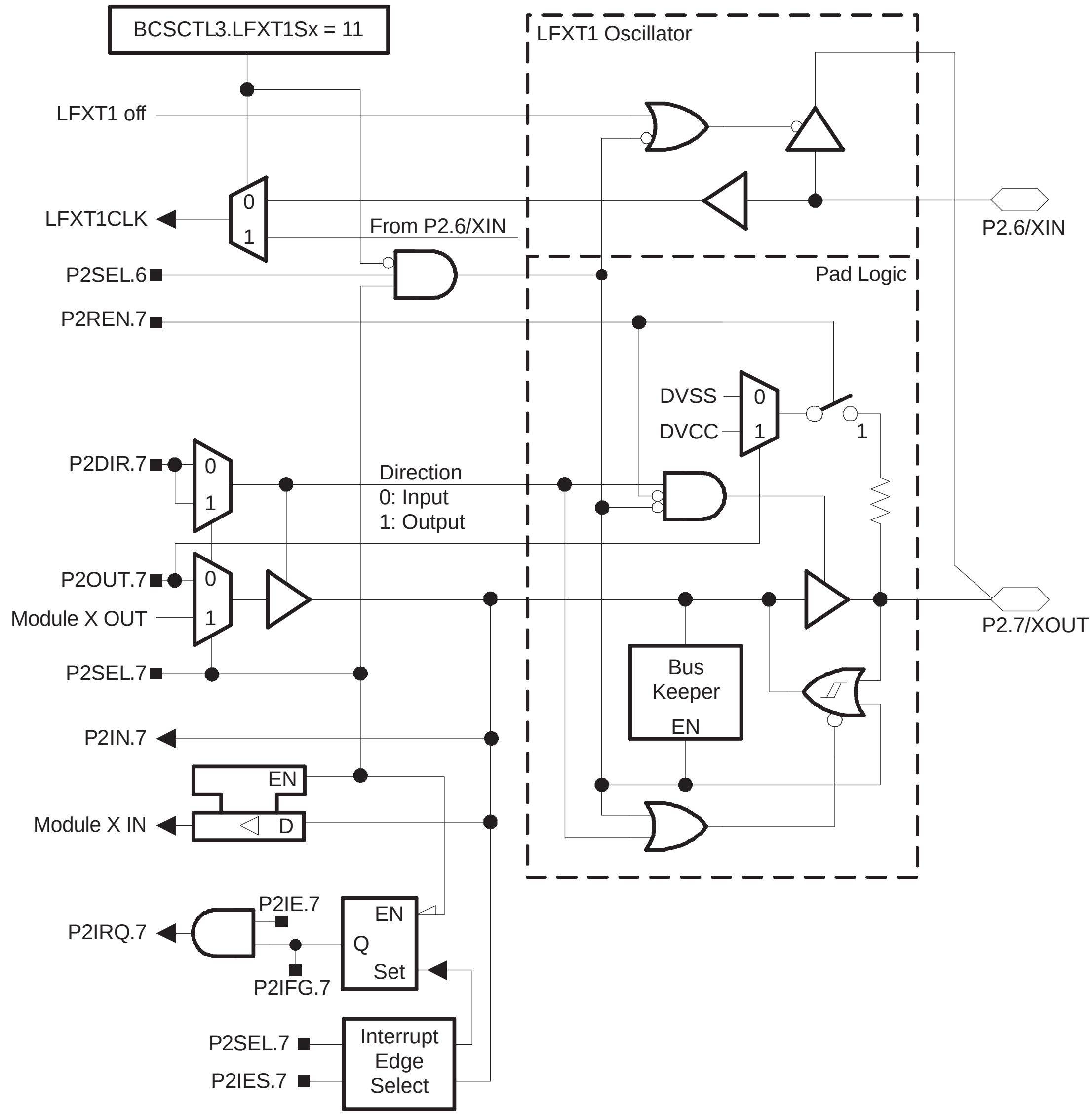


Port P2 (P2.6) Pin Functions

PIN NAME (P2.X)	X	FUNCTION (1)	CONTROL BITS/SIGNALS (2)	
			P2DIR.x	P2SEL.x
P2.6/XIN	6	P2.6 (I/O)	I: 0; O: 1	0
		XIN (3)	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)

Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger and Crystal Oscillator Output

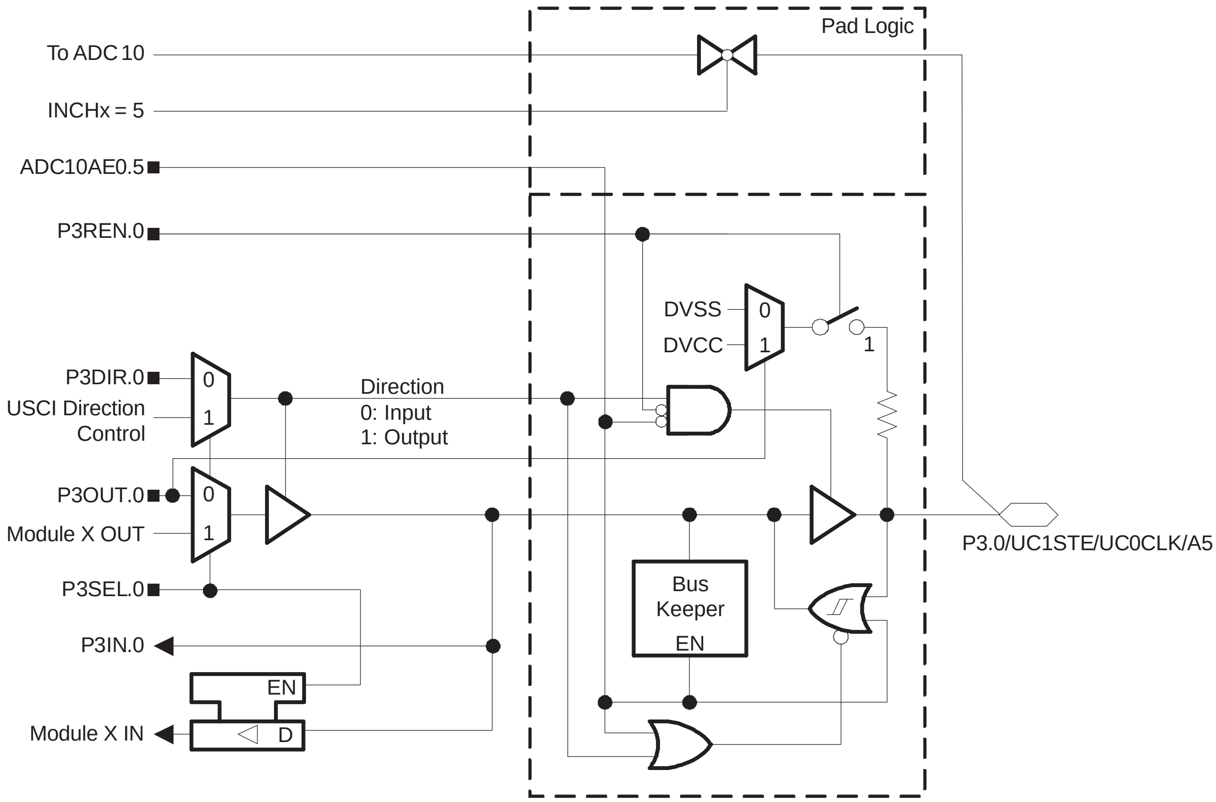


Port P2 (P2.7) Pin Functions

PIN NAME (P2.X)	X	FUNCTION(1)	CONTROL BITS/SIGNALS(2)	
			P2DIR.x	P2SEL.x
XOUT/P2.7	6	P2.7 (I/O)	I: 0; O: 1	0
		XOUT(3) (4)	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) If the pin XOUT/P2.7 is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

Port P3 Pin Schematic: P3.0, Input/Output With Schmitt Trigger

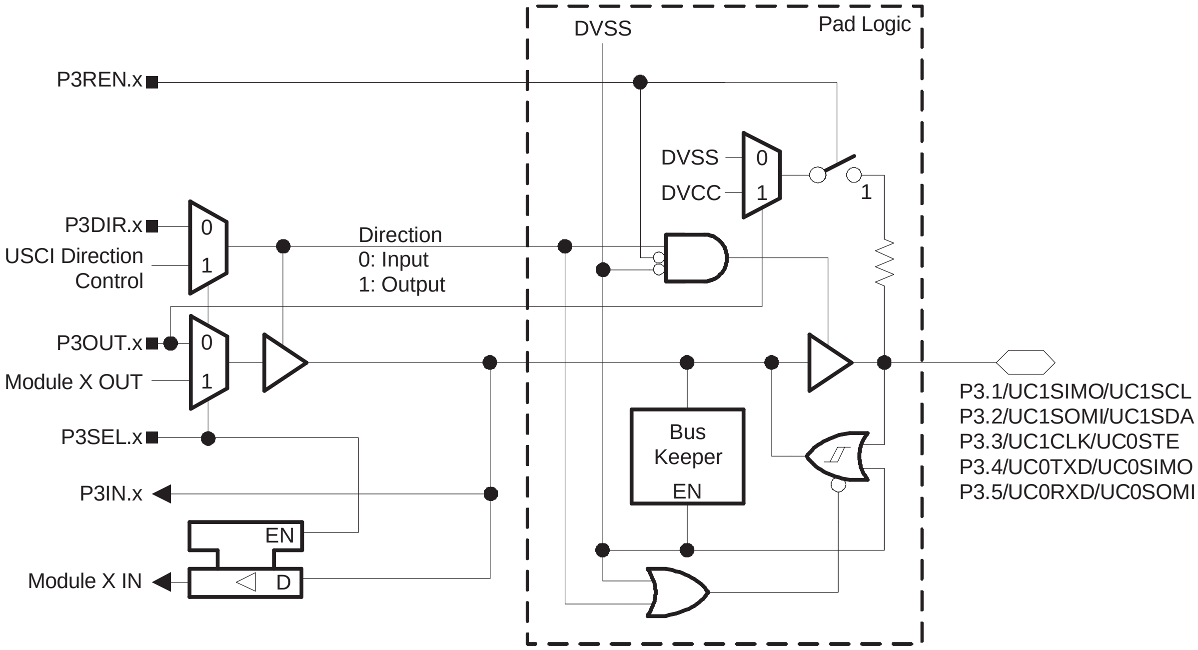


Port P3 (P3.0) Pin Functions

PIN NAME (P1.X)	X	Y	FUNCTION(1)	CONTROL BITS/SIGNALS(2)		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.0/UC1STE/UC0CLK/A5	0	5	P3.0(3) (I/O)	I: 0; O: 1	0	0
			UC1STE/UC0CLK(4) (5)	X	1	0
			A5(6)	X	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) The pin direction is controlled by the USCI module.
(5) UC0CLK function takes precedence over UC1STE function. If the pin is required as UC0CLK input or output USCI1 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(6) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P3 Pin Schematic: P3.1 to P3.5, Input/Output With Schmitt Trigger

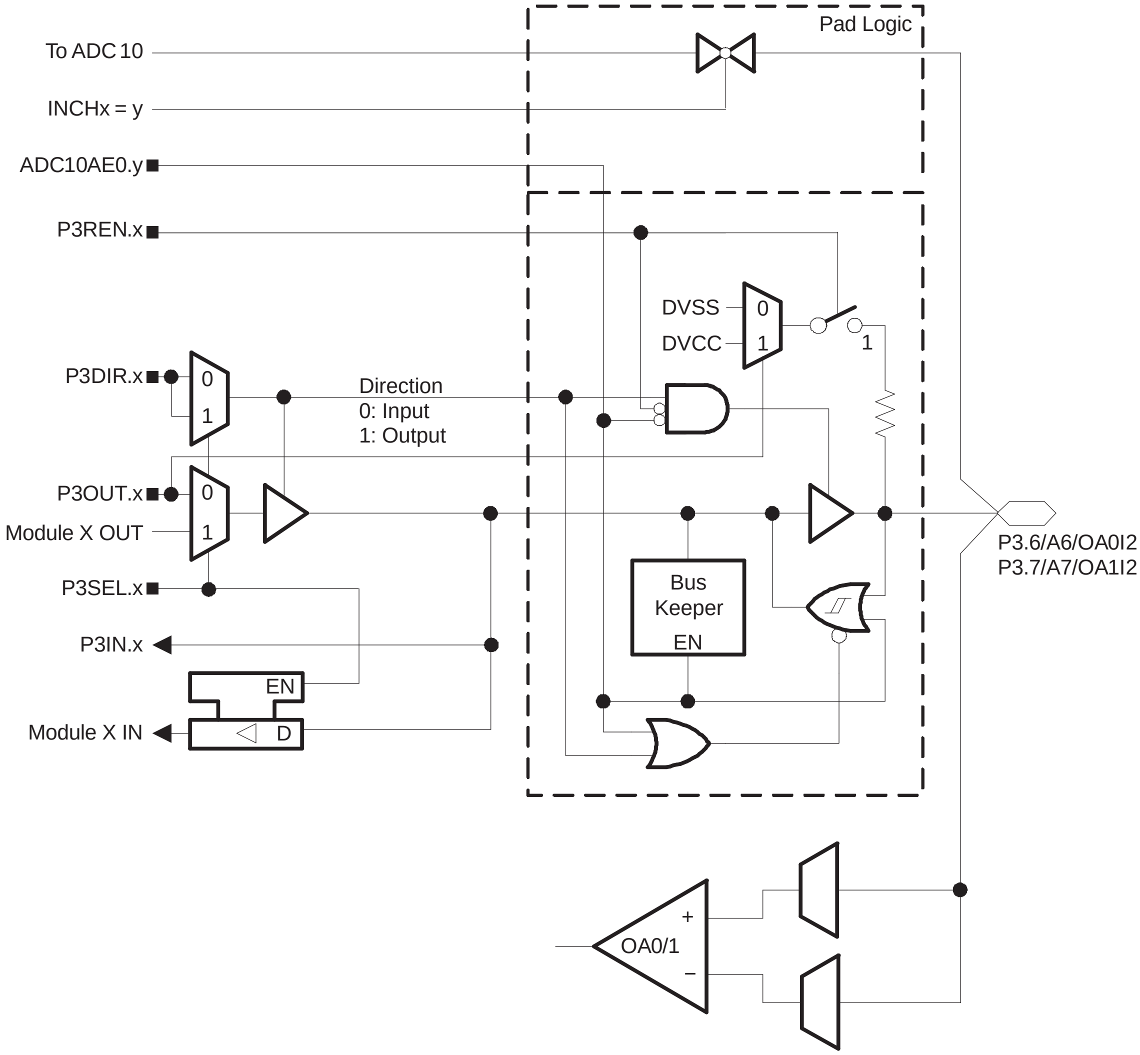


Port P3 (P3.1 to P3.5) Pin Functions

PIN NAME (P3.X)	X	FUNCTION[1]	CONTROL BITS/SIGNALS[2]	
			P3DIR.x	P3SEL.x
P3.1/UC1SIMO/UC1SDA	1	P3.1[3] (I/O)	I: 0; O: 1	0
		UC1SIMO/UC1SDA[4]	X	1
P3.2/UC1SOMI/UC1SCL	1	P3.2[5] (I/O)	I: 0; O: 1	0
		UC1SOMI/UC1SCL[6]	X	1
P3.3/UC1CLK/UC0STE	1	P3.3[5] (I/O)	I: 0; O: 1	0
		UC1CLK/UC0STE[6] [7]	X	1
P3.4/UC0TXD/UC0SIMO	1	P3.4[5] (I/O)	I: 0; O: 1	0
		UC0TXD/UC0SIMO[6]	X	1
P3.5/UC0RXD/UC0SOMI	1	P3.5[5] (I/O)	I: 0; O: 1	0
		UC0RXD/UC0SOMI[6]	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) The pin direction is controlled by the USCI module.
(5) Default after reset (PUC/POR)
(6) The pin direction is controlled by the USCI module.
(7) UC1CLK function takes precedence over UC0STE function. If the pin is required as UC1CLK input or output, USCI0 is orced to 3-wire SPI mode even if 4-wire SPI mode is selected.

Port P3 Pin Schematic: P3.6 to P3.7, Input/Output With Schmitt Trigger

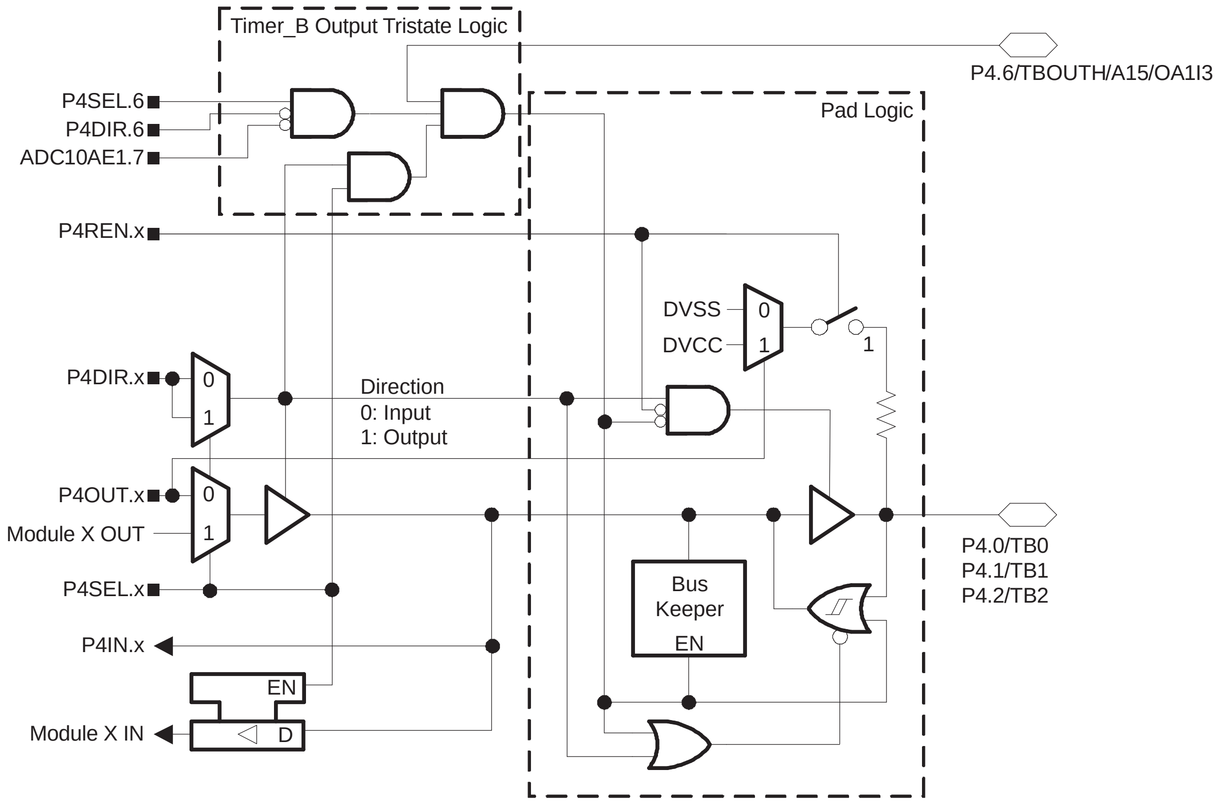


Port P3 (P3.6, P3.7) Pin Functions

PIN NAME (P3.X)	X	Y	FUNCTION (1) (2)	CONTROL BITS/SIGNALS (3)		
				P3DIR.x	P3SEL.x	ADC10AE0.y
P3.6/A6/OA0I2	6	6	P3.6 (4) (I/O)	I: 0; O: 1	0	0
			A6/OA0I2 (5)	X	X	1
P3.7/A7/OA1I2	7	7	P3.7 (4) (I/O)	I: 0; O: 1	0	0
			A7/OA1I2 (5)	X	X	1

(1) N/A: Not available or not applicable
(2) UC0CLK function takes precedence over UC0STE function. If the pin is required as UC1CLK input or output, USCI0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(3) X: Don't care
(4) Default after reset (PUC/POR)
(5) Setting the ADC10AE0.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 Pin Schematic: P4.0 to P4.2, Input/Output With Schmitt Trigger

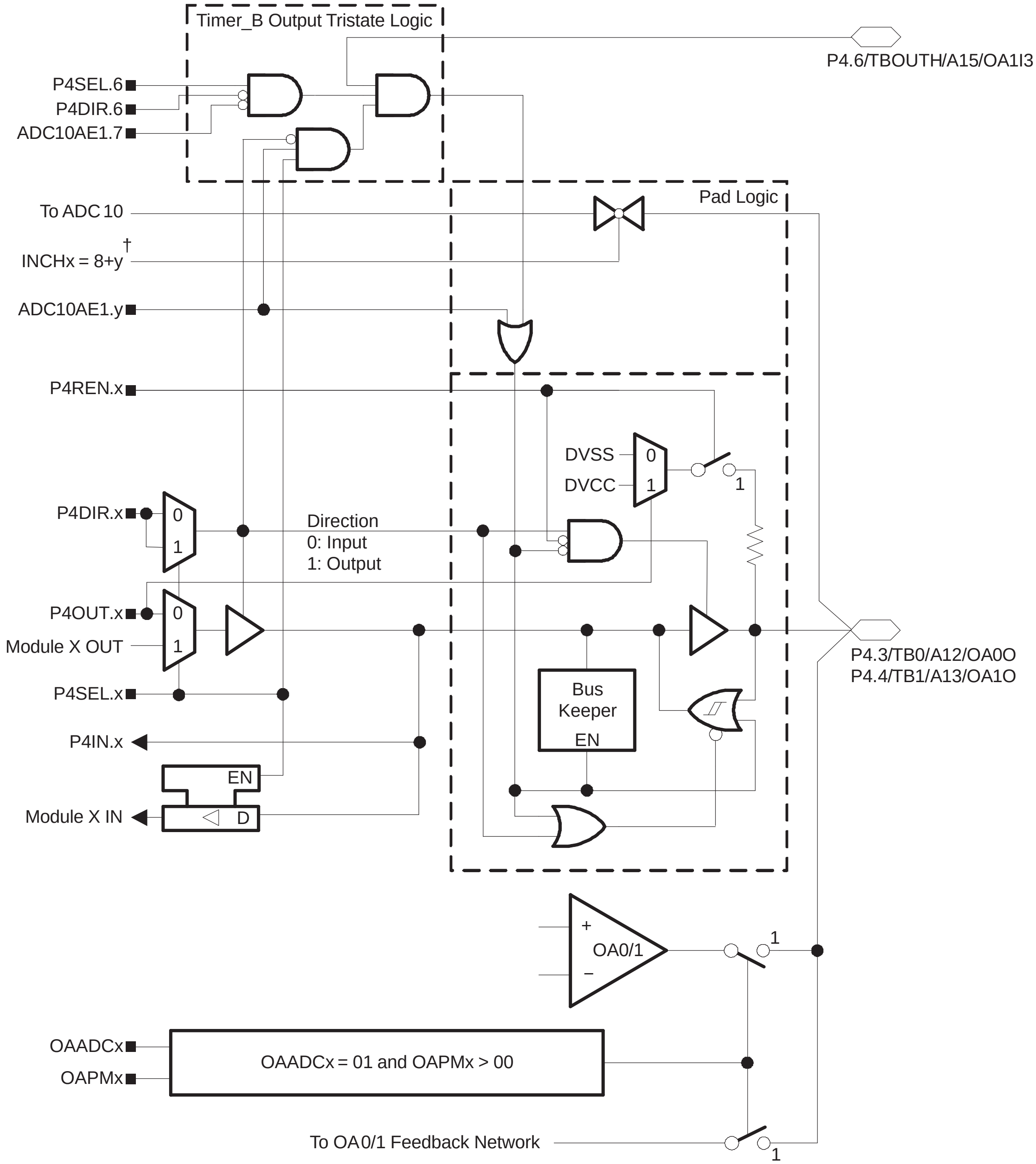


Port P4 (P4.0 to P4.2) Pin Functions

PIN NAME (P4.X)	X	FUNCTION (1)	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0 (2) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI0A	0	1
		Timer_B3.TB0	1	1
P4.1/TB1	1	P4.1 (2) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI1A	0	1
		Timer_B3.TB1	1	1
P4.2/TB2	2	P4.2 (2) (I/O)	I: 0; O: 1	0
		Timer_B3.CCI2A	0	1
		Timer_B3.TB2	1	1

(1) N/A: Not available or not applicable.
(2) Default after reset (PUC/POR)

Port P4 Pin Schematic: P4.3 to P4.4, Input/Output With Schmitt Trigger



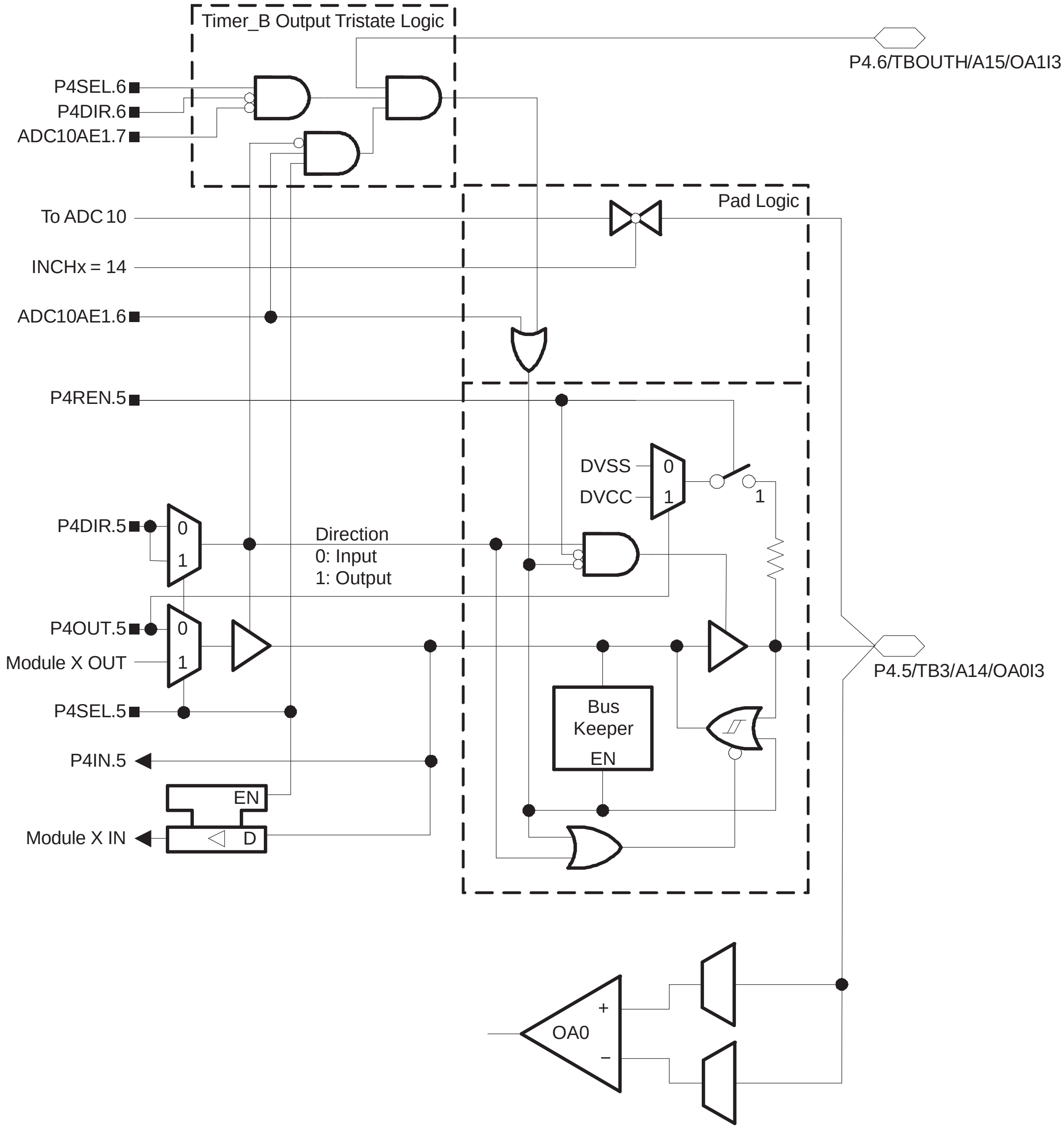
† If OAADCx = 11 and not OAFCx = 000, the ADC input A12 or A13 is internally connected to the OA0 or OA1 output, respectively, and the connections from the ADC and the operational amplifiers to the pad are disabled.

Port P4 (P4.3 to P4.4) Pin Functions

PIN NAME (P4.X)	X	Y	FUNCTION (1)	CONTROL BITS/SIGNALS (2)		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.3/TB0/A12/OA0O	3	4	P4.3 (3) (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI0B	0	1	0
			Timer_B3.TB0	1	1	0
			A12/OA0O (4)	X	X	1
P4.4/TB1/A13/OA1O	4	5	P4.4 (3) (I/O)	I: 0; O: 1	0	0
			Timer_B3.CCI1B	0	1	0
			Timer_B3.TB1	1	1	0
			A13/OA1O (4)	X	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 Pin Schematic: P4.5, Input/Output With Schmitt Trigger

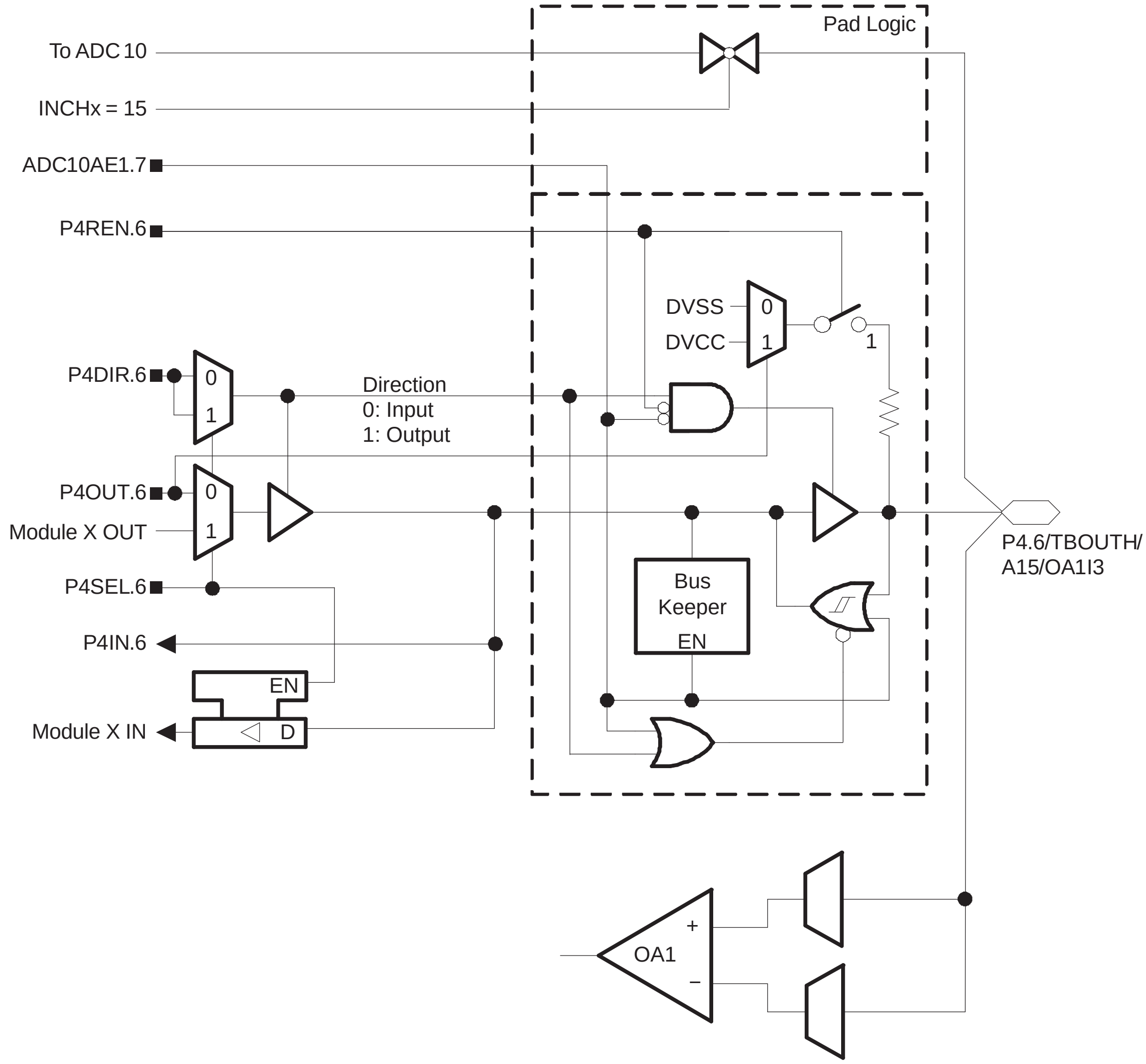


Port P4 (P4.5) Pin Functions

PIN NAME (P4.X)	X	Y	FUNCTION(1)	CONTROL BITS/SIGNALS(2)		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.5/TB3/A14/OA0I3	5	6	P4.5(3) (I/O)	I: 0; O: 1	0	0
			Timer_B3.TB2	1	1	0
			A14/OA0I3(4)	X	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 Pin Schematic: P4.6, Input/Output With Schmitt Trigger

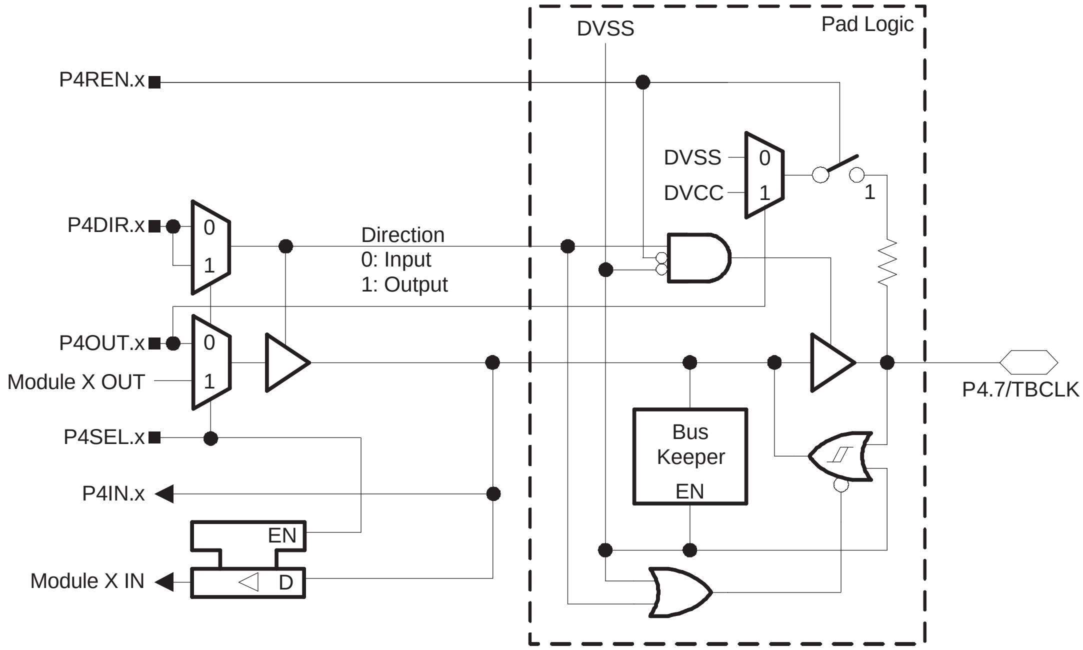


Port P4 (P4.6) Pin Functions

PIN NAME (P4.X)	X	Y	FUNCTION (1)	CONTROL BITS/SIGNALS (2)		
				P4DIR.x	P4SEL.x	ADC10AE1.y
P4.6/TBOUTH/A15/OA1I3	6	7	P4.6 (3) (I/O)	I: 0; O: 1	0	0
			TBOUTH	0	1	0
			DV_{SS}	1	1	0
			A15/OA1I3 (4)	X	X	1

(1) N/A: Not available or not applicable
(2) X: Don't care
(3) Default after reset (PUC/POR)
(4) Setting the ADC10AE1.y bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P4 Pin Schematic: P4.7, Input/Output With Schmitt Trigger



Port P4 (Pr.7) Pin Functions

PIN NAME (P4.X)	X	FUNCTION[1]	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.7/TBCLK	7	P4.7[2] (I/O)	I: 0; O: 1	0
		Timer_B3.TBCLK	0	1
		DV_{SS}	1	1

(1) N/A: Not available or not applicable
(2) Default after reset (PUC/POR)

JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 28). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

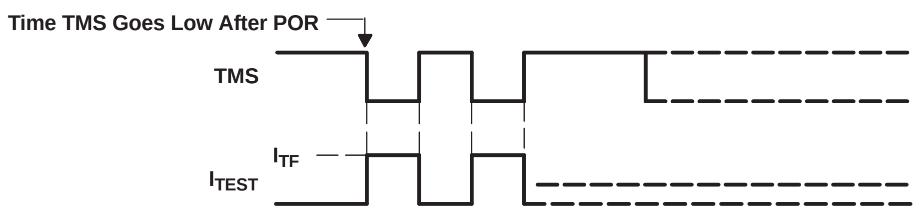


Figure 28. Fuse Check Mode Current, MSP430F22xx

NOTE

The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the Bootstrap Loader section for more information.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F2274MDATEP	Active	Production	TSSOP (DA) | 38	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	M430F2274MEP
MSP430F2274MRHATEP	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	M4F2274 MRHATEP
V62/08631-01XE	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	M4F2274 MRHATEP
V62/08631-01YE	Active	Production	TSSOP (DA) | 38	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	M430F2274MEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSP430F2274-EP :

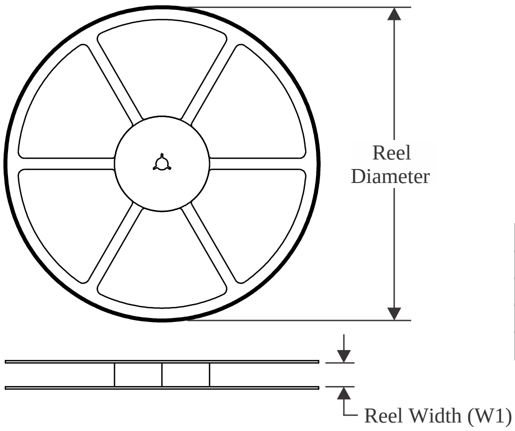
- Catalog : MSP430F2274

NOTE: Qualified Version Definitions:

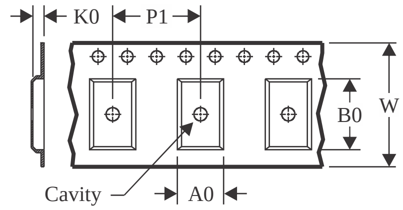
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

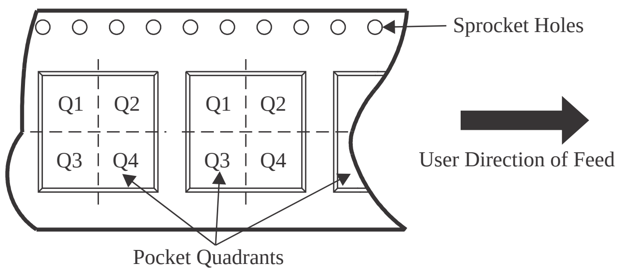


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

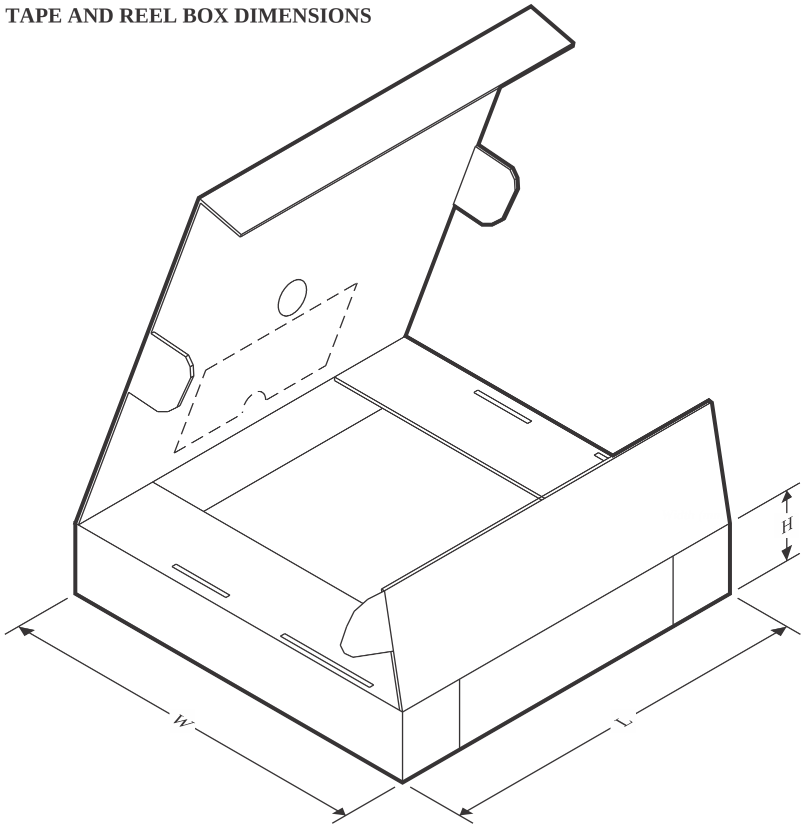
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2274MRHATEP	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

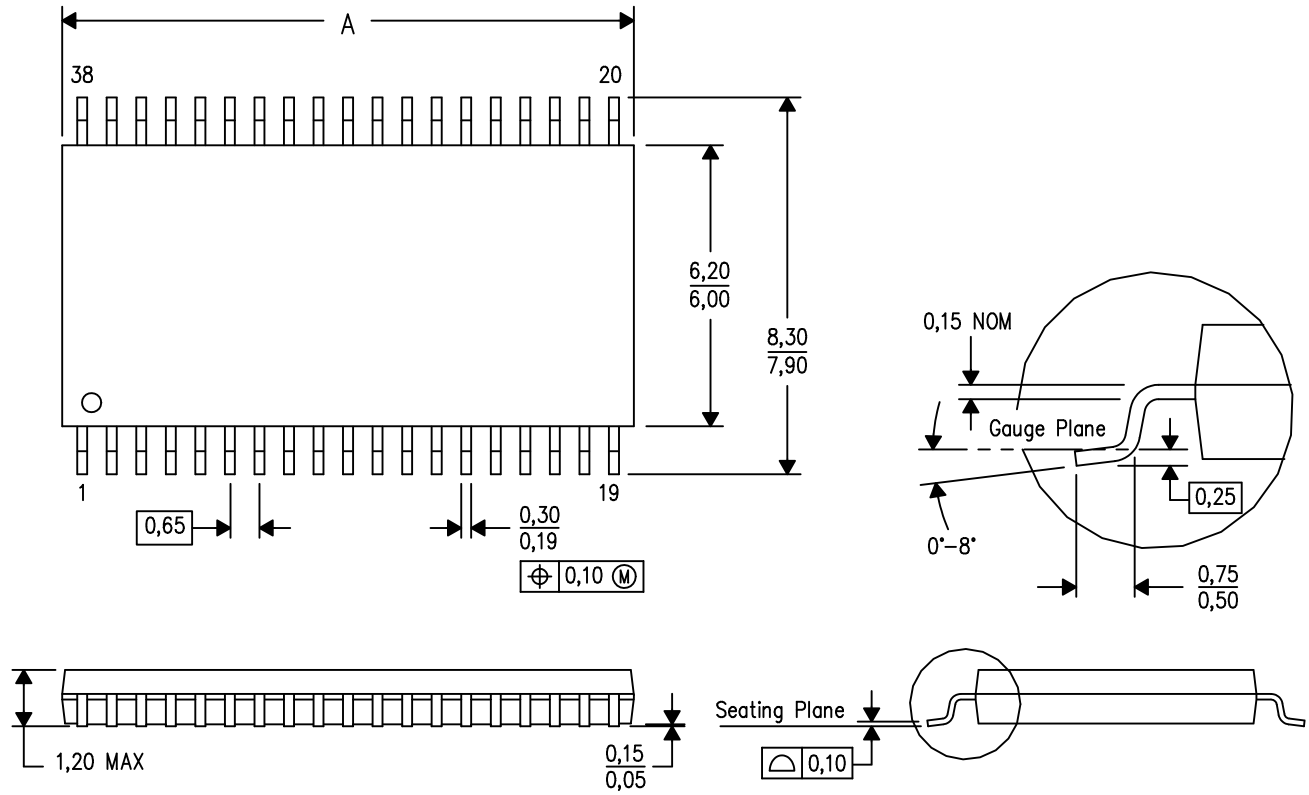


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2274MRHATEP	VQFN	RHA	40	250	213.0	191.0	35.0

DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN

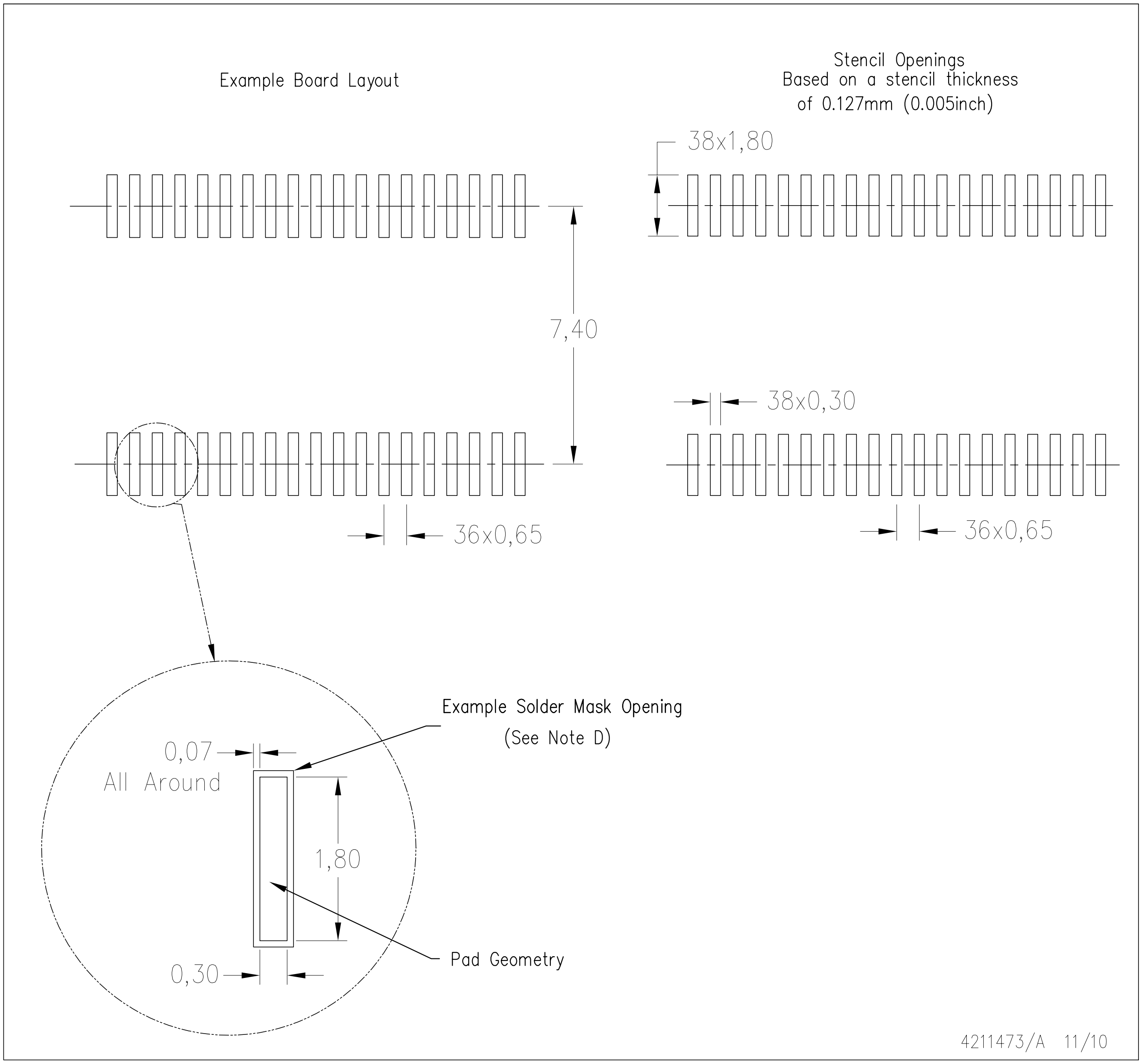


DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
(D) MO–153 Variation	DB–1	DC	DD–1

4040066/F 01/2009

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
(D) Falls within JEDEC MO–153, except 30 pin body length.

DA (R–PDSO–G38) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- D. Contact the board fabrication site for recommended soldermask tolerances.

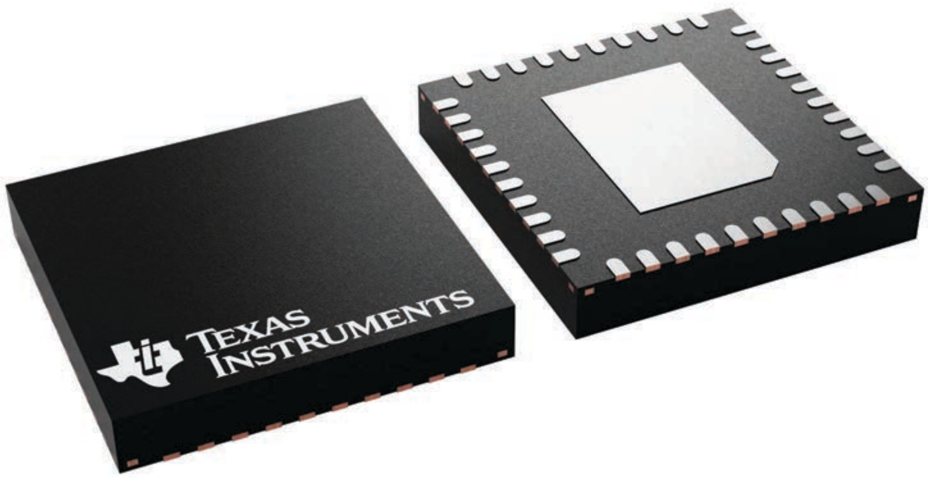
RHA 40

VQFN - 1 mm max height

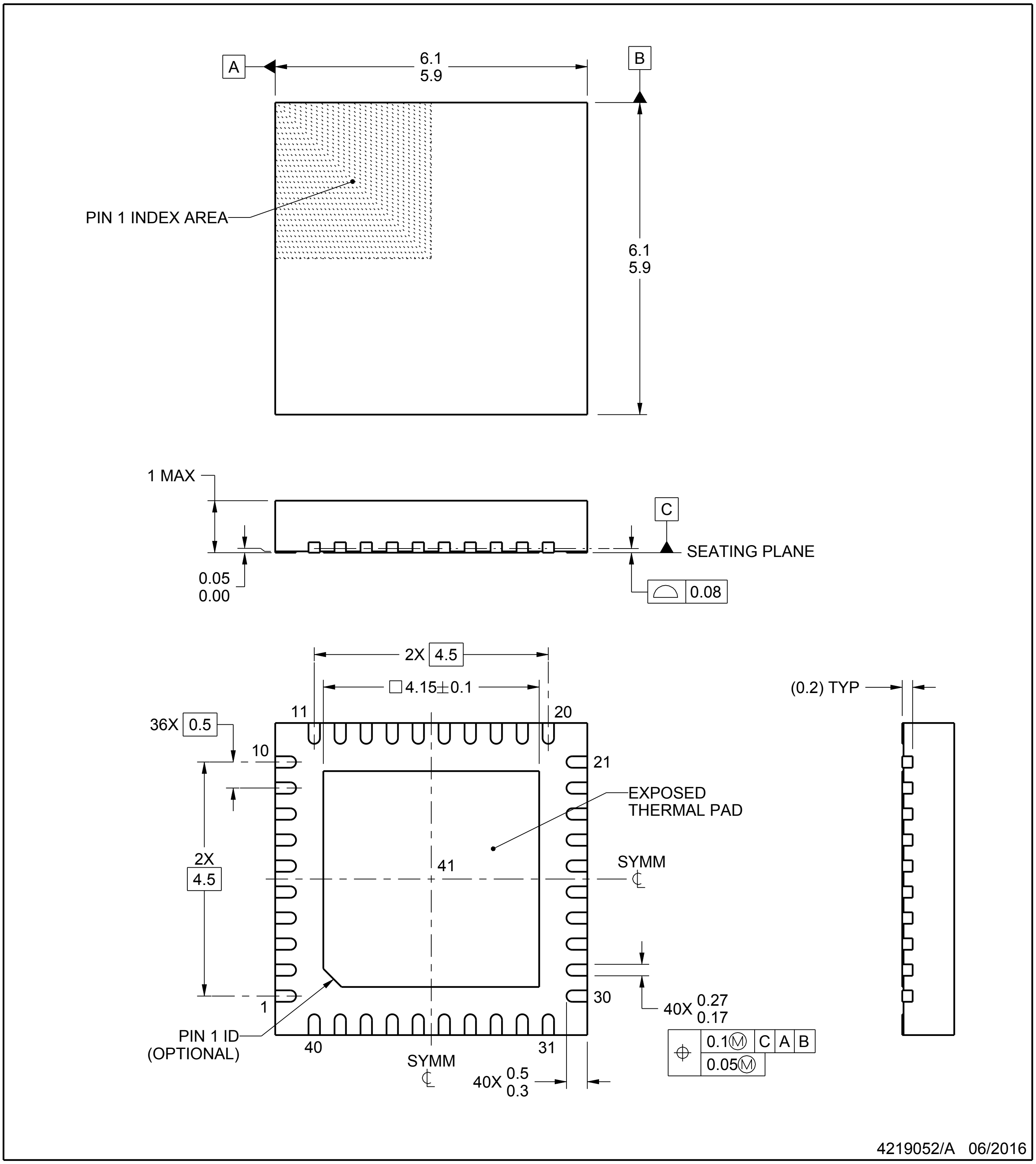
6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

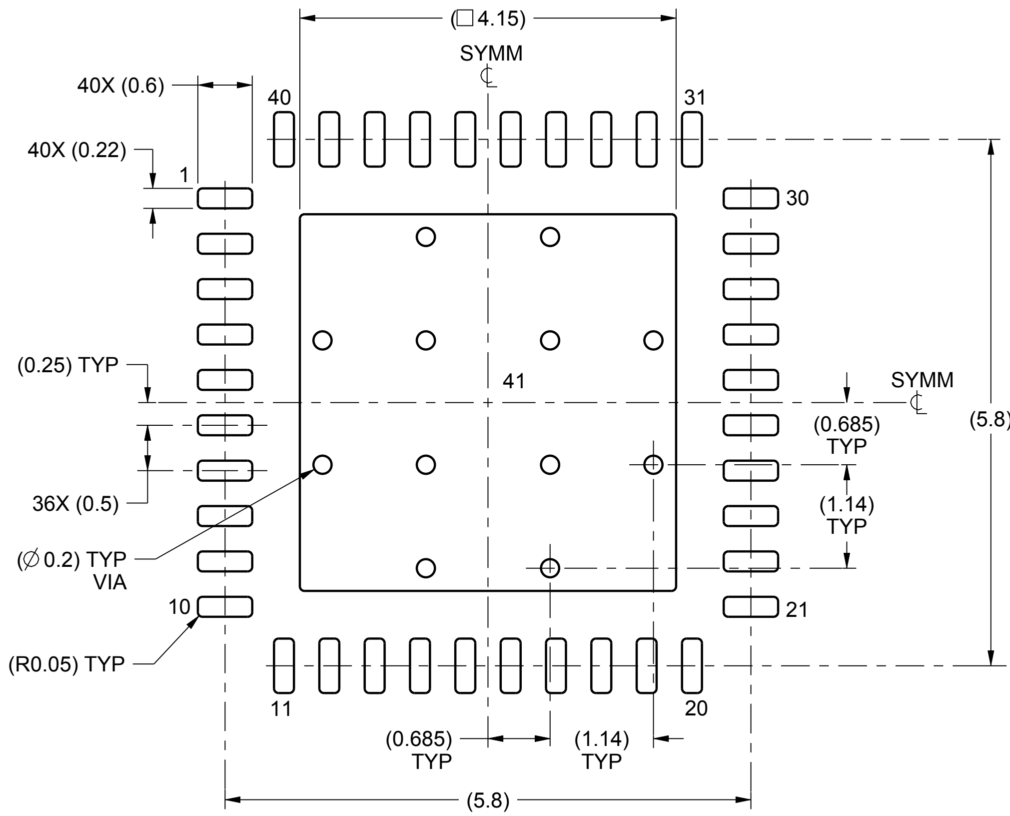


4225870/A

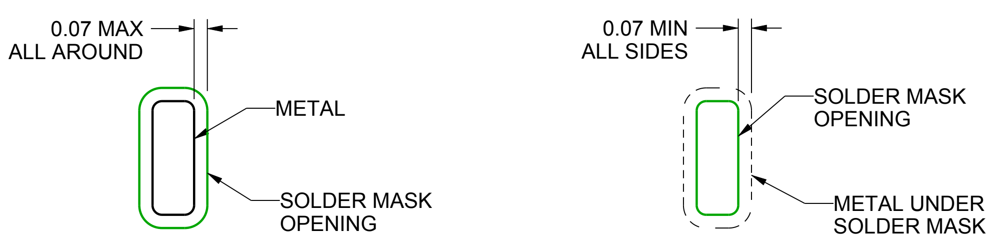


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:12X



NON SOLDER MASK
DEFINED
(PREFERRED)

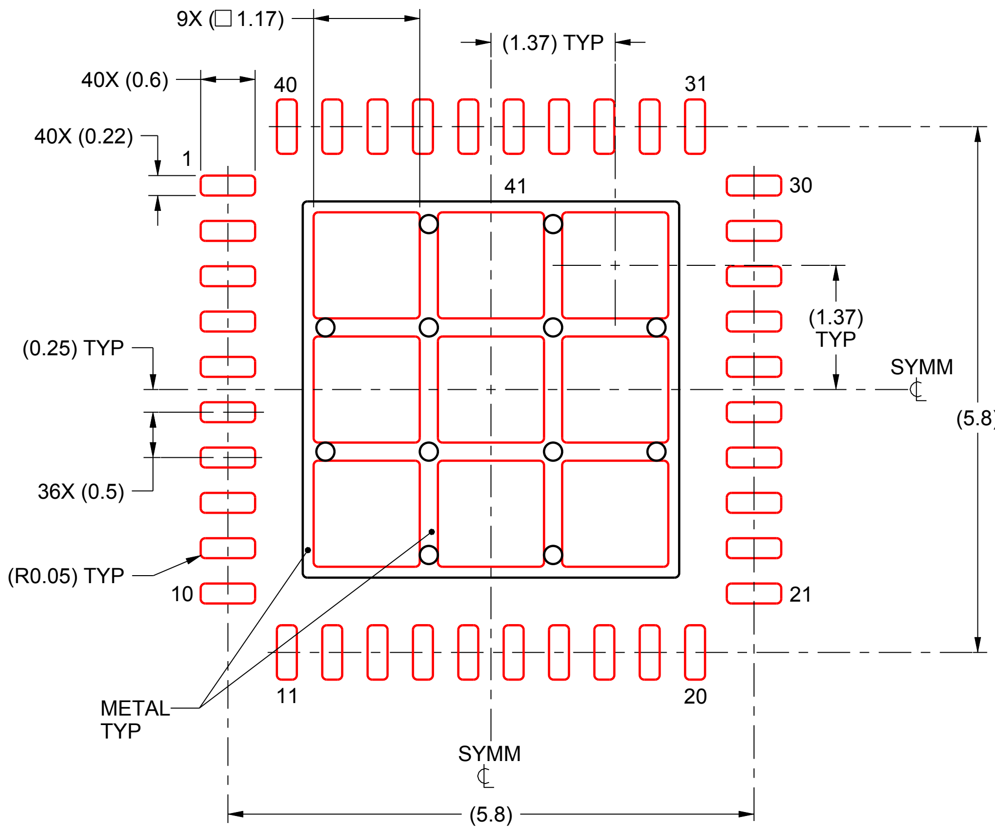
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219052/A 06/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4219052/A 06/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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