LP8772x-Q1 Three Buck Converters, One Linear Regulator and One Load Switch for mmWave Radar Sensors

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
- Functional safety-compliant device
  - Developed for functional safety applications
  - Documentation to aid ISO 26262 functional safety system design up to ASIL-B
  - BUCK, LDO and load switch output and Input supply overvoltage and undervoltage monitoring
  - Q&A Watchdog
  - Level or PWM error signal monitor (ESM)
  - ABIST and CRC
- Input voltage: 3.3 V nominal (3 V to 4 V range)
- 3 high-efficiency, low noise, high frequency step-down DC/DC converters:
  - Output voltage: 0.8 V, 0.82 V, 0.9 V to 1.9 V with 20 mV output voltage step
  - Maximum output current: 3.5 A
  - Switching frequency: 4.4 MHz, 8.8 MHz, and 17.6 MHz
- 600 mA linear regulator with bypass \ load switch mode (LDO_LS1)
  - Input voltage, LDO mode: 1.2 V to 4 V
  - Output voltage: 0.6 V to 3.4 V with 50 mV output voltage step
  - Input voltage, bypass \ load switch mode: 1.6 V to 3.4 V
- 400 mA load switch (LS2)
  - Input voltage range: 1.6 V to 3.6 V
  - On resistance 3.3-V input, 200 mA: 75 mΩ -typ
- Output short-circuit and overload protection
- Regulator output dynamic voltage scaling (DVS) through I2C interface
- Input overvoltage protection (OVP) and undervoltage lockout (UVLO)
- Two general purpose voltage monitors shared with LDO_LS1 and LS2 output
- Overtemperature warning and protection
- I2C interface supporting standard, fast mode, fast-mode+ and optional I2C address selection

2 Applications

- Satellite radar
- Short and medium range corner radar
- Ultra-short range radar
- Long range front radar
- Low ripple, low noise applications

3 Description

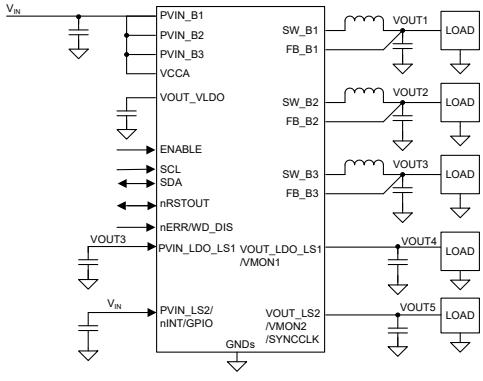
The LP8772x-Q1 device is designed to meet the power management requirements of the AWR, IWR, and other MMICs in various automotive and industrial radar applications. The device has three step-down DC/DC converters, a LDO regulator, and a load switch. The LDO is powered externally and intended for supplying Ethernet device or any other device in the system. The load switch is intended to cut off the 3.3 V IO supply during the sensor sleep mode. The device is controlled by I2C communication interface and by enable signals.

The low noise step-down DC/DC converters support factory programmed switching frequency of 17.6 MHz or 8.8 MHz or 4.4 MHz. High switching frequency and low noise across wide frequency range, enables LDO-free power solution which helps to reduce the solution cost and improve thermal performance. The switching clock is forced to PWM mode for excellent RF performance and can also be synchronized to an external clock. The LP8772x-Q1 device supports remote voltage sensing to compensate IR drop between the regulator output and the point-of-load (POL) which improves the accuracy of the output voltage.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (2)
LP8772x-Q1	RAG (VQFN-HR, 24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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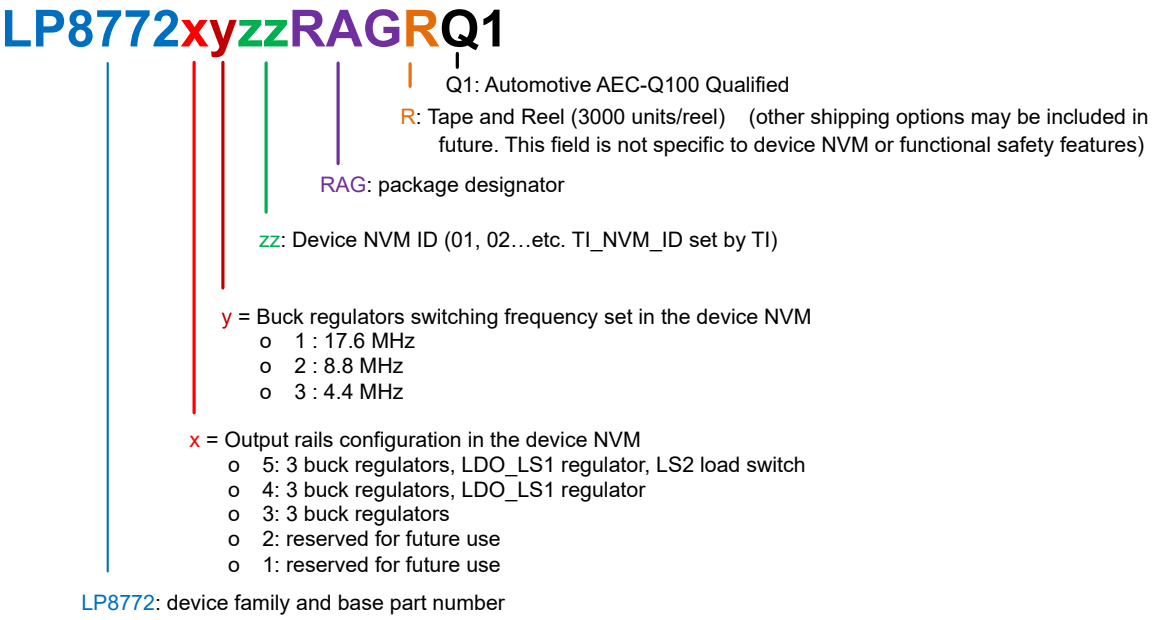
4 Description (continued)

The LP8772x-Q1 device supports programmable start-up and shutdown delays and sequences which are synchronized to the ENABLE signal. These sequences can also include GPO signal to control external regulators, load switches, and processor reset. The default settings for the device are programmed into nonvolatile memory (NVM) / one time programmable (OTP) memory at the factory and user cannot change the device default NVM / OTP settings. The device controls the output slew rate to minimize output voltage overshoot and in-rush current during device start-up.

LP8772x-Q1 family devices follow the **LP8772xyzzRAGRQ1** orderable part number scheme, where:



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5 Pin Configuration and Functions

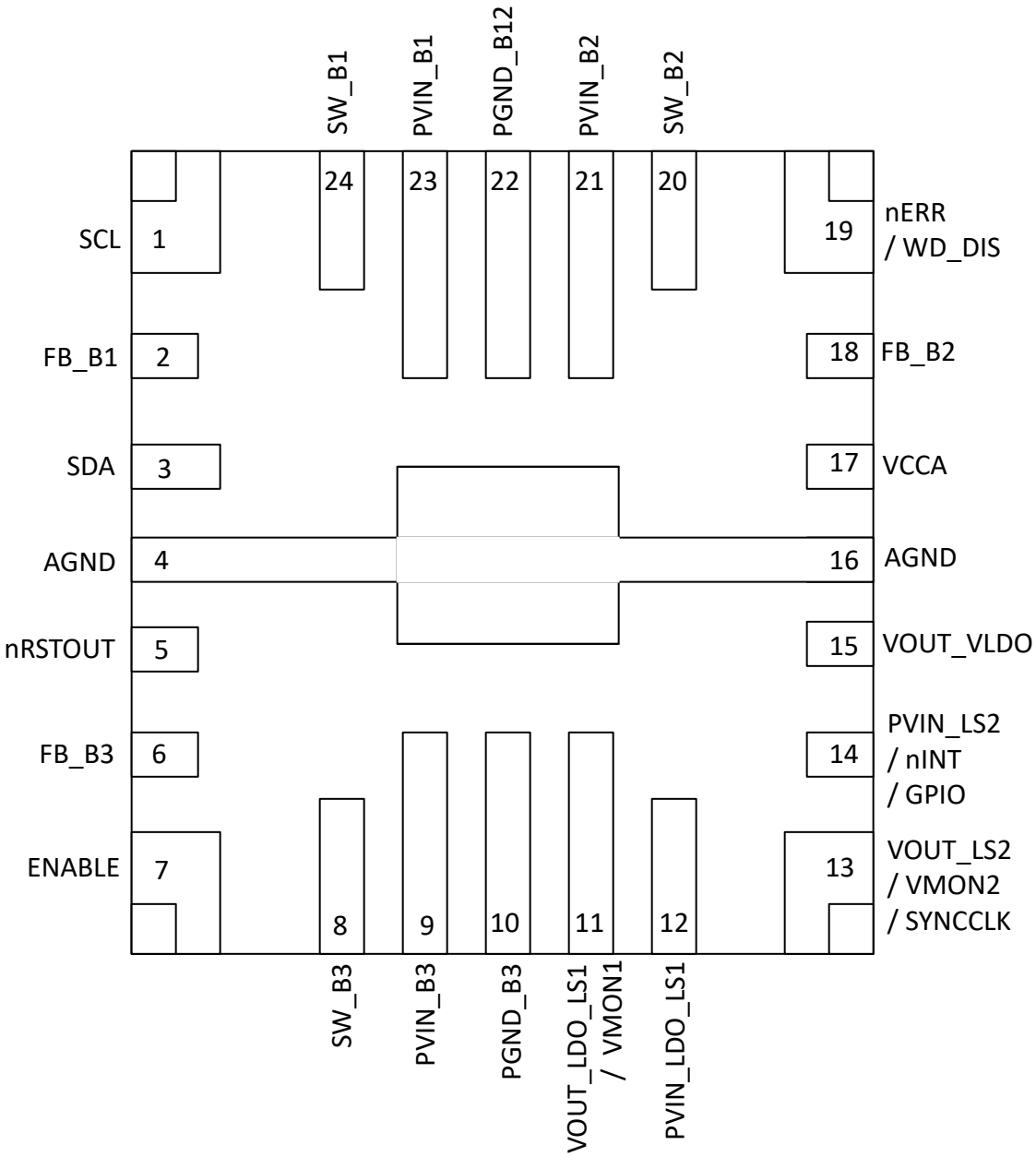

Figure 5-1. Package 24-Pin VQFN-HR Top View

Table 5-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
1	SCL	I	Digital	I2C interface serial clock (external pull up).	VCCA
2	FB_B1	—	Analog	Output voltage feedback for BUCK1.	GND
3	SDA	I / O	Digital	I2C interface bidirectional serial data (external pull up).	VCCA
4	AGND	—	Ground	Ground.	Ground
5	nRSTOUT	O	Digital	Reset output.	Floating
6	FB_B3	—	Analog	Output voltage feedback for BUCK3.	Ground
7	ENABLE	I	Digital	Programmable ENABLE signal.	Not applicable

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Table 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION	CONNECTION IF NOT USED
NO.	NAME				
8	SW_B3	—	Analog	BUCK3 switch node.	Floating
9	PVIN_B3	—	Power	Power input for BUCK3. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	PMIC input supply
10	PGND_B3	—	Ground	Power ground for BUCK3.	Ground
11	VOUT_LDO_LS1/VMON1	—	Power	Output voltage of LDO_LS1	Floating
		—	Analog	Alternative programmable function: Voltage monitoring input	GND
12	PVIN_LDO_LS1	—	Power	Input voltage of LDO_LS1	VCCA
13	VOUT_LS2/VMON2/SYNCCLK	—	Power	Output of Load Switch 2	GND
		—	Analog	Alternative programmable function: Voltage monitoring input	GND
		I	Digital	Alternative programmable function: External clock input.	GND
14	PVIN_LS2/nINT/GPIO	—	Power	Input supply for Load Switch 2	Ground
		O	Digital	Alternative programmable function: Interrupt output for System MCU	Floating
		I/O	Digital	Alternative programmable function (output): General purpose output. Alternative programmable function (input): I2C address selection through external pull -up / pull-down	Floating
15	VOUT_VLDO	—	Power	Internal LDO regulator filter node. LDO is used for internal purposes.	-
16	AGND	—	Ground	Ground.	Ground
17	VCCA	—	Power	Supply voltage for internal LDO. VCCA and PVIN_Bxx pins must be connected together in the application and be locally bypassed.	System supply
18	FB_B2	—	Analog	Output voltage feedback for BUCK2.	Ground
19	nERR/WD_DIS	I	Digital	Primary function: System MCU Error Monitoring Input.	Ground
		I	Digital	Alternative programmable function: Watchdog Disable Input.	Ground
20	SW_B2	—	Analog	BUCK2 switch node.	Floating
21	PVIN_B2	—	Power	Power input for BUCK2. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
22	PGND_B12	—	Ground	Power ground for BUCK1 and BUCK2.	Ground
23	PVIN_B1	—	Power	Power input for BUCK1. The separate power pins PVIN_Bxx are not connected together internally – PVIN_Bxx and VCCA pins must be connected together in the application and be locally bypassed.	System supply
24	SW_B1	—	Analog	BUCK1 switch node.	Floating

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5.1 Digital Signal Descriptions

Table 5-2. Input Signal Descriptions

PIN NAME	POWER DOMAIN (recommended max)	INTERNAL PU/PD	DEGLITCH TIME
nERR	VCCA	10 kΩ PU to VCCA	15 µs
WD_DIS	VCCA	-	30 µs
SCL	VCCA	-	-
SDA	VCCA	-	-
VMON1	VCCA	-	LDO_LS1_VMON1_DEGLITCH_SEL
VMON2	VCCA	-	LS2_VMON2_DEGLITCH_SEL
SYNCCLK	VCCA	400 kΩ PD to GND	-
ENABLE	VCCA	400 kΩ PD to GND	8 µs
GPIO (I2C Address select)	VCCA	-	8 µs

ENABLE input is always functional when VCCA is at the valid level. Other input buffers are disabled until the valid VCCA supply is present and the device startup has progressed to a certain state. The input buffers are enabled after the OTP is read.

Table 5-3. Output Signal Descriptions

PIN NAME	POWER DOMAIN	PIN MODE	OUTPUT TYPE	INTERNAL PU/PD
SDA	VCCA	-		-
nRSTOUT	VCCA	-	Open-drain or push-pull Active low or active high	In OD mode 10 kΩ programmable PU to VCCA when output driven high. PU disabled when output driven low.
nINT/GPO	VCCA	-	Open-drain or push-pull Active low or active high	In OD mode 10 kΩ programmable PU to VCCA when output driven high. PU disabled when output driven low.

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6 Device and Documentation Support

6.1 Documentation Support

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.4 Trademarks

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6.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2023	*	Initial Release

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP87725101RAGRQ1	Active	Production	VQFN-HR (RAG) | 24	5000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LP8772 5101-Q1
LP87725101RAGRQ1.A	Active	Production	VQFN-HR (RAG) | 24	5000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LP8772 5101-Q1
LP8772510ERAGRQ1	Active	Production	VQFN-HR (RAG) | 24	5000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LP8772 510E-Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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