LMX2615-SP Space Grade 40MHz to 15GHz Wideband Synthesizer With Phase Synchronization and JESD204B Support

1 Features

- Radiation specifications:
  - Single event latch-up >120MeV-cm^2/mg
  - Total ionizing dose to 100krad(Si)
  - SMD 5962R1723601VXC
- 40MHz to 15.2GHz output frequency
- –110dBc/Hz phase noise at 100kHz offset with 15GHz carrier
- 45fs RMS jitter at 8GHz (100Hz to 100MHz)
- Programmable output power
- PLL key specifications:
  - Figure of merit: –236dBc/Hz
  - Normalized 1/f noise: –129dBc/Hz
  - Up to 200MHz phase detector frequency
- Synchronization of output phase across multiple devices
- Support for SYSREF with programmable delay
- 3.3V single power supply operation
- 71 pre-selected pin modes
- 11 × 11mm² 64-lead CQFP ceramic package
- Operating temperature range: –55°C to +125°C

2 Applications

- Space communications
- Space radar systems
- Phased array antennas and beam forming
- High-speed data converter clocking (supports JESD204B)

3 Description

The LMX2615-SP is a high performance wideband phase-locked loop (PLL) with integrated voltage controlled oscillator (VCO) and voltage regulators that can output any frequency from 40MHz and 15.2GHz without a doubler, which eliminates the need for ½ harmonic filters. The VCO on this device covers an entire octave so the frequency coverage is complete down to 40MHz. The high performance PLL with a figure of merit of –236dBc/Hz and high phase detector frequency can attain very low in-band noise and integrated jitter.

The LMX2615-SP allows users to synchronize the output of multiple instances of the device. This means that deterministic phase can be obtained from a device in any use case including the one with fractional engine or output divider enabled. The device also adds support for either generating or repeating SYSREF (compliant to JESD204B standard), making the device designed low-noise clock source for high-speed data converters.

Device Information

PART NUMBER	GRADE	PACKAGE
LMX2615-MKT-MS	Mechanical Sample(1)	64-lead CQFP
LMX2615W-MPR	Engineering Model(2)	64-lead CQFP
5962R1723601VXC	Flight Model	64-lead CQFP Mass = 1787mg(3)

(1) These units are package only and contain no die; they are intended for mechanical evaluation only.
(2) These units are not suitable for production or flight use; they are intended for engineering evaluation only. See Section 10.1 for details.
(3) Nominal value.

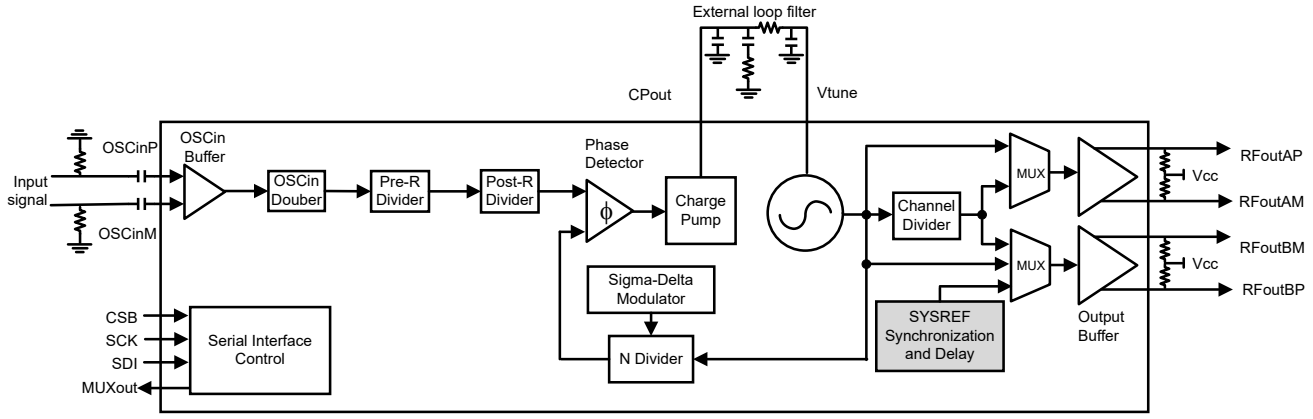

Figure 3-1. Simplified Schematic

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4 Pin Configuration and Functions

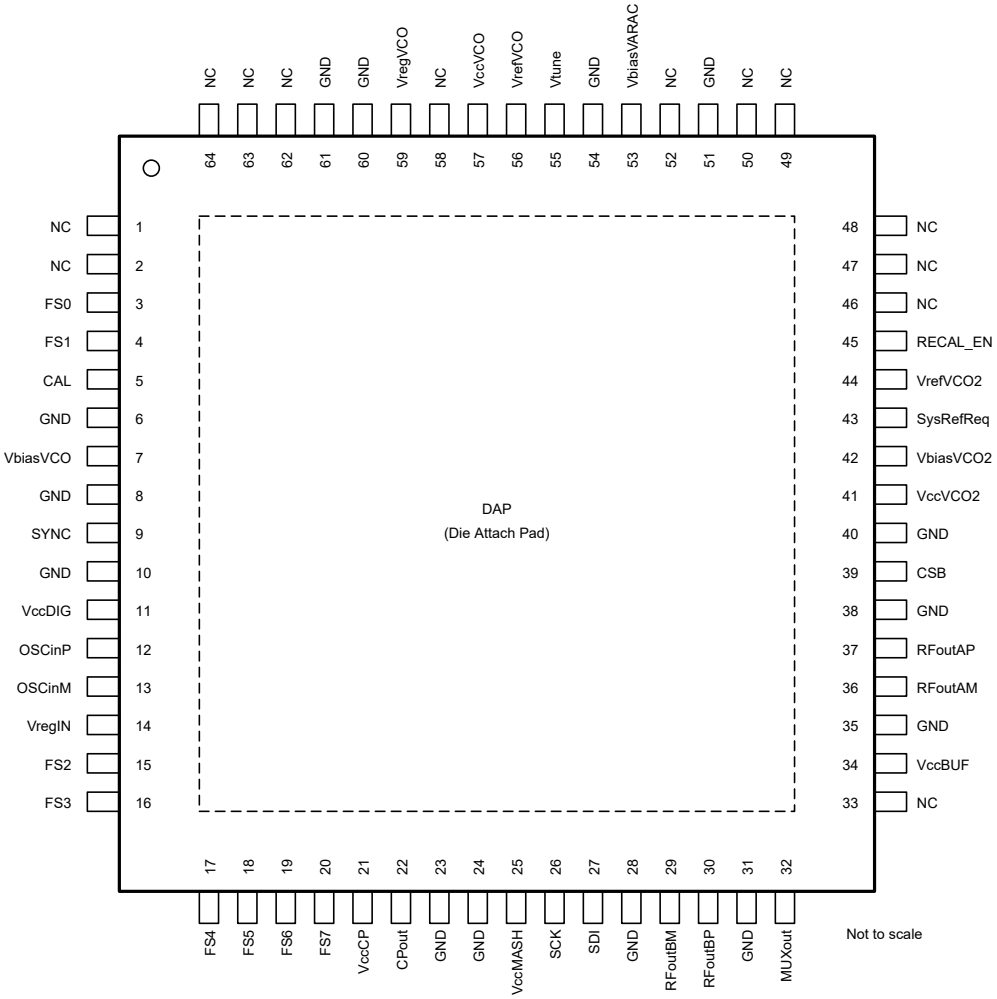


Figure 4-1. HBD Package 64-Pin CQFP Top View

Table 4-1. Pin Functions

PIN		Type[1]	DESCRIPTION
NO.	NAME		
1	NC	NC	No connection. Pin can be grounded or left unconnected.
2	NC	NC	No connection. Pin can be grounded or left unconnected.
3	FS0	I	Pin mode parallel pin control bit 0. This is the LSB.
4	FS1	I	Pin mode parallel pin control bit 1.
5	CAL	I	Chip Enable pin. Active High powers on the device. In Pin mode, a Low-to-High transition to this pin activates a VCO calibration.
6	GND	G	Ground.
7	VbiasVCO	BP	VCO bias. Requires connecting 10µF capacitor to ground. Place close to pin.
8	GND	G	Ground.
9	SYNC	I	Phase synchronization SYNC signal input pin.
10	GND	G	Ground.
11	VccDIG	P	Digital supply. Connect to 3.3V with a low ESR 1µF decoupling capacitor to ground.
12	OSCinP	I	Reference input clock (+). High input impedance. Requires connecting series capacitor (1µF recommended).

Table 4-1. Pin Functions (continued)

PIN		Type[1]	DESCRIPTION
NO.	NAME		
13	OSCinM	I	Complementary pin to OSCinP.
14	VregIN	BP	Input reference path regulator decoupling. Requires connecting 1µF capacitor to ground. Place close to pin.
15	FS2	I	Pin mode parallel pin control bit 2.
16	FS3	I	Pin mode parallel pin control bit 3.
17	FS4	I	Pin mode parallel pin control bit 4.
18	FS5	I	Pin mode parallel pin control bit 5.
19	FS6	I	Pin mode parallel pin control bit 6.
20	FS7	I	Pin mode parallel pin control bit 7. This is the MSB. When this pin is Low, only RFoutA is active, otherwise both outputs are active.
21	VccCP	P	Charge pump supply. Connect to 3.3V with a low ESR 1µF decoupling capacitor to ground.
22	CPout	O	Charge pump output. Recommend connecting C1 of loop filter close to this pin.
23	GND	G	Ground.
24	GND	G	Ground.
25	VccMASH	P	Digital supply. Connect to 3.3V with a low ESR 1µF decoupling capacitor to ground.
26	SCK	I	SPI input clock.
27	SDI	I	SPI input data.
28	GND	G	Ground.
29	RFoutBM	O	Complementary pin to RFoutBP.
30	RFoutBP	O	Differential output B (+). Requires connecting a 50Ω resistor pullup to V_{CC} as close as possible to pin. Can be used as a RF output or SYSREF output.
31	GND	G	Ground.
32	MUXout	O	Multiplexed output pin. Configurable as lock detect output, SPI read back data output or high-impedance (approximately 8kΩ to ground).
33	NC	NC	No connection. Pin can be grounded or left unconnected.
34	VccBUF	P	Output buffer supply. Connect to 3.3V with a low ESR 0.1µF decoupling capacitor to ground.
35	GND	G	Ground.
36	RFoutAM	O	Complementary pin to RFoutAP.
37	RFoutAP	O	Differential output A (+). Requires connecting a 50Ω resistor pullup to V_{CC} as close as possible to pin.
38	GND	G	Ground.
39	CSB	I	SPI chip select.
40	GND	G	Ground.
41	VccVCO2	P	VCO supply. Connect to 3.3V with a low ESR 1µF decoupling capacitor to ground. This pin and VccVCO pin must be tied to the same supply source.
42	VbiasVCO2	BP	VCO bias. Requires connecting 1µF capacitor to ground.
43	SysRefReq	I	SYSREF request input for JESD204B support.
44	VrefVCO2	BP	VCO supply reference. Requires connecting 10µF capacitor to ground.
45	RECAL_EN	I	Active High enables the automatic recalibration feature. Internal 200kΩ pull-up.
46	NC	NC	No connection. Pin can be grounded or left unconnected.
47	NC	NC	No connection. Pin can be grounded or left unconnected.
48	NC	NC	No connection. Pin can be grounded or left unconnected.
49	NC	NC	No connection. Pin can be grounded or left unconnected.
50	NC	NC	No connection. Pin can be grounded or left unconnected.
51	GND	G	Ground.

Table 4-1. Pin Functions (continued)

PIN		Type(1)	DESCRIPTION
NO.	NAME		
52	NC	NC	No connection. Pin can be grounded or left unconnected.
53	VbiasVARAC	BP	VCO Varactor bias. Requires connecting 10µF capacitor to ground.
54	GND	G	Ground.
55	Vtune	I	VCO tuning voltage input. Connect a 1.5nF or more capacitor to ground.
56	VrefVCO	BP	VCO supply reference. Requires connecting 10µF capacitor to ground.
57	VccVCO	P	VCO supply. Connect to 3.3V with a low ESR 1µF decoupling capacitor to ground. This pin and VccVCO2 pin must be tied to the same supply source.
58	NC	NC	No connection. Pin can be grounded or left unconnected.
59	VregVCO	BP	VCO regulator node. Requires connecting 1µF capacitor to ground.
60	GND	G	Ground.
61	GND	G	Ground.
62	NC	NC	No connection. Pin can be grounded or left unconnected.
63	NC	NC	No connection. Pin can be grounded or left unconnected.
64	NC	NC	No connection. Pin can be grounded or left unconnected.
—	DAP	G	Die Attach Pad. The metal lid, seal ring and DAP are internally connected to GND. Connect DAP to PCB ground plane using multiple vias for good thermal performance.

(1) The definitions below define the I/O type for each pin.

- I = Input
- O = Output
- BP = Bypass
- G = Ground
- NC = No connect
- P = Power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage(1)	–0.3	3.6	V
V_{DIG}	Digital pin voltage (FS0 - FS7, SYNC, SysRefReq, RECAL_EN, CAL, SCK, SDI, CSB)	−0.3	V_{CC}+0.3	V
$\|V_{OSC}\|$	Differential AC voltage between OSCinP and OSCinM		2.1	V_{PP}
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage	3.2	3.3	3.45	V
T_C	Case temperature	–55	25	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		CQFP	UNIT
		64 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (2)	7.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) DAP

5.5 Electrical Characteristics

3.2V ≤ V_{CC} ≤ 3.45V, –55°C ≤ T_C ≤ +125°C. Typical values are at V_{CC} = 3.3V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{CC}	Supply current	OUTA_PD = 0, OUTB_PD = 1 OUTA_MUX = OUTB_MUX = 1 OUTA_PWR = 31, CPG = 7 f_{OSC} = f_{PD} = 100MHz, f_{VCO} = f_{OUT} = 14.5GHz			360		mA
	Power on reset current	RESET = 1			289		
	Power down current	POWERDOWN = 1			6		
OUTPUT CHARACTERISTICS							
P_{OUT}	Single-ended output power(1) (2)	50Ω resistor pullup OUTx_PWR = 31	f_{OUT} = 8GHz		6		dBm
			f_{OUT} = 15GHz		4		
INPUT SIGNAL PATH							
f_{OSC}	Reference input frequency	OSC_2X = 0		5		1000	MHz
		OSC_2X = 1		5		200	
		Category 3 phase synchronization				50	
V_{OSC}	Reference input voltage	Single-ended AC coupled sine wave input with complementary side AC coupled to ground with 50Ω resistor	f_{OSC} ≥ 20MHz	0.4		2	V_{PP}
			10MHz ≤ f_{OSC} < 20MHz	0.8		2	
			5MHz ≤ f_{OSC} < 10MHz	1.6		2	
PHASE DETECTOR AND CHARGE PUMP							
f_{PD}	Phase detector frequency(3)	MASH_ORDER = 0		0.125		250	MHz
		MASH_ORDER > 0		5		200	
I_{CPout}	Charge-pump leakage current	CPG = 0			15		nA
	Effective charge pump current. This is the sum of the up and down currents	CPG = 4			3		mA
		CPG = 1			6		
		CPG = 5			9		
		CPG = 3			12		
		CPG = 7			15		
$PN_{PLL\_1/f}$	Normalized PLL 1/f noise	f_{PD} = 100MHz, f_{VCO} = 12GHz(4)			–129		dBc/Hz
PN_{PLL_FOM}	Normalized PLL noise floor				–236		dBc/Hz

3.2V ≤ V_{CC} ≤ 3.45V, –55°C ≤ T_C ≤ +125°C. Typical values are at V_{CC} = 3.3V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VCO CHARACTERISTICS							
f_{VCO}	VCO frequency			7600		15200	MHz
PN_{VCO}	VCO phase noise	VCO1 f_{VCO} = 8.1GHz	100kHz		–105		dBc/Hz
			1MHz		–127		
			10MHz		–148		
			100MHz		–155		
		VCO2 f_{VCO} = 9.3GHz	100kHz		–103		
			1MHz		–125		
			10MHz		–146		
			100MHz		–153		
		VCO3 f_{VCO} = 10.4GHz	100kHz		–103		
			1MHz		–125		
			10MHz		–147		
			100MHz		–158		
		VCO4 f_{VCO} = 11.4GHz	100kHz		–101		
			1MHz		–124		
			10MHz		–146		
			100MHz		–158		
		VCO5 f_{VCO} = 12.5GHz	100kHz		–102		
			1MHz		–126		
			10MHz		–147		
			100MHz		–156		
		VCO6 f_{VCO} = 13.6GHz	100kHz		–101		
			1MHz		–124		
			10MHz		–146		
			100MHz		–160		
		VCO7 f_{VCO} = 14.7GHz	100kHz		–101		
			1MHz		–124		
			10MHz		–146		
			100MHz		–157		
t_{VCOCAL}	VCO calibration time	Switch across the entire frequency band; f_{OSC} = f_{PD} = 100MHz; No assist calibration			650		µs
K_{VCO}	VCO Gain	8.1GHz			94		MHz/V
		9.3GHz			106		
		10.4GHz			122		
		11.4GHz			148		
		12.5GHz			185		
		13.6GHz			202		
		14.7GHz			233		
$\lvert\Delta T_{CL}\rvert$	Allowable temperature drift when VCO is not re-calibrated				125		°C
H2	VCO second harmonic	f_{VCO} = 8GHz, divider disabled			–30		dBc
H3	VCO third harmonic	f_{VCO} = 8GHz, divider disabled			–25		

3.2V ≤ V_{CC} ≤ 3.45V, –55°C ≤ T_C ≤ +125°C. Typical values are at V_{CC} = 3.3V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DIGITAL INTERFACE (Applies to SCK, SDI, CSB, CAL, RECAL_EN, MUXout, SYNC, SysRefReq, FSx)							
V_{IH}	High-level input voltage			1.6			V
V_{IL}	Low-level input voltage					0.4	V
I_{IH}	High-level input current			–100		100	µA
I_{IL}	Low-level input current			–100		100	µA
V_{OH}	High-level output voltage	MUXout pin	Load current = –5mA	V_{CC} – 0.6			V
V_{OL}	Low-level output voltage		Load current = 5mA			0.6	V

(1) Single-ended output power obtained after de-embedding microstrip trace losses and matching with a manual tuner. Unused port terminated to 50Ω load.
(2) Output power, spurs, and harmonics can vary based on board layout and components.
(3) For lower VCO frequencies, the N divider minimum value can limit the phase-detector frequency.
(4) The PLL noise contribution is measured using a clean reference and a wide loop bandwidth and is composed into flicker and flat components. PLL_flat = PLL_FOM + 20× log(f_{VCO}/f_{PD}) + 10 × log(f_{PD} / 1Hz). PLL_flicker (offset) = PLL_1/f + 20 × log(f_{VCO} / 1GHz) – 10× log(offset / 10kHz). Once these two components are found, the total PLL noise can be calculated as PLL_Noise = 10 × log($10^{PLL\_Flat / 10} + 10^{PLL\_flicker /10}$)

5.6 Timing Requirements

(3.2V ≤ V_{CC} ≤ 3.45V, –55°C ≤ T_A ≤ +125°C, except as specified. Nominal values are at V_{CC} = 3.3V, T_A = 25°C)

			MIN	NOM	MAX	UNIT
SYNC AND SYSREFREQ TIMING						
t_{SETUP}	Setup time for pin relative to OSCIN rising edge	See Figure 5-1	2.5			ns
t_{HOLD}	Hold time for pin relative to OSCIN rising edge		2.5			ns
SPI TIMING						
f_{SPI}	SPI SCK speed	t_{CWL} + t_{CWH} ≥ 500ns			2	MHz
t_{CE}	Clock to enable low time	See Figure 5-2	50			ns
t_{CS}	Clock to data wait time		50			ns
t_{CH}	Clock to data hold time		50			ns
t_{CWH}	Clock pulse width high		200			ns
t_{CWL}	Clock pulse width low		200			ns
t_{CES}	Enable to clock setup time		50			ns
t_{EWH}	Enable pulse width high		100			ns
t_{CD}	Falling clock edge to data wait time				200	ns

5.7 Timing Diagrams

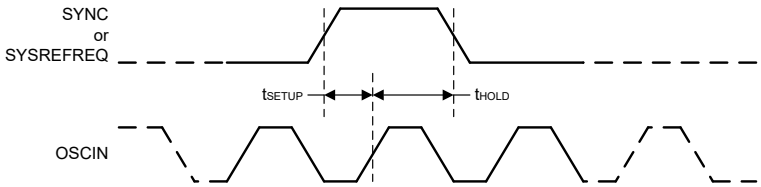


Figure 5-1. Trigger Signals Timing Diagram

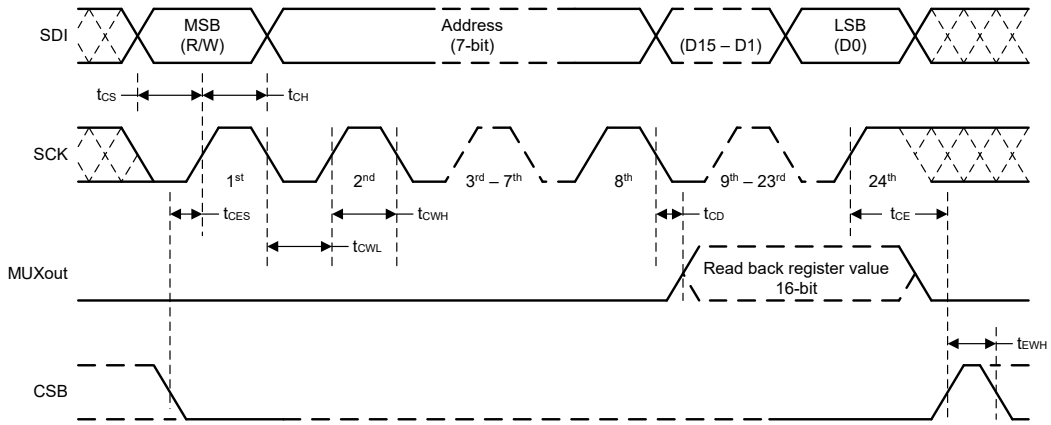


Figure 5-2. SPI Timing Diagram

LMX2615-SP supports SPI Mode 0 (CPOL=0, CPHA=0) and Mode 3 (CPOL=01 CPHA=1).

To write registers:

- The R/W bit must be set to 0.
- The data on SDI pin is clocked into the shift register upon the rising edge of the clocks on SCK pin. On the rising edge of the 24th clock cycle, the data is transferred from the data field into the selected register bank.
- The CSB pin can be held high after programming, which causes the LMX2615-SP to ignore clock pulses.
- If the SCK and SDI lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared between devices, the phase noise can be degraded during the time of this programming.

To read back registers:

- The R/W bit must be set to 1.
- The data field contents on the SDI line are ignored.
- The read back data on MUXout pin is clocked out starting from the falling edge of the 8th clock cycle.
- MUXout pin is tri-state only if MUXOUT_CTRL = 0.

5.8 Typical Characteristics

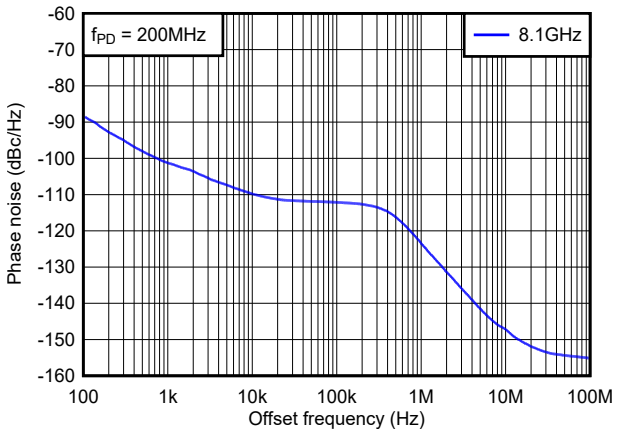


Figure 5-3. Closed-Loop Phase Noise at 8.1GHz

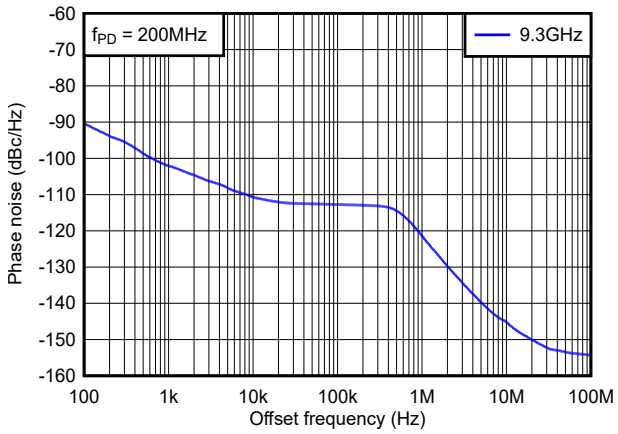


Figure 5-4. Closed-Loop Phase Noise at 9.3GHz

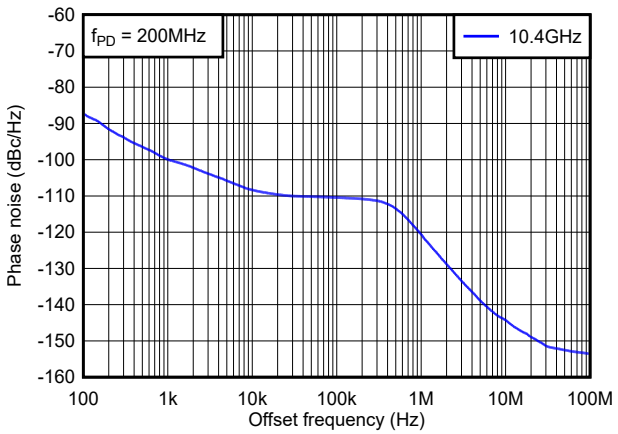


Figure 5-5. Closed-Loop Phase Noise at 10.4GHz

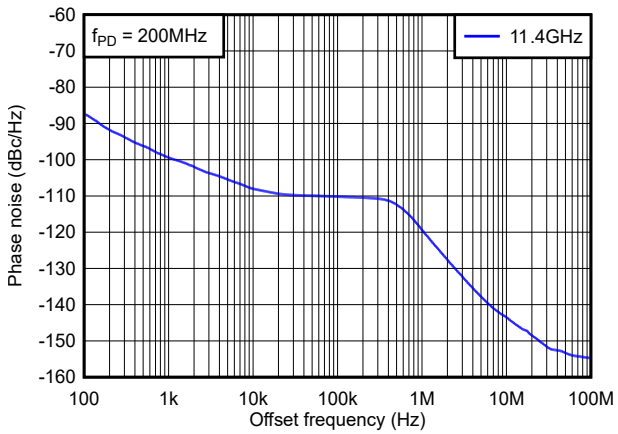


Figure 5-6. Closed-Loop Phase Noise at 11.4GHz

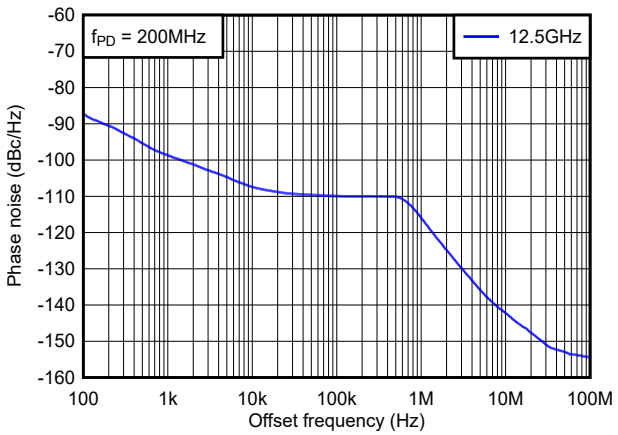


Figure 5-7. Closed-Loop Phase Noise at 12.5GHz

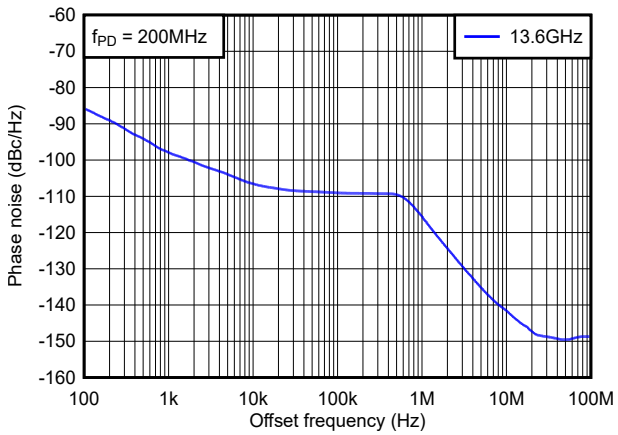


Figure 5-8. Closed-Loop Phase Noise at 13.6GHz

5.8 Typical Characteristics (continued)

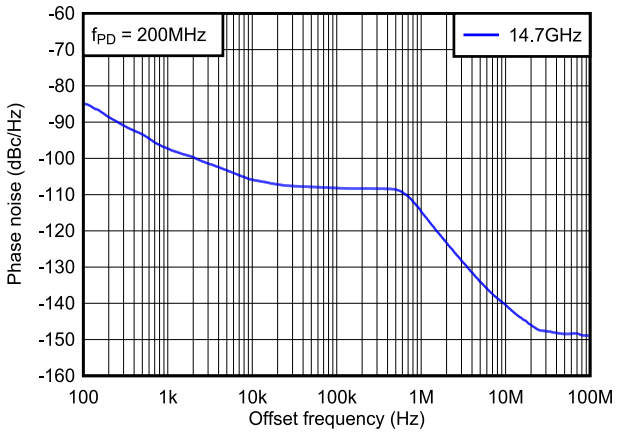


Figure 5-9. Closed-Loop Phase Noise at 14.7GHz

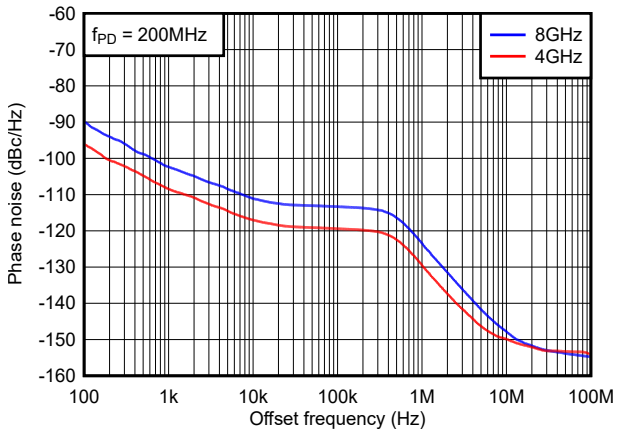


Figure 5-10. Closed-Loop Phase Noise with CHDIV enabled

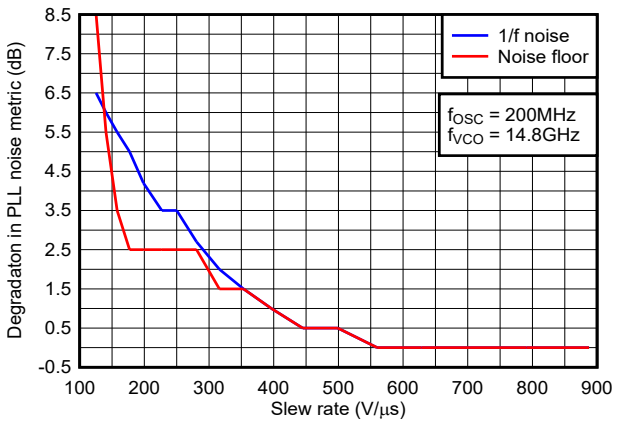


Figure 5-11. PLL Phase Noise Metrics vs f_{OSC} Slew Rate

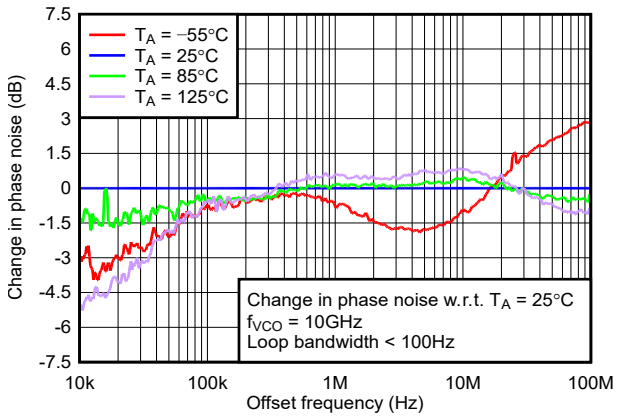


Figure 5-12. Change in VCO Phase Noise Over Temperature

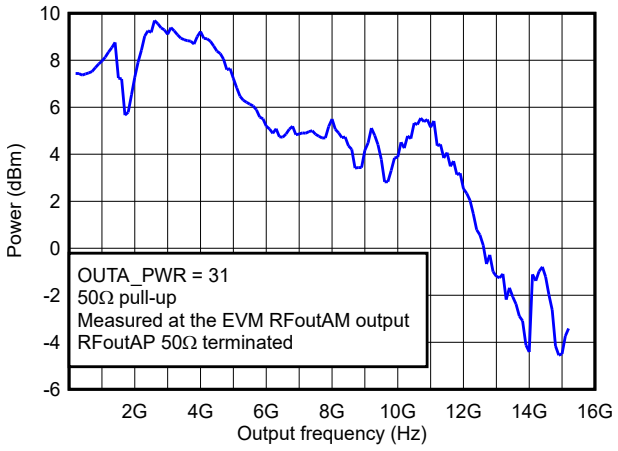


Figure 5-13. Output Power vs Frequency

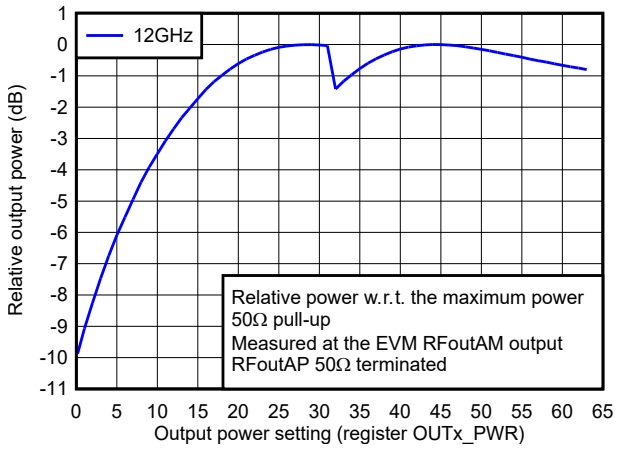


Figure 5-14. Output Power vs Power Setting

6 Detailed Description

6.1 Overview

The LMX2615-SP is a high-performance, wideband frequency synthesizer with integrated VCO and output divider. The VCO operates from 7600MHz to 15200MHz and this can be combined with the output divider to produce any frequency in the range of 40MHz to 15.2GHz. Within the input path there are two dividers .

The PLL is fractional-N PLL with programmable delta-sigma modulator up to 4^{th} order. The fractional denominator is a programmable and 32-bits long, which can provide fine frequency steps easily below 1Hz resolution as well as be used to do exact fractions like 1/3, 7/1000, and many others.

For applications where deterministic or adjustable phase is desired, the SYNC pin can be used to get the phase relationship between the OSCin and RFout pins deterministic. Once this is done, the phase can be adjusted in very fine steps of the VCO period divided by the fractional denominator.

The ultra-fast VCO calibration is ideal for applications where the frequency must be swept or abruptly changed. The frequency can be manually programmed.

The JESD204B support includes using the RFoutB output to create a differential SYSREF output that can be either a single pulse or a series of pulses that occur at a programmable distance away from the rising edges of the output signal.

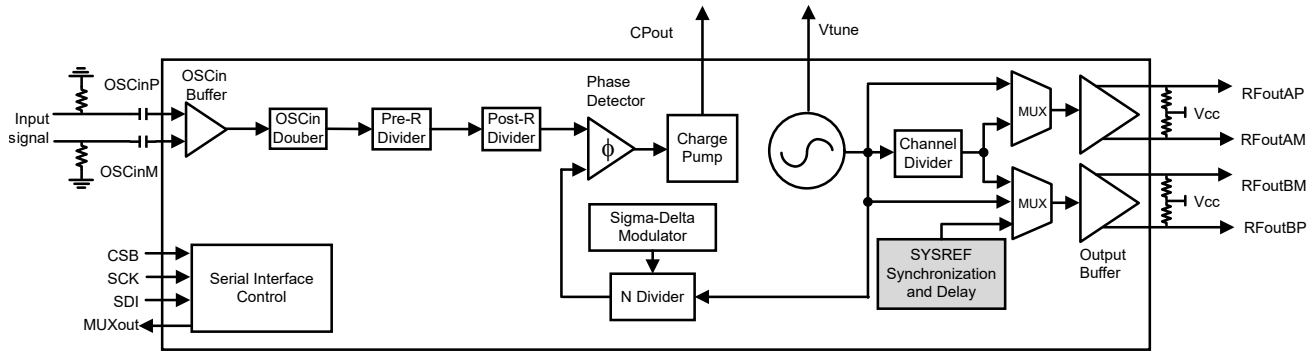
The LMX2615-SP device requires only a single 3.3V power supply. The internal power supplies are provided by integrated LDOs, eliminating the need for high performance external LDOs.

Table 6-1 shows the range of several of the doubler, dividers, and fractional settings.

Table 6-1. Range of Doubler, Divider, and Fractional Settings

PARAMETER	MIN	MAX	COMMENTS
OSCin doubler	0 (1X)	1 (2X)	The low noise doubler can be used to increase the phase detector frequency to improve phase noise and avoid spurs. This is in reference to the OSC_2X bit.
Pre-R divider	1 (bypass)	128	Only use the Pre-R divider if the input frequency is too high for the Post-R divider.
Post-R divider	1 (bypass)	255	The maximum input frequency for the Post-R divider is 250MHz. Use the Pre-R divider if necessary.
N divider	≥ 28	524287	The minimum divide depends on fractional order and VCO frequency. See Section 6.3.5 for more details.
Fractional numerator	0 (Integer channel)	$2^{32} – 2 = 4294967294$	The fractional numerator is programmable. This numerator is ignored when fractional order = integer mode.
Fractional denominator	1	$2^{32} – 1 = 4294967295$	The fractional denominator is programmable, This denominator is not a fixed denominator.
Fractional order (MASH_ORDER)	0	4	Order 0 is integer mode and the order can be programmed.
Channel divider	2	192	This is the series of several dividers. Also, be aware that above 11.5GHz, the maximum allowable channel divider value is 6.
Output frequency	Approx. 40MHz	15.2GHz	This is implied by the minimum VCO frequency divided by the maximum channel divider value.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Reference Oscillator Input

The OSCin pins are used as a frequency reference input to the device. The input is high impedance and requires AC-coupling capacitors at the pin. The OSCin pins can be driven single-ended with a CMOS clock or XO. Differential clock input is also supported, making interfacing with high-performance system clock devices such as TI's LMK series clock devices simpler. As the OSCin signal is used as a clock for the VCO calibration, a proper reference signal must be applied at the OSCin pin at the time of programming FCAL_EN = 1. Reference clock signal can be presented at OSCin before the LMX2615-SP device is powered up.

6.3.2 Reference Path

The reference path consists of an OSCin doubler (OSC_2X), Pre-R divider, and a Post-R divider.

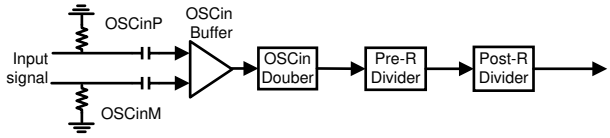


Figure 6-1. Reference Path Diagram

The OSCin doubler (OSC_2X) can double up low OSCin frequencies. Pre-R (PLL_R_PRE) and Post-R (PLL_R) dividers both divide frequency down. The phase detector frequency, f_{PD}, is calculated in Equation 1

$$f_{PD} = f_{OSC} \times OSC\_2X / (PLL\_R\_PRE \times PLL\_R) \quad (1)$$

For Equation 1, remember:

- If the OSCin doubler is used, the OSCin signal must have a 50% duty cycle as both the rising and falling edges are used.
- If the OSCin doubler is not used, only rising edges of the OSCin signal are used and duty cycle is not critical.

6.3.2.1 OSCin Doubler (OSC_2X)

The OSCin doubler allows one to double the input reference frequency up to 400MHz while adding minimal noise. In some situations using the doubler to go to a higher frequency than the maximum phase detector frequency can be advantageous because the Pre-R divider can be able to divide down this frequency to phase detector frequency that is advantageous for fractional spurs.

6.3.2.2 Pre-R Divider (PLL_R_PRE)

The Pre-R divider is useful for reducing the input frequency to help meet the maximum 250MHz input frequency limitation to the PLL-R divider. Otherwise, Pre-R divider does not have to be used.

6.3.2.3 Post-R Divider (PLL_R)

The Post-R divider can be used to further divide down the frequency to the phase detector frequency. When the divider is used (PLL_R > 1), the input frequency to this divider is limited to 250MHz.

6.3.3 State Machine Clock

The state machine clock is a divided down version of the OSCin signal that is used internally in the device. This divide value 1, 2, 4, 8, 16 or 32 is determined by CAL_CLK_DIV programming word. This state machine clock impacts various features like the VCO calibration. The state machine clock is calculated as $f_{SM} = f_{OSC} / 2^{CAL\_CLK\_DIV}$. Maximum state machine clock frequency is 50MHz.

6.3.4 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the Post-R divider and N divider and generates a correction current corresponding to the phase error until the two signals are aligned in phase. This charge-pump current is software programmable to many different levels, allowing modification of the closed-loop bandwidth of the PLL.

6.3.5 N Divider and Fractional Circuitry

The N divider includes fractional compensation and can achieve any fractional denominator from 1 to ($2^{32} – 1$). The integer portion of N is the whole part of the N divider value, and the fractional portion, N_{frac} = NUM / DEN, is the remaining fraction. In general, the total N divider value is determined by N + NUM / DEN. The N, NUM and DEN are software programmable. The higher the denominator, the finer the resolution step of the output. For example, even when using f_{PD} = 200MHz, the output can increment in steps of 200MHz / ($2^{32} – 1$) = 0.047Hz. Equation 2 shows the relationship between the phase detector and VCO frequencies.

$$f_{VCO} = f_{PD} \times \text{IncludedDivide} \times (N + NUM / DEN) \quad (2)$$

The sigma-delta modulator that controls this fractional division is also programmable from integer mode to fourth order. To make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

The N divider has minimum value restrictions based on the modulator order and VCO frequency. Furthermore, the PFD_DLY_SEL bit must be programmed in accordance to the Table 6-2. PFD_DLY_SEL is used to optimize phase noise, the recommended values apply to most PLL configurations. These values can be slightly alternated to suit actual application needs.

In SYNC mode, IncludedDivide can be larger than one, otherwise IncludedDivide is just 1. See Table 6-11 for details.

Table 6-2. Minimum N Divider Restrictions

MASH_ORDER	f_{VCO} / IncludedDivide (MHz)	MINIMUM N	PFD_DLY_SEL
0	≤ 12500	29	1
	> 12500	33	2
1	≤ 10000	30	1
	10000 – 12500	34	2
	> 12500	38	3
2	≤ 4000	31	1
	7500 – 10000	35	2
	> 10000	39	3
3	≤ 4000	33	1
	7500 – 10000	41	3
	> 10000	45	4
4	≤ 4000	45	3
	7500 – 10000	53	5
	> 10000	57	6

6.3.6 MUXout Pin

The MUXout pin can be configured as lock detect indicator for the PLL or as an serial data output (SDO) for the SPI to read back registers. Field MUXOUT_LD_SEL (register R0[2]) configures this output.

Table 6-3. MUXout Pin Configurations

MUXOUT_LD_SEL	FUNCTION
0	Serial data output for readback
1	Lock detect indicator

When lock detect indicator is selected, there are two types of indicator and the indicators can be selected with the field LD_TYPE (register R59[0]). The first indicator is called “VCOCal” (LD_TYPE = 0) and the second indicator is called “Vtune and VCOCal” (LD_TYPE = 1).

6.3.6.1 Serial Data Output for Readback

In this mode, the MUXout pin becomes the serial data output of the SPI. This output can be configured to tri-state (MUXOUT_CTRL = 0) so line sharing is possible. Readback is very useful when LMX2615-SP is used in full assist mode and VCO calibration data are retrieved and saved for future use. Readback can also be used to read back the lock status using the field rb_LD_VTUNE(register R110[10:9]).

6.3.6.2 Lock Detect Indicator Set as Type “VCOCal”

In this mode the MUXout pin is asserted HIGH after a VCO calibration is completed (no matter if the calibration is successful or not) and the lock detect delay timer is time out. During a VCO calibration and before the lock delay timer is time out, MUXout pin is LOW. The programmable lock detect timer (LD_DLY) adds an additional delay after the VCO calibration finishes before the lock detect indicator is asserted high. LD_DLY is a 16 bit unsigned quantity that corresponds to 4 times the number of state machine clock cycles. For example, given f_{OSC} = 100MHz, CAL_CLK_DIV = 1, then state machine clock frequency = f_{OSC} / $2^{CAL\_CLK\_DIV}$ = 50MHz. If LD_DLY = 1000, the delay time is equal to 80µs. MUXout pin remains in the current state no matter if the PLL is actually locked or not. In other words, if the PLL goes out of lock or the input reference goes away when the current state is high, then the current state remains high. This lock detect setting is useful for measuring VCO calibration time.

6.3.6.3 Lock Detect Indicator Set as Type “Vtune and VCOCal”

In this mode the MUXout pin is high when the VCO calibration has finished, the lock detect delay timer is finished running, and the PLL is locked. This indicator can remain in the current state (high or low) if the OSCin signal is lost. The true status of the indicator is updated and resume operation only when a valid input reference to the OSCin pin is returned. An alternative method to monitor the OSCin of the PLL is recommended. This indicator is reliable as long as the reference to OSCin is present.

Since both types of lock detect indicator requires a completion of VCO calibration, at least one VCO calibration has to be performed in full assist mode, otherwise the lock detector does not work.

6.3.7 VCO (Voltage-Controlled Oscillator)

The LMX2615-SP includes a fully integrated VCO. The VCO takes the voltage from the loop filter and converts this into a frequency. The VCO frequency is related to the other frequencies as shown in Equation 2.

6.3.7.1 VCO Calibration

To reduce the VCO tuning gain and therefore improve the VCO phase-noise performance, the VCO frequency range is divided into several different frequency bands. The entire range, 7600MHz to 15200MHz, covers an octave that allows the divider to take care of frequencies below the lower bound. This creates the need for frequency calibration to determine the correct frequency band given a desired output frequency. The frequency calibration routine is activated any time that the R0 register is programmed with the FCAL_EN = 1. A valid OSCin signal must present before VCO calibration begins.

The VCO also has an internal amplitude calibration algorithm to optimize the phase noise which is also activated any time the R0 register is programmed.

The optimum internal settings for this are temperature dependent. If the temperature is allowed to drift too much without being re-calibrated, some minor phase noise degradation can result. The maximum allowable drift for continuous lock, ΔT_{CL}, is stated in the electrical specifications. For this device, a number of 125°C means the device never loses lock if the device is operated under recommended operating conditions.

The LMX2615-SP allows the user to assist the VCO calibration. In general, there are three kinds of assistance, as shown in Table 6-4:

Table 6-4. Assisting the VCO Calibration Speed

ASSISTANCE LEVEL	DESCRIPTION	VCO_SEL	VCO_SEL_FORCE VCO_CAPCTRL_FORCE VCO_DACISET_FORCE	VCO_CAPCTRL VCO_DACISET
No assist	User does nothing to improve VCO calibration speed.	7	0	Don't Care
Partial assist	Upon every frequency change, before the FCAL_EN bit is checked, the user provides the initial starting VCO_SEL.	Choose by table	0	Don't Care
Full assist	The user forces the VCO core (VCO_SEL), amplitude settings (VCO_DACISET), and frequency band (VCO_CAPCTRL) and manually sets the value.	Choose by readback	1	Choose by readback

For the no assist method, just set VCO_SEL = 7 and this is done. For partial assist, the VCO calibration time can be improved by changing the VCO_SEL bit according to the target frequency. Note that the frequencies in Table 6-5 is not the exact VCO core range, but actually favors choosing the VCO. This is not only optimal for VCO calibration time, but required for reliable locking. Both method requires programming R0, with FCAL_EN = 1, to complete the VCO calibration.

Table 6-5. Minimum VCO_SEL for Partial Assist

f_{VCO} (MHz)	VCO CORE (MIN)
7600 - 8740	VCO1
8740 - 10000	VCO2
10000 - 10980	VCO3
10980 -12100	VCO4
12100 - 13080	VCO5
13080 - 14180	VCO6
14180 - 15200	VCO7

Full assist mode completely skips the VCO calibration process, this method results in the shortest VCO frequency switching time. Operation of this mode requires a one-time VCO calibration to get the VCO parameters (VCO_SEL, VCO_DACISET and VCO_CAPCTRL) for all the frequency of interests. This data is manually applied to the LMX2615-SP device. When the xxx_FORCE bits are set, the device uses this data to setup the VCO. Programming of R0 is not necessary in full assist mode. However, if R0 with FCAL_EN = 1 is programmed, a VCO calibration takes place but the VCO parameters remain as the written values.

6.3.7.2 Watchdog Feature

The watchdog feature is used to the scenario when radiation is present during VCO calibration which can cause the VCO calibration to fail. When this feature is enabled, the watchdog timer runs during VCO calibration. If this timer runs out before the VCO calibration is finished, then the VCO calibration is restarted. The WD_CNTRL word sets how many times this calibration can be restarted by the watchdog feature.

6.3.7.3 RECAL Feature

The RECAL feature is used to mitigate the scenario when the VCO is in lock, but then radiation causes the VCO to go out of lock. When the RECAL_EN pin is high, if the PLL loses lock and stays out of lock for a time specified by the WD_DLY word, then RECAL triggers a VCO re-calibration. Lock detector must be set to "Vtune and VCOCal" (LD_TYPE = 1) and the lock detect timer (LD_DLY) must be non-zero. Suggested minimum lock detector timer delay time is 200µs for 50MHz state machine clock frequency.

6.3.7.4 Determining the VCO Gain

The VCO gain varies between the seven cores and is the lowest at the lowest end of the band and highest at the highest end of each band. For a more accurate estimation, use Table 6-6:

Table 6-6. VCO Gain

f1 (MHz)	f2 (MHz)	$K_{VCO}1$	$K_{VCO}2$
7600	8740	78	114
8740	10000	91	125
10000	10980	112	136
10980	12100	136	168
12100	13080	171	206
13080	14180	188	218
14180	15200	218	248

Equation 3 can estimate the VCO gain for an arbitrary VCO frequency, f_{VCO}:

$$K_{VCO} = K_{VCO}1 + (K_{VCO}2 - K_{VCO}1) \times (f_{VCO} - f1) / (f2 - f1) \quad (3)$$

6.3.8 Channel Divider

To go below the VCO lower bound of 7600MHz, the channel divider can be used. The channel divider consists of four segments, and the total division value is equal to the multiplication of them. Therefore, not all values are valid.

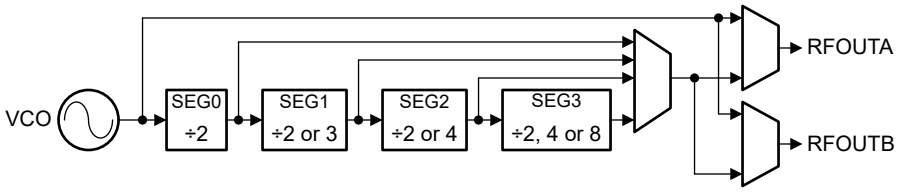


Figure 6-2. Channel Divider

When the channel divider is used, there are limitations on the values.

Table 6-7. Channel Divider Limitations

CHDIV[4:0]	EQUIVALENT DIVISION VALUE	VCO FREQUENCY LIMITATION
0	2	None
1	4	
2	6	
3	8	$f_{VCO} \leq 11.5GHz$
4	12	
5	16	
6	24	
7	32	
8	48	
9	64	
10	96	
11	128	
12	192	

The channel divider is powered up whenever an output (OUTx_MUX) is selected to the channel divider or SYSREF_EN = 1, regardless of whether the channel divider is powered down or not. When an output is not

used, TI recommends selecting the VCO output to verify that the channel divider is not unnecessarily powered up.

Table 6-8. Channel Divider

OUTA MUX	OUTB MUX	SYSREF_EN	CHANNEL DIVIDER
Channel Divider	X	X	Powered up
X	Channel Divider	X	
X	X	1	
All Other Cases			Powered down

6.3.9 Output Buffer

The RF output buffer type is open collector and requires an external pullup to V_{CC}. This component can be a 50Ω resistor or an inductor. The inductor has less controlled impedance, but higher power. For the inductor case, follow this with a resistive pad. The output power can be programmed to various levels or disabled while still keeping the PLL in lock. If using a resistor, limit OUTx_PWR setting to 31; higher than this tends to actually reduce power. Note that states 32 through 47 are redundant and must be ignored. In other words, after state 31, the next higher power setting is 48.

Table 6-9. OUTx_PWR Recommendations

f_{OUT}	Restrictions	Comments
10MHz ≤ f_{OUT} ≤ 5GHz	None	At lower frequencies, the output buffer impedance is high, so the 50Ω pullup makes the output impedance look somewhat like 50Ω. Typically, maximum output power is near a setting of OUTx_PWR = 50.
5GHz < f_{OUT} ≤ 10GHz	OUTx_PWR ≤ 31	In this range, parasitic inductances have some impact, so the output setting is restricted.
10GHz < f_{OUT}	OUTx_PWR ≤ 20	At these higher frequency ranges, keep below 20 for highest power and optimal noise floor.

6.3.10 Powerdown Modes

The LMX2615-SP can be powered up and down using the CAL pin or the POWERDOWN bit. In Pin mode, a Low-to-High transition to the CAL pin activates a VCO calibration.

6.3.11 Treatment of Unused Pins

This device has several pins for many features and there is a preferred way to treat these pins if not needed. For the input pins, a series resistor is recommend, but the pins can be directly shorted.

Table 6-10. Recommended Treatment of Pins

Pins	SPI Mode	Pin Mode	Recommended Treatment if NOT Used
FS0, FS1, FS2, FS3, FS4, FS5, FS6, FS7	Never Used	Always Used	GND with 1kΩ
SYNC, SysRefReq	Sometimes Used	Never Used	GND with 1kΩ
OSCinP, OSCinM	Always Used	Always Used	GND with 50Ω after the AC-coupling capacitor. If one side of complementary side is used and other side is not, impedance looking out must be similar for both of these pins.
SCK, SDI	Always Used	Never Used	GND with 1kΩ
CSB	Always Used	Never Used	VCC with 1kΩ
RECAL_EN	Sometimes Used	Sometimes Used	GND with 1kΩ
CAL	Sometimes Used	Always Used	VCC with 1kΩ
RFoutA, RFoutB	Sometimes Used	Sometimes Used	VCC with 50Ω. If one side of complementary side is used and the other side is not, impedance looking out must be similar for both of these pins.
MUXout	Sometimes Used	Sometimes Used	GND with 10kΩ

6.3.12 Phase Synchronization

6.3.12.1 General Concept

The SYNC pin allows one to synchronize the LMX2615-SP such that the delay from the rising edge of the OSCin signal to the output signal is deterministic. Initially, the devices are locked to the input, but are not synchronized. The user sends a synchronization pulse that is reclocked to the next rising edge of the OSCin pulse. After a given time, t_1, the phase relationship from OSCin to f_{OUT} is deterministic. This time is dominated by the sum of the VCO calibration time, the analog setting time of the PLL loop, and the MASH_RST_COUNT if used in fractional mode.

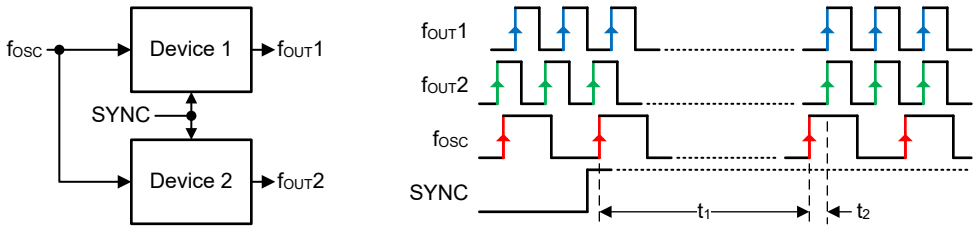


Figure 6-3. Devices Are Now Synchronized to OSCin Signal

When SYNC mode is enabled (VCO_PHASE_SYNC = 1), part of the channel divider (IncludedDivide) can be included in the feedback path. When IncludedDivide is not equal to 1:

- N divider is smaller. Care must be taken not to violate the minimum N divider restriction.
- SEG1_EN must be equal to 1.
- If IncludedDivide = 6, make use of the FCAL_HPFD_ADJ register to reduce the phase detector frequency being used during VCO calibration to less than 50MHz.

Table 6-11. IncludedDivide With VCO_PHASE_SYNC = 1

OUTx_MUX	CHANNEL DIVIDER	IncludedDivide
OUTA_MUX = OUTB_MUX = 1 ("VCO")	Don't Care	1 (bypassed)
All other valid conditions	Divisible by 3	SEG0 × SEG1 = 6
	All other values	SEG0 × SEG1 = 4

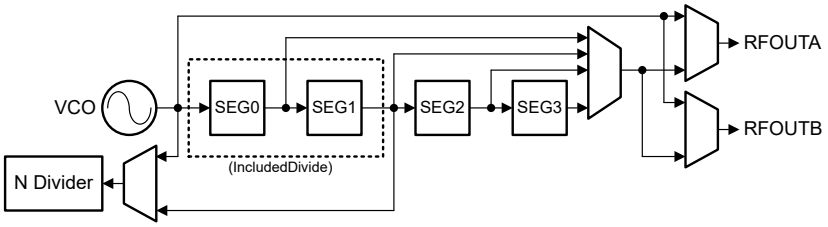


Figure 6-4. Phase SYNC Diagram

6.3.12.2 Categories of Applications for SYNC

The requirements for SYNC depend on certain setup conditions. Figure 6-5 gives the different categories. In Category 3 SYNC, the setup and hold times of the trigger signal at the SYNC pin with respect to the OSCin pin are critical.

Table 6-12. SYNC Pin Timing Characteristics for Category 3 SYNC

Parameter	Description	Min	Max	Unit
f_{OSC}	Input reference clock frequency		50	MHz
t_{SETUP}	Setup time between SYNC and OSCin rising edges	2.5		ns
t_{HOLD}	Hold time between SYNC and OSCin rising edges	2.5		ns

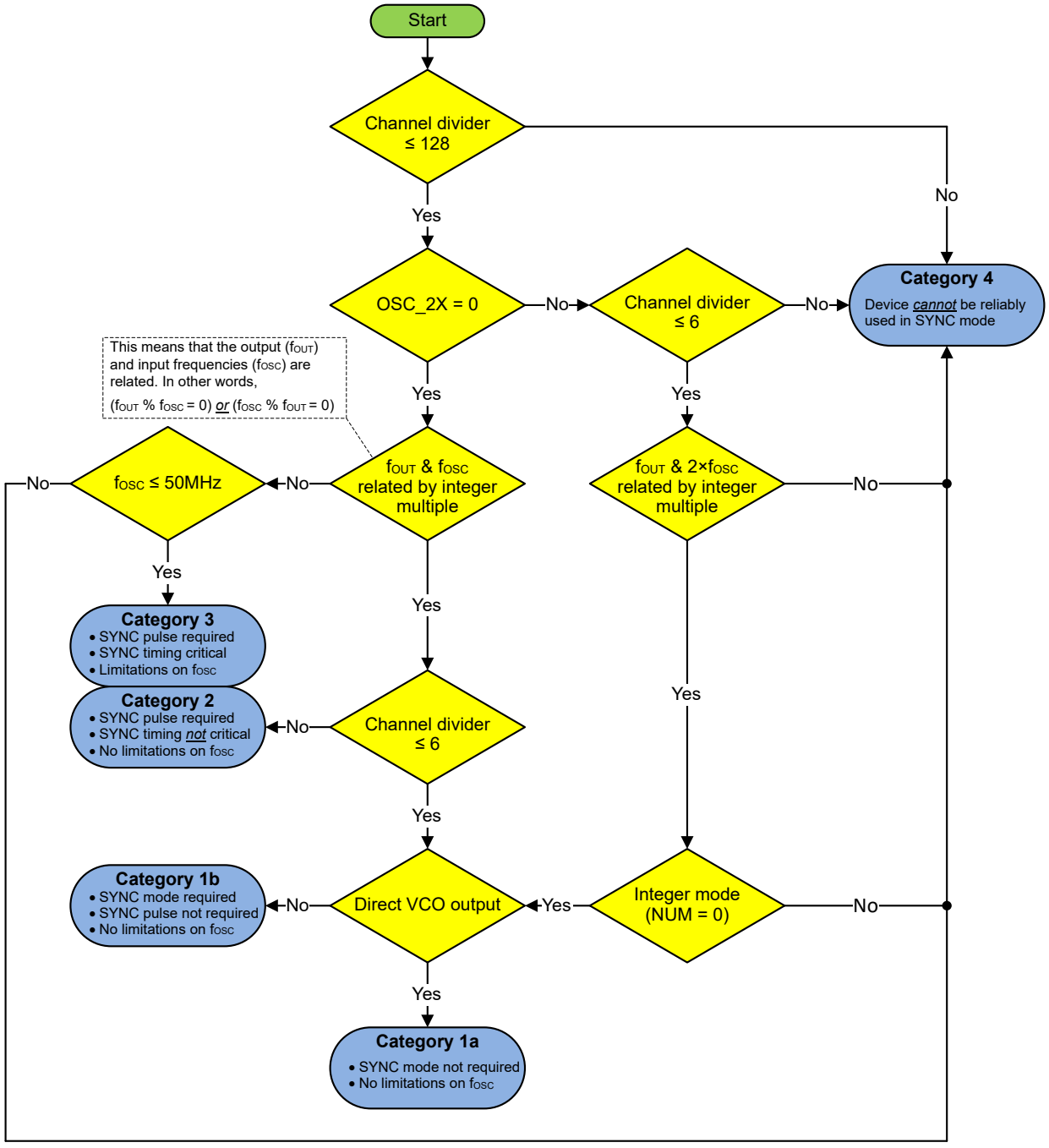


Figure 6-5. Determining the SYNC Category

6.3.12.3 Procedure for Using SYNC

This procedure must be used to put the device in SYNC mode.

1. Use the flowchart to determine the SYNC category.
2. Make determinations for OSCin and using SYNC based on the category
   a. If Category 4, SYNC cannot be performed in this setup.
   b. If Category 3, verify that the maximum f_{OSC} frequency for SYNC mode is not violated and there are hardware accommodations to use the SYNC pin.
3. If the channel divide is used, determine the IncludedDivide value from Table 6-11.

4. If not done already, divide the N divider and fractional values by IncludedDivide (Equation 2) to account for the included channel divide.
5. Program the device with the VCO_PHASE_SYNC = 1.
6. Apply the SYNC, if required
   a. If Category 2, a rising edge can be sent to the SYNC pin and the timing of this is not critical.
   b. If Category 3, the timing of the SYNC signal with respect to OSCin clock as shown in Table 6-12 must obey.

6.3.12.4 SYNC Input Pin

If not using the SYNC pin, then the INPIN_IGNORE bit must be set to one, otherwise the pin causes issues with lock detect. If the pin is desired for to be used and VCO_PHASE_SYNC = 1, then set INPIN_IGNORE = 0.

6.3.13 Phase Adjust

The MASH_SEED word can use the sigma-delta modulator to shift output signal phase with respect to the input reference. If a SYNC pulse is sent or the MASH is reset with MASH_RST_N = 0, then this phase shift is from the initial phase of zero. If the MASH_SEED word is written to, then this phase is added. The phase shift is calculated as Equation 4.

$$\text{Phase shift in degrees} = 360 \times (\text{MASH\_SEED} / \text{PLL\_DEN}) \times (\text{IncludedDivide} / \text{CHDIV}) \quad (4)$$

Example:

MASH_SEED = 1

Denominator = 12

Channel divider = 16

Phase shift (VCO_PHASE_SYNC = 0) = 360 × (1/12) × (1/16) = 1.875 degrees

Phase Shift (VCO_PHASE_SYNC = 1) = 360 × (1/12) × (4/16) = 7.5 degrees

There are several considerations when using MASH_SEED:

- Phase shift can be done with a PLL_NUM = 0, but MASH_ORDER must be greater than zero.
- For MASH_ORDER = 1, the phase shifting only occurs when MASH_SEED is a multiple of PLL_DEN.
- For MASH_ORDER = 2, PLL_N ≥ 45.
- For MASH_ORDER = 3, PLL_N ≥ 49.
- For MASH_ORDER = 4, PLL_N ≥ 54.
- For phase adjustment, the condition PLL_DEN > PLL_NUM + MASH_SEED must be satisfied.
- When MASH_SEED and phase SYNC are used together with IncludedDivide > 1, additional constraints can be necessary to produce a monotonic relationship between MASH_SEED and the phase shift, especially when the VCO frequency is below 10GHz. These constraints are application specific, but some general guidelines are to reduce modulator order and increase the N divider.
  - Use MASH_ORDER ≤ 2.
  - When using the 2nd order modulator for VCO frequencies below 10GHz (when IncludedDivide = 6) or 9GHz (when IncludedDivide = 4), increase the PLL_N value much higher or change to the 1st order modulator.
- Setting MASH_SEED > 0 can impact fractional spurs. If used with a PLL_NUM = 0, this setting can create fractional spurs. If used with a non-zero numerator, this setting can either help or hurt spurs and this effect can be simulated with the TI PLLatinum Sim tool.
- The programming of the MASH_SEED word is cumulative. *Cumulative* means that the programmed value is added to the current value. Whenever the MASH_RST_N bit is toggled or the VCO is re-calibrated, the current value is set to MASH_SEED. Static phase adjust involves setting the MASH_SEED word to the desired value and toggling the MASH_RST_N bit to force this value. Dynamic phase adjust involves setting

MASH_SEED to a smaller value and repetitively program the MASH_SEED word to add to the cumulative value for MASH_SEED. For example, we program MASH_SEED to get 10 degrees of phase shift. If we program the same value of MASH_SEED 3 times, we get 30 degrees of phase shift.

6.3.14 Fine Adjustments for Phase Adjust and Phase SYNC

Phase SYNC refers to the process of getting the same phase relationship for every power up cycle and each time assuming that a given programming procedure is followed. However, there are some adjustments that can be made to get the most accurate results. As for the consistency of the phase SYNC, the only source of variation can be if the VCO calibration chooses a different VCO core and capacitor, which can introduce a bimodal distribution with about 10ps of variation. If this 10ps is not desirable, then the variation can be eliminated by reading back the VCO parameters and forcing these values to verify the same calibration settings every time. The delay through the device varies from part to part and can be on the order of 60ps. This part to part variation can be calibrated out with the MASH_SEED. The variation in delay through the device also changes on the order of +2.5ps/°C, but devices on the same board likely have similar temperatures. In summary, the device can be made to have consistent delay through the part and there are means to adjust out any remaining errors with the MASH_SEED. This tends only to be an issue at higher output frequencies when the period is shorter.

6.3.15 SYSREF

The LMX2615-SP can generate a SYSREF output signal that is synchronized to f_{OUT} with a programmable delay. This output can be a single pulse, series of pulses, or a continuous stream of pulses. To use the SYSREF capability, the PLL must first be placed in SYNC mode with VCO_PHASE_SYNC = 1.

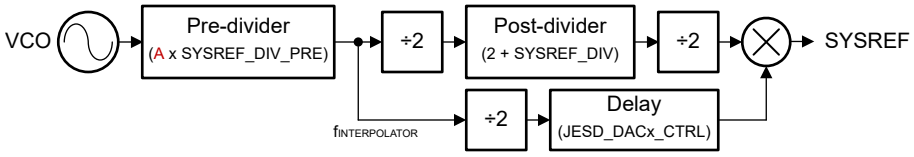


Figure 6-6. SYSREF Block Diagram

$$f_{SYSREF} = f_{VCO} / [(A \times SYSREF\_DIV\_PRE) \times 2 \times (2 + SYSREF\_DIV) \times 2], \text{ where A is the IncludedDivide value.} \quad (5)$$

As Figure 6-6 shows, the SYSREF feature uses IncludedDivide and SYSREF_DIV_PRE to generate $f_{INTERPOLATOR}$. This frequency is used for re-clocking of the rising and falling edges at the SysRefReq pin. In master mode, the $f_{INTERPOLATOR}$ is further divided down to generate finite series or continuous stream of pulses.

Table 6-13. SYSREF Specification

PARAMETER	MIN	TYP	MAX	UNIT
f_{VCO}	7600		15200	MHz
$f_{INTERPOLATOR}$	0.8		1.5	GHz
SYSREF_DIV_PRE	1, 2, or 4			
SYSREF_DIV	0, 1, 2, ..., 2047			
Pulses for pulsed mode (SYSREF_PULSE_CNT)	1		15	

The delay can be programmed using the JESD_DAC1_CTRL, JESD_DAC2_CTRL, JESD_DAC3_CTRL, and JESD_DAC4_CTRL words. By concatenating these words into a larger word called "SYSREFPHASESHIFT", the relative delay can be found. The sum of these words must always be 63. Altogether, there are 252 useful programmable steps. The delay time of each step is equal to:

$$\text{SYSREF delay time} = [(A \times SYSREF\_DIV\_PRE) \times 2] / 252 / f_{VCO}, \text{ where A is the IncludedDivide value.} \quad (6)$$

Table 6-14. SYSREF Delay

SYSREFPHASESHIFT	JESD_DAC1_CTRL	JESD_DAC2_CTRL	JESD_DAC3_CTRL	JESD_DAC4_CTRL
0	36	27	0	0
1	35	28	0	0

Table 6-14. SYSREF Delay (continued)

SYSREFPHASESHIFT	JESD_DAC1_CTRL	JESD_DAC2_CTRL	JESD_DAC3_CTRL	JESD_DAC4_CTRL
...	...	...	0	0
36	0	63	0	0
37	0	62	1	0
...	0	...	...	0
99	0	0	63	0
100	0	0	62	1
...	0	0	...	...
162	0	0	0	63
163	1	0	0	62
...	...	0	0	...
225	63	0	0	0
226	62	1	0	0
...	...	...	0	0
251	37	26	0	0

In master mode, the SysRefReq pin is pulled HIGH and stay HIGH to allow continuous SYSREF clock output. To generate SYSREF pulses, a Low-to-High transition is required at the SysRefReq pin.

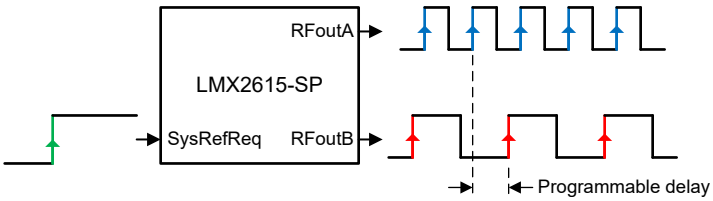


Figure 6-7. SYSREF Pulsed/Continuous Mode

The SYSREF can be used in a repeater mode, which just echos the signal at SysRefReq pin, after being re-clocked to the $f_{INTERPOLATOR}$ frequency and then output to RFoutB. In repeater mode, the mode can repeat 1, 2, 4, 8, or infinite (continuous) pulses.

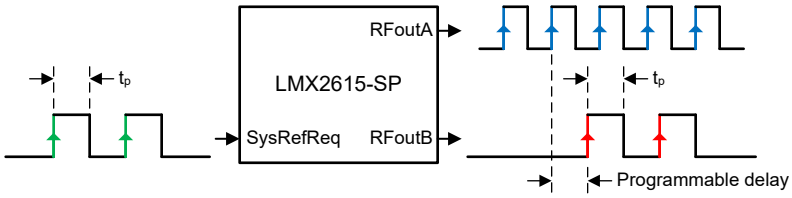


Figure 6-8. SYSREF Repeater Mode

To use SYSREF, do these steps:

1. Put the device in SYNC mode using the procedure already outlined.
2. Figure out IncludedDivide the same way as SYNC mode.
3. Calculate the SYSREF_DIV_PRE value such that the interpolator frequency ($f_{INTERPOLATOR}$) is in the range of 800MHz to 1500MHz.
4. If using master mode (SYSREF_REPEAT = 0), verify SysRefReq pin is HIGH and stays HIGH for continuous SYSREF clock generation. To generate SYSREF pulses, set SYSREF_PULSE = 1, set up the pulse count as desired. Pulses are generated with a LOW-to-HIGH transition at SysRefReq pin.
5. If using repeater mode, set SYSREF_REPEAT = 1, apply the SYSREF signal to the SysRefReq pin.
6. Adjust the delay between the RFoutA and RFoutB signal using the JESD_DACx_CTL fields.

6.3.16 Pin Modes

The LMX2615-SP has 8 pins that can be used to program pre-selected modes. A few rules of operation for these pin modes are as follows:

- Set the pin mode as desired. Pin Mode 0 is SPI mode.
- The rise time for the supply needs to be < 50ms.
- Fractional denominator for all pin modes is 4250000000.
- When changing between pin modes, after the pins are changed, the CAL pin must be toggled to calibrate the VCO.
- If the FS7 pin is low, then only the RFoutA output is active. If the FS7 pin is high, then both the RFoutA and RFoutB outputs are active.

Table 6-15 shows all the pin mode configurations.

Table 6-15. Pin Modes

MODE	f_{OSC} (MHz)	f_{PD} (MHz)	CPG (mA)	f_{OUT} (MHz)	CHDIV	f_{VCO} (MHz)	N	FRACTION
0	SPI Mode							
1	10	20	15	160	48	7680	384	0 / 4250000000
2	10	10	15	395	24	9480	948	0 / 4250000000
3	10	20	15	720	12	8640	432	0 / 4250000000
4	10	20	15	1280	6	7680	384	0 / 4250000000
5	100	200	15	300	32	9600	48	0 / 4250000000
6	100	200	15	1000	8	8000	40	0 / 4250000000
7	100	200	15	1200	8	9600	48	0 / 4250000000
8	20	40	15	6199.855	2	12399.71	309	4219187500 / 4250000000
9	100	200	15	2000	4	8000	40	0 / 4250000000
10	50	100	15	250	32	8000	80	0 / 4250000000
11	50	100	15	500	16	8000	80	0 / 4250000000
12	50	100	15	850	12	10200	102	0 / 4250000000
13	20	40	15	5654.912	2	11309.824	282	3168800000 / 4250000000
14	10	20	15	1517.867839	6	9107.207034	455	1531494725 / 4250000000
15	10	20	15	1708.670653	6	10252.02392	512	2555082575 / 4250000000
16	50	100	15	2500	4	10000	100	0 / 4250000000
17	Reserved. Do not use this pin mode.							
18	10	20	15	3035.735678	4	12142.94271	607	625326300 / 4250000000
19	50	100	15	3200	4	12800	128	0 / 4250000000
20	10	20	15	3417.341306	4	13669.36522	683	1990110100 / 4250000000
21	50	100	15	4500	2	9000	90	0 / 4250000000
22	50	100	15	4800	2	9600	96	0 / 4250000000
23	50	100	15	5350	2	10700	107	0 / 4250000000
24	50	100	15	6800	2	13600	136	0 / 4250000000
25	10	20	15	6834	2	13668	683	1700000000 / 4250000000
26	10	20	15	6834.682611	2	13669.36522	683	1990109675 / 4250000000
27	10	20	15	6834.6875	2	13669.375	683	1992187500 / 4250000000
28	10	20	15	6834.75	2	13669.5	683	2018750000 / 4250000000
29	50	100	15	9600	1	9600	96	0 / 4250000000
30	50	100	15	9650	1	9650	96	2125000000 / 4250000000
31	50	100	15	13500	1	13500	135	0 / 4250000000
32	100	100	15	70	128	8960	89	2550000000 / 4250000000

Table 6-15. Pin Modes (continued)

MODE	f_{OSC} (MHz)	f_{PD} (MHz)	CPG (mA)	f_{OUT} (MHz)	CHDIV	f_{VCO} (MHz)	N	FRACTION
33	18.75	37.5	15	393.75	24	9450	252	0 / 4250000000
34	18.75	37.5	15	422.4990441	24	10139.97706	270	1697399952 / 4250000000
35	37.5	75	15	422.4990441	24	10139.97706	135	848699976 / 4250000000
36	20	40	15	6785.552	2	13571.104	339	1179800000 / 4250000000
37	20	40	15	2088.38	4	8353.52	208	3561500000 / 4250000000
38	100	100	15	2210	4	8840	88	1700000000 / 4250000000
39	100	100	15	2238	4	8952	89	2210000000 / 4250000000
40	20	40	15	2254.35	4	9017.4	225	1848750000 / 4250000000
41	20	40	15	2270	4	9080	227	0 / 4250000000
42	20	40	15	2280	4	9120	228	0 / 4250000000
43	18.75	37.5	15	6759.984705	2	13519.96941	360	2263199800 / 4250000000
44	37.5	75	15	6759.984705	2	13519.96941	180	1131599900 / 4250000000
45	20	40	15	8125	1	8125	203	531250000 / 4250000000
46	20	40	15	8175	1	8175	204	1593750000 / 4250000000
47	20	40	15	8200	1	8200	205	0 / 4250000000
48	20	40	15	8210	1	8210	205	1062500000 / 4250000000
49	20	40	15	8212.5	1	8212.5	205	1328125000 / 4250000000
50	20	40	15	8275	1	8275	206	3718750000 / 4250000000
51	20	40	15	8300	1	8300	207	2125000000 / 4250000000
52	20	40	15	8400	1	8400	210	0 / 4250000000
53	20	40	15	8450	1	8450	211	1062500000 / 4250000000
54	20	40	15	8460	1	8460	211	2125000000 / 4250000000
55	20	40	15	8484	1	8484	212	425000000 / 4250000000
56	20	40	15	8496	1	8496	212	1700000000 / 4250000000
57	20	40	15	8212	1	8212	205	1275000000 / 4250000000
58	10	20	15	12860	1	12860	643	0 / 4250000000
59	10	20	15	13000	1	13000	650	0 / 4250000000
60	10	20	15	13022.5	1	13022.5	651	531250000 / 4250000000
61	10	20	15	13125	1	13125	656	1062500000 / 4250000000
62	10	20	15	13222.5	1	13222.5	661	531250000 / 4250000000
63	20	40	15	12209.697	1	12209.697	305	1030306250 / 4250000000
64	10	20	15	13390	1	13390	669	2125000000 / 4250000000
65	10	20	15	13417.5	1	13417.5	670	3718750000 / 4250000000
66	20	40	15	12689.697	1	12689.697	317	1030412500 / 4250000000
67	20	40	15	13906.667	1	13906.667	347	2833368750 / 4250000000
68	20	40	15	14192.727	1	14192.727	354	3477243750 / 4250000000
69	10	20	15	8212.5	1	8212.5	410	2656250000 / 4250000000
70	100	50	15	1250	8	10000	200	0 / 4250000000
71	50	100	15	1250	8	10000	100	0 / 4250000000
72	18.75	37.5	15	1875	6	11250	300	0 / 4250000000

6.4 Device Functional Modes

Table 6-16. Device Functional Modes

MODE	DESCRIPTION	SOFTWARE SETTINGS
RESET	Registers are held in the reset state. This device does have a power on reset, but good practice is to also do a software reset if there is any possibility of noise on the programming lines, especially if there is sharing with other devices. Also realize that there are registers not disclosed in the data sheet that are reset as well.	RESET = 1 POWERDOWN = 0
POWERDOWN	Device is powered down.	POWERDOWN = 1 or CAL Pin = Low
Pin Mode	Device settings are determined by pin states.	One of FS0, FS1, ... FS7 pins is NOT low
Normal operating mode	This is used with at least one output on as a frequency synthesizer and the device can be controlled through the SPI	ALL of FS0, FS1, ... FS7 pins are low
SYNC mode	This is used where part of the channel divider is in the feedback path to provide deterministic phase.	VCO_PHASE_SYNC = 1
SYSREF mode	In this mode, RFoutB is used to generate pulses for SYSREF.	VCO_PHASE_SYNC =1, SYSREF_EN = 1

6.5 Programming

When not in pin mode, the LMX2615-SP is programmed using 24-bit shift registers. The shift register consists of a R/W bit (MSB), followed by a 7-bit address field and a 16-bit data field. For the R/W bit, 0 is for write, and 1 is for read. The address field ADDRESS[6:0] is used to decode the internal register address. The remaining 16 bits form the data field DATA[15:0]. While CSB is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). See Figure 5-2 for timing details.

6.5.1 Recommended Initial Power-Up Sequence

For the most reliable programming, TI recommends this procedure:

1. Apply power to device.
2. Program RESET = 1 to reset registers.
3. Program registers as shown in the register map in **REVERSE** order from highest to lowest.
   - Programming of register R114 is only needed one wants to change the default states for WD_CNTRL or WD_DLY.
   - Programming of registers R113 down to R76 is not required, but if the registers are programmed, the registers must be done so as the register map shows.
   - Programming of registers R75 down to R0 (with FCAL_EN = 1) is required, unless otherwise specified.
   - Make sure R0 with FCAL_EN = 1 is the last programmed register in this step, otherwise the VCO does not get calibrated.
4. Wait 10ms to verify the internal LDOs have settled down.
5. Program register R0 one additional time with FCAL_EN = 1 to verify that the VCO calibration runs from a stable state.

6.5.2 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies is as follows:

1. Change frequency related registers such as PLL_N and PLL_NUM.
2. Program any necessary registers such as PFD_DLY_SEL.
3. Program FCAL_EN = 1 to calibrate the VCO.

6.6 Register Maps

6.6.1 Register Map

Table 6-17. Complete Register Map Table

REG	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	POR
R0	0	VCO_PHASE_SYNC	1	0	0	0	OUT_MUTE	FCAL_HPFD_ADJ		0	0	1	FCAL_EN	MUXOUT_LD_SEL	RESET	POWER DOWN	0x241C
R1	0	0	0	0	1	0	0	0	0	0	0	0	MUXOUT_CTRL	CAL_CLK_DIV			0x80C
R2	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0x500
R3	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0x642
R4	0	0	0	0	1	1	1	0	0	1	0	0	0	0	1	1	0xE43
R5	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0x3E8
R6	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0x7802
R7	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0	0xB2
R8	0	VCO_DACISET_FORCE	1	0	VCO_CAPCTRL_FORCE	0	0	0	0	0	0	0	0	0	0	0	0x2000
R9	0	0	0	OSC_2X	0	1	1	0	0	0	0	0	0	1	0	0	0x1604
R10	0	0	0	1	0	0	0	0	1	1	0	1	1	0	0	0	0x10D8
R11	0	0	0	0	PLL_R								1	0	0	0	0x18
R12	0	1	0	1	0	0	0	0	PLL_R_PRE								0x5001
R13	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x4000
R14	0	0	0	1	1	1	1	0	0	CPG			0	0	0	0	0x1E70
R15	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	0x64F
R16	0	0	0	0	0	0	0	VCO_DACISET									0x80
R17	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0x12C
R18	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0x64
R19	0	0	1	0	0	1	1	1	VCO_CAPCTRL								0x27B7
R20	1	1	VCO_SEL			VCO_SEL_FORCE	0	0	0	1	0	0	1	0	0	0	0xF848
R21	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0x401
R22	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0x1
R23	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0x7C
R24	0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	0	0x71A
R25	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0	0x624
R26	0	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	0xDB0
R27	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0x2
R28	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0x488
R29	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0	0x318C
R30	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0	0x318C
R31	0	SEG1_EN	0	0	0	0	1	1	1	1	1	0	1	1	0	0	0x43EC
R32	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1	0x393
R33	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1	0x1E21
R34	0	0	0	0	0	0	0	0	0	0	0	0	0	PLL_N[18:16]			0x0
R35	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0x4
R36	PLL_N[15:0]																0x46
R37	1	0	PFD_DLY_SEL						0	0	0	0	0	1	0	0	0x404
R38	PLL_DEN[31:16]																0xFD51
R39	PLL_DEN[15:0]																0xDA80
R40	MASH_SEED[31:16]																0x0
R41	MASH_SEED[15:0]																0x0
R42	PLL_NUM[31:16]																0x0
R43	PLL_NUM[15:0]																0x0
R44	0	0	OUTA_PWR						OUTB_PD	OUTA_PD	MASH_RESET_N	0	0	MASH_ORDER			0x1FA3

Table 6-17. Complete Register Map Table (continued)

REG	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	POR
R45	1	1	0	OUTA_MUX		0	0	0	1	1	OUTB_PWR						0xC8DF
R46	0	0	0	0	0	1	1	1	1	1	1	1	1	1	OUTB_MUX		0x7FD
R47	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0x300
R48	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0x300
R49	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0x4180
R50	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R51	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0x80
R52	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0x420
R53	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R54	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R55	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R56	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R57	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0x20
R58	INPIN_ IGNORE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0x8001
R59	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD_ TYPE	0x1
R60	LD_DLY																0x9C4
R61	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0xA8
R62	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	0x322
R63	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R64	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0x1388
R65	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R66	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0x1F4
R67	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R68	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0x3E8
R69	MASH_RST_COUNT[31:16]																0x0
R70	MASH_RST_COUNT[15:0]																0xC350
R71	0	0	0	0	0	0	0	0	SYSREF_DIV_PRE			SYSREF _PULSE	SYSREF _EN	SYSREF_ REPEAT	0	0	0x80
R72	0	0	0	0	0	SYSREF_DIV											0x1
R73	0	0	0	0	JESD_DAC2_CTRL						JESD_DAC1_CTRL						0x3F
R74	SYSREF_PULSE_CNT				JESD_DAC4_CTRL						JESD_DAC3_CTRL						0x0
R75	0	0	0	0	1	CHDIV					0	0	0	0	0	0	0x800
R76	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0xC
R77	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R78	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0x64
R79	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R80	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R81	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R82	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R83	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R84	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R85	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R86	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R87	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R88	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R89	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R90	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R91	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R92	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R93	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R94	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R95	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R96	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R97	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0

Table 6-17. Complete Register Map Table (continued)

REG	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	POR
R98	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R99	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R100	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R101	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R102	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R103	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R104	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0
R105	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0x4440
R106	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0x7
R107	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Read
R108	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Read
R109	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Read
R110	0	0	0	0	0	rb_LD_VTUNE		-	rb_VCO_SEL			-	-	-	-	-	Read
R111	0	0	0	0	0	0	0	0	rb_VCO_CAPCTRL								Read
R112	0	0	0	0	0	0	0	rb_VCO_DACISET									Read
R113	rb_IO_STATUS																Read
R114	0	0	0	0	0	0	WD_DLY							WD_CNTRL			0x26F

Table 6-18 lists the memory-mapped registers for the Device registers.

Table 6-18. Device Registers

Offset	Acronym	Register Name	Section
0x0	R0		Go
0x1	R1		Go
0x2	R2		Go
0x3	R3		Go
0x4	R4		Go
0x5	R5		Go
0x6	R6		Go
0x7	R7		Go
0x8	R8		Go
0x9	R9		Go
0xA	R10		Go
0xB	R11		Go
0xC	R12		Go
0xD	R13		Go
0xE	R14		Go
0xF	R15		Go
0x10	R16		Go
0x11	R17		Go
0x12	R18		Go
0x13	R19		Go
0x14	R20		Go
0x15	R21		Go
0x16	R22		Go

Table 6-18. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x17	R23		Go
0x18	R24		Go
0x19	R25		Go
0x1A	R26		Go
0x1B	R27		Go
0x1C	R28		Go
0x1D	R29		Go
0x1E	R30		Go
0x1F	R31		Go
0x20	R32		Go
0x21	R33		Go
0x22	R34		Go
0x23	R35		Go
0x24	R36		Go
0x25	R37		Go
0x26	R38		Go
0x27	R39		Go
0x28	R40		Go
0x29	R41		Go
0x2A	R42		Go
0x2B	R43		Go
0x2C	R44		Go
0x2D	R45		Go
0x2E	R46		Go
0x2F	R47		Go
0x30	R48		Go
0x31	R49		Go
0x32	R50		Go
0x33	R51		Go
0x34	R52		Go
0x35	R53		Go
0x36	R54		Go
0x37	R55		Go
0x38	R56		Go
0x39	R57		Go
0x3A	R58		Go
0x3B	R59		Go
0x3C	R60		Go

Table 6-18. Device Registers (continued)

Offset	Acronym	Register Name	Section
0x3D	R61		Go
0x3E	R62		Go
0x3F	R63		Go
0x40	R64		Go
0x41	R65		Go
0x42	R66		Go
0x43	R67		Go
0x44	R68		Go
0x45	R69		Go
0x46	R70		Go
0x47	R71		Go
0x48	R72		Go
0x49	R73		Go
0x4A	R74		Go
0x4B	R75		Go
0x4C	R76		Go
0x4D	R77		Go
0x4E	R78		Go
0x4F - 0x68	R79 - R104		Go
0x69	R105		Go
0x6A	R106		Go
0x6B - 0x6D	R107 - R109		Go
0x6E	R110		Go
0x6F	R111		Go
0x70	R112		Go
0x71	R113		Go
0x72	R114		Go

Complex bit access types are encoded to fit into small table cells. Table 6-19 shows the codes that are used for access types in this section.

Table 6-19. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset

6.6.1.1 R0 Register (Offset = 0x0) [reset = 0x241C]

R0 is shown in Figure 6-9 and described in Table 6-20.

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Figure 6-9. R0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	VCO_PHASE_SYNC	RESERVED				OUT_MUTE	FCAL_HPFD_ADJ		RESERVED			FCAL_EN	MUXOUT_LD_SEL	RESET	POWERDOWN
R/W-0x0	R/W-0x0	R/W-0x9				R/W-0x0	R/W-0x0		R/W-0x1			R/W-0x1	R/W-0x1	R/W-0x0	R/W-0x0

Table 6-20. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0x0	Program 0x0 to this field.
14	VCO_PHASE_SYNC	R/W	0x0	Phase Sync Mode Enable. In this state, part of the channel divider is put in the feedback path to provide deterministic phase. The action of toggling this bit from 0 to 1 also sends an asynchronous SYNC pulse. 0: Normal operation 1: Phase SYNC enabled
13 - 10	RESERVED	R/W	0x9	Program 0x8 to this field.
9	OUT_MUTE	R/W	0x0	Mute output (RFOUTA/B) during VCO calibration. 0: No mute 1: Mute enabled
8 - 7	FCAL_HPFD_ADJ	R/W	0x0	Adjustment to decrease the f_{PD} frequency for use in VCO calibration. $f_{PD\_CAL} = f_{PD} / 2^{FCAL\_HPFD\_ADJ}$ 0: $f_{PD} \leq 50MHz$ 1: $50MHz < f_{PD} \leq 100MHz$ 2: $100MHz < f_{PD} \leq 200MHz$ 3: $f_{PD} > 200MHz$
6 - 4	RESERVED	R/W	0x1	Program 0x1 to this field.
3	FCAL_EN	R/W	0x1	Writing register R0 with this bit set to a '1' enables and triggers the VCO calibration. 0: No calibration 1: Calibration enabled
2	MUXOUT_LD_SEL	R/W	0x1	Selects the functionality of the MUXout pin. 0: Register read back 1: Lock detect
1	RESET	R/W	0x0	Register reset. This resets all registers and state machines. Program RESET = 1 after Vcc power up to provide consistent performance. 0: Normal operation 1: Reset
0	POWERDOWN	R/W	0x0	Powers down device. 0: Normal operation 1: Powered down

6.6.1.2 R1 Register (Offset = 0x1) [reset = 0x80C]

R1 is shown in Figure 6-10 and described in Table 6-21.

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Figure 6-10. R1 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												MUXOUT_CTRL	CAL_CLK_DIV		
R/W-0x80												R/W-0x1	R/W-0x4		

Table 6-21. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R/W	0x80	Program 0x80 to this field.
3	MUXOUT_CTRL	R/W	0x1	Sets the MUXOUT pin status. 0: Tri-state 1: Normal operation
2 - 0	CAL_CLK_DIV	R/W	0x4	Divides down the f_{OSC} frequency to the state machine clock frequency (f_{SM}). $f_{SM} = f_{OSC} / 2^{CAL\_CLK\_DIV}$. Verify that the state machine clock frequency is 50MHz or less. 0: $f_{OSC} \leq$ 50MHz 1: 50MHz < $f_{OSC} \leq$ 100MHz 2: 100MHz < $f_{OSC} \leq$ 200MHz 3: 200MHz < $f_{OSC} \leq$ 400MHz 4: 400MHz < $f_{OSC} \leq$ 800MHz 5: f_{OSC} > 800MHz

6.6.1.3 R2 Register (Offset = 0x2) [reset = 0x500]

R2 is shown in Figure 6-11 and described in Table 6-22.

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Figure 6-11. R2 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x500															

Table 6-22. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x500	Program 0x500 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.4 R3 Register (Offset = 0x3) [reset = 0x642]

R3 is shown in Figure 6-12 and described in Table 6-23.

Return to Summary Table.

Figure 6-12. R3 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x642															

Table 6-23. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x642	Program 0x642 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.5 R4 Register (Offset = 0x4) [reset = 0xE43]

R4 is shown in Figure 6-13 and described in Table 6-24.

Return to Summary Table.

Figure 6-13. R4 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0xE43															

Table 6-24. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0xE43	Program 0xE43 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.6 R5 Register (Offset = 0x5) [reset = 0x3E8]

R5 is shown in Figure 6-14 and described in Table 6-25.

Return to Summary Table.

Figure 6-14. R5 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x3E8															

Table 6-25. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x3E8	Program 0x3E8 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.7 R6 Register (Offset = 0x6) [reset = 0x7802]

R6 is shown in Figure 6-15 and described in Table 6-26.

Return to Summary Table.

Figure 6-15. R6 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x7802															

Table 6-26. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x7802	Program 0x7802 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.8 R7 Register (Offset = 0x7) [reset = 0xB2]

R7 is shown in Figure 6-16 and described in Table 6-27.

Return to Summary Table.

Figure 6-16. R7 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0xB2															

Table 6-27. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0xB2	Program 0xB2 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.9 R8 Register (Offset = 0x8) [reset = 0x2000]

R8 is shown in Figure 6-17 and described in Table 6-28.

Return to Summary Table.

Figure 6-17. R8 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 6-17. R8 Register (continued)

RESERVED	VCO_DACISET_FORCE	RESERVED	VCO_CAPCTRL_FORCE	RESERVED
R/W-0x0	R/W-0x0	R/W-0x2	R/W-0x0	R/W-0x0

Table 6-28. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0x0	Program 0x0 to this field.
14	VCO_DACISET_FORCE	R/W	0x0	Forces VCO_DACISET Value. Useful for fully assisted VCO calibration and debugging purposes. 0: Normal operation 1: Use VCO_DACISET value instead of the value obtained from VCO calibration.
13 - 12	RESERVED	R/W	0x2	Program 0x2 to this field.
11	VCO_CAPCTRL_FORCE	R/W	0x0	Forces VCO_CAPCTRL value. Useful for fully assisted VCO calibration and debugging purposes. 0: Normal operation 1: Use VCO_CAPCTRL value instead of the value obtained from VCO calibration.
10 - 0	RESERVED	R/W	0x0	Program 0x0 to this field.

6.6.1.10 R9 Register (Offset = 0x9) [reset = 0x1604]

R9 is shown in Figure 6-18 and described in Table 6-29.

Return to Summary Table.

Figure 6-18. R9 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			OSC_2X	RESERVED											
R/W-0x0			R/W-0x1	R/W-0x604											

Table 6-29. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	R/W	0x0	Program 0x0 to this field.
12	OSC_2X	R/W	0x1	Reference path Doubler 0: Disabled 1: Enabled
11 - 0	RESERVED	R/W	0x604	Program 0x604 to this field.

6.6.1.11 R10 Register (Offset = 0xA) [reset = 0x10D8]

R10 is shown in Figure 6-19 and described in Table 6-30.

Return to Summary Table.

Figure 6-19. R10 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x10D8															

Table 6-30. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x10D8	Program 0x10D8 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.12 R11 Register (Offset = 0xB) [reset = 0x18]

R11 is shown in Figure 6-20 and described in Table 6-31.

Return to Summary Table.

Figure 6-20. R11 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PLL_R								RESERVED			
R/W-0x0				R/W-0x1								R/W-0x8			

Table 6-31. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R/W	0x0	Program 0x0 to this field.
11 - 4	PLL_R	R/W	0x1	Reference path Post-R divider. This is the divider after the Pre-R divider.
3 - 0	RESERVED	R/W	0x8	Program 0x8 to this field.

6.6.1.13 R12 Register (Offset = 0xC) [reset = 0x5001]

R12 is shown in Figure 6-21 and described in Table 6-32.

Return to Summary Table.

Figure 6-21. R12 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PLL_R_PRE							
R/W-0x50								R/W-0x1							

Table 6-32. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R/W	0x50	Program 0x50 to this field.
7 - 0	PLL_R_PRE	R/W	0x1	PLL Pre-R divider value.

6.6.1.14 R13 Register (Offset = 0xD) [reset = 0x4000]

R13 is shown in Figure 6-22 and described in Table 6-33.

Return to Summary Table.

Figure 6-22. R13 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x4000															

Table 6-33. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x4000	Program 0x4000 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.15 R14 Register (Offset = 0xE) [reset = 0x1E70]

R14 is shown in Figure 6-23 and described in Table 6-34.

Return to Summary Table.

Figure 6-23. R14 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									CPG			RESERVED			
R/W-0x3C									R/W-0x7			R/W-0x0			

Table 6-34. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 7	RESERVED	R/W	0x3C	Program 0x3C to this field.

Table 6-34. R14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6 - 4	CPG	R/W	0x7	Effective charge pump gain . This is the sum of the up and down currents. 0: 0mA 1: 6mA 2: Reserved 3: 12mA 4: 3mA 5: 9mA 6: Reserved 7: 15mA
3 - 0	RESERVED	R/W	0x0	Program 0x0 to this field.

6.6.1.16 R15 Register (Offset = 0xF) [reset = 0x64F]

R15 is shown in Figure 6-24 and described in Table 6-35.

Return to Summary Table.

Figure 6-24. R15 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x64F															

Table 6-35. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x64F	Program 0x64F to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.17 R16 Register (Offset = 0x10) [reset = 0x80]

R16 is shown in Figure 6-25 and described in Table 6-36.

Return to Summary Table.

Figure 6-25. R16 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							VCO_DACISET								
R/W-0x0							R/W-0x80								

Table 6-36. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	R/W	0x0	Program 0x0 to this field.
8 - 0	VCO_DACISET	R/W	0x80	Programmable current setting for the VCO that is applied when VCO_DACISET_FORCE = 1.

6.6.1.18 R17 Register (Offset = 0x11) [reset = 0x12C]

R17 is shown in Figure 6-26 and described in Table 6-37.

Return to Summary Table.

Figure 6-26. R17 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x12C															

Table 6-37. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x12C	Program 0x12C to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.19 R18 Register (Offset = 0x12) [reset = 0x64]

R18 is shown in Figure 6-27 and described in Table 6-38.

Return to Summary Table.

Figure 6-27. R18 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x64															

Table 6-38. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x64	Program 0x64 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.20 R19 Register (Offset = 0x13) [reset = 0x27B7]

R19 is shown in Figure 6-28 and described in Table 6-39.

Return to Summary Table.

Figure 6-28. R19 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VCO_CAPCTRL							
R/W-0x27								R/W-0xB7							

Table 6-39. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R/W	0x27	Program 0x27 to this field.
7 - 0	VCO_CAPCTRL	R/W	0xB7	Programmable band within VCO core that applies when VCO_CAPCTRL_FORCE = 1. Valid values are 183 to 0, where the higher number is a lower frequency.

6.6.1.21 R20 Register (Offset = 0x14) [reset = 0xF848]

R20 is shown in Figure 6-29 and described in Table 6-40.

Return to Summary Table.

Figure 6-29. R20 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		VCO_SEL			VCO_SEL_FORCE	RESERVED									
R/W-0x3		R/W-0x7			R/W-0x0	R/W-0x48									

Table 6-40. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	RESERVED	R/W	0x3	Program 0x3 to this field.

Table 6-40. R20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13 - 11	VCO_SEL	R/W	0x7	User specified start VCO for calibration. Also is the VCO core that is forced by VCO_SEL_FORCE = 1. 0: Reserved 1: VCO1 2: VCO2 ….. 7: VCO7
10	VCO_SEL_FORCE	R/W	0x0	Forces the VCO to use the core specified by VCO_SEL value. 0: Disabled 1: Enabled
9 - 0	RESERVED	R/W	0x48	Program 0x48 to this field.

6.6.1.22 R21 Register (Offset = 0x15) [reset = 0x401]

R21 is shown in Figure 6-30 and described in Table 6-41.

Return to Summary Table.

Figure 6-30. R21 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x401															

Table 6-41. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x401	Program 0x401 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.23 R22 Register (Offset = 0x16) [reset = 0x1]

R22 is shown in Figure 6-31 and described in Table 6-42.

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Figure 6-31. R22 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x1															

Table 6-42. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x1	Program 0x1 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.24 R23 Register (Offset = 0x17) [reset = 0x7C]

R23 is shown in Figure 6-32 and described in Table 6-43.

Return to Summary Table.

Figure 6-32. R23 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x7C															

Table 6-43. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x7C	Program 0x7C to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.25 R24 Register (Offset = 0x18) [reset = 0x71A]

R24 is shown in Figure 6-33 and described in Table 6-44.

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Figure 6-33. R24 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x71A															

Table 6-44. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x71A	Program 0x71A to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.26 R25 Register (Offset = 0x19) [reset = 0x624]

R25 is shown in Figure 6-34 and described in Table 6-45.

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Figure 6-34. R25 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x624															

Table 6-45. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x624	Program 0x624 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.27 R26 Register (Offset = 0x1A) [reset = 0xDB0]

R26 is shown in Figure 6-35 and described in Table 6-46.

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Figure 6-35. R26 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0xDB0															

Table 6-46. R26 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0xDB0	Program 0xDB0 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.28 R27 Register (Offset = 0x1B) [reset = 0x2]

R27 is shown in Figure 6-36 and described in Table 6-47.

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Figure 6-36. R27 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 6-36. R27 Register (continued)

RESERVED
R/W-0x2

Table 6-47. R27 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x2	Program 0x2 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.29 R28 Register (Offset = 0x1C) [reset = 0x488]

R28 is shown in Figure 6-37 and described in Table 6-48.

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Figure 6-37. R28 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x488															

Table 6-48. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x488	Program 0x488 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.30 R29 Register (Offset = 0x1D) [reset = 0x318C]

R29 is shown in Figure 6-38 and described in Table 6-49.

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Figure 6-38. R29 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x318C															

Table 6-49. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x318C	Program 0x318C to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.31 R30 Register (Offset = 0x1E) [reset = 0x318C]

R30 is shown in Figure 6-39 and described in Table 6-50.

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Figure 6-39. R30 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x318C															

Table 6-50. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x318C	Program 0x318C to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.32 R31 Register (Offset = 0x1F) [reset = 0x43EC]

R31 is shown in Figure 6-40 and described in Table 6-51.

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Figure 6-40. R31 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	SEG1_EN	RESERVED													
R/W-0x0	R/W-0x1	R/W-0x3EC													

Table 6-51. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0x0	Program 0x0 to this field.
14	SEG1_EN	R/W	0x1	Enables SEG1 when channel divider is engaged. 0: Disabled (only valid when CHDIV = 0x0 (Divide by 2) and not in SYNC mode) 1: Enabled (use for other CHDIV values)
13 - 0	RESERVED	R/W	0x3EC	Program 0x3EC to this field.

6.6.1.33 R32 Register (Offset = 0x20) [reset = 0x393]

R32 is shown in Figure 6-41 and described in Table 6-52.

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Figure 6-41. R32 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x393															

Table 6-52. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x393	Program 0x393 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.34 R33 Register (Offset = 0x21) [reset = 0x1E21]

R33 is shown in Figure 6-42 and described in Table 6-53.

Return to Summary Table.

Figure 6-42. R33 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x1E21															

Table 6-53. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x1E21	Program 0x1E21 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.35 R34 Register (Offset = 0x22) [reset = 0x0]

R34 is shown in Figure 6-43 and described in Table 6-54.

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Figure 6-43. R34 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PLL_N[18:16]	
R/W-0x0														R/W-0x0	

Table 6-54. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 3	RESERVED	R/W	0x0	Program 0x0 to this field.
2 - 0	PLL_N[18:16]	R/W	0x0	Upper 3 bits of N-divider, total 19 bits, split as 16 + 3.

6.6.1.36 R35 Register (Offset = 0x23) [reset = 0x4]

R35 is shown in Figure 6-44 and described in Table 6-55.

Return to Summary Table.

Figure 6-44. R35 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x4															

Table 6-55. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x4	Program 0x4 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.37 R36 Register (Offset = 0x24) [reset = 0x46]

R36 is shown in Figure 6-45 and described in Table 6-56.

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Figure 6-45. R36 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_N[15:0]															
R/W-0x46															

Table 6-56. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PLL_N[15:0]	R/W	0x46	PLL N divider value.

6.6.1.38 R37 Register (Offset = 0x25) [reset = 0x404]

R37 is shown in Figure 6-46 and described in Table 6-57.

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Figure 6-46. R37 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PFD_DLY_SEL						RESERVED							
R/W-0x0		R/W-0x4						R/W-0x4							

Table 6-57. R37 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	RESERVED	R/W	0x0	Program 0x2 to this field.
13 - 8	PFD_DLY_SEL	R/W	0x4	PFD_DLY_SEL must be adjusted in accordance to the N-divider value. See Table 6-2 for details.
7 - 0	RESERVED	R/W	0x4	Program 0x4 to this field.

6.6.1.39 R38 Register (Offset = 0x26) [reset = 0xFD51]

R38 is shown in Figure 6-47 and described in Table 6-58.

Return to Summary Table.

Figure 6-47. R38 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN[31:16]															
R/W-0xFD51															

Table 6-58. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PLL_DEN[31:16]	R/W	0xFD51	Fractional denominator(MSB).

6.6.1.40 R39 Register (Offset = 0x27) [reset = 0xDA80]

R39 is shown in Figure 6-48 and described in Table 6-59.

Return to Summary Table.

Figure 6-48. R39 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN[15:0]															
R/W-0xDA80															

Table 6-59. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PLL_DEN[15:0]	R/W	0xDA80	Fractional denominator.

6.6.1.41 R40 Register (Offset = 0x28) [reset = 0x0]

R40 is shown in Figure 6-49 and described in Table 6-60.

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Figure 6-49. R40 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_SEED[31:16]															
R/W-0x0															

Table 6-60. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	MASH_SEED[31:16]	R/W	0x0	MASH_SEED(MSB).

6.6.1.42 R41 Register (Offset = 0x29) [reset = 0x0]

R41 is shown in Figure 6-50 and described in Table 6-61.

Return to Summary Table.

Figure 6-50. R41 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_SEED[15:0]															
R/W-0x0															

Table 6-61. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	MASH_SEED[15:0]	R/W	0x0	Sets the initial state of the fractional engine. Useful for producing a phase shift and fractional spur optimization.

6.6.1.43 R42 Register (Offset = 0x2A) [reset = 0x0]

R42 is shown in Figure 6-51 and described in Table 6-62.

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Figure 6-51. R42 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_NUM[31:16]															
R/W-0x0															

Table 6-62. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PLL_NUM[31:16]	R/W	0x0	Fractional numerator (MSB).

6.6.1.44 R43 Register (Offset = 0x2B) [reset = 0x0]

R43 is shown in Figure 6-52 and described in Table 6-63.

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Figure 6-52. R43 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_NUM[15:0]															
R/W-0x0															

Table 6-63. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PLL_NUM[15:0]	R/W	0x0	Fractional numerator.

6.6.1.45 R44 Register (Offset = 0x2C) [reset = 0x1FA3]

R44 is shown in Figure 6-53 and described in Table 6-64.

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Figure 6-53. R44 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		OUTA_PWR						OUTB_PD	OUTA_PD	MASH_RESET_N	RESERVED		MASH_ORDER		
R/W-0x0		R/W-0x1F						R/W-0x1	R/W-0x0	R/W-0x1	R/W-0x0		R/W-0x3		

Table 6-64. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	RESERVED	R/W	0x0	Program 0x0 to this field.
13 - 8	OUTA_PWR	R/W	0x1F	Sets current that controls output power for output A. 0 is minimum current.
7	OUTB_PD	R/W	0x1	Powers down output B. 0: Normal operation 1: Power down
6	OUTA_PD	R/W	0x0	Powers down output A. 0: Normal operation 1: Power down
5	MASH_RESET_N	R/W	0x1	Active low reset for MASH. 0: Reset 1: Normal operation
4 - 3	RESERVED	R/W	0x0	Program 0x0 to this field.
2 - 0	MASH_ORDER	R/W	0x3	Sets the MASH order. 0: Integer mode 1: First order modulator 2: Second order modulator 3: Third order modulator 4: Fourth order modulator 5 - 7: Reserved

6.6.1.46 R45 Register (Offset = 0x2D) [reset = 0xC8DF]

R45 is shown in Figure 6-54 and described in Table 6-65.

Return to Summary Table.

Figure 6-54. R45 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			OUTA_MUX		RESERVED					OUTB_PWR					
R/W-0x6			R/W-0x1		R/W-0x3					R/W-0x1F					

Table 6-65. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	R/W	0x6	Program 0x6 to this field.
12 - 11	OUTA_MUX	R/W	0x1	Selects input to OUTA output. 0: Channel divider 1: VCO 2: Reserved 3: Reserved
10 - 6	RESERVED	R/W	0x3	Program 0x3 to this field.
5 - 0	OUTB_PWR	R/W	0x1F	Sets current that controls output power for output B. 0 is minimum current.

6.6.1.47 R46 Register (Offset = 0x2E) [reset = 0x7FD]

R46 is shown in Figure 6-55 and described in Table 6-66.

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Figure 6-55. R46 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														OUTB_MUX	
R/W-0x1FF														R/W-0x1	

Table 6-66. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 2	RESERVED	R/W	0x1FF	Program 0x1FF to this field.
1 - 0	OUTB_MUX	R/W	0x1	Selects input to the OUTB output. 0: Channel divider 1: VCO 2: SYSREF 3: Reserved

6.6.1.48 R47 Register (Offset = 0x2F) [reset = 0x300]

R47 is shown in Figure 6-56 and described in Table 6-67.

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Figure 6-56. R47 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x300															

Table 6-67. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x300	Program 0x300 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.49 R48 Register (Offset = 0x30) [reset = 0x300]

R48 is shown in Figure 6-57 and described in Table 6-68.

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Figure 6-57. R48 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x300															

Table 6-68. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x300	Program 0x300 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.50 R49 Register (Offset = 0x31) [reset = 0x4180]

R49 is shown in Figure 6-58 and described in Table 6-69.

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Figure 6-58. R49 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x4180															

Table 6-69. R49 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x4180	Program 0x4180 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.51 R50 Register (Offset = 0x32) [reset = 0x0]

R50 is shown in Figure 6-59 and described in Table 6-70.

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Figure 6-59. R50 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x0															

Table 6-70. R50 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x0	Program 0x0 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.52 R51 Register (Offset = 0x33) [reset = 0x80]

R51 is shown in Figure 6-60 and described in Table 6-71.

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Figure 6-60. R51 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x80															

Table 6-71. R51 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x80	Program 0x80 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.53 R52 Register (Offset = 0x34) [reset = 0x420]

R52 is shown in Figure 6-61 and described in Table 6-72.

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Figure 6-61. R52 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x420															

Table 6-72. R52 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x420	Program 0x420 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.54 R53 Register (Offset = 0x35) [reset = 0x0]

R53 is shown in Figure 6-62 and described in Table 6-73.

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Figure 6-62. R53 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x0															

Table 6-73. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x0	Program 0x0 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.55 R54 Register (Offset = 0x36) [reset = 0x0]

R54 is shown in Figure 6-63 and described in Table 6-74.

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Figure 6-63. R54 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x0															

Table 6-74. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x0	Program 0x0 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.56 R55 Register (Offset = 0x37) [reset = 0x0]

R55 is shown in Figure 6-64 and described in Table 6-75.

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Figure 6-64. R55 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 6-64. R55 Register (continued)

RESERVED
R/W-0x0

Table 6-75. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x0	Program 0x0 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.57 R56 Register (Offset = 0x38) [reset = 0x0]

R56 is shown in Figure 6-65 and described in Table 6-76.

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Figure 6-65. R56 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x0															

Table 6-76. R56 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x0	Program 0x0 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.58 R57 Register (Offset = 0x39) [reset = 0x20]

R57 is shown in Figure 6-66 and described in Table 6-77.

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Figure 6-66. R57 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x20															

Table 6-77. R57 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x20	Program 0x20 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.59 R58 Register (Offset = 0x3A) [reset = 0x8001]

R58 is shown in Figure 6-67 and described in Table 6-78.

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Figure 6-67. R58 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INPIN_IGNORE	RESERVED														
R/W-0x1	R/W-0x1														

Table 6-78. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INPIN_IGNORE	R/W	0x1	Ignores SYNC and SYSREF pins. This bit must be set to 1 unless VCO_PHASE_SYNC = 1. 0: SYNC and SYSREF pins are activated 1: SYNC and SYSREF pins are deactivated

Table 6-78. R58 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14 - 0	RESERVED	R/W	0x1	Program 0x1 to this field.

6.6.1.60 R59 Register (Offset = 0x3B) [reset = 0x1]

R59 is shown in Figure 6-68 and described in Table 6-79.

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Figure 6-68. R59 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															LD_TYPE
R/W-0x0															R/W-0x1

Table 6-79. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1	RESERVED	R/W	0x0	Program 0x0 to this field.
0	LD_TYPE	R/W	0x1	Defines Lock Detect Type. VCOCal Lock Detect asserts a high output after the VCO has finished calibration and the LD_DLY timeout counter is finished. Vtune and VCOCal Lock Detect asserts a high output when VCOCal lock detect asserts a signal and the tuning voltage to the VCO is within acceptable limits. RECAL feature requires using this lock detect type. 0: VCOCal Lock Detect 1: Vtune and VCOCal Lock Detect

6.6.1.61 R60 Register (Offset = 0x3C) [reset = 0x9C4]

R60 is shown in Figure 6-69 and described in Table 6-80.

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Figure 6-69. R60 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LD_DLY															
R/W-0x9C4															

Table 6-80. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	LD_DLY	R/W	0x9C4	For the VCOCal Lock Detect, this is the delay in state machine clock cycles that is added after the calibration is finished before the VCOCal Lock Detect is asserted high. Delay time = LD_DLY × 4 / f_{SM}.

6.6.1.62 R61 Register (Offset = 0x3D) [reset = 0xA8]

R61 is shown in Figure 6-70 and described in Table 6-81.

Return to Summary Table.

Figure 6-70. R61 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0xA8															

Table 6-81. R61 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0xA8	Program 0xA8 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.63 R62 Register (Offset = 0x3E) [reset = 0x322]

R62 is shown in Figure 6-71 and described in Table 6-82.

Return to Summary Table.

Figure 6-71. R62 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x322															

Table 6-82. R62 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x322	Program 0x322 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.64 R63 Register (Offset = 0x3F) [reset = 0x0]

R63 is shown in Figure 6-72 and described in Table 6-83.

Return to Summary Table.

Figure 6-72. R63 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x0															

Table 6-83. R63 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x0	Program 0x0 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.65 R64 Register (Offset = 0x40) [reset = 0x1388]

R64 is shown in Figure 6-73 and described in Table 6-84.

Return to Summary Table.

Figure 6-73. R64 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x1388															

Table 6-84. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x1388	Program 0x1388 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.66 R65 Register (Offset = 0x41) [reset = 0x0]

R65 is shown in Figure 6-74 and described in Table 6-85.

Return to Summary Table.

Figure 6-74. R65 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 6-74. R65 Register (continued)

RESERVED
R/W-0x0

Table 6-85. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x0	Program 0x0 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.67 R66 Register (Offset = 0x42) [reset = 0x1F4]

R66 is shown in Figure 6-75 and described in Table 6-86.

Return to Summary Table.

Figure 6-75. R66 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x1F4															

Table 6-86. R66 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x1F4	Program 0x1F4 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.68 R67 Register (Offset = 0x43) [reset = 0x0]

R67 is shown in Figure 6-76 and described in Table 6-87.

Return to Summary Table.

Figure 6-76. R67 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x0															

Table 6-87. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x0	Program 0x0 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.69 R68 Register (Offset = 0x44) [reset = 0x3E8]

R68 is shown in Figure 6-77 and described in Table 6-88.

Return to Summary Table.

Figure 6-77. R68 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x3E8															

Table 6-88. R68 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x3E8	Program 0x3E8 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.70 R69 Register (Offset = 0x45) [reset = 0x0]

R69 is shown in Figure 6-78 and described in Table 6-89.

Return to Summary Table.

Figure 6-78. R69 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_RST_COUNT[31:16]															
R/W-0x0															

Table 6-89. R69 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	MASH_RST_COUNT [31:16]	R/W	0x0	Upper 16 bits of MASH_RST_COUNT. This register is used to add a delay when using phase SYNC. The delay must be set at least four times the PLL lock time. This delay is expressed in state machine clock periods. One of these periods is equal to $2^{CAL\_CLK\_DIV} / f_{OSC}$.

6.6.1.71 R70 Register (Offset = 0x46) [reset = 0xC350]

R70 is shown in Figure 6-79 and described in Table 6-90.

Return to Summary Table.

Figure 6-79. R70 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_RST_COUNT[15:0]															
R/W-0xC350															

Table 6-90. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	MASH_RST_COUNT [15:0]	R/W	0xC350	Lower 16 bits of MASH_RST_COUNT.

6.6.1.72 R71 Register (Offset = 0x47) [reset = 0x80]

R71 is shown in Figure 6-80 and described in Table 6-91.

Return to Summary Table.

Figure 6-80. R71 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SYSREF_DIV_PRE			SYSREF_PULSE	SYSREF_EN	SYSREF_REPEAT	RESERVED	
R/W-0x0								R/W-0x4			R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	

Table 6-91. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R/W	0x0	Program 0x0 to this field.
7 - 5	SYSREF_DIV_PRE	R/W	0x4	This divider is used to get the frequency input to the SYSREF interpolator within acceptable limits. 1: Bypassed 2: Divide by 2 4: Divide by 4 All other values are reserved.
4	SYSREF_PULSE	R/W	0x0	When in master mode (SYSREF_REPEAT = 0), this allows multiple pulses (as determined by SYSREF_PULSE_CNT) to be sent out whenever the SysRefReq pin goes high. 0: Continuous SYSREF clock 1: SYSREF pulses

Table 6-91. R71 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SYSREF_EN	R/W	0x0	Enables SYSREF mode. SYSREF requires VCO_PHASE_SYNC = 1. 0: Disabled 1: Enabled
2	SYSREF_REPEAT	R/W	0x0	Defines the SYSREF mode. 0: Master mode. Pulses are generated at the output. 1: Repeater Mode. Pulses are generated in response to the SysRefReq pin.
1 - 0	RESERVED	R/W	0x0	Program 0x0 to this field.

6.6.1.73 R72 Register (Offset = 0x48) [reset = 0x1]

R72 is shown in Figure 6-81 and described in Table 6-92.

Return to Summary Table.

Figure 6-81. R72 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SYSREF_DIV										
R/W-0x0					R/W-0x1										

Table 6-92. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	R/W	0x0	Program 0x0 to this field.
10 - 0	SYSREF_DIV	R/W	0x1	This divider further divides the output frequency for the SYSREF.

6.6.1.74 R73 Register (Offset = 0x49) [reset = 0x3F]

R73 is shown in Figure 6-82 and described in Table 6-93.

Return to Summary Table.

Figure 6-82. R73 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				JESD_DAC2_CTRL						JESD_DAC1_CTRL					
R/W-0x0				R/W-0x0						R/W-0x3F					

Table 6-93. R73 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R/W	0x0	Program 0x0 to this field.
11 - 6	JESD_DAC2_CTRL	R/W	0x0	Programmable delay adjustment for SysRef mode.
5 - 0	JESD_DAC1_CTRL	R/W	0x3F	Programmable delay adjustment for SysRef mode.

6.6.1.75 R74 Register (Offset = 0x4A) [reset = 0x0]

R74 is shown in Figure 6-83 and described in Table 6-94.

Return to Summary Table.

Figure 6-83. R74 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYSREF_PULSE_CNT				JESD_DAC4_CTRL						JESD_DAC3_CTRL					
R/W-0x0				R/W-0x0						R/W-0x0					

Table 6-94. R74 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	SYSREF_PULSE_CNT	R/W	0x0	Used in SYSREF_REPEAT mode to define how many pulses are sent.
11 - 6	JESD_DAC4_CTRL	R/W	0x0	Programmable delay adjustment for SysRef mode.

Table 6-94. R74 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5 - 0	JESD_DAC3_CTRL	R/W	0x0	Programmable delay adjustment for SysRef mode.

6.6.1.76 R75 Register (Offset = 0x4B) [reset = 0x800]

R75 is shown in Figure 6-84 and described in Table 6-95.

Return to Summary Table.

Figure 6-84. R75 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					CHDIV					RESERVED					
R/W-0x1					R/W-0x0					R/W-0x0					

Table 6-95. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	R/W	0x1	Program 0x1 to this field.
10 - 6	CHDIV	R/W	0x0	Channel divider (equivalent division) controls divider value of each segment of the channel divider. 0: Divide by 2 1: Divide by 4 2: Divide by 6 3: Divide by 8 4: Divide by 12 5: Divide by 16 6: Divide by 24 7: Divide by 32 8: Divide by 48 9: Divide by 64 10: Divide by 96 11: Divide by 128 12: Divide by 192 All other values are reserved.
5 - 0	RESERVED	R/W	0x0	Program 0x0 to this field.

6.6.1.77 R76 Register (Offset = 0x4C) [reset = 0xC]

R76 is shown in Figure 6-85 and described in Table 6-96.

Return to Summary Table.

Figure 6-85. R76 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0xC															

Table 6-96. R76 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0xC	Program 0xC to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.78 R77 Register (Offset = 0x4D) [reset = 0x0]

R77 is shown in Figure 6-86 and described in Table 6-97.

Return to Summary Table.

Figure 6-86. R77 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x0															

Table 6-97. R77 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x0	Program 0x0 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.79 R78 Register (Offset = 0x4E) [reset = 0x64]

R78 is shown in Figure 6-87 and described in Table 6-98.

Return to Summary Table.

Figure 6-87. R78 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x64															

Table 6-98. R78 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x64	Program 0x64 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.80 R79 - R104 Register (Offset = 0x4F - 0x68) [reset = 0x0]

R79 - R104 is shown in Figure 6-88 and described in Table 6-99.

Return to Summary Table.

Figure 6-88. R79 - R104 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x0															

Table 6-99. R79 - R104 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x0	Program 0x0 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.81 R105 Register (Offset = 0x69) [reset = 0x4440]

R105 is shown in Figure 6-89 and described in Table 6-100.

Return to Summary Table.

Figure 6-89. R105 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x4440															

Table 6-100. R105 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x4440	Program 0x4440 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.82 R106 Register (Offset = 0x6A) [reset = 0x7]

R106 is shown in Figure 6-90 and described in Table 6-101.

Return to Summary Table.

Figure 6-90. R106 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0x7															

Table 6-101. R106 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R/W	0x7	Program 0x7 to this field. After programming R0 with RESET = 1, no need to program this register.

6.6.1.83 R107 - R109 Register (Offset = 0x6B - 0x6D) [Read only]

R107 - R109 is shown in Figure 6-91 and described in Table 6-102.

Return to Summary Table.

Figure 6-91. R107 - R109 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R															

Table 6-102. R107 - R109 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESERVED	R	-	Not used. Read back only.

6.6.1.84 R110 Register (Offset = 0x6E) [Read only]

R110 is shown in Figure 6-92 and described in Table 6-103.

Return to Summary Table.

Figure 6-92. R110 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					rb_LD_VTUNE		RESERVED	rb_VCO_SEL			RESERVED				
R-0x0					R		R-0x0	R			R-0x0				

Table 6-103. R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	R	0x0	Not used. Read back only.
10 - 9	rb_LD_VTUNE	R	-	Read back field for the lock detect. Applicable only when R0 is programmed at least one time with LD_TYPE = 1. 0: Unlocked (Fvco Low) 1: Invalid 2: Locked 3: Unlocked (Fvco High)
8	RESERVED	R	0x0	Not used. Read back only.
7 - 5	rb_VCO_SEL	R	-	Read back the actual VCO that the calibration has selected.
4 - 0	RESERVED	R	0x0	Not used. Read back only.

6.6.1.85 R111 Register (Offset = 0x6F) [Read only]

R111 is shown in Figure 6-93 and described in Table 6-104.

Return to Summary Table.

Figure 6-93. R111 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								rb_VCO_CAPCTRL							
R-0x0								R							

Table 6-104. R111 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R	0x0	Not used. Read back only.
7 - 0	rb_VCO_CAPCTRL	R	-	Read back field for the actual VCO_CAPCTRL value that is chosen by the VCO calibration.

6.6.1.86 R112 Register (Offset = 0x70) [Read only]

R112 is shown in Figure 6-94 and described in Table 6-105.

Return to Summary Table.

Figure 6-94. R112 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								rb_VCO_DACISET							
R-0x0								R							

Table 6-105. R112 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	R	0x0	Not used. Read back only.
8 - 0	rb_VCO_DACISET	R	-	Read back field for the actual VCO_DACISET value that is chosen by the VCO calibration.

6.6.1.87 R113 Register (Offset = 0x71) [Read only]

R113 is shown in Figure 6-95 and described in Table 6-106.

Return to Summary Table.

Figure 6-95. R113 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rb_IO_STATUS															
R															

Table 6-106. R113 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	rb_IO_STATUS	R	-	Reads back status of mode pins. Bit 0: RECAL_EN pin Bit 1: FS0 pin ….. Bit 8: FS7 pin

6.6.1.88 R114 Register (Offset = 0x72) [reset = 0x26F]

R114 is shown in Figure 6-96 and described in Table 6-107.

Return to Summary Table.

Figure 6-96. R114 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						WD_DLY							WD_CNTRL		
R-0x0						R/W-0x4D							R/W-0x7		

Table 6-107. R114 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R	0x0	Program 0x0 to this field.
9 - 3	WD_DLY	R/W	0x4D	Delay for the internal watchdog timer. Delay time = WD_DLY × 2^{14} / state machine clock frequency.
2 - 0	WD_CNTRL	R/W	0x7	Watchdog Control 0: Digital Watchdog disabled. 1: Watchdog triggers 1 time 2: Watchdog triggers up to 2 times 3: Watchdog triggers up to 3 times 4: Watchdog triggers up to 4 times 5: Watchdog triggers up to 5 times 6: Watchdog triggers up to 6 times 7: Watchdog retriggers as many times as necessary with no limit.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 OSCin Configuration

OSCin supports single-ended or differential clock. There must be a AC-coupling capacitor in series before the device pin. The OSCin inputs are high impedance CMOS with internal bias voltage. TI recommends putting termination shunt resistors to terminate the differential traces (if there are 50Ω characteristic traces, place 50Ω resistors). The OSCin and OSCin* side must be matched in layout. A series AC-coupling capacitor must immediately follow OSCin pins in the board layout, then the shunt termination resistors to ground must be placed after.

Input clock definitions are shown in Figure 7-1:

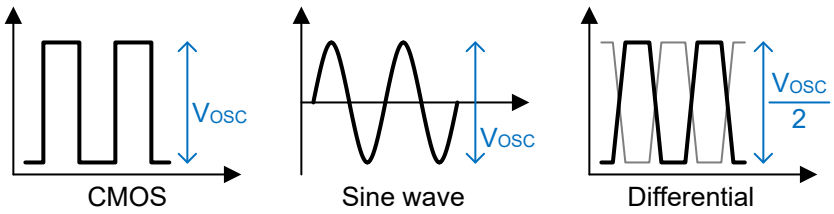

Figure 7-1. Input Clock Definitions

7.1.2 OSCin Slew Rate

The slew rate of the OSCin signal can have an impact on the spurs and phase noise of the LMX2615-SP if the rate is too low. In general, the best performance is for a high slew rate, but lower amplitude signal, such as LVDS.

7.1.3 RF Output Buffer Power Control

The OUTA_PWR and OUTB_PWR registers control the amount of drive current for the output. This current creates a voltage across the pullup component and load. Keep the OUTx_PWR setting at 31 or less as higher settings consume more current consumption and can also lead to higher output power. Optimal noise floor is typically obtained by setting OUTx_PWR in the range of 15 to 25.

7.1.4 RF Output Buffer Pullup

The choice of output buffer components is very important and can have a profound impact on the output power. The pullup component can be a resistor or inductor or combination thereof. The signal swing is created by a current flowing this pullup, so a higher impedance implies a higher signal swing. However, as this pullup component can be treated as if the component is in parallel with the load impedance, there are diminishing returns as the impedance gets much larger than the load impedance. The output impedance of the device varies as a function of frequency and is a complex number, but typically has a magnitude on the order of 100Ω, but this decreases with frequency.

The output can be used differentially or single-ended. If using single-ended, the pullup is still needed, and user needs to terminate the unused complimentary side such that the impedance as seen from the pin looking out is similar to the pin that is being used. Following are some typical components that can be useful.

Table 7-1. Output Pullup Configuration

COMPONENT	VALUE	PART NUMBER
Inductor	1nH, 13.6GHz SRF	Toko LL1005-FH1N0S
	3.3nH, 6.8GHz SRF	Toko LL1005-FH3N3S
	10nH, 3.8GHz SRF	Toko LL1005-FH10NU
Resistor	50Ω	Vishay FC0402E50R0BST1
Capacitor	Varies with frequency	ATC 520L103KT16T ATC 504L50R0FTNCFT

7.1.4.1 Resistor Pullup

One strategy for the choice of the pullup component is to use a resistor (R). This is typically chosen to be 50Ω and under the assumption that the part output impedance is high, then the output impedance is theoretically 50Ω, regardless of output frequency. As the output impedance of the device is not infinite, the output impedance when the pullup resistor is used is less than 50Ω, but reasonably close. There is some drop across the resistor, but this does not seem to have a large impact on signal swing for a 50Ω resistor provided that OUTx_PWR ≤ 31.

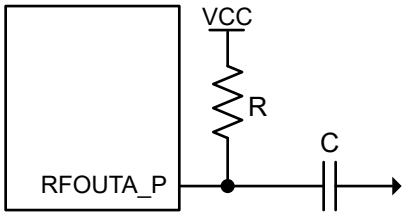

Figure 7-2. Resistor Pullup

7.1.4.2 Inductor Pullup

Another strategy is to select an inductor (L) pullup. This allows a higher impedance without any concern of creating any DC drop across the component. Ideally, the inductor must be chosen large enough so that the impedance is high relative to the load impedance and also be operating away from the self-resonant frequency. For instance, consider a 3.3nH pullup inductor with a self-resonant frequency of 7GHz driving a 50Ω spectrum analyzer input. This inductor theoretically has j50Ω input impedance around 2.4GHz. At this frequency, this in parallel with load is about 35Ω, which is a 3dB power reduction. At 1.4GHz, this inductor has impedance of about j29Ω. This in parallel with the 50Ω load has a magnitude of 25Ω, which is the same as with a 50Ω pullup. The main issue with the inductor pullup is the impedance does not look nicely matched to the load.

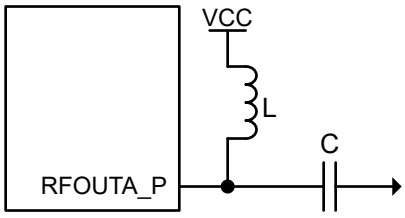

Figure 7-3. Inductor Pullup

As the output impedance is not so nicely matched, but there is higher output power, using a resistive pad is desired to get the best impedance control. A 6dB pad (R1 = 18Ω, R2 = 68Ω) is likely more attenuation than necessary. A 3dB or even 1dB pad can suffice. Two AC-coupling capacitor is required before the pad. In the configuration shown in Figure 7-4, one of them is placed to ground to minimize the number of components in the high frequency path for lower loss.

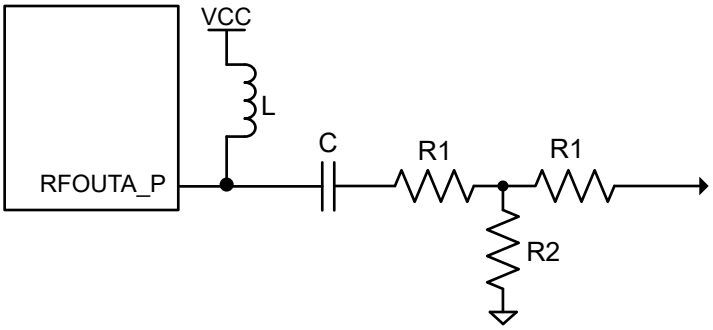

Figure 7-4. Inductor Pullup With Pad

For the resistive pad, Table 7-2 shows some common values:

Table 7-2. Resistive T-Pad Values

ATTENUATION (dB)	R1 (Ω)	R2 (Ω)
1	2.7	420
2	5.6	220
3	6.8	150
4	12	100
5	15	82
6	18	68

7.1.4.3 Combination Pullup

The resistor gives a good low frequency response, while the inductor gives a good high frequency response with worse matching. Having the impedance of the pullup to be high is desired, but if a resistor is used, then there can be too much DC drop. If an inductor is used, finding one that is good at low frequencies and around the self-resonant frequency of the inductor is difficult. One approach to address this is to use a series resistor and inductor followed by a resistive pad.

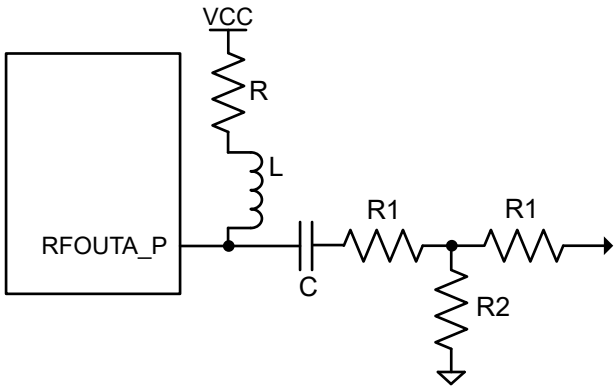

Figure 7-5. Inductor and Resistor Pullup

7.1.5 RF Output Treatment for the Complimentary Side

Regardless of whether both sides of the differential outputs are used, both sides must see a similar load.

7.1.5.1 Single-Ended Termination of Unused Output

The unused output must see a roughly the same impedance as looking out of the pin to minimize harmonics and get the best output power. As placement of the pullup components is critical for the best output power, the routing does not need to be perfectly symmetrical. Give highest priority routing to the used output (RFoutA_P in this case).

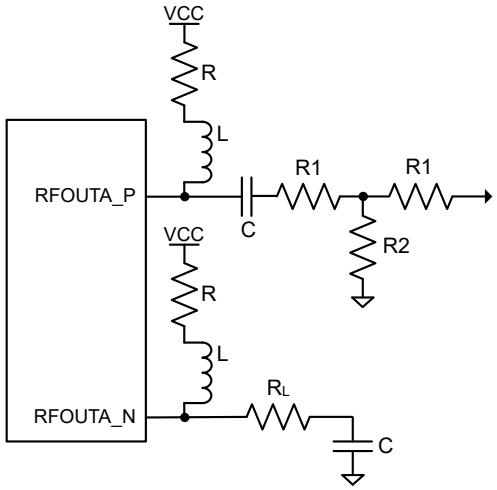

Figure 7-6. Termination of Unused Output: Single-Ended

7.1.5.2 Differential Termination

For differential termination this can be done by doing the same termination to both sides, or connecting the grounds together is also possible. This approach can also be accompanied by a differential to single-ended balun for the highest possible output power.

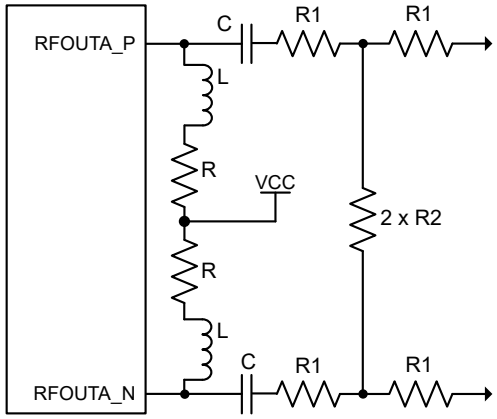

Figure 7-7. Termination of Unused Output: Differential

7.2 External Loop Filter

The LMX2615-SP requires an external loop filter that is application-specific and can be designed by the PLLatinum simulation tool. For the LMX2615-SP, it matters what impedance is seen from the Vtune pin looking outwards. This impedance is dominated by the component C3 for a third order filter or C1 for a second order filter. If there is at least 1.5nF for the capacitance that is shunt with this pin, the VCO phase noise is close to the best possible value. If there is less, the VCO phase noise in the 100kHz to 1MHz region degrades. This capacitor must be placed close to the Vtune pin.

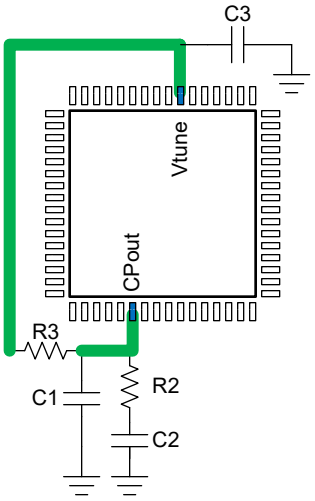

Figure 7-8. External Loop Filter

7.3 Typical Application

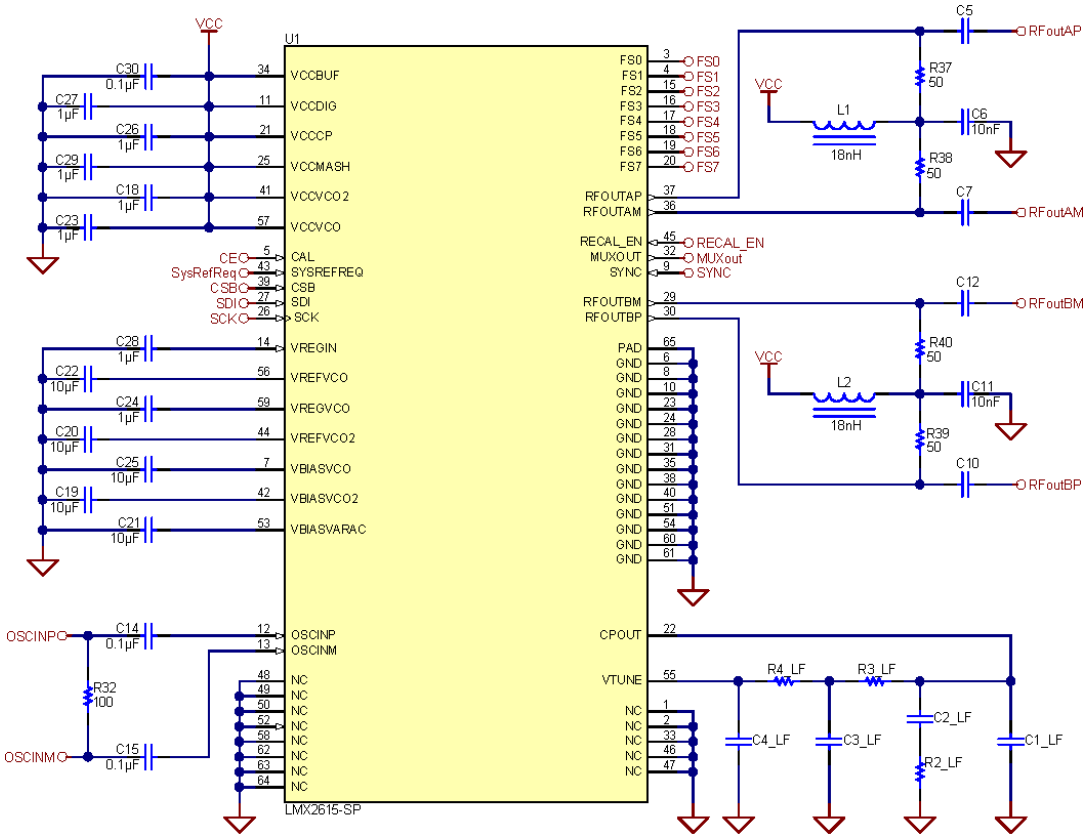

Figure 7-9. Typical Application Schematic

7.3.1 Design Requirements

The design of the loop filter is complex and is typically done with software. The PLLatinum Sim software is an excellent resource for doing this and the design is shown in Figure 7-10.

Figure 7-10. PLLatinum Sim Tool

7.3.2 Detailed Design Procedure

The integration of phase noise over a certain bandwidth (jitter) is an performance specification that translates to signal-to-noise ratio. Phase noise inside the loop bandwidth is dominated by the PLL, while the phase noise outside the loop bandwidth is dominated by the VCO. Generally, jitter is lowest if loop bandwidth is designed to the point where the two intersect. A higher phase margin loop filter design has less peaking at the loop bandwidth and thus lower jitter. The tradeoff with this is that longer lock times and spurs must be considered in design as well.

7.3.3 Application Curve

Using the settings described, the performance measured using a clean 100MHz input reference is shown. Note the loop bandwidth is about 350kHz, as simulations predict.

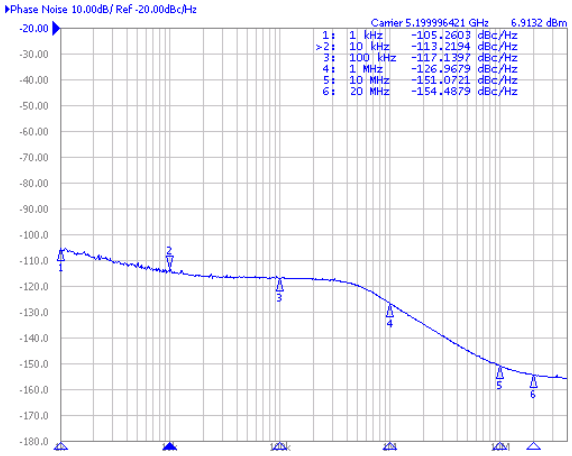

Figure 7-11. Results for Loop Filter Design

7.4 Power Supply Recommendations

TI recommends placement of bypass capacitors close to the pins. Consult the EVM instructions for layout examples. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree. This device has integrated LDOs, which improves the resistance to power supply noise. However, the pullup components on the RFoutA and RFoutB pins on the outputs have a direct connection to the power supply, so extra care must be made to verify that the voltage is clean for these pins.

Current consumption of the LMX2615-SP depends on the configuration. With LMX2615EVM-CVAL default configuration, Table 7-3 shown the typical current drawn from each voltage supply pin. All voltage supply pins can be tied together to share the same supply source or the pins can be separated with individual supply source. However, VccVCO and VccVCO2 must be tied to the same supply source.

Table 7-3. Individual Voltage Supply Pin Current

Pin Number	Pin Name	Current (mA)
11	VccDIG	25
21	VccCP	18
34	VccBUF	137 (One output active)
		258 (Two outputs active)
25	VccMASH	59
57, 41	VccVCO + VccVCO2	118 (One output active)
		130 (Two outputs active)
Total		357 (One output active)
		490 (Two outputs active)

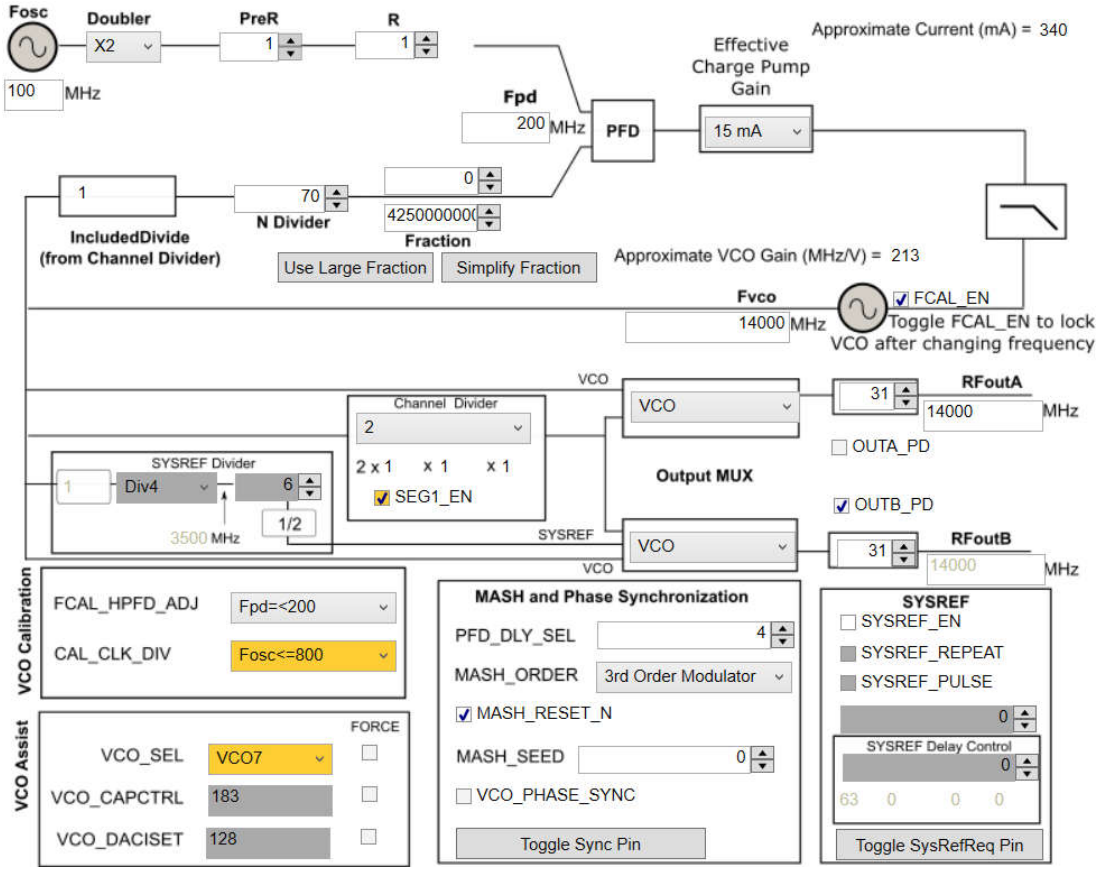

Figure 7-12. LMX2615EVM-CVAL Default Configuration

7.5 Layout

7.5.1 Layout Guidelines

In general, the layout guidelines are similar to most other PLL devices. Here are some specific guidelines.

- GND pins can be routed on the package back to the DAP.
- For the outputs, keep the pullup component as close as possible to the pin and use the same component on each side of the differential pair.
- If a single-ended output is needed, the other side must have the same loading and pullup. However, the routing for the used side can be optimized by routing the complementary side through a via to the other side of the board. On this side, use the same pullup and make the load look equivalent to the side that is used.
- Verify DAP on device is well-grounded with many vias, preferably copper filled.
- Have a thermal pad that is as large as the LMX2615-SP exposed pad. Add vias to the thermal pad to maximize thermal performance.
- Use a low loss dielectric material, for the best output power.
- Place voltage supply bypass capacitor close to the pin.

7.5.2 Layout Example

In addition to the layout guidelines already given, here are some additional comments for this specific layout example

- The most critical part of the layout that the placement of the pullup components (R37, R38, R39, and R40) is close to the pin for optimal output power.
- For this layout, most of the loop filter (C1_LF, C2_LF, C3_LF, R2_LF, R3_LF, and R4_LF) are on the back side of the board. However note that C4_LF is on the top side right next to the Vtune pin. In the event that this C4_LF capacitor is open. Move one of loop capacitors in this spot. For instance, if a 3rd order loop filter is used, technically C3_LF is non-zero and C4_LF is open. However, for this layout example that is designed for a 4th order loop filter, make R3_LF = 0Ω, C3_LF = open, and C4_LF to be whatever C3_LF would have been.

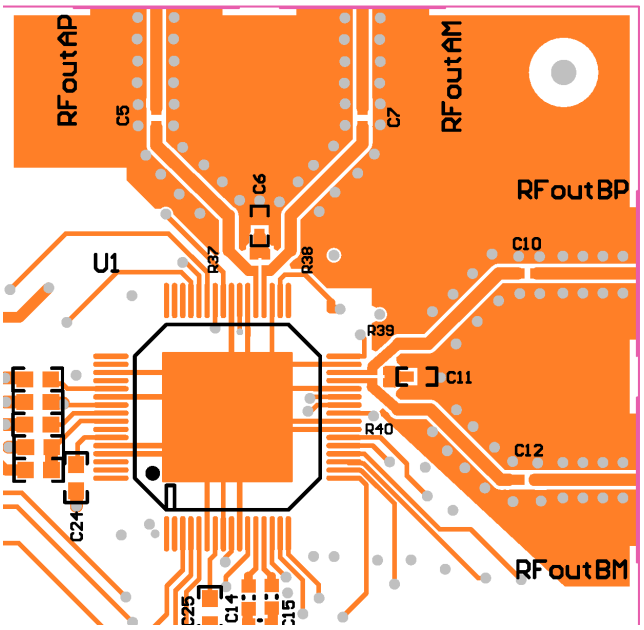

Figure 7-13. LMX2615-SP Layout Example

7.5.3 Footprint Example on PCB Layout

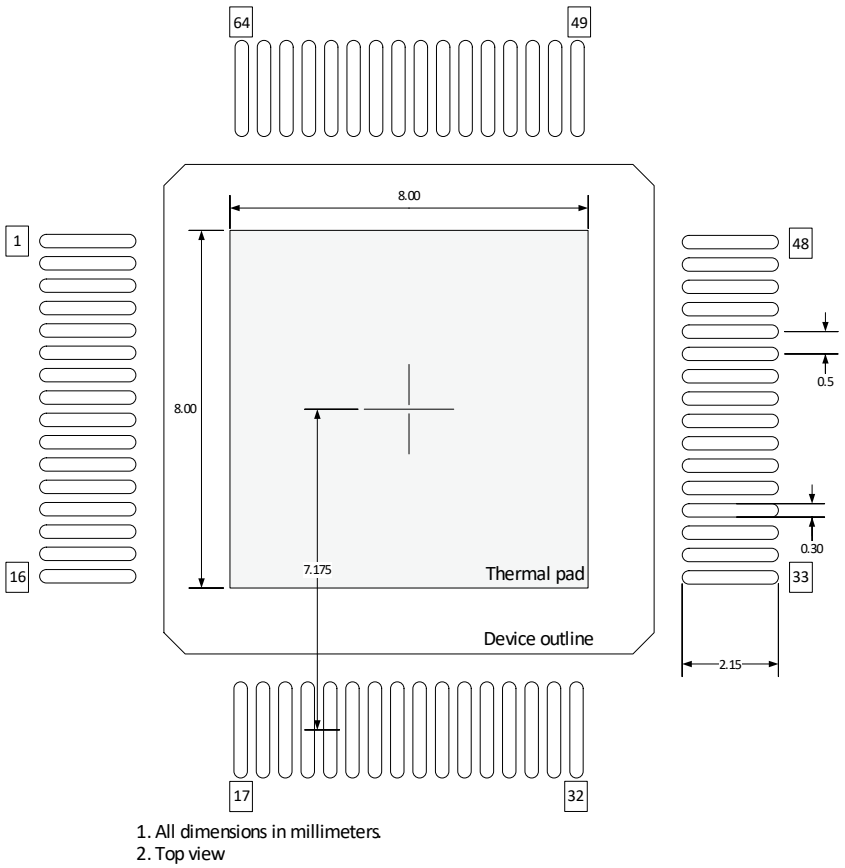

Figure 7-14. LMX2615-SP PCB Land Pattern Example

7.5.4 Radiation Environments

Careful consideration must be given to environmental conditions when using a product in a radiation environment.

7.5.4.1 Total Ionizing Dose

Radiation Hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the ordering information. Testing and qualification of these product is done on a wafer level according to MIL-STD-883, test method 1019. Wafer level TID data are available with lot shipments.

7.5.4.2 Single Event Effect

One time single event effect (SEE), including single event latch-up (SEL), single event functional interrupt (SEFI) and single event upset (SEU), testing is performed according to EIA/JEDEC Standard, EIA/JEDEC57. A test report is available upon request.

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

Texas Instruments has several software tools to aid in the development at www.ti.com. Among these tools are:

- EVM software to understand how to program the device and for programming the EVM board.
- EVM board instructions for seeing typical measured data with detailed measurement conditions and a complete design.
- PLLatinum Sim program for designing loop filters, simulating phase noise, and simulating spurs.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas instruments, *AN-1879 Fractional N Frequency Synthesis* application note
- Texas instruments, *PLL Performance, Simulation, and Design Handbook* design guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2020) to Revision E (December 2025)	Page
• Added package mass and links in the *Device Information* table	1
• Updated the content for various pins	3
• Added DAP pin	3
• Added SCK, SDI and CSB in digital pin voltage	6
• Added CDM rating	6
• Changed t_{CD} specification to the maximum column	9

- Added timing requirements for SYNC and SYSREFREQ 9
- Added trigger signals timing diagram; modified SPI timing diagram 9
- Updated the typical plots 11
- Added a row for fractional numerator in Table 6-1 13
- Added the last sentence 14
- Added maximum state machine clock frequency 15
- Updated the content and the values in Table 6-2 15
- Changed line sharing is possible 16
- Changed phase detector cycles to state machine clock cycles 16
- Content is updated 16
- Removed equation 3 16
- Removed Table 6 16
- Changed WD_DLY to WD_CNTRL 17
- Changed LD_DLY to WD_DLY 17
- Removed equivalent division value of 72 18
- Updated Figure 6-2 and Table 6-7 18
- Removed SPI mode statement. Added Pin mode statement 19
- Fixed typo error 19
- Updated Figure 6-3, Figure 6-4 and Table 6-11 20
- Changed the setup time, hold time and the flow chart for SYNC 20
- Updated the procedure for using SYNC 21
- Deleted the first sentence 22
- Added phase adjustment content 22
- Updated SYSREF block diagram and equations; updated the value in Table 6-14 23
- Changed "...R75 down to R0 is required..." to "...R75 down to R0 (with FCAL_EN = 1) is required..." 28
- Updated the content 28
- Changed register R1 bit 3 name from 1 to MUXOUT_CTRL in Table 6-17 29
- Changed register R11 bit 4 name from 1 to PLL_R in Table 6-17 29
- Added POR column in Table 6-17 29
- Changed the description of RESET in Table 6-20 34
- Added MUXOUT_CTRL in Figure 6-10 and Table 6-21 34
- Updated Figure 7-1 62
- Changed the impedance values 63
- Added External Loop Filter section 65
- Updated Figure 7-10 66
- Updated Figure 7-11 67
- Changed the title of Figure 7-14 70
- Added link to the engineering sample technical document 74

Changes from Revision C (November 2018) to Revision D (May 2020) **Page**

- Added SMD number and orderable part 1
- Deleted LMX2615W-MLS from the *Device Information* table 1
- Deleted sentence "See application section on phase noise due to the charge pump." from *PLL Phase Detector and Charge Pump* section 15
- Changed *Typical Application Schematic* graphic 66
- Changed *Layout Example* graphic 69

Changes from Revision B (June 2018) to Revision C (November 2018) **Page**

- Changed device status from Advanced Information to Production Data 1
- Changed output power, VCO Calibration time, and harmonics 7

- Added Typical Performance Characteristics 11
- Changed Updated Max Frequencies for higher divides to be based on 11.5GHz, not 15.2GHz 18
- Added FS7 Pin description 25
- Added Typical Application..... 66
- Added more details including capacitor requirements for Vtune pin..... 69
- Added Layout Example..... 69

Changes from Revision A (June 2018) to Revision B (August 2018) **Page**

- Changed Typical jitter to 45fs 1
- Added Max Digital pin and OSCin Voltage..... 6
- Changed Typical VCO Gain..... 7
- Changed readback timing diagram and added tCD. 9
- Changed VCO Frequency range to 7600 to 15200MHz 13
- Changed VCO calibration updated to new VCO range of 7600 to 15200MHz 16
- Changed Ordering of VCOs in calibration time table 16
- Added Watchdog feature description..... 17
- Changed RECAL feature description..... 17
- Changed VCO Gain table 18
- Changed Channel divider description and picture 18
- Changed Channel Divider usage for VCO frequency 18
- Changed 5GHz, not 5MHz 19
- Added information on what to do with unused pins..... 19
- Changed Case of Fosc%Fout=0 is now category 2..... 20
- Changed Recommendation for CAL and RECAL_EN 25
- Changed RECAL_EN to CAL pin 25
- Changed pin mode 17 to not be used..... 25
- Added 10ms delay to recommended initial power up sequence and more details on what registers to program..... 28
- Added Register Map Table 29

Changes from Revision * (May 2017) to Revision A (June 2018) **Page**

- Changed the //ESD Ratings// table 6
- Changed ambient temperature parameter to case temperature in the //Recommended Operating Conditions// table..... 6
- Deleted the junction temperature parameter from the //Recommended Operating Conditions// table..... 6
- Changed the supply voltage minimum value from: 3.15V to: 3.2V..... 7
- Changed the test conditions to the supply current parameter..... 7
- Changed the power on reset current typical value for the RESET=1 test condition from: 270mA to: 289mA.... 7
- Changed the power on reset current typical value for the POWERDOWN=1 test condition from: 5mA to: 6mA..... 7
- Changed the test conditions and added minimum values to the reference input voltage parameter..... 7
- Added phase detector frequency test conditions..... 7
- Changed VCO phase noise test conditions and typical values..... 7
- Changed the text to clarify that output power assumes that load is matched and losses are de-embedded..... 7
- Changed the *Assisting the VCO Calibration Speed* and the *MINIMUM VCO_SEL for Partial Assist* tables.... 16
- Added *Typical Calibration times for f_{OSC} = f_{PD} = 100MHz based on VCO_SEL* table 16
- Changed the MASH_SEED considerations in the *Phase Adjust* section..... 22

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Engineering Samples

Engineering samples (LMX2615W-MPR) have the same package, pinout, programming, and typical performance as the flight devices (5962R1723601VXC). Samples are tested at room temperature to meet the electrical specifications, but have not received or passed the full space production flow or testing. Engineering samples can be QCI rejects that failed full space production tests, such as radiation or reliability.

For more information about engineering samples, see the Texas Instruments Engineering Evaluation Units versus MIL-PRF-38535 QML Class V Processing brochure.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R1723601VXC	Active	Production	CFP (HBD) | 64	14 | TUBE	ROHS Exempt	NIAU	Level-1-NA-UNLIM	-55 to 125	5962R1723601VXC LMX2615WRQMLV
LMX2615-MKT-MS	Active	Production	CFP (HBD) | 64	1 | TUBE	-	Call TI	Call TI	25 to 25	LMX2615-MKT-MS MECHANICAL
LMX2615W-MPR	Active	Production	CFP (HBD) | 64	14 | TUBE	ROHS Exempt	NIAU	Level-1-NA-UNLIM	25 to 25	LMX2615W-MPR ENG SAMPLE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

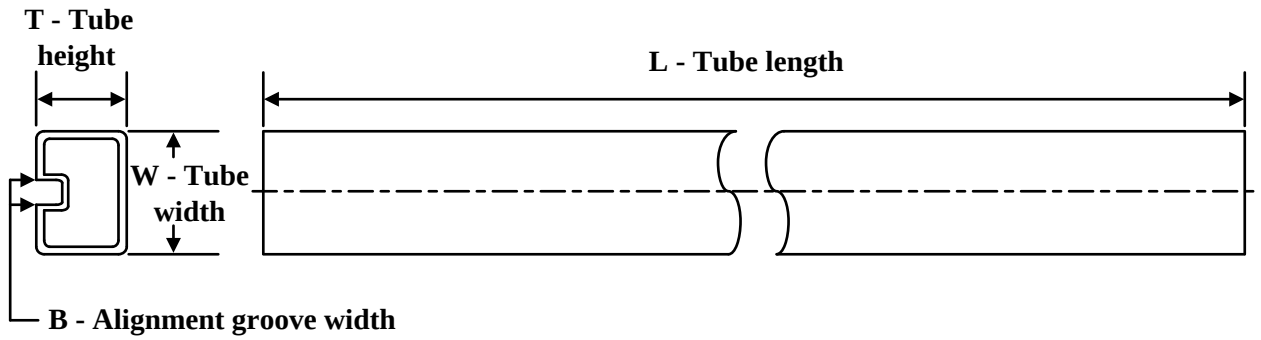
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

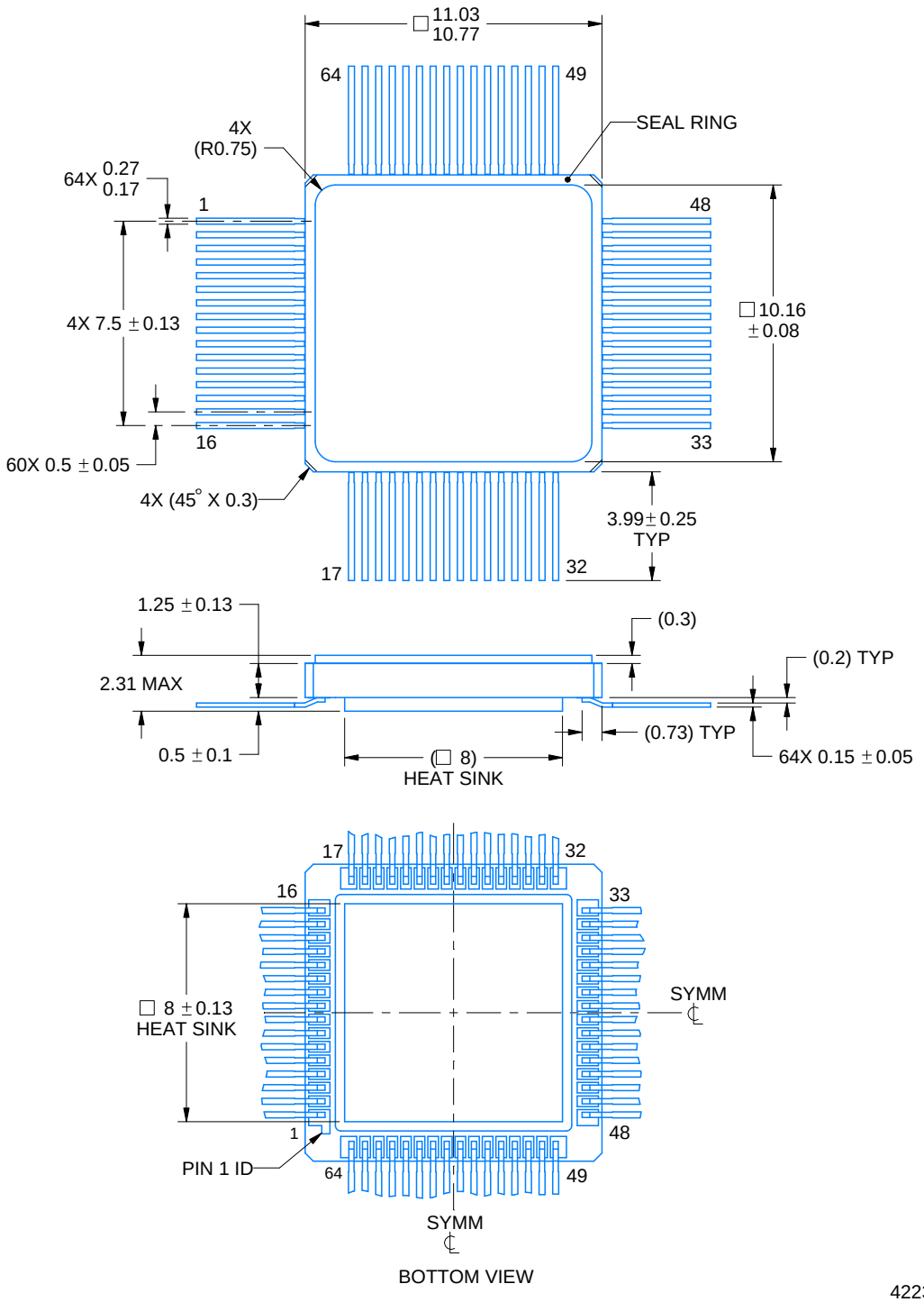
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R1723601VXC	HBD	CFP (HSL)	64	14	495	33	11176	16.51
LMX2615W-MPR	HBD	CFP (HSL)	64	14	495	33	11176	16.51

PACKAGE OUTLINE

HBD0064A

CFP - 2.31 mm max height

CERAMIC FLATPACK



4223243/A 01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. Ground pad to be electronic connected to heat sink and seal ring.
5. The leads are gold plated and can be solder dipped.

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