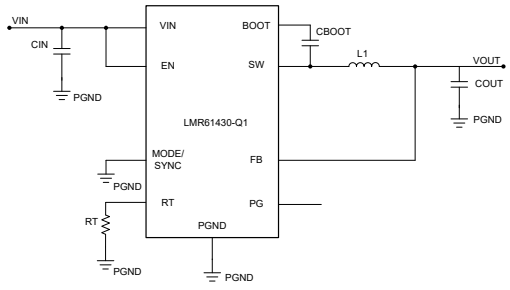
LMR61430-Q1 36V, 3A, Automotive, Sync Buck Converter With Mitigated Interference and Noise Technology (MINT) and Optimized Spread Spectrum for Flat Output Noise

1 Features

- Mitigated interference and noise technology – architecture 1 (MINT 1):
  - Low output noise optimized dual random spread spectrum (DRSS)
  - Facilitates CISPR 25 class 5 compliance
  - Low inductance HotRod™ QFN package
- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Wide operating input voltage: 3V to 36V (42V absolute maximum)
- Programmable output voltage options available in fixed 3.3V/ADJ and 5V/ADJ
  - Adjustable output voltage range from 1V to 20V
- Ultra-low quiescent current
  - Shutdown current: 0.75µA
  - No load standby current: 3.8µA
- Optimized control loop for low output capacitance
- Switching frequency from 200kHz – 2.2MHz
- Low minimum t_{ON} (30ns typical)
- FPWM, PFM, or external frequency synchronization available
- Designed for scalable power supplies
  - Pin compatible with LMR60406-Q1, LMR60410-Q1, LMR60420-Q1, LMR60430-Q1, LMR61440-Q1, LMR60440-Q1, LMR60441-Q1, LMR60450-Q1, and LMR60460-Q1
- Power-Good output for power sequencing

2 Applications

- Low-power radar
- Camera applications
- Autonomous systems
- Low-noise displays and instrumentation



Simplified Schematic – Fixed Output

3 Description

The LMR61430-Q1 is a 3V to 36V (42V transient), 3A, synchronous buck converter in an ultra compact 2.5mm × 2mm QFN-9 package with wettable flanks. The LMR61430-Q1 with mitigated interference and noise technology using architecture 1 features (MINT 1) enables the device to achieve low EMI performance and low output noise to facilitate noise-sensitive designs.

All device variants are capable of output voltages ranging from 1V to 20V in adjustable output configuration. Each variant is also capable of delivering a fixed output voltage by connecting the output voltage node directly to the feedback pin. The *Device Comparison Table* provides details on the fixed output voltage options. The current-mode control architecture with 30ns minimum on-time allows high conversion ratios at high frequencies, fast transient response, and excellent load and line regulation.

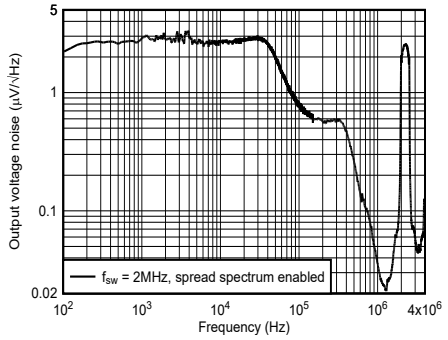
Open drain power-good output facilitates power sequencing requirements. The MODE/SYNC pin of the LMR61430-Q1 allows the user to select between forced pulse width modulation (FPWM), auto mode, or external synchronization mode of operation.

The LMR61430-Q1 is designed to offer reduced output capacitance leading to compact PCB layout and system cost savings. The LMR61430-Q1 is a part of a family of pin-compatible devices ranging in current levels from 0.6A to 6A.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMR61430-Q1	RAK (WQFN-HR, 9)	2.5mm × 2.0mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Output Noise Spectral Density

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4 Device Comparison Table

ORDERABLE PART NUMBER(1)	OUTPUT CURRENT	OUTPUT VOLTAGE	WETTABLE FLANKS	PACKAGE SIZE
LMR614303SRAKRQ1	3A	3.3V fixed / adjustable	Yes	2.5mm × 2mm
LMR614305SRAKRQ1	3A	5V fixed / adjustable	Yes	2.5mm × 2mm

(1) For other variant options, contact TI.

5 Pin Configuration and Functions

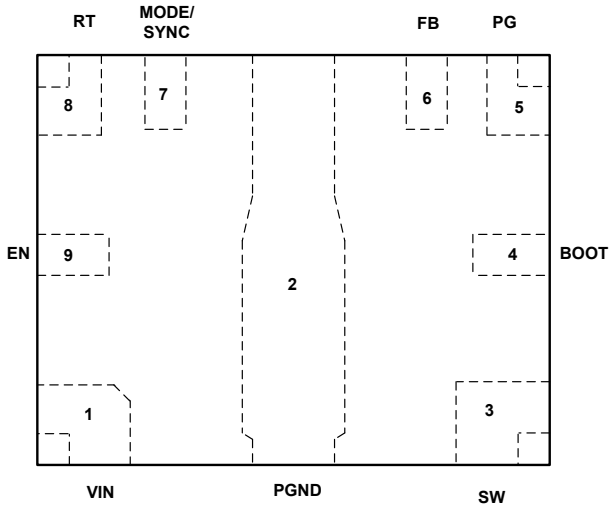


Figure 5-1. RAK Package 9-Pin WQFN-HR (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	VIN	P	Regulator input power pin to the high-side power MOSFET and internal VCC regulator. Connect to the input supply and the positive terminal of the input filter capacitor. The path from the VIN pin to the input capacitor must be as short as possible.
2	PGND	G	Power ground. This pin connects to the source of the low-side MOSFET internally. Connect to system ground, and the ground terminal of the CIN and COUT capacitors. The path to CIN must be as short as possible.
3	SW	P	Regulator switch node. Connect to the power inductor and bootstrap capacitor.
4	BOOT	P	High-side MOSFET driver supply for bootstrap gate drive. Connect a high quality 100nF capacitor between this pin and SW as close to the device as possible.
5	PG	O	Open drain power-good output. Connect to a suitable voltage supply through a current limiting pull up resistor. High = regulator power good, Low = output out of regulation. Goes low when EN = low. See also Section 7.3.8.
6	FB	I	Feedback pin. Connect this pin directly to the output voltage node for fixed V_{OUT} operation. See Section 4 for the voltage level for each device variant. Connect to the center point of a feedback voltage divider placed between V_{OUT} node and PGND to program an adjustable output voltage.
7	MODE/SYNC	I	Operational mode input pin. Connect this pin to the RT pin to select FPWM switching or connect this pin to GND to select PFM switching in light loads. To synchronize to an external clock, connect a 100kΩ resistor to ground and drive directly from the clock. See the *Electrical Characteristics* table for acceptable voltage levels and timing requirements.
8	RT	I	Frequency programming pin. A resistor from RT to PGND sets the oscillator frequency between 200kHz and 2.2MHz.
9	EN	I	Enable pin for the regulator. Drive this pin high to enable the device and low to disable the device. If the enable function is not needed, connect this pin to the VIN pin. See the *Electrical Characteristics* table for more information on acceptable voltage levels.

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	42	V
Input voltage	EN/UVLO TO PGND	–0.3	42	V
Input voltage	RT, MODE/SYNC to PGND	–0.3	42	V
Input voltage	FB to PGND	–0.3	20	V
Output voltage	PG to PGND	–0.3	20	V
Output voltage	SW to PGND(2)	–0.3	V_{IN} + 0.3	V
Output voltage	BOOT to SW	–0.3	5.5	V
Temperature	Operating junction temperature, T_J	–40	150	°C
Temperature	Storage temperature, T_{stg}	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Do not externally drive the SW pin. A voltage of 5V below PGND and peak voltage not exceeding 42V for less than 20ns is allowed during switching transitions.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	3	36	V
Input voltage	EN	0	36	V
Input voltage	PG	0	18	V
Input voltage	MODE/SYNC, RT	0	5.5	V
Output voltage	VOUT	1.0	20(1)	V
Output current	IOUT	0	3.0	A
Temperature	Operating junction temperature, T_J	–40	150	°C

(1) Contact TI for information regarding output voltages outside of this range. Under no conditions must the output voltage be allowed to fall below zero volts.

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE RAK (WQFN-HR) 9 PINs	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JESD 51-7)(2)	84.5	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(3)	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC(1)		DEVICE	UNIT
		RAK (WQFN-HR)	
		9 PINs	
Ψ_{JB}	Junction-to-board characterization parameter	23.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. This value was calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. This value does not represent the performance obtained in an actual application.
(3) Based on thermal simulation of proposed EVM layout.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V, V_{EN} = V_{IN}, V_{OUT} = 3.3V, F_{SW} = 2MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (VIN PIN)						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising (needed to start up)	3.3	3.5	3.7	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling (once operating)			2.65	V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			1		V
$VIN_{OVP(R)}$	VIN OVP rising threshold	V_{IN} rising needed to switch device into PFM operation	35	37	39	V
$VIN_{OVP(F)}$	VIN OVP falling threshold	V_{IN} falling needed to switch device from PFM to FPWM operation	34	36	38	V
$VIN_{OVP(H)}$	VIN OVP hysteresis		0.6	0.95	1.2	V
$I_{Q(FIX-3.3V)}$	Total V_{IN} quiescent current, fixed 3.3V output, no switching	V_{IN} = 13.5V, I_{OUT} = 0A, V_{FB} = 3.3V + 4%, T_J = 25°C, auto mode enabled		3.8	5	µA
$I_{Q(ADJ-3.3V)}$	Total V_{IN} quiescent current, adjustable 3.3V output, no switching	V_{IN} = 13.5V, I_{OUT} = 0A, V_{FB} = 1V + 4%, auto mode enabled, T_J = 25°C		3.8	5	µA
I_{Q-SD}	V_{IN} shutdown supply current	V_{EN} = 0V, T_J = 25°C		0.75	1.1	µA
ENABLE (EN PIN)						
$V_{EN-TH(R)}$	Enable voltage rising threshold	V_{EN} rising	1.15	1.25	1.35	V
$V_{EN-TH(F)}$	Enable input low threshold	V_{EN} falling	0.9	1	1.1	V
V_{EN-HYS}	Enable voltage hysteresis			275		mV
I_{EN-LKG}	Enable input leakage current	V_{EN} = V_{IN}		1	675	nA
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Internal feedback reference voltage	FPWM mode	0.99	1.0	1.01	V
I_{FB-LKG}	Feedback pin input leakage current	V_{FB} = 1V, adjustable output voltage		0.09	50	nA
$V_{OUT(3.3V)}$	3.3V fixed output voltage	FPWM mode, FB pin short to VOUT	3.24	3.3	3.35	V
$V_{OUT(5V)}$	5.0V fixed output voltage	FPWM mode, FB short to VOUT	4.9	5	5.075	V
STARTUP						
t_{SS}	Internal fixed soft-start time	Time from first SW pulse to V_{REF} at 90% of set point		6		ms
CURRENT LIMITS AND HICCUP						
I_{HS-LIM}	High side peak current limit	Duty-cycle approaches 0%	4.2	5.4	7.5	A
I_{LS-LIM}	Low side valley current limit	Valley current limit on LS FET	3.4	4.4	5.5	A
$I_{LS-NEG-LIM}$	Low side negative current limit	Sinking current limit on LS FET, FPWM mode	–2.2	–1.6	–1.0	A
$I_{L-ZC-LIM}$	Zero-cross current limit	Auto mode		80		mA
V_{HIC}	Overcurrent hiccup threshold on FB pin	LS FET on-time > 165ns, not during soft start	0.14	0.2	0.25	V

6.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 13.5V, V_{EN} = V_{IN}, V_{OUT} = 3.3V, F_{SW} = 2MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD (PG PIN)						
$V_{PG-OVP(R)}$	PG overvoltage rising threshold	% of FB voltage (adj)	105	107	109.7	%
$V_{PG-OVP(F)}$	PG overvoltage falling threshold	% of FB voltage (adj)	104	106	108	%
$V_{PG-UVP(R)}$	PG undervoltage rising threshold	% of FB voltage (adj)	92	94	96.5	%
$V_{PG-UVP(F)}$	PG undervoltage falling threshold	% of FB voltage (adj)	91	93	95	%
$t_{PG-DEGLITCH}$	Deglitch filter delay on PG falling edge		42	52	81	µs
$t_{PG-DEASSERT}$	PG deassertion time		1.0	2.0	3.0	ms
$V_{IN(PG-VALID)}$	Minimum VIN for valid PG output	$V_{OL(PG)}$ < 0.4V, R_{PU} = 10kΩ, V_{PU} = 5V			1.25	V
$R_{ON(PG)}$	PG ON resistance	I_{PG} = 1mA		165	420	Ω
SWITCHING FREQUENCY (RT PIN)						
$f_{SW1(FPWM)}$	Switching frequency, FPWM operation	R_{RT} = 15.2kΩ, 1%	1800	2000	2200	kHz
$f_{SW2(FPWM)}$	Switching frequency, FPWM operation	R_{RT} = 32.8kΩ, 1%	900	1000	1100	kHz
SYNCHRONIZATION (MODE/SYNC PIN)						
V_{IH_FPWM}	MODE/SYNC pin voltage to enter FPWM		0.5		0.85	V
V_{IL_FPWM}	MODE/SYNC pin voltage to exit FPWM		0.35		0.7	V
V_{IH_CLK}	External clock input high level threshold		1.3			V
V_{IL_CLK}	External clock input low level threshold				0.35	V
$t_{CLKIN(TON)}$	Minimum positive pulse width of external sync signal			150		ns
$t_{CLKIN(TOFF)}$	Minimum negative pulse width of external sync signal			150		ns
POWER STAGE						
$R_{DS-ON-HS}$	High-side FET ON resistance	I_{SW} = 500mA, $V_{BOOT-SW}$ = 3.8V		65	140	mΩ
$R_{DS-ON-LS}$	Low-side FET ON resistance			40	85	mΩ
t_{ON-MIN} (1)	Minimum on-time			30		ns
$t_{OFF-MIN}$ (1)	Minimum off-time			100		ns
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown(1)	Shutdown threshold		165		ºC
		Recovery threshold		156		ºC

(1) Not tested in production.

6.6 Typical Characteristics

V_{IN} = 13.5V, T_A = 25°C (unless otherwise noted). Specified temperatures are ambient.

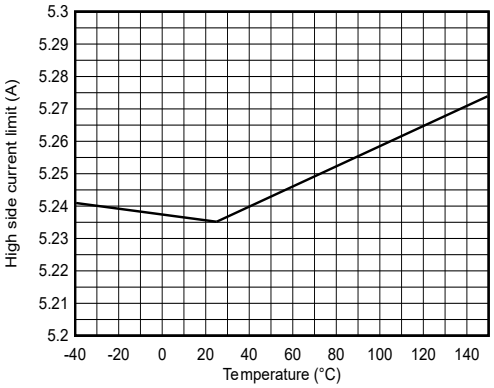


Figure 6-1. High-Side MOSFET Current Limit

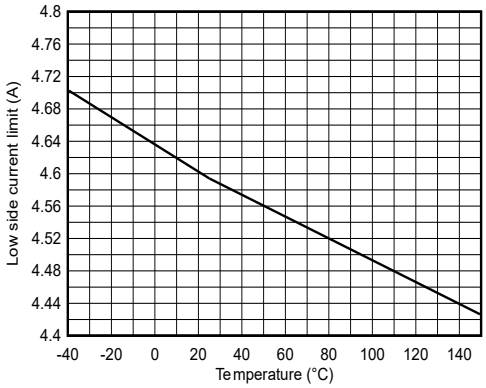


Figure 6-2. Low-Side MOSFET Current Limit

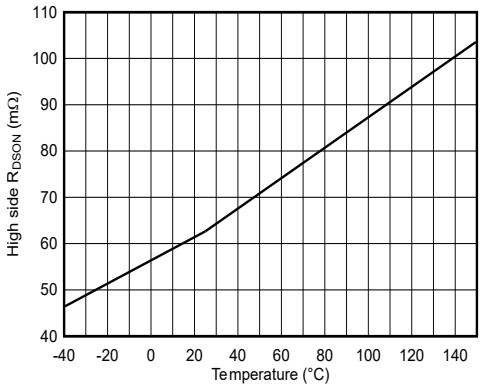


Figure 6-3. High-Side MOSFET R_{DS-ON}

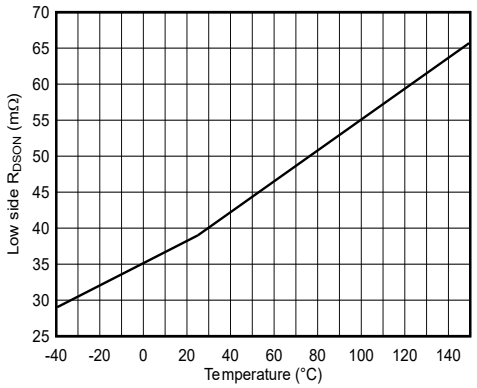
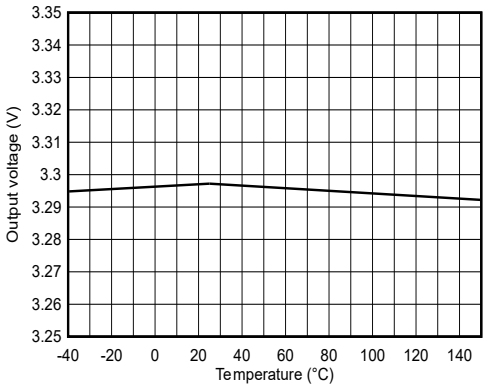


Figure 6-4. Low-Side MOSFET R_{DS-ON}



3.3V Fixed

Figure 6-5. Output Voltage Accuracy

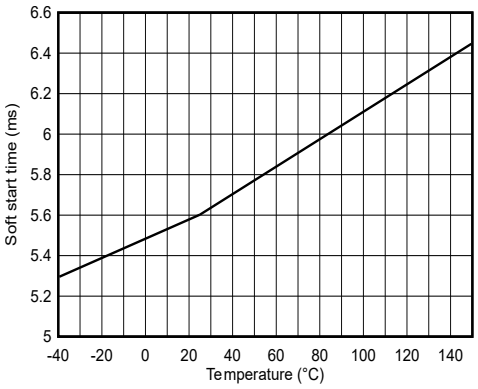


Figure 6-6. Soft-Start Time

6.6 Typical Characteristics (continued)

V_{IN} = 13.5V, T_A = 25°C (unless otherwise noted). Specified temperatures are ambient.

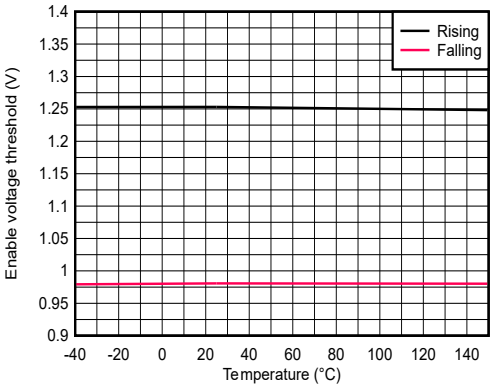


Figure 6-7. Enable Threshold Voltage

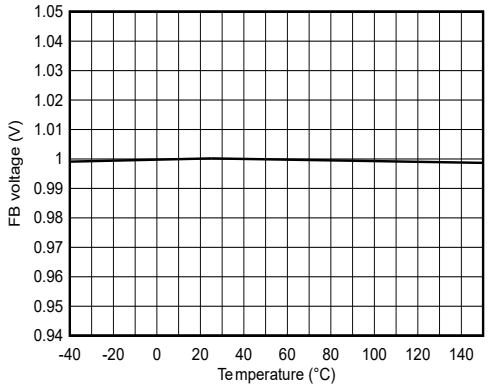


Figure 6-8. Feedback Voltage Accuracy

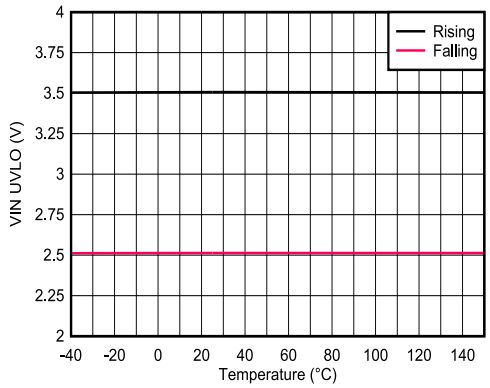


Figure 6-9. Input Voltage UVLO

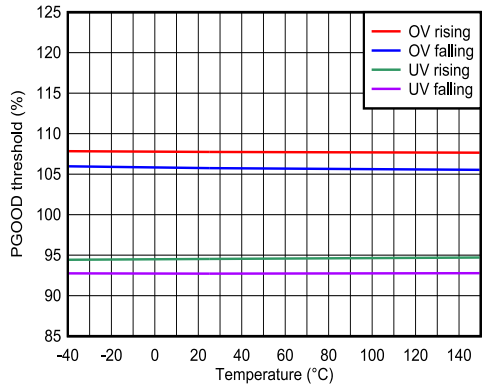


Figure 6-10. PGOOD Thresholds

7 Detailed Description

7.1 Overview

The LMR61430-Q1 is a highly-efficient, 3V to 36V, ultra-low IQ, synchronous buck converter that enables high power density and low EMI. The LMR61430-Q1 is designed to minimize the end-product cost and size by reducing the number of external passive components required to generate a stable design. Intended for demanding automotive applications, LMR61430-Q1 devices are AEC-Q100 qualified and have electrical characteristics specified up to a maximum junction temperature of 150ºC.

The LMR61430-Q1 offers key features that allow for design flexibility depending on the desired operating conditions:

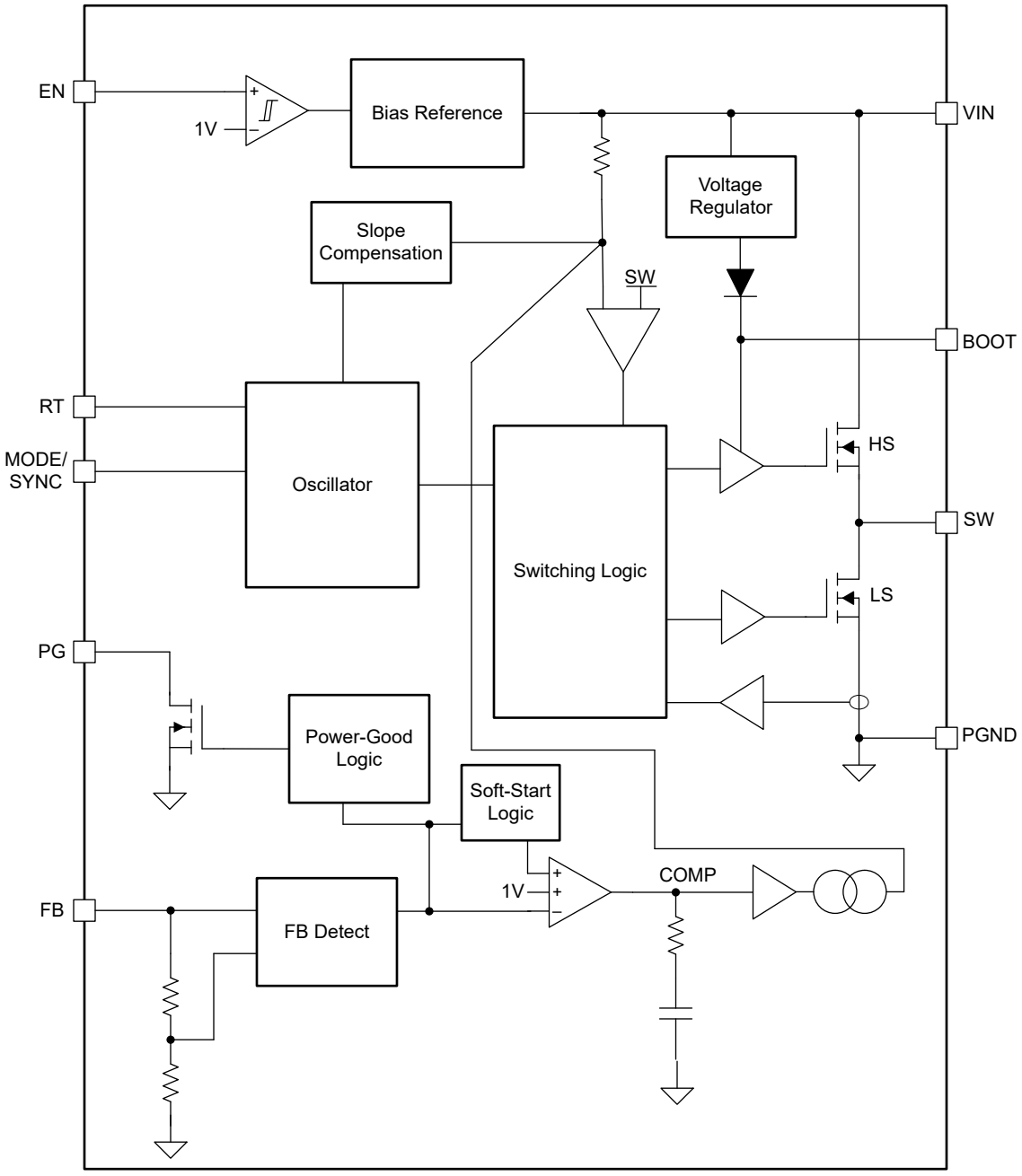
- Precision enable through the EN pin allows for accurate power on and power off of the device.
- Switching frequency selection with the RT pin allows designers to select the switching frequency between 200kHz and 2.2MHz.
- The MODE/SYNC pin allows for designers to select the mode of operation, or to synchronize to an external clock frequency.
- The PG pin enables power supply sequencing and notification of the status of the output voltage without the need for external voltage supervisors.

Each converter features a pair of integrated power MOSFETs designed for delivering up to 3A of output current. All variants of the LMR61430-Q1 allow for every device to be configured to either a fixed output voltage or an adjustable output voltage depending on the presence of feedback resistors. The fixed output voltage setting is determined by the specific orderable part number, which can be found in the *Device Comparison Table*.

The LMR61430-Q1 offers several protection features that make the device an excellent choice for demanding applications. The feedback pin has a voltage rating which makes sure the pin is able to withstand an output voltage short circuit to battery even when in fixed output voltage configuration. The device disables FPWM switching when the input voltage exceeds $VIN_{OVP(R)}$ which prevents negative currents from overcharging the input voltage in the event that the output voltage is shorted to the input supply. Thermal shutdown disables switching and allows the LMR61430-Q1 to cool before attempting to restart.

The current-mode control architecture with 30ns minimum on-time allows high conversion ratios at high frequencies, easy loop compensation, fast transient response, and excellent load and line regulation. The converters also feature a HotRod package with advanced spread spectrum that enables low noise and low EMI performance and eases qualification of automotive and noise-sensitive designs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Undervoltage Lockout (UVLO)

LMR61430-Q1 features a precision enable and undervoltage lockout (UVLO) feature which enables the user to select the voltage level at which the device powers on and off based on the voltage present at the EN pin. To power on the device the voltage between EN pin and PGND pin must exceed the enable voltage rising threshold $V_{EN-TH(R)}$ (1.25V typical). After $V_{EN-TH(R)}$ has been crossed, and the minimum supply voltage, $VIN_{UVLO(R)}$, have both been satisfied, the part begins the soft-start sequence described in Section 7.3.2.

The EN pin can be used to power down the device by reducing the voltage between the EN pin and PGND pin below the enable input low threshold $V_{EN-TH(F)}$ 1V (typical).

A resistor divider between VIN and PGND with the center point connected to the EN pin can be used to implement the VIN UVLO. To begin, select the input voltage at which the device turns off, select the value of R_{ENT}, then calculate the required R_{ENB}. After R_{ENB} has been calculated, the resulting turn-on input voltage can be calculated. See Figure 7-1, Equation 1, and Equation 2 to determine the EN resistors required. If the VIN UVLO feature is not needed, the EN pin can be connected directly to VIN.

$$R_{ENB} = \frac{V_{EN-TH(F)}}{\left(VIN_{turn-off} - V_{EN-TH(F)}\right)} \times R_{ENT} \quad (1)$$

$$VIN_{turn-on} = \left(1 + \frac{R_{ENT}}{R_{ENB}}\right) \times V_{EN-TH(R)} \quad (2)$$

Where:

- $VIN_{turn-off}$ represents the input voltage at which the LMR61430-Q1 turns off.
- $VIN_{turn-on}$ represents the input voltage at which the LMR61430-Q1 turns on.

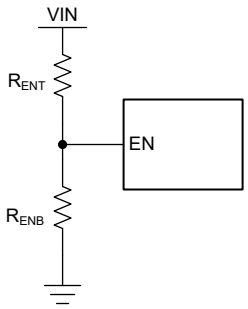


Figure 7-1. VIN UVLO Using the EN Pin

7.3.2 Soft Start and Recovery from Dropout

The LMR61430-Q1 uses soft start to prevent output voltage overshoots and large inrush currents during start-up. The soft-start time is fixed internally at 6ms (typical). The LMR61430-Q1 device operates correctly even if there is a voltage present on the output before the device is enabled.

To start-up the LMR61430-Q1 and initiate the soft-start sequence, the voltage applied to the VIN and EN pins must exceed $VIN_{UVLO(R)}$ and $V_{EN-TH(R)}$ respectively. After these conditions are met, the soft-start sequence initiates and the output voltage reaches the set-point in 6ms (typical).

Dropout occurs when the input voltage falls below the voltage level of the output voltage setpoint. During this condition, the output voltage tracks the input voltage.

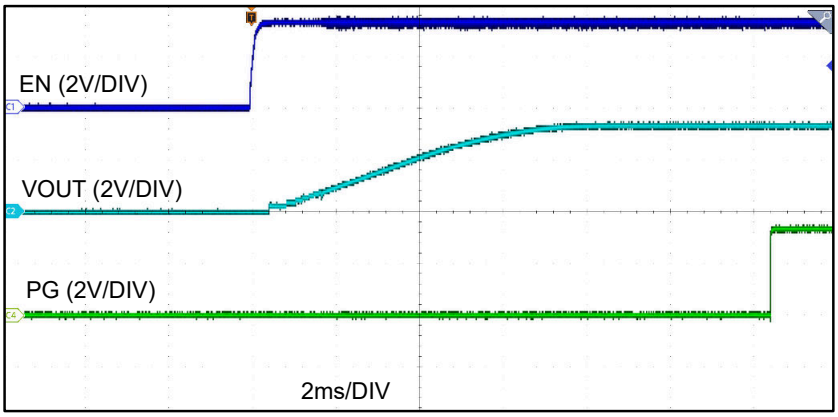


Figure 7-2. Enable Soft Start

7.3.3 Frequency Selection With RT

A resistor placed between the RT pin and PGND is used to select the set point switching frequency of the LMR61430-Q1 typically between 200kHz and 2.2MHz. The set point switching frequency represents the switching frequency which can occur if the LMR61430-Q1 is operating in continuous conduction mode with spread spectrum disabled. Use the following equation to determine the RT resistor value for a desired set point switching frequency.

$$RT = \frac{\frac{1}{f_{sw}} - 69.6 \times 10^{-9}}{2.825 \times 10^{-11}} \quad (3)$$

Where:

- RT: represents the RT resistor value in ohms (Ω)
- f_{sw}: represents the set point switching frequency in hertz (Hz)

7.3.4 MODE/SYNC Pin Control

The MODE/SYNC pin of the LMR61430-Q1 is an input pin used to select the mode of operation of the device or to synchronize the switching frequency to an external clock frequency. In the absence of an external clock, the RT resistor determines the switching frequency. Do not float the MODE/SYNC pin. If this pin is driven by a high impedance source, connect a pull up or pull down resistor to prevent this pin from floating. For more information on the modes of operation, see also Section 7.4.

The MODE/SYNC pin can be used to dynamically change the mode of operation for systems that require more than a single mode of operation. There are three selectable modes of operation:

- AUTO mode: pulse frequency modulation (PFM) operation is enabled during light load and diode emulation prevents reverse current through the inductor. See also Section 7.4.2.2.
- FPWM mode: in FPWM mode, diode emulation is disabled if the input voltage is less than $VIN_{OVP(R)}$, allowing current to flow backwards through the inductor. This action allows operation at full frequency even without load current. See also Section 7.4.2.3.
- SYNC mode: the internal clock aligns to an external signal applied to the MODE/SYNC pin. The frequency of the external clock must be within the range of 1 × to 2 × the frequency set by the RT resistor. The high level of the external clock must be greater than or equal to V_{IH_CLK}, and the low level of the external clock must be less than or equal to V_{IL_CLK}. The external clock must not exceed the MODE/SYNC pin rating provided in . As long as output voltage can be regulated at full frequency and is not limited by minimum off time or minimum on time, the clock frequency is matched to the frequency of the signal applied to the MODE/SYNC pin. While the device is in SYNC mode, the device operates as though in FPWM mode. Diode emulation is disabled, allowing the frequency applied to the MODE/SYNC pin to be matched without a load.

To dynamically change between modes of operation, a valid sync signal must be applied. The following table shows a summary of the pulse dependent mode selection settings.

Table 7-1. Pulse-Dependent Mode Selection Settings

MODE/SYNC INPUT	MODE
> V_{IH_FPWM}	FPWM with spread spectrum factory setting
< V_{IL_FPWM}	AUTO mode with spread spectrum factory setting
Synchronization clock	SYNC mode

If dynamically switching between modes of operation is not needed, this pin can be held at a constant voltage resulting in a fixed mode of operation. For auto mode, this pin can be short circuited to PGND or pulled below V_{IL_FPWM}. For FPWM mode, this pin can be short circuited to the RT pin or pulled up to V_{IH_FPWM} with an external voltage source. See also Section 6.5.

7.3.5 Output Voltage Selection

The LMR61430-Q1 allows users to configure the output voltage of the LMR61430-Q1 to be either fixed or adjustable depending on the presence of a feedback resistor divider connected to the FB pin. The fixed output voltage is determined based on the orderable part number. See also Section 4. If fixed output voltage is desired, the FB pin can be shorted directly to the output voltage rail. There must be less than 1Ω between the FB pin and the output voltage rail for the device to enter into fixed output voltage. If an adjustable output voltage is desired, the parallel combination of the top and bottom feedback resistors must exceed 3kΩ. After the top feedback resistor is selected, R_{FBT}, the following equation can be used to select the bottom feedback resistor, R_{FBB}.

$$R_{FBB} = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R_{FBT} \quad (4)$$

Where V_{FB} is typically 1V.

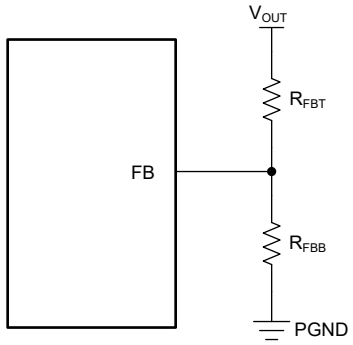


Figure 7-3. Feedback Resistor Setup for Adjustable VOUT

7.3.6 Current Limit

The LMR61430-Q1 uses two current limits to limit the total load current delivered to the output. These limits are known as the high-side peak current limit (I_{HS-LIM}) and the low-side valley current limit (I_{LS-LIM}). After I_{HS-LIM} is reached, the high-side MOSFET is turned off and the low side MOSFET is turned ON until the inductor current falls below I_{LS-LIM}. This action can result in a reduction in switching frequency and can be referred to as soft current limit. Because of the inductor current is limited to switch between I_{HS-LIM} and I_{LS-LIM}, the maximum output current is very close to the average between these two values. If the load demands a current that is greater than the maximum output current, the output voltage decreases. If the output voltage decreases such that the voltage on the FB pin drops below V_{HIC}, then the device enters into hiccup mode. See also Section 7.3.7.

The high-side current limit in LMR61430-Q1 varies as the duty cycle varies. This behavior is characteristic of peak current mode control and helps avoid subharmonic oscillation at higher duty cycles. Figure 7-4 shows the typical high-side current limit.

The LMR61430-Q1 also implements a negative current limit ($I_{LS-NEG-LIM}$) to limit the amount of current the low-side MOSFET can sink. After the negative current limit is reached, the low-side MOSFET turns off.

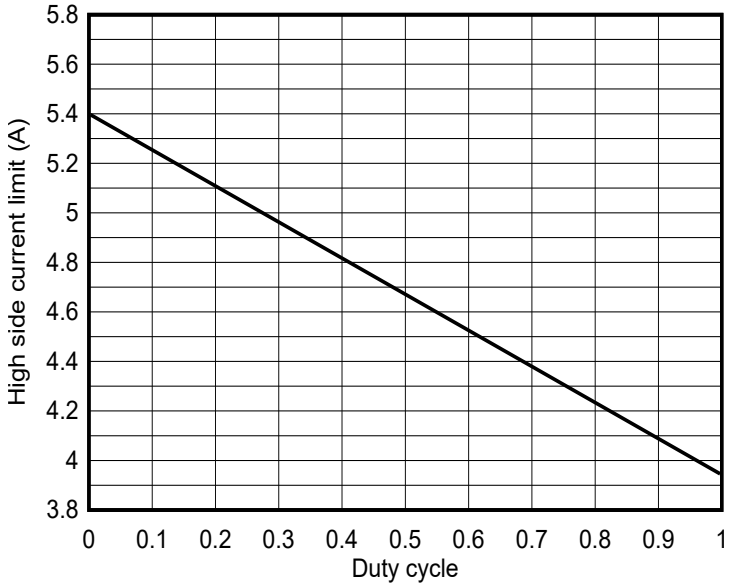


Figure 7-4. Typical High-Side Current Limit I_{HS-LIM} as a Function of Duty Cycle D

7.3.7 Hiccup Mode

To prevent excessive heating and power consumption under sustained short-circuit conditions, a hiccup mode is included. If an over current condition is maintained, the LMR61430-Q1 device shuts off the output and waits for approximately 85ms, after which the LMR61430-Q1 restarts operation by activating soft start.

The LMR61430-Q1 enters into hiccup mode of operation after the following conditions are met:

- The soft-start sequence has completed
- The voltage on FB pin drops below V_{HIC}

Hiccup mode of operation is categorized by periods of non-switching followed by periods of switching where the device tries to startup and regulate the output voltage to the desired set point. After the fault on the output is removed, the device enters soft start and starts up normally. See also Section 7.3.2 for details on soft start.

7.3.8 Power-Good Function

The power-good function of the LMR61430-Q1 can be used to reset a system microprocessor whenever the output voltage is out of regulation or to facilitate power sequencing of down stream components. This feature is an optional feature that is implemented by including a pullup resistor between the PG pin and an excellent voltage supply. See also the *Recommended Operating Conditions* table for the recommended range of pullup reference voltage.

The power-good output is valid after the soft-start sequence has completed and after the input voltage has risen above $V_{IN(PG-VALID)}$. After both of these conditions are met, the voltage between PG and GND indicates whether the output voltage is within regulation or not. A logic HIGH signal indicates that the output voltage is within regulation while a logic LOW signal represents that the output voltage is not in regulation. A deglitch filter has been included to make sure that spurious glitches on the output voltage do not effect the PG pin output.

The PG pin is pulled low under the following conditions:

- Output voltage is higher than the PG overvoltage rising threshold ($V_{PG-OVP(R)}$) for a duration of at least $t_{PG-DEGLITCH}$
- Output voltage falls lower than the PG undervoltage falling threshold ($V_{PG-UV(F)}$) for a duration of at least $t_{PG-DEGLITCH}$

After the PG pin has been pulled low following a fault condition at the output, the PG pin voltage must remain low for at least $t_{PG-DEASSERT}$ or about 2ms (typical). After $t_{PG-DEASSERT}$ has passed, one of the following conditions must be satisfied for the PG pin voltage to be pulled up:

- Assuming recovery form an undervoltage fault, the output voltage must rise higher than the PG undervoltage rising threshold ($V_{PG-UV(R)}$) and remain below the over-voltage rising threshold ($V_{PG-OVP(R)}$) for a duration of at least $t_{PG-DEGLITCH}$.
- Assuming recovery from an overvoltage fault, the output voltage must fall lower than the PG overvoltage falling threshold ($V_{PG-OVP(F)}$) and remain above the undervoltage falling threshold for a duration of at least $t_{PG-DEGLITCH}$.

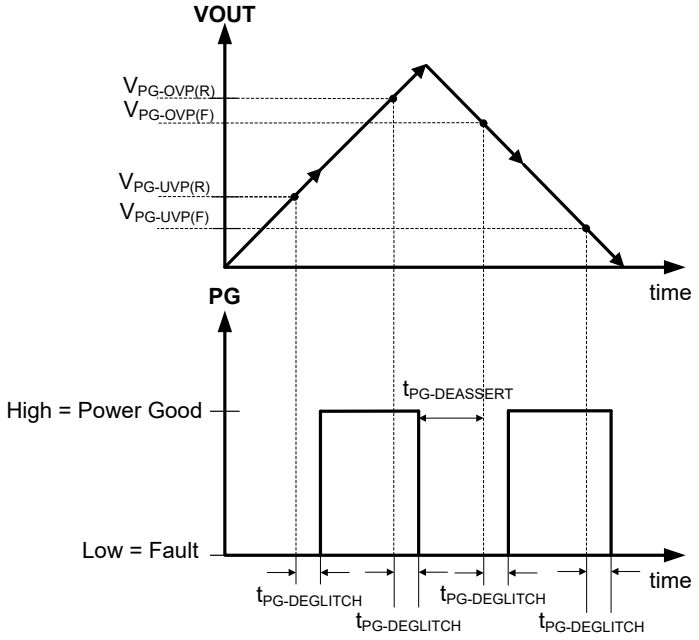


Figure 7-5. Power-Good Thresholds

7.4 Device Functional Modes

7.4.1 Shutdown

The LMR61430-Q1 shuts down most internal circuitry and both high-side and low-side power switches connected to the switch node under any of the following conditions:

1. EN is below $V_{EN-TH(R)}$
2. VIN is below $VIN_{UVLO(R)}$
3. Junction temperature exceeds T_{SD}

Note that the above conditions have hysteresis. Also, PG remains active to a very low input voltage, $V_{IN(PG-VALID)}$.

7.4.2 Active Mode

The LMR61430-Q1 is in an active mode whenever the EN pin voltage has risen above $V_{EN-TH(R)}$, the input voltage exceeds $VIN_{UVLO(R)}$, and no other fault conditions are present. The simplest way to enable the LMR61430-Q1 is to connect the EN pin to VIN, which allows self start-up when the applied input voltage exceeds the $VIN_{UVLO(R)}$.

In active mode, the LMR61430-Q1 is in one of the following modes:

- Continuous conduction mode (CCM) with fixed switching frequency when the load current is above half of the inductor current ripple
- Auto mode - light load operation: pulse frequency modulation (PFM) where switching frequency is reduced at light load
- FPWM mode - light load operation: CCM mode when the load current is lower than half of the inductor current ripple

- Minimum on-time: at high input voltage and low output voltages, the switching frequency is reduced to maintain regulation
- Dropout mode: when switching frequency is reduced to minimize voltage dropout between input and output

7.4.2.1 Continuous Conduction Mode (CCM)

In CCM, the LMR61430-Q1 supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) switches with varying duty cycle (D). During the HS switch on time, the SW pin voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current, i_L, increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the V_{SW} to swing below ground by the voltage drop across the LS switch. The converter loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on time of the HS switch over the switching period:

$$D = \frac{T_{ON}}{T_{SW}} \tag{5}$$

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = \frac{V_{OUT}}{V_{IN}} \tag{6}$$

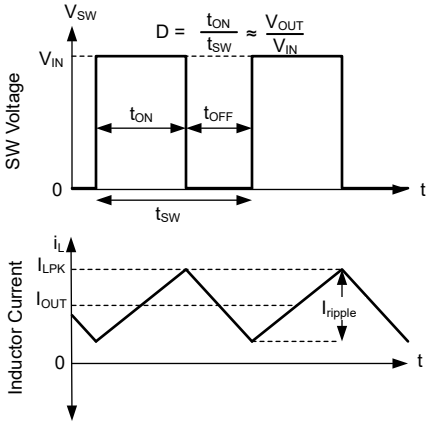


Figure 7-6. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

7.4.2.2 Auto Mode - Light Load Operation

If MODE/SYNC voltage is below $V_{IL(MODE/SYNC)}$, reverse current in the inductor is not allowed – this feature is called diode emulation (DEM). DEM occurs when the load current is less than half of the inductor ripple current. After the inductor current falls below the zero-cross current limit, the LS FET turns off and inductor current flows through the body diode of the LS FET. After current is reduced to a low value with fixed input voltage, on time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called pulse frequency modulation (PFM) mode regulation.

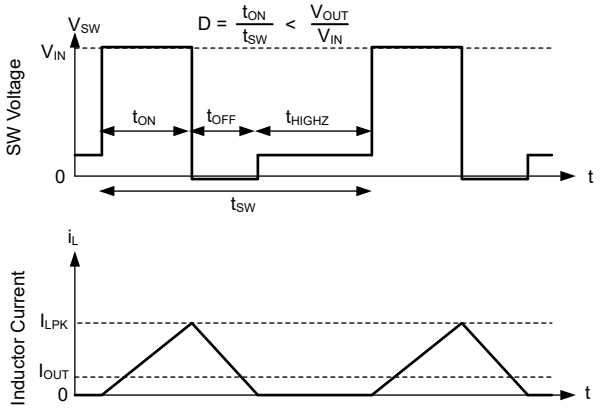


Figure 7-7. PFM Operation

In PFM operation, a small positive DC offset can be observed on the output voltage as the output capacitors become overcharged due to lack of load. If this DC offset on V_{OUT} is not acceptable, a dummy load at V_{OUT} or FPWM mode can be used to reduce or eliminate this offset. This offset typically does not exceed 1% of V_{OUT} that the device regulates to while heavily loaded.

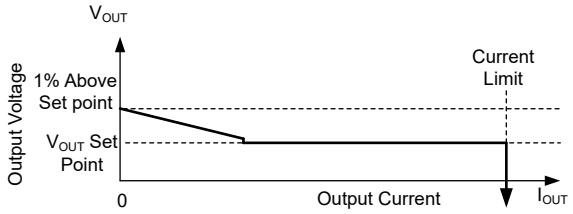


Figure 7-8. Steady State Output Voltage vs Output Current in Auto Mode

7.4.2.3 FPWM Operation - Light Load Operation

In forced pulse width modulation (FPWM) mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry. See also Section 6.5.

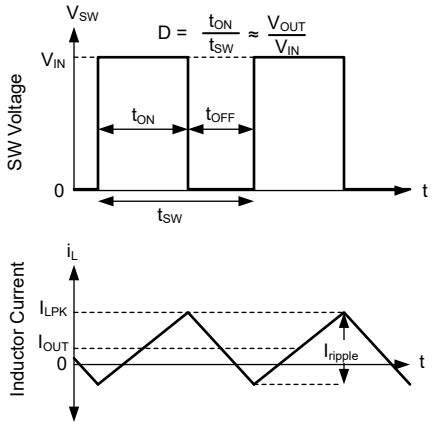


Figure 7-9. FPWM Mode Operation

FPWM mode can be achieved in any of the following ways:

- Connect MODE/SYNC directly to RT pin.
- Apply an external voltage across MODE/SYNC and PGND that is greater than $V_{IH(MODE/SYNC)}$.
- Apply an appropriate external clock signal. See also Table 7-1.

Under operating conditions where the minimum on-time or minimum off-time can be exceeded, the frequency reduces even while operating in FPWM to maintain minimum timing specifications. Additionally, in cases where the input voltage exceeds $VIN_{OVP(R)}$ the LMR61430-Q1 prevents negative currents from flowing through the inductor and the LMR61430-Q1 implements PFM switching. After the input voltage falls below $VIN_{OVP(F)}$, the device again operates in FPWM and allows negative inductor currents.

7.4.2.4 Minimum On-Time

Minimum on-time refers to the minimum amount of time the high-side MOSFET can turn on. The LMR61430-Q1 regulates the output voltage even if the input-to-output voltage ratio requires an on-time less than the minimum on-time, t_{ON-MIN}, for the given frequency setting. The LMR61430-Q1 accomplishes this action by folding back the switching frequency to support the same input-to-output voltage ratio while maintaining an on-time of t_{ON-MIN}. The LMR61430-Q1 can support a minimum on-time of 30ns (typical). Use Equation 7 to estimate the on-time for a given operating condition.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \tag{7}$$

Where:

- t_{ON} = high-side MOSFET on-time
- V_{OUT} = output voltage
- V_{IN} = input voltage
- f_{SW} = switching frequency

7.4.2.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency, duty cycle is limited by minimum off time. After this limit is reached as Figure 7-10 shows, if clock frequency is to be maintained, the output voltage falls. Instead of allowing the output voltage to drop, the LMR61430-Q1 extends the high-side switch on time past the end of the clock cycle until the needed peak inductor current is achieved. The clock is allowed to start a new cycle after peak inductor current is achieved or after a predetermined maximum on time of approximately 10µs passes. As a result, after the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off time, frequency drops to maintain regulation. After the input voltage increases beyond the output voltage setpoint, the output voltage increases as though in soft start as described in Section 7.3.2.

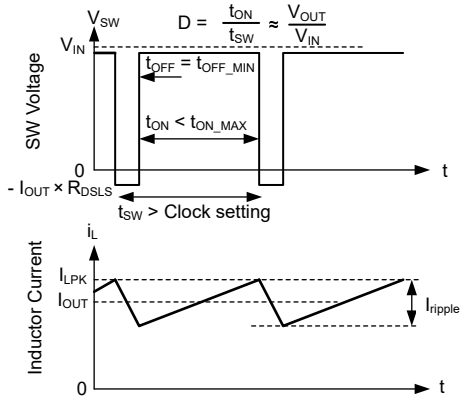


Figure 7-10. Dropout Waveforms

8 Application and Implementation

Note

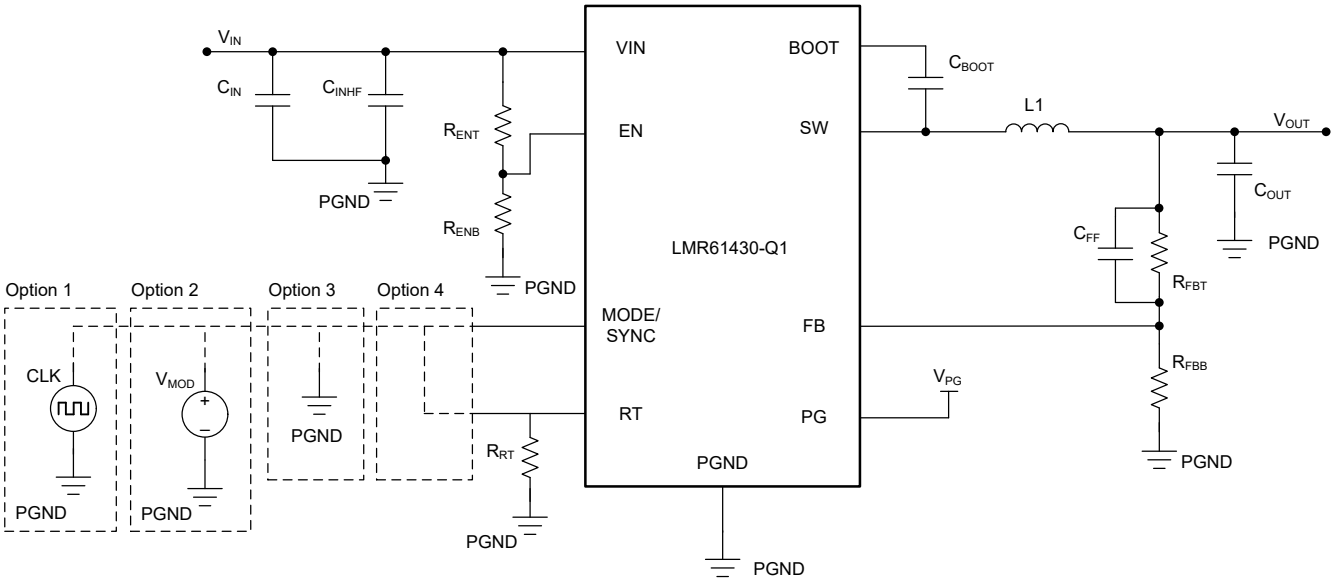
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMR61430-Q1 is a step-down DC–DC converter, typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3A. The following design procedure can be used to select components for the LMR61430-Q1.

8.2 Typical Application

Figure 8-1 shows a typical application circuit for the LMR61430-Q1. This device is designed to function over a wide range of external components and system parameters. As a quick-start guide, Table 8-1 provides typical component values for a range of the most common operating conditions.



Option 1	To synchronize to an external clock, drive the MODE/SYNC pin directly from the clock.
Option 2	A suitable voltage V_{MOD} can be used at the MODE/SYNC to dynamically change between auto and FPWM modes.
Option 3	Ground the MODE/SYNC to run the device in auto mode.
Option 4	Connect the MODE/SYNC to RT to run the device in FPWM mode.

Figure 8-1. LMR61430-Q1 Reference Schematic

See also *MODE/SYNC Pin Control*.

Table 8-1. Recommended Passive Components

F_{SW} (kHz)	V_{OUT} (V)	I_{OUT} (A)	L (µH)	C_{OUT} (1)	RFBT (kΩ)	RFBB (kΩ)	C_{IN} (µF)	C_{BOOT} (nF)	RT (kΩ)
2000	3.3	3	1.5	22	SHUNT	DNP	4.7	100	15
2000	5	3	1.5	22	SHUNT	DNP	4.7	100	15

(1) Rated capacitance

8.2.1 Design Requirements

For this design example, use the parameters listed in the following table as the input parameters.

Table 8-2. Design Parameters

DESIGN PARAMETER	VALUE	COMMENT
Input voltage range	12V (typical), 4V to 36V	This converter runs continuously up to 36V.
Output voltage	3.3V	Fixed option used
Output current range	4A	
Switching frequency	2MHz	
Light load mode	Switchable	
Spread spectrum	Enabled	Factory option

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency Selection

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses and typically results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. For this example, 2MHz is used. See also Section 7.3.3 for details on RT resistor selection.

8.2.2.2 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, use the maximum device current. Use Equation 8 to calculate the value of inductance. The constant K is the percentage of inductor current ripple. For this example, select K = 0.2 and find an inductance of L = 1.5µH. Select the standard value of 1.5µH.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{sw} \times K \times I_{OUTmax}} \times \frac{V_{OUT}}{V_{IN}} \quad (8)$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, $I_{HS\text{-}LIM}$ (see Section 6.5). This size makes sure that the inductor does not saturate, even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, $I_{LS\text{-}LIM}$, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This action can lead to component damage. Do not allow the inductor to saturate. Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, powered iron cores have more core losses at frequencies above about 1MHz. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

Use Equation 9 to find the minimum inductance value to avoid subharmonic oscillations:

$$L_{min} = M \times \frac{V_{OUT}}{f_{sw}} \quad (9)$$

Where:

- M = 0.34

While Equation 9 defines the theoretical minimum inductance required to avoid subharmonic instability, TI strongly recommends to select an inductor value at least *twice* the calculated minimum. This selection provides additional design margin to account for component tolerances, temperature variations, and transient response requirements.

8.2.2.3 Output Capacitor Selection

The LMR61430-Q1 is designed to optimize the required output capacitance while also allowing for high performance. This section describes the theory to calculate the required output capacitance to achieve a certain set of design parameters.

The peak current mode control scheme of the LMR61430-Q1 device allows operation over a wide range of inductor and output capacitor combinations. The output capacitance is responsible for maintaining the desired output voltage during operation. The output capacitance impacts several key performance factors including:

- The amount of output voltage ripple during steady state operation
- The overshoot and undershoot of the output voltage when a load transient occurs
- Loop stability

During steady state operation, the inductor supplies a triangular current to the load. The AC portion of this triangular current is filtered out by the output capacitance while the DC portion passes through to the load. The AC current through the output capacitance and the equivalent series resistance (ESR) of this capacitance both contribute to the output voltage ripple. Use the following equation to estimate the amount of peak to peak output voltage ripple required for a given output capacitance:

$$V_{ripple} \approx \Delta I_L \times \sqrt{ESR^2 + \frac{1}{(8 \times f_{sw} \times C_{OUT})^2}} \quad (10)$$

Where:

- ΔI_L = the peak to peak inductor current

See Table 8-1 for typical output capacitor values for 3.3V and 5V output voltage applications. In this example, a single 22µF multilayer ceramic capacitor is used. For other output voltage and switching frequency designs, WEBENCH can be used as a starting point for selecting the value of the output capacitor.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic capacitor placed on the output can help reduce high-frequency noise. Small-case size ceramic capacitors in the range of 10nF to 100nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

Most ceramic capacitors deliver far less capacitance than the rating of the capacitor indicates. Be sure to check any capacitor selected for initial accuracy, temperature derating, and voltage derating. Table 8-1 has been generated assuming typical derating of 16V, X7R, automotive grade capacitors. If lower voltage rated, non-automotive grade, or lower temperature rated capacitors are used, more capacitors than listed are likely to be needed.

8.2.2.4 Input Capacitor Selection

Input capacitors serve two important functions. The first is to reduce input voltage ripple into the LMR61430-Q1 and the input filter of the system. The second is to reduce high frequency noise. These two functions are implemented most effectively with separate capacitors. See the following table.

Table 8-3. Input Capacitor

CAPACITOR	RECOMMENDED VALUE	COMMENT
C_{IN_HF}	0.1µF	This capacitor is used to suppress high frequency noise originating during switching events. Place the capacitor as close to the LMR61430-Q1 devices as design rules allow. Position is more important than exact capacity. After high frequency propagates into a system, suppressing or filtering can be hard. Because this capacitor is exposed to battery voltage in systems that operate directly off of battery, TI recommends 50V or greater rating.
C_{IN}	4.7µF	This capacitance is used to suppress input ripple and transients due to output load transients. If C_{IN} is too small, input voltage can dip during load transients resetting the system if the system is operated under low voltage conditions. TI recommends 4.7µF adjacent to the LMR61430-Q1 device. Because this capacitor is exposed to battery voltage in systems that operate directly off of battery, TI recommends 50V or greater rating.

The values of C_{IN_HF} and C_{IN} presented in Table 8-3 can be used in most applications. If a certain amount of input voltage ripple is required, use the calculated input capacitance based on Equation 11, but not less than recommended in the above table.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{\Delta V_{IN\_PP} \times f_{sw}} \tag{11}$$

Where:

- D = Duty Cycle = V_{OUT}/V_{IN}
- I_{OUT} = DC output current
- ΔV_{IN_PP} = peak to peak input voltage ripple
- f_{SW} = switching frequency

Use Equation 12 to compare the RMS current rating of the selected input capacitors to make sure the input capacitors are capable of supplying the input switching current.

$$I_{IN\_RMS\_max} = I_{OUT} \times \sqrt{D \times (1 - D) + \frac{1}{12} \times \left(\frac{V_{OUT}}{L \times f_{sw} \times I_{OUT}}\right)^2 \times (1 - D)^2 \times D} \tag{12}$$

8.2.2.5 Bootstrap Capacitor (CBOOT) Selection

The bootstrap capacitor (C_{BOOT}) is connected between the BOOT and SW pins and provides the gate charge for the high-side MOSFET. Place this capacitor as close to the LMR61430-Q1 as design rules allow. TI recommends a high quality ceramic capacitor of 100nF and at least 10V.

8.2.2.6 FB Voltage Divider for Adjustable Output Voltages

The LMR61430-Q1 device can be configured to operate in either fixed or adjustable output voltage modes. For fixed output voltages as specified by the device orderable part number, simply connect the output voltage rail directly to the FB pin. When other output voltages are required, a resistor divider between the output voltage rail and ground with the FB pin as the center point set the output. Use the following equation to calculate the output voltage given a specific feedback divider.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FBT}}{R_{FBB}}\right) \tag{13}$$

Alternatively, if the output voltage and R_{FBT} are already known, use the following equation to calculate the value of R_{FBB}.

$$R_{FBB} = R_{FBT} \times \frac{V_{FB}}{V_{OUT} - V_{FB}} \tag{14}$$

Note that typically 100kΩ is used for R_{FBT}.

8.2.2.6.1 Feedforward Capacitor (CFF) Selection

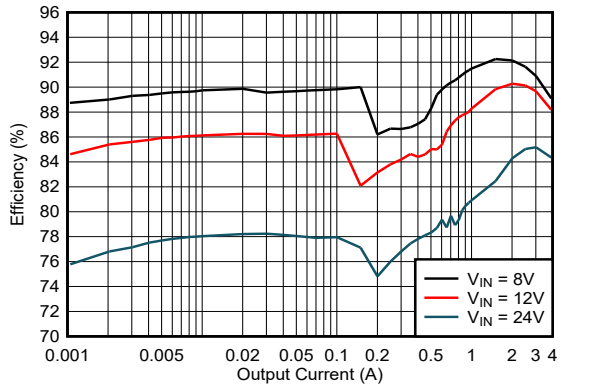
In cases where an adjustable output voltage configuration is required, a feedforward capacitor (CFF) can be placed in parallel with the RFBT to improve transient performance and loop-phase margin. *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* application note is helpful when experimenting with a feedforward capacitor.

8.2.2.7 R_{PG} - PG Pullup Resistor

The PG pin is an open drain output that is used as a monitoring pin. If needed, a 100kΩ can be used to pull up to a suitable voltage supply. See also Section 6.3 for a range of recommended PG pin pullup voltages. Other considerations, such as power consumption, can increase any of the values listed above.

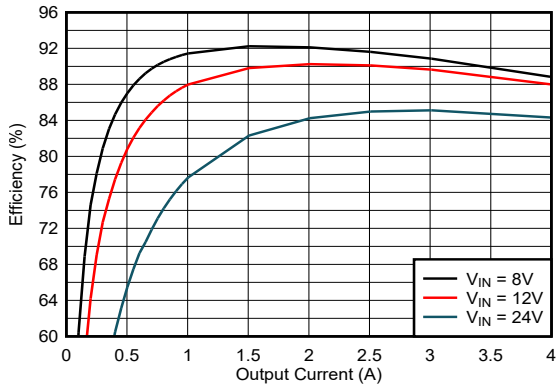
8.2.3 Application Curves

The following characteristics apply to the Figure 8-1 circuit. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12V, T_A = 25°C.



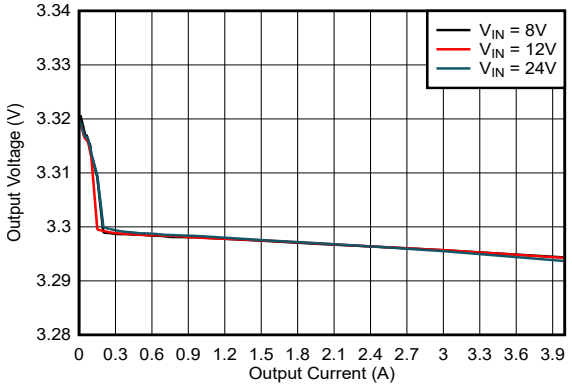
Device type = 4A 3.3V fixed output Mode = Auto
F_{SW} = 2MHz

Figure 8-2. Efficiency



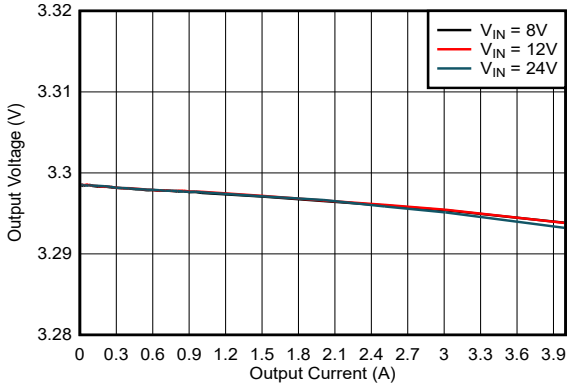
Device type = 4A 3.3V fixed output Mode = FPWM
F_{SW} = 2MHz

Figure 8-3. Efficiency



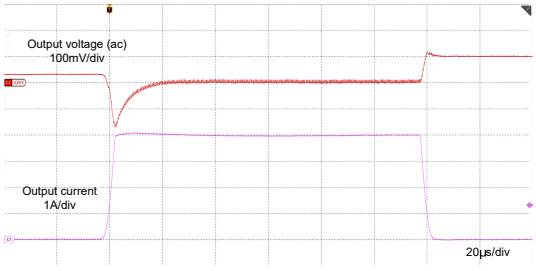
Device type = 4A 3.3V output Mode = Auto
F_{SW} = 2MHz

Figure 8-4. Load Regulation



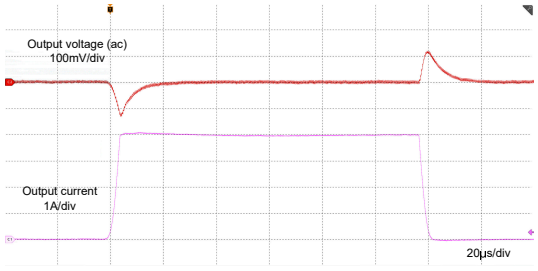
Device type = 4A 3.3V output Mode = FPWM
F_{SW} = 2MHz

Figure 8-5. Load Regulation



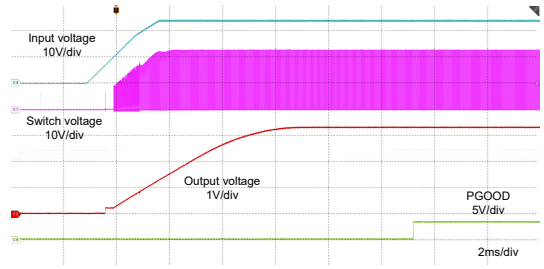
LMR61440-Q1 3.3V fixed output Mode = Auto
F_{SW} = 2MHz C_{OUT} = 1 × 22µF

Figure 8-6. 0A to 4A Load Transient - Auto Mode



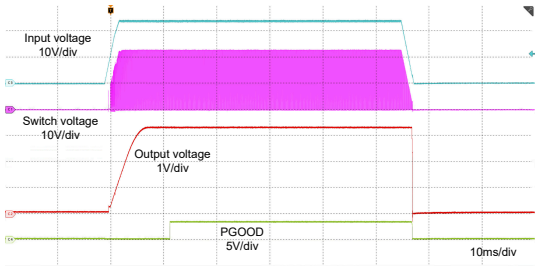
LMR61440-Q1 3.3V fixed output Mode = FPWM
F_{SW} = 2MHz C_{OUT} = 1 × 22µF

Figure 8-7. 0A to 4A Load Transient - FPWM Mode



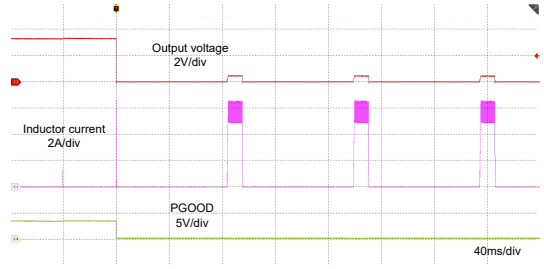
LMR61440-Q1 3.3V fixed output Mode = FPWM
F_{SW} = 2MHz V_{IN} = 24V I_{OUT} = 3A

Figure 8-8. Start-Up Operation



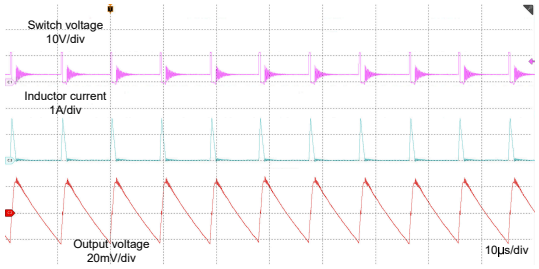
LMR61440-Q1 3.3V fixed output Mode = FPWM
F_{SW} = 2MHz V_{IN} = 24V I_{OUT} = 3A

Figure 8-9. Start-Up and Shut-Down Behavior



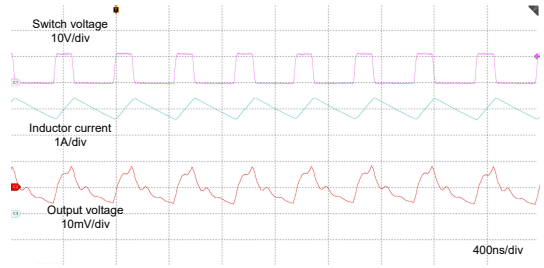
LMR61440-Q1 3.3V fixed output Mode = Auto
F_{SW} = 2MHz V_{IN} = 24V

Figure 8-10. Short-Circuit Applied



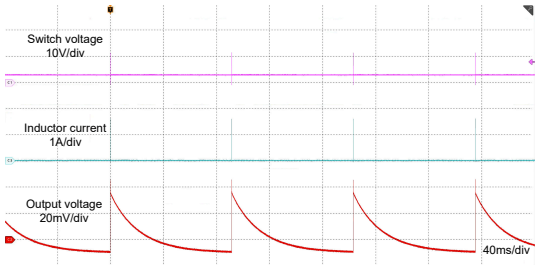
LMR61440-Q1 3.3V output Mode = Auto
I_{OUT} = 100mA F_{SW} = 2MHz V_{IN} = 12V

Figure 8-11. Steady State Waveform



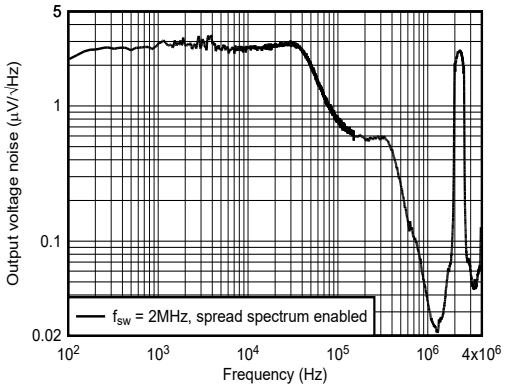
LMR61440-Q1 3.3V output Mode = FPWM
I_{OUT} = 4A F_{SW} = 2MHz V_{IN} = 12V

Figure 8-12. Steady State Waveform



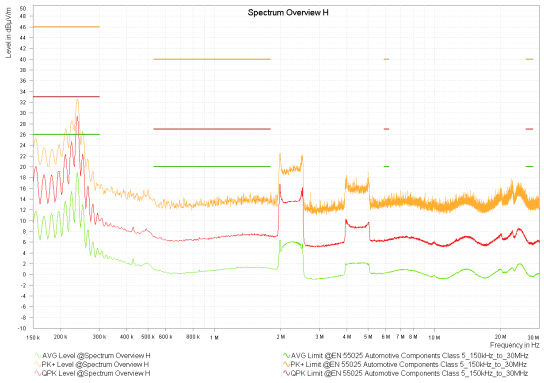
LMR61440-Q1 3.3V output Mode = Auto
I_{OUT} = 0A F_{SW} = 2MHz V_{IN} = 12V

Figure 8-13. Steady State Waveform



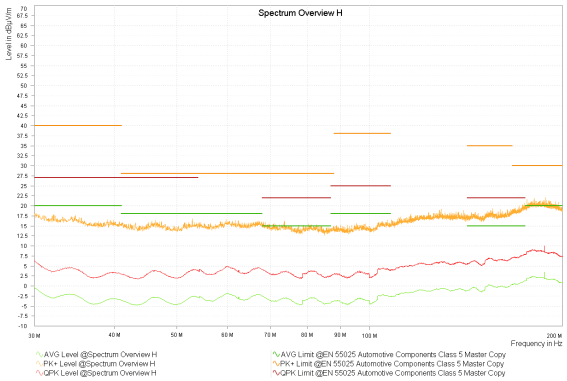
LMR61440-Q1 3.3V output I_{OUT} = 4A
F_{SW} = 2MHz V_{IN} = 12V

Figure 8-14. Output Voltage Noise Spectral Density



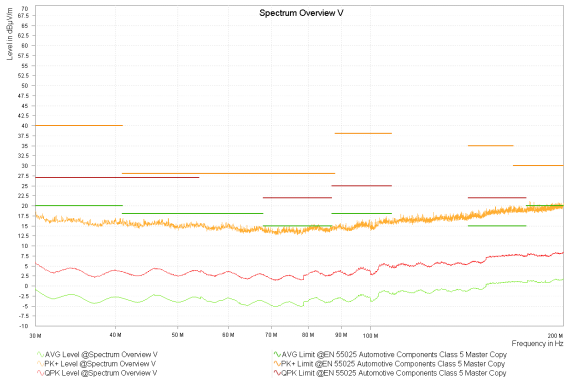
V_{IN} = 12V V_{OUT} = 3.3V F_{SW} = 2MHz
I_{OUT} = 4A

Figure 8-15. Radiated EMI (Monopole) vs CISPR 25 Limits



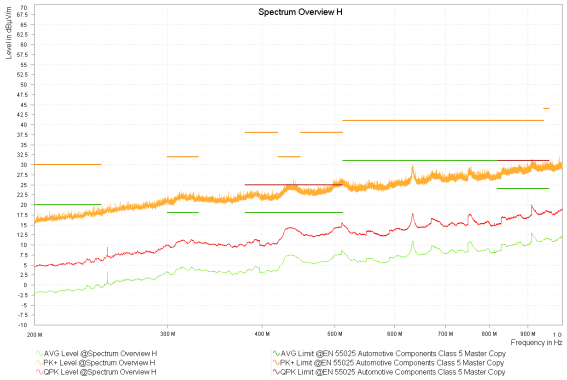
V_{IN} = 12V V_{OUT} = 3.3V F_{SW} = 2MHz
I_{OUT} = 4A

Figure 8-16. Radiated EMI (Bicon Horizontal) vs CISPR 25 Limits



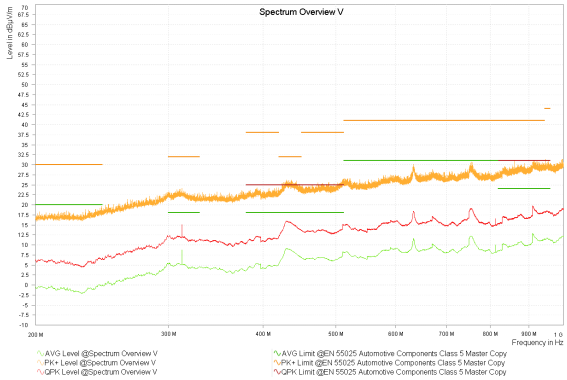
V_{IN} = 12V V_{OUT} = 3.3V F_{SW} = 2MHz
I_{OUT} = 4A

Figure 8-17. Radiated EMI (Bicon Vertical) vs CISPR 25 Limits



V_{IN} = 12V V_{OUT} = 3.3V F_{SW} = 2MHz
I_{OUT} = 4A

Figure 8-18. Radiated EMI (Log Periodic Horizontal) vs CISPR 25 Limits



V_{IN} = 12V V_{OUT} = 3.3V F_{SW} = 2MHz
I_{OUT} = 4A

Figure 8-19. Radiated EMI (Log Periodic Vertical) vs CISPR 25 Limits

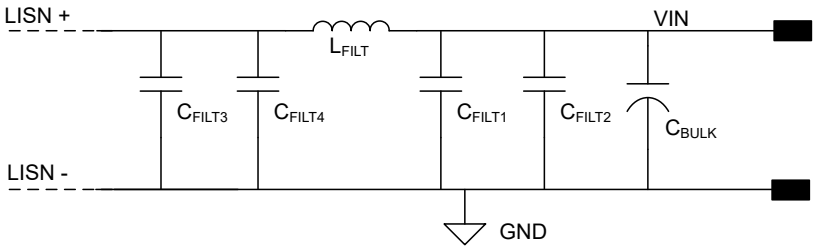


Figure 8-20. Typical Input EMI Filter Schematic

Table 8-4. Typical EMI Filter Components

F_{SW}(kHz)	C_{FILT1}(µF)	C_{FILT2}(µF)	C_{FILT3}(µF)	C_{FILT4}(µF)	L_{FILT}(µH)	C_{BULK}(µF)
2000	2.2	2.2	2.2	2.2	2.2	47

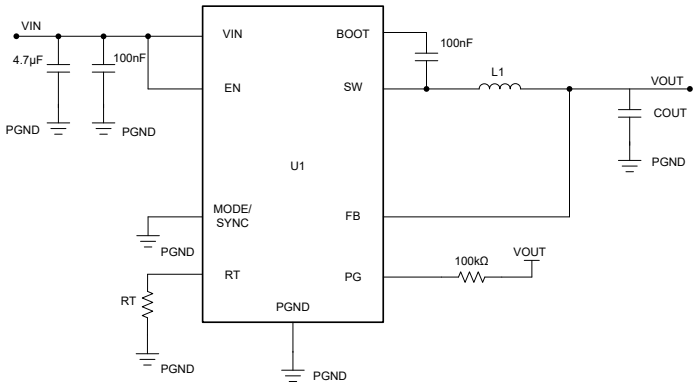


Figure 8-21. Example Application Circuit

Table 8-5. BOM for Typical Applications Curves

U1	F_{SW} (kHz)	V_{OUT}	L1 (µH)	NOMINAL C_{OUT} (µF)	RT(kΩ)
LMR614403SRAKRQ1	2000	3.3	1.5	1 × 22	15

8.3 Power Supply Recommendations

The characteristics of the input supply must be compatible with the specifications found in this datasheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. Use the following equation to calculate the average input current.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (15)$$

where

η is the efficiency.

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an underdamped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to limit the distance from the input supply to the regulator or plan to use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help dampen the input resonant circuit and reduce

any overshoots. A value in the range of 20µF to 100µF is typically sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This action can lead to instability, as well as some of the effects mentioned above, unless designed carefully. The *AN-2162 Simple Success With Conducted EMI From DC/DC Converters* application note provides helpful suggestions when designing an input filter for any switching regulator.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). TI does not recommend the use of a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

8.4 Layout

8.4.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the excellent performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent, the EMI performance of the regulator is dependent on the PCB layout. In a buck converter, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in Figure 8-22. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this disrupt, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. Figure 8-23 shows a recommended layout for the critical components of the LMR61430-Q1.

- *Place the input capacitors as close as possible to the VIN and GND terminals.*
- *Use wide traces for the C_{BOOT} capacitor.* Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins.
- *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, the latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and as a heat dissipation path.
- *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- *Provide enough PCB area for proper heat-sinking.* Enough copper area must be used to make sure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
- *Keep the switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies* application note
- *Simple Switcher PCB Layout Guidelines* application note
- *Construction Your Power Supply- Layout Considerations* seminar
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application note

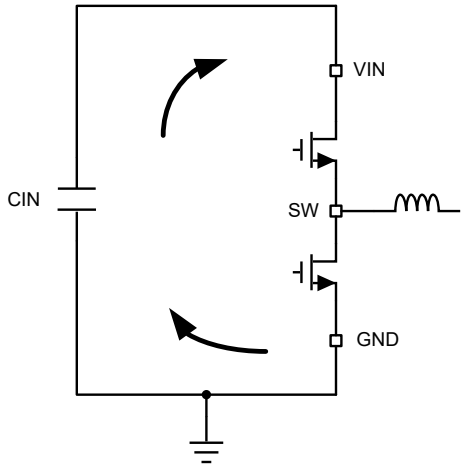


Figure 8-22. Current Loops With Fast Edges

8.4.1.1 Ground and Thermal Plane Considerations

As mentioned above, TI recommends to use one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. A ground plane also provides a quiet reference potential for the control circuitry. The PGND pin is connected to the source of the internal low-side MOSFET switch. This pin must be connected directly to the ground of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations.

TI recommends to provide adequate device heat sinking by using the PGND of the IC as the primary thermal path. Thermal vias must be evenly distributed under the PGND pin. Use as much copper as possible for system ground plane on the top and bottom layers for the best heat dissipation. TI recommends to use a four-layer board with the copper thickness, starting from the top, as: 2oz, 1oz, 1oz, 2oz. A four-layer board with enough copper thickness and proper layout provides low current conduction impedance, proper shielding and lower thermal resistance.

Resources for thermal PCB design:

- *AN-2020 Thermal Design By Insight, Not Hindsight*application note
- *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application note
- *Semiconductor and IC Package Thermal Metrics* application note
- *Thermal Design made Simple with LM43603 and LM43602* application note
- *PowerPAD™ Thermally Enhanced Package* application note
- *PowerPAD™ Made Easy* application brief
- *Using New Thermal Metrics* application note

8.4.2 Layout Example

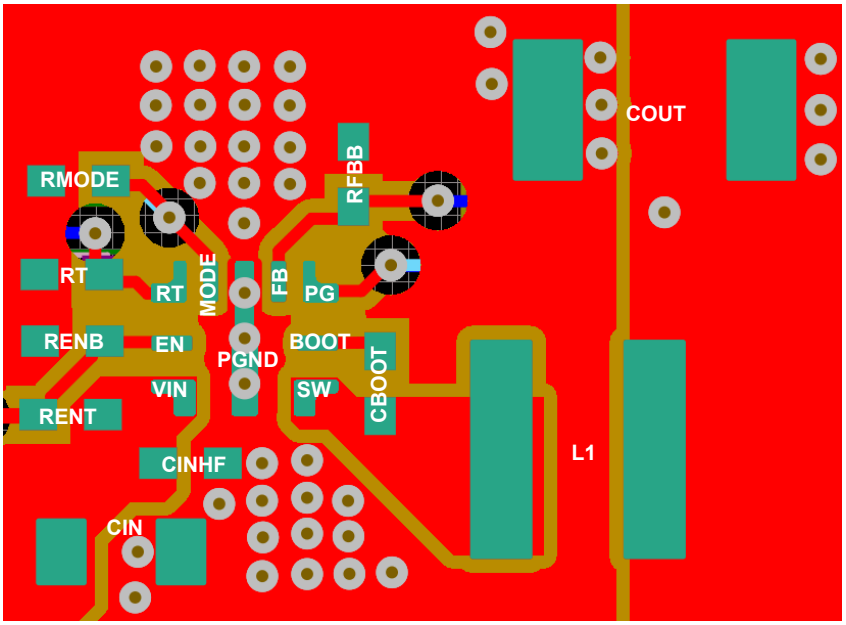


Figure 8-23. Example of Recommended Layout for Fixed Output Voltage Configuration

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.1.2 Device Nomenclature

Figure 9-1 shows the device naming nomenclature of the LMR61430-Q1. See the *Device Comparison Table* for the availability of each variant. Contact a TI sales representatives or visit TI's E2E support forum for detail and availability of other options; minimum order quantities apply.

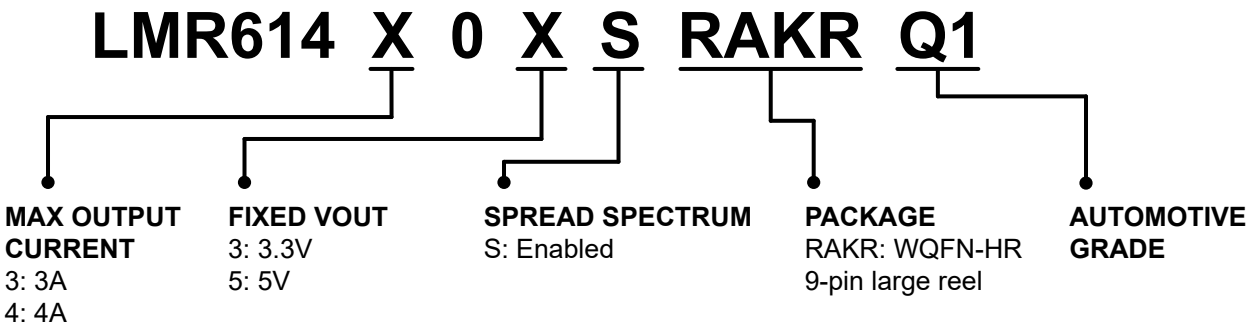


Figure 9-1. Device Naming Nomenclature

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, AN-1149 *Layout Guidelines for Switching Power Supplies* application note
- Texas Instruments, *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x* application note
- Texas Instruments, *Constructing Your Power Supply – Layout Considerations* application note
- Texas Instruments, AN-1229 *Simple Switcher PCB Layout Guidelines* application note
- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *PowerPAD™ Made Easy* application brief
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application note
- Texas Instruments, *Thermal Design made Simple with LM43603 and LM43602* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, AN-2020 *Thermal Design By Insight, Not Hindsight* application note
- Texas Instruments, AN-1520 *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application note
- Texas Instruments, *AN-2162 Simple Success with Conducted EMI for DC-DC Converters* application note
- Texas Instruments, *Understanding and Applying Current-Mode Control Theory* application note
- Texas Instruments, *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
August 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, see also the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMR614303SRAKRQ1	Active	Production	WQFN-HR (RAK) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	133SQ
LMR614305SRAKRQ1	Active	Production	WQFN-HR (RAK) | 9	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	135SQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

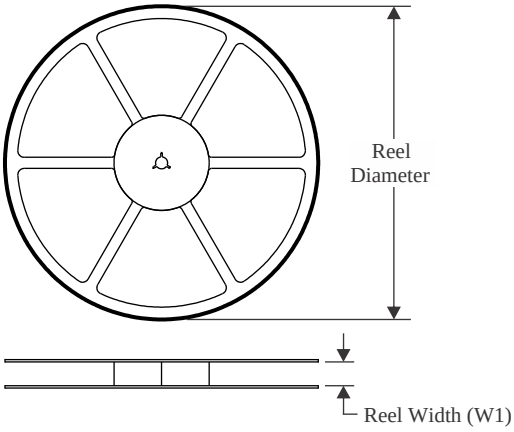
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

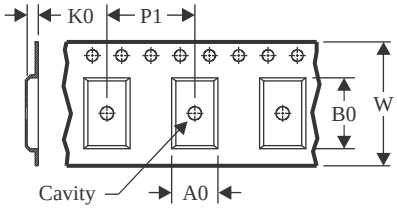
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

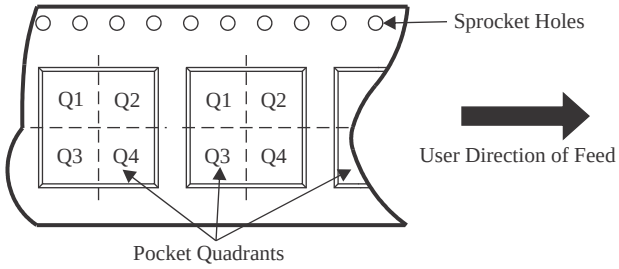


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

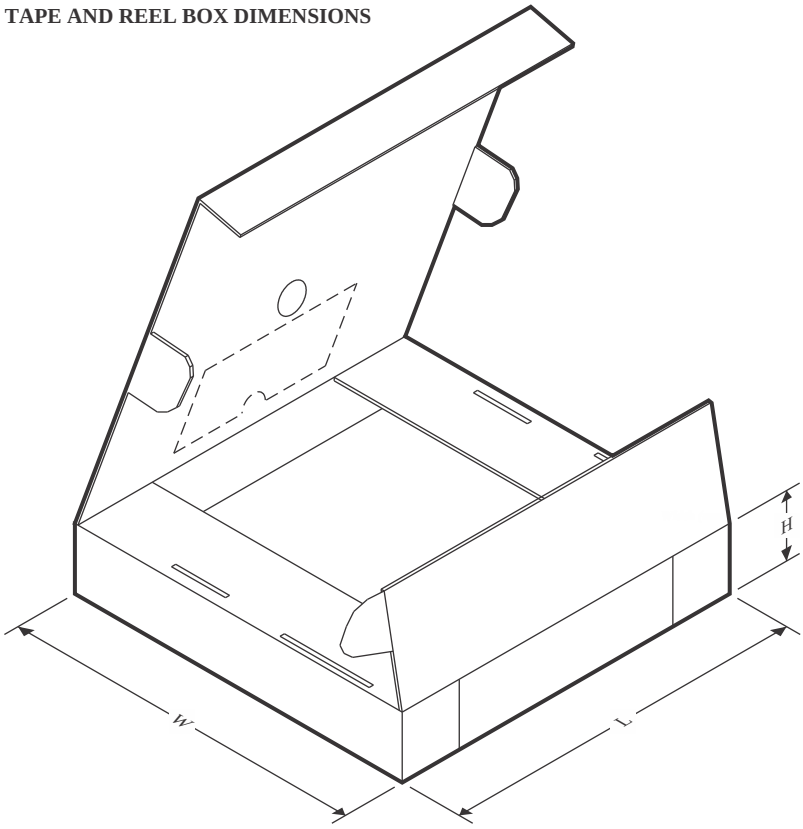
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR614303SRAKRQ1	WQFN-HR	RAK	9	3000	180.0	8.4	2.3	2.8	1.15	4.0	8.0	Q1
LMR614305SRAKRQ1	WQFN-HR	RAK	9	3000	180.0	8.4	2.3	2.8	1.15	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

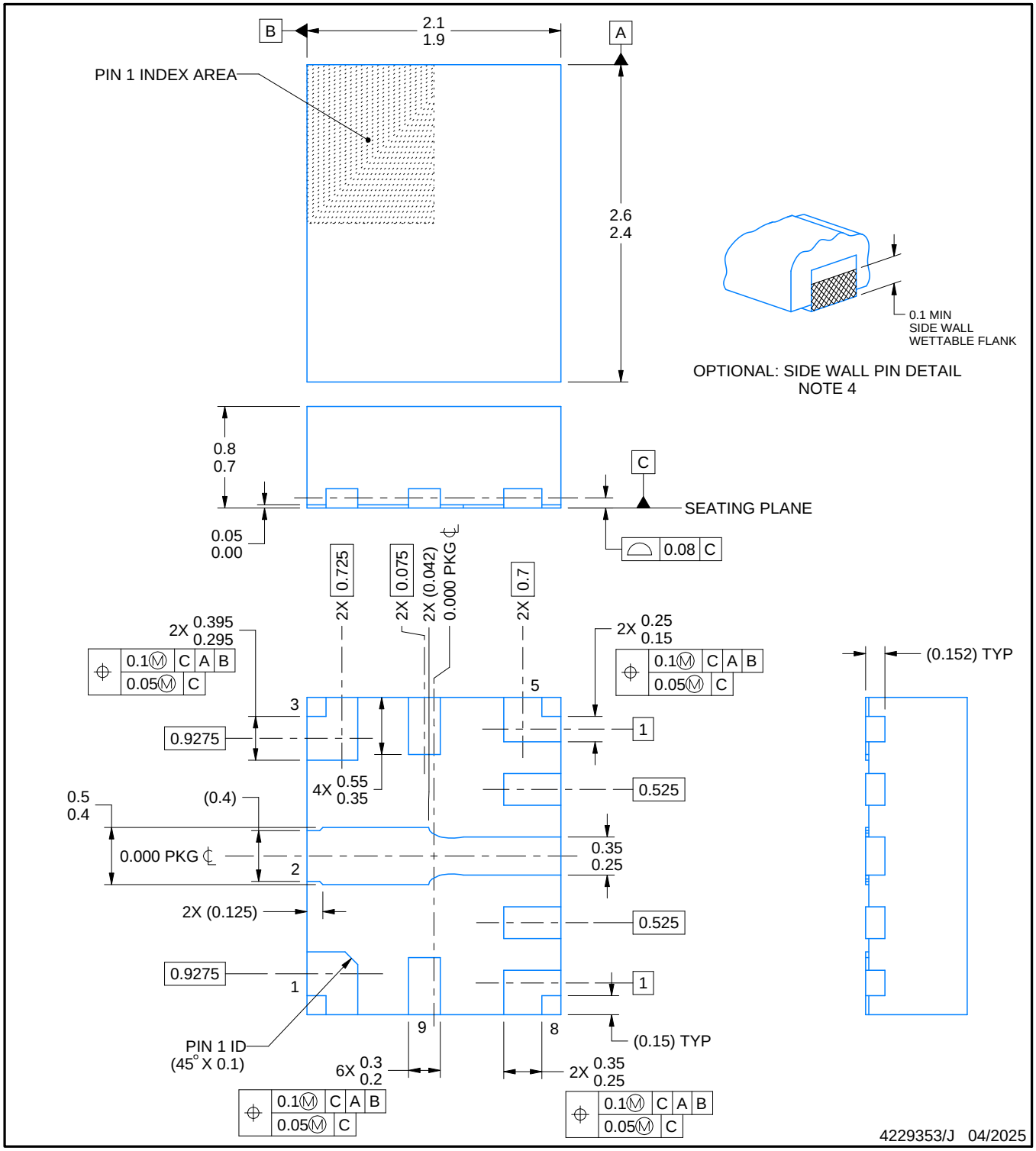
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR614303SRAKRQ1	WQFN-HR	RAK	9	3000	210.0	185.0	35.0
LMR614305SRAKRQ1	WQFN-HR	RAK	9	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RAK0009A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

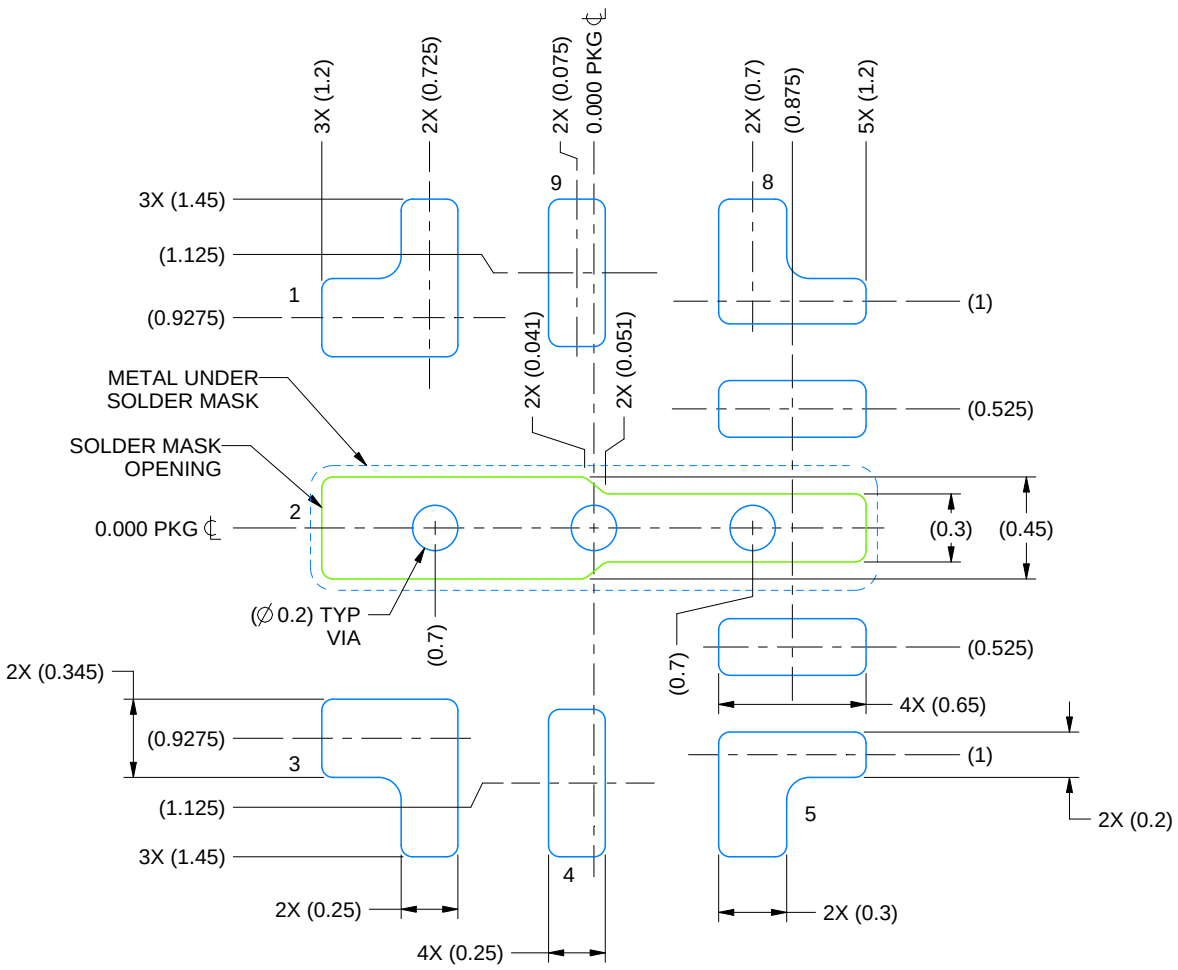
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.

EXAMPLE BOARD LAYOUT

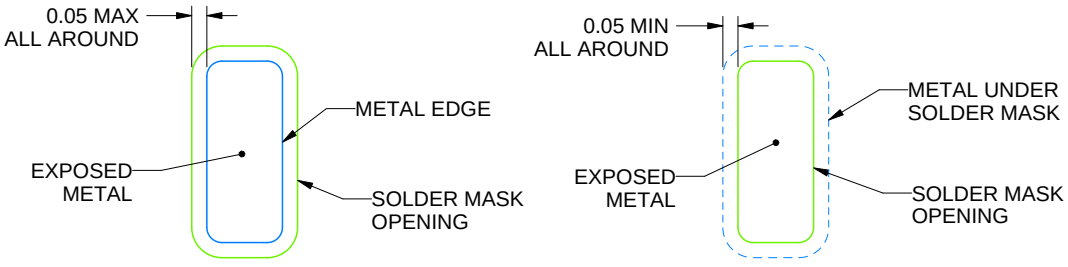
RAK0009A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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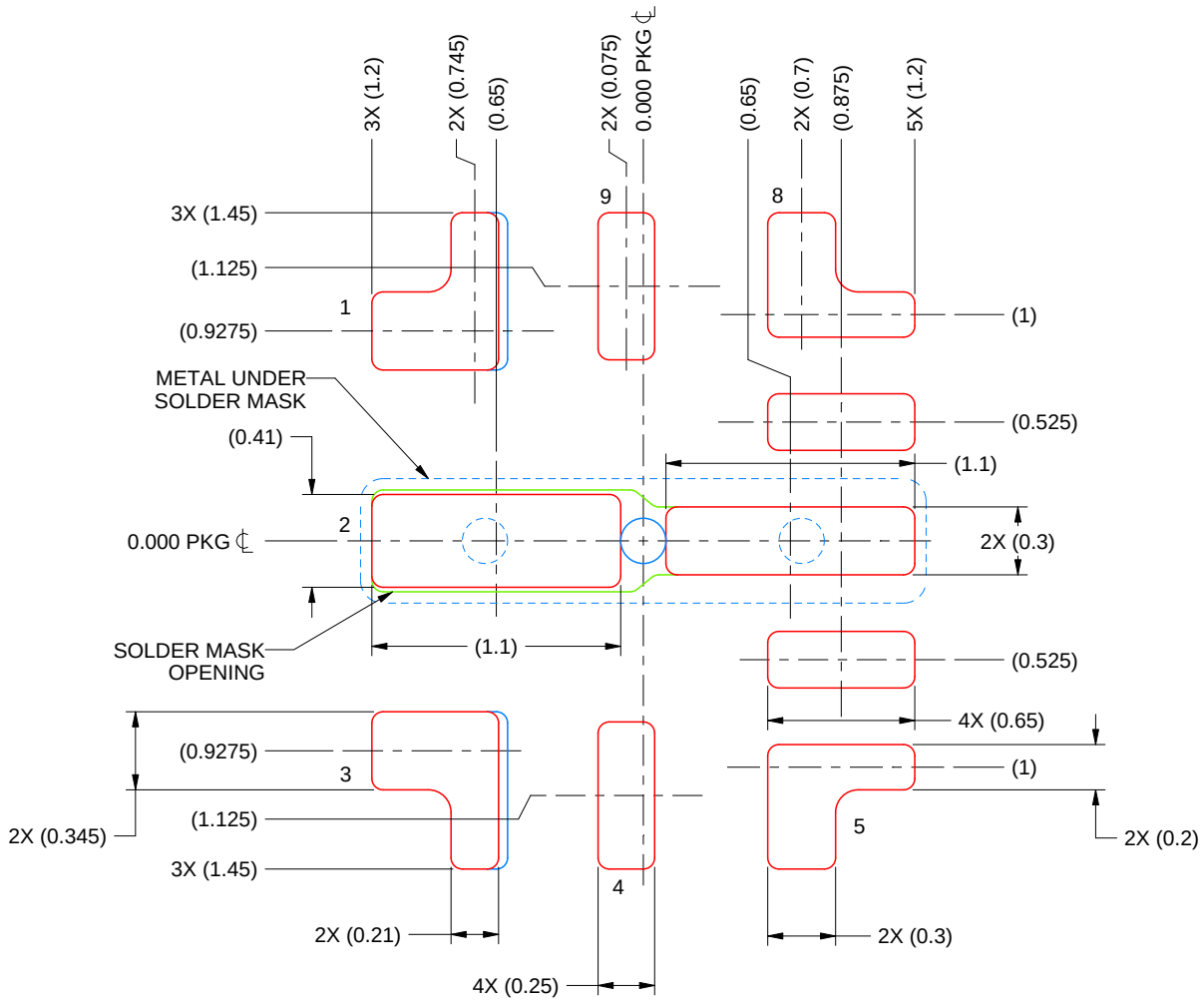
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 30X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS: 1 & 3: 91%
PAD 2: 84%

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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