

## LMP90080-Q1 Multi-Channel 16-Bit Sensor AFE with Background Calibration

Check for Samples: [LMP90080-Q1](#)

### FEATURES

- 16-Bit Low-Power Sigma Delta ADC
- True Continuous Background Calibration at All Gains
- In-Place System Calibration Using Expected Value Programming
- Low-Noise Programmable Gain (1x - 128x)
- Continuous Background Open/Short and Out of Range Sensor Diagnostics
- 8 Output Data Rates (ODR) with Single-Cycle Settling
- 2 Matched Excitation Current Sources from 100  $\mu$ A to 1000  $\mu$ A
- 4-DIFF / 7-SE Inputs
- 2-DIFF / 4-SE Inputs
- 7 General Purpose Input/Output Pins
- Chopper-Stabilized Buffer for Low Offset
- SPI 4/3-Wire with CRC Data Link Error Detection
- 50 Hz to 60 Hz Line Rejection at ODR  $\leq$ 13.42 SPS
- Independent Gain and ODR Selection per Channel
- Supported by WEBENCH® Sensor AFE Designer
- Automatic Channel Sequencer

### KEY SPECIFICATIONS

- ENOB/NFR: Up to 16/16 Bits
- Offset Error (typ): 8.4 nV
- Gain Error (typ): 7 ppm
- Total Noise: <10  $\mu$ V-rms
- Integral Non-Linearity (INL Max):  $\pm$ 1 LSB
- Output Data Rates (ODR): 1.6775 - 214.65 SPS
- Analog Voltage,  $V_A$ : +4.75V to +5.5 V
- Operating Temp Range: -40 to +150°C
- Package: 28 Pin Exposed Pad

### APPLICATIONS

- Temperature and Pressure Transmitters
- Strain Gauge Interface
- Industrial Process Control

### DESCRIPTION

The LMP90080-Q1 is a highly integrated, multi-channel, low-power 16-bit Sensor AFE. The devices feature a precision, 16-bit Sigma Delta Analog-to-Digital Converter (ADC) with a low-noise programmable gain amplifier and a fully differential high impedance analog input multiplexer. A true continuous background calibration feature allows calibration at all gains and output data rates without interrupting the signal path. The background calibration feature essentially eliminates gain and offset errors across temperature and time, providing measurement accuracy without sacrificing speed and power consumption.

Another feature of the LMP90080-Q1 is continuous background sensor diagnostics, allowing the detection of open and short circuit conditions and out-of-range signals, without requiring user intervention, resulting in enhanced system reliability.

Two sets of independent external reference voltage pins allow multiple ratiometric measurements. In addition, two matched programmable current sources are available in the LMP90080-Q1 to excite external sensors such as resistive temperature detectors and bridge sensors. Furthermore, seven GPIO pins are provided for interfacing to external LEDs and switches to simplify control across an isolation barrier.

Collectively, these features make the LMP90080-Q1 a complete analog front-end for low-power, precision sensor applications such as temperature, pressure, strain gauge, and industrial process control. The LMP90080-Q1 is ensured over the extended temperature range of -40°C to +150°C and is available in a 28-pin package with an exposed pad.



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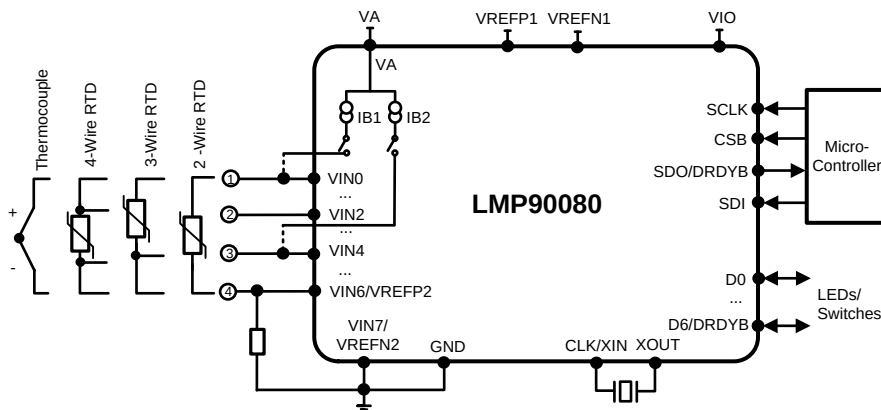
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## Typical Application



## Block Diagram

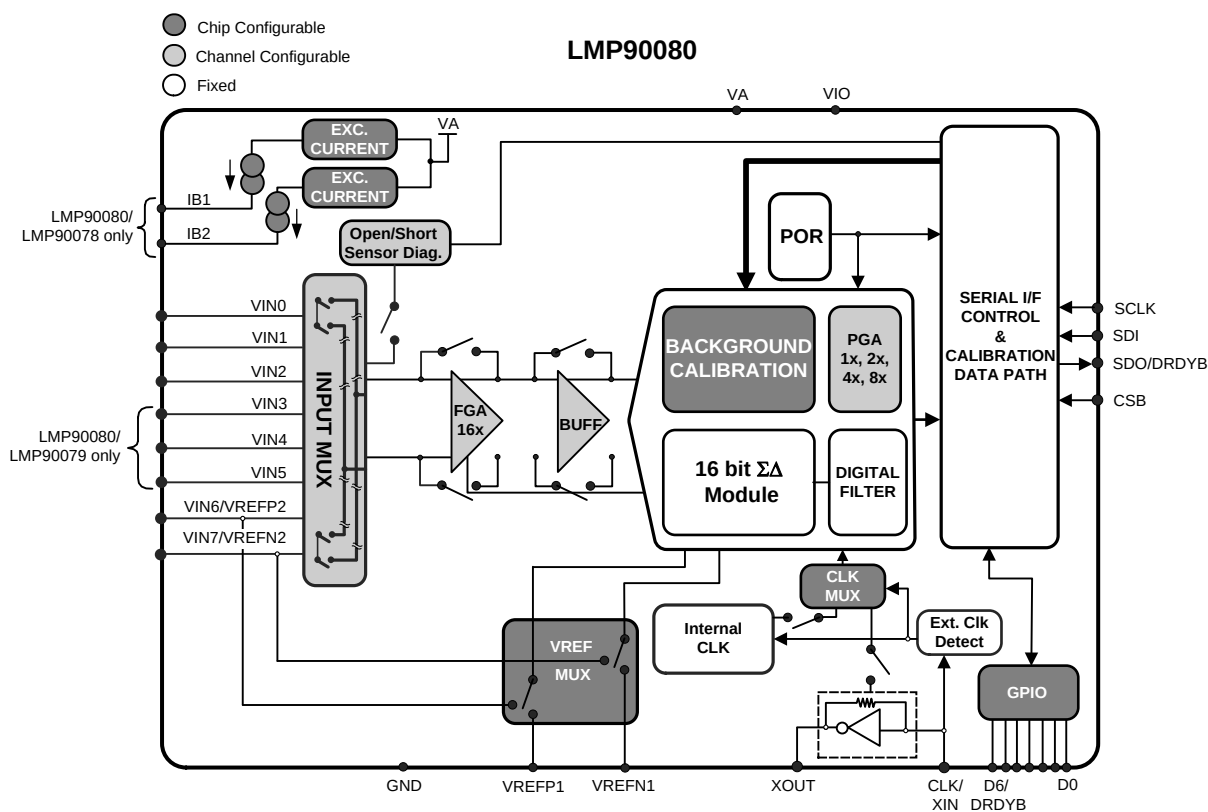


Figure 1. Block Diagram

## True Continuous Background Calibration

The LMP90080-Q1 features a 16 bit  $\Sigma\Delta$  core with continuous background calibration to compensate for gain and offset errors in the ADC, virtually eliminating any drift with time and temperature. The calibration is performed in the background without user or ADC input interruption, making it unique in the industry and eliminating down time associated with field calibration required with other solutions. Having this continuous calibration improves performance over the entire life span of the end product.

## Continuous Background Sensor Diagnostics

Sensor diagnostics are also performed in the background, without interfering with signal path performance, allowing the detection of sensor shorts, opens, and out-of-range signals, which vastly improves system reliability. In addition, the fully flexible input multiplexer described below allows any input pin to be connected to any ADC input channel providing additional sensor path diagnostic capability.

## Flexible Input MUX Channels

The flexible input MUX allows interfacing to a wide range of sensors such as thermocouples, RTDs, thermistors, and bridge sensors. The LMP90080-Q1's multiplexer supports 4 differential channels. Each effective input voltage that is digitized is  $V_{IN} = V_{INX} - V_{INY}$ , where x and y are any input. In addition, the input multiplexer of the LMP90080-Q1 also supports 7 single-ended channels, where the common ground is any one of the inputs.

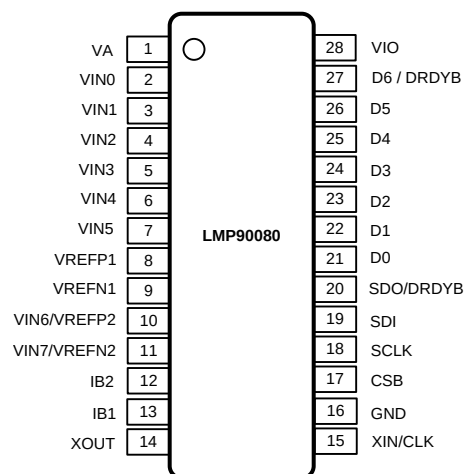
## Programmable Gain Amplifiers (FGA & PGA)

The LMP90080-Q1 contains an internal 16x fixed gain amplifier (FGA) and a 1x, 2x, 4x, or 8x programmable gain amplifier (PGA). This allows accurate gain settings of 1x, 2x, 4x, 8x, 16x, 32x, 64x, or 128x through configuration of internal registers. Having an internal amplifier eliminates the need for external amplifiers that are costly, space consuming, and difficult to calibrate.

## Excitation Current Sources (IB1 & IB2)

Two matched internal excitation currents, IB1 and IB2, can be used for sourcing currents to a variety of sensors. The current range is from 100  $\mu$ A to 1000  $\mu$ A in steps of 100  $\mu$ A.

## Connection Diagram



**Figure 2. 28-pin HTSSOP**

## Pin Descriptions

| Pin #   | Pin Name      | Type           | Function                                                       |
|---------|---------------|----------------|----------------------------------------------------------------|
| 1       | VA            | Analog Supply  | Analog power supply pin                                        |
| 2 - 4   | VIN0 - VIN2   | Analog Input   | Analog input pins                                              |
| 5 - 7   | VIN3 - VIN5   | Analog Input   | Analog input pins                                              |
| 8       | VREFP1        | Analog Input   | Positive reference input                                       |
| 9       | VREFN1        | Analog Input   | Negative reference input                                       |
| 10      | VIN6 / VREFP2 | Analog Input   | Analog input pin or VREFP2 input                               |
| 11      | VIN7 / VREFN2 | Analog Input   | Analog input pin or VREFN2 input                               |
| 12 - 13 | IB2 & IB1     | Analog output  | Excitation current sources for external RTDs                   |
| 14      | XOUT          | Analog output  | External crystal oscillator connection                         |
| 15      | XIN / CLK     | Analog input   | External crystal oscillator connection or external clock input |
| 16      | GND           | Ground         | Power supply ground                                            |
| 17      | CSB           | Digital Input  | Chip select bar                                                |
| 18      | SCLK          | Digital Input  | Serial clock                                                   |
| 19      | SDI           | Digital Input  | Serial data input                                              |
| 20      | SDO / DRDYB   | Digital Output | Serial data output and data ready bar                          |
| 21 - 26 | D0 - D5       | Digital IO     | General purpose input/output (GPIO) pins                       |
| 27      | D6 / DRDYB    | Digital IO     | General purpose input/output pin or data ready bar             |
| 28      | VIO           | Digital Supply | Digital input/output supply pin                                |
|         | Thermal Pad   |                | Leave the thermal pad floating                                 |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings<sup>(1)(2)(3)(4)</sup>

|                                                        |                            |                     |
|--------------------------------------------------------|----------------------------|---------------------|
| Analog Supply Voltage, VA                              |                            | -0.3V to 6.0V       |
| Digital I/O Supply Voltage, VIO                        |                            | -0.3V to 6.0V       |
| Reference Voltage, VREF                                |                            | -0.3V to VA+0.3V    |
| Voltage on Any Analog Input Pin to GND <sup>(5)</sup>  |                            | -0.3V to VA+0.3V    |
| Voltage on Any Digital Input PIN to GND <sup>(5)</sup> |                            | -0.3V to VIO+0.3V   |
| Voltage on SDO <sup>(5)</sup>                          |                            | -0.3V to VIO + 0.3V |
| Input Current at Any Pin <sup>(5)</sup>                |                            | 5mA                 |
| Output Current Source or Sink by SDO                   |                            | 3mA                 |
| Total Package Input and Output Current                 |                            | 20mA                |
| ESD Susceptibility                                     | Human Body Model (HBM)     | 2500V               |
|                                                        | Machine Model (MM)         | 200V                |
|                                                        | Charged Device Model (CDM) | 1250V               |
| Junction Temperature (T <sub>JMAX</sub> )              |                            | +150°C              |
| Storage Temperature Range                              |                            | -65°C to +150°C     |

- (1) All voltages are measured with respect to GND, unless otherwise specified
- (2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the [Electrical Characteristics](#). The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (3) For soldering specifications see product folder at <http://www.ti.com> and <http://www.ti.com/lit/SNOA549>
- (4) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (5) When the input voltage (VIN) exceeds the power supply (VIN < GND or VIN > VA), the current at that pin must be limited to 5mA and VIN has to be within the Absolute Maximum Rating for that pin. The 20 mA package input current rating limits the number of pins that can safely exceed the power supplies with current flow to four pins.

## Operating Ratings

|                                                                         |                                                          |
|-------------------------------------------------------------------------|----------------------------------------------------------|
| Analog Supply Voltage, $V_A$                                            | +4.75V to 5.5V                                           |
| Digital I/O Supply Voltage, $V_{IO}$                                    | +2.7V to 5.5V                                            |
| Full Scale Input Range, $V_{IN}$                                        | $\pm V_{REF} / PGA$                                      |
| Reference Voltage, $V_{REF}$                                            | +0.5V to $V_A$                                           |
| Temperature Range for Electrical Characteristics                        | $T_{MIN} = -40^{\circ}\text{C}$                          |
|                                                                         | $T_{MAX} = +150^{\circ}\text{C}$                         |
| Operating Temperature Range                                             | $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |
| Junction to Ambient Thermal Resistance ( $\theta_{JA}$ ) <sup>(1)</sup> | 41°C/W                                                   |

- (1) The maximum power dissipation is a function of  $T_{J(MAX)}$  AND  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$ .

## Electrical Characteristics

Unless otherwise noted, the key for the condition is (VA = VIO = VREF) / ODR (SPS) / buffer / calibration / gain . Boldface limits apply for  $T_{MIN} \leq T_A \leq T_{MAX}$ ; the typical values apply for  $T_A = +25^{\circ}\text{C}$ .

| Symbol     | Parameter                                          | Conditions                                              | Min    | Typ                         | Max   | Units            |
|------------|----------------------------------------------------|---------------------------------------------------------|--------|-----------------------------|-------|------------------|
| n          | Resolution                                         |                                                         |        | 16                          |       | Bits             |
| ENOB / NFR | Effective Number of Bits and Noise Free Resolution | 5V / all / ON / OFF / all. Shorted input.               |        | See <a href="#">Table 1</a> |       | Bits             |
| ODR        | Output Data Rates                                  |                                                         | 1.6675 | See                         | 214.6 | SPS              |
|            | Gain                                               | FGA × PGA                                               | 1      | See <a href="#">Table 1</a> | 128   |                  |
| INL        | Integral Non-Linearity <sup>(1)</sup>              | 5V / 214.65 / ON / ON / 1 - 128                         |        | ± 1                         |       | LSB              |
|            | Total Noise                                        | 5V / all / ON / OFF / all. Shorted input.               |        | See <a href="#">Table 2</a> |       | μV               |
| OE         | Offset Error                                       | 5V / all / ON or OFF / ON / all                         |        | Below Noise Floor (rms)     |       | μV               |
|            |                                                    | 5V / 214.65 / ON / ON / 1                               |        | 1.79                        | 15    | μV               |
|            |                                                    | 5V / 214.65 / ON / ON / 128                             |        | 0.0112                      | 10    | μV               |
|            | Offset Drift Over Temp <sup>(1)</sup>              | 5V / 214.65 / ON or OFF/OFF/1-8                         |        | 100                         |       | nV/°C            |
|            |                                                    | 5V / 214.65 / ON / ON / 1-8                             |        | 3                           |       | nV/°C            |
|            |                                                    | 5V / 214.65 / ON / OFF / 16                             |        | 25                          |       | nV/°C            |
|            |                                                    | 5V / 214.65 / ON / ON / 16                              |        | 0.4                         |       | nV/°C            |
|            |                                                    | 5V / 214.65 / ON / OFF / 128                            |        | 6                           |       | nV/°C            |
|            |                                                    | 5V / 214.65 / ON / ON / 128                             |        | 0.125                       |       | nV/°C            |
|            | Offset Drift over Time <sup>(1)</sup>              | 5V / 214.65 / ON / OFF / 1, $T_A = 150^{\circ}\text{C}$ |        | 2360                        |       | nV / 1000 hours  |
|            |                                                    | 5V / 214.65 / ON / ON / 1, $T_A = 150^{\circ}\text{C}$  |        | 100                         |       | nV / 1000 hours  |
| GE         | Gain Error <sup>(1)</sup>                          | 5V / 214.65 / ON / ON / 1                               | -80    | 7                           | 80    | ppm              |
|            |                                                    | 5V / 214.65 / ON / ON / 16                              |        | 50                          |       | ppm              |
|            |                                                    | 5V / 214.65 / ON / ON / 64                              |        | 50                          |       | ppm              |
|            |                                                    | 5V / 214.65 / ON / ON / 128                             |        | 100                         |       | ppm              |
|            | Gain Drift over Temp <sup>(1)</sup>                | 5V / 214.65 / ON / ON / all                             |        | 0.5                         |       | ppm/°C           |
|            | Gain Drift over Time <sup>(1)</sup>                | 5V / 214.65 / ON / OFF / 1, $T_A = 150^{\circ}\text{C}$ |        | 5.9                         |       | ppm / 1000 hours |
|            |                                                    | 5V / 214.65 / ON / ON / 1, $T_A = 150^{\circ}\text{C}$  |        | 1.6                         |       | ppm / 1000 hours |

### CONVERTER'S CHARACTERISTIC

|      |                                            |                                            |    |     |  |    |
|------|--------------------------------------------|--------------------------------------------|----|-----|--|----|
| CMRR | Input Common Mode Rejection Ratio          | DC, 5V / 214.65 / ON / ON / 1              | 90 | 120 |  | dB |
|      |                                            | 50/60 Hz, 5V / 214.65 / OFF / OFF / 1      |    | 117 |  | dB |
|      | Reference Common Mode Rejection            | VREF = 2.5V                                |    | 101 |  | dB |
| PSRR | Power Supply Rejection Ratio               | DC, 5V / 214.65 / ON / ON / 1              | 85 | 112 |  | dB |
| NMRR | Normal Mode Rejection Ratio <sup>(1)</sup> | 47 Hz to 63 Hz, 5V / 13.42 / OFF / OFF / 1 | 78 |     |  | dB |
|      | Cross-talk <sup>(1)</sup>                  | 5V / 214.65 / OFF / OFF / 1                | 95 | 143 |  | dB |

### POWER SUPPLY CHARACTERISTICS

|     |                        |  |      |     |     |   |
|-----|------------------------|--|------|-----|-----|---|
| VA  | Analog Supply Voltage  |  | 4.75 | 5.0 | 5.5 | V |
| VIO | Digital Supply Voltage |  | 2.7  | 3.3 | 5.5 | V |

(1) This parameter is specified by design and/or characterization and is not tested in production.

## Electrical Characteristics (continued)

Unless otherwise noted, the key for the condition is (VA = VIO = VREF) / ODR (SPS) / buffer / calibration / gain . Boldface limits apply for  $T_{MIN} \leq T_A \leq T_{MAX}$ ; the typical values apply for  $T_A = +25^{\circ}\text{C}$ .

| Symbol                                                  | Parameter                             | Conditions                                   | Min         | Typ         | Max         | Units |
|---------------------------------------------------------|---------------------------------------|----------------------------------------------|-------------|-------------|-------------|-------|
| IVA                                                     | Analog Supply Current                 | 5V / 13.42 / OFF / OFF / 1, ext. CLK         |             | 464         | 700         | μA    |
|                                                         |                                       | 5V / 13.42 / ON / OFF / 64, ext. CLK         |             | 690         | 1000        | μA    |
|                                                         |                                       | 5V / 214.65 / ON / OFF / 64, int. CLK        |             | 1760        | 2150        | μA    |
|                                                         |                                       | 5V / 214.65 / OFF / OFF / 1, int. CLK        |             | 941         | 1250        | μA    |
|                                                         |                                       | Standby, 5V, int. CLK                        |             | 5           | 40          | μA    |
|                                                         |                                       | Standby, 5V, ext. CLK                        |             | 300         |             | μA    |
|                                                         |                                       | Power-down, 5V, int/ext CLK                  |             | 4.6         | 40          | μA    |
| REFERENCE INPUT                                         |                                       |                                              |             |             |             |       |
| VREFP                                                   | Positive Reference                    |                                              | VREFN + 0.5 |             | VA          | V     |
| VREFN                                                   | Negative Reference                    |                                              | GND         |             | VREFP - 0.5 | V     |
| VREF                                                    | Differential Reference                | VREF = VREFP - VREFN                         | 0.5         |             | VA          | V     |
| ZREF                                                    | Reference Impedance                   | VREF = 3V / 13.42 / OFF / OFF / 1            |             | 10          |             | MOhm  |
| IREF                                                    | Reference Input                       | VREF = 3V / 13.42 / ON or OFF /ON or OFF/all |             | ±2          |             | μA    |
| CREFP                                                   | Capacitance of the Positive Reference | gain = 1 <sup>(2)</sup>                      |             | 6           |             | pF    |
| CREFN                                                   | Capacitance of the Negative Reference | gain = 1 <sup>(2)</sup>                      |             | 6           |             | pF    |
| ILREF                                                   | Reference Leakage Current             | Power-down                                   |             | 1           |             | nA    |
| ANALOG INPUT                                            |                                       |                                              |             |             |             |       |
| VINP                                                    | Positive Input                        | Gain = 1-8, buffer ON                        | GND + 0.1   |             | VA - 0.1    | V     |
|                                                         |                                       | Gain = 16 - 128, buffer ON                   | GND + 0.4   |             | VA - 1.5    | V     |
|                                                         |                                       | Gain = 1-8, buffer OFF                       | GND         |             | VA          | V     |
| VINN                                                    | Negative Input                        | Gain = 1-8, buffer ON                        | GND + 0.1   |             | VA - 0.1    | V     |
|                                                         |                                       | Gain = 16 - 128, buffer ON                   | GND + 0.4   |             | VA - 1.5    | V     |
|                                                         |                                       | Gain = 1-8, buffer OFF                       | GND         |             | VA          | V     |
| VIN                                                     | Differential Input                    | VIN = VINP - VINN                            |             | ±VREF / PGA |             |       |
| ZIN                                                     | Differential Input Impedance          | ODR = 13.42 SPS                              |             | 15.4        |             | MOhm  |
| CINP                                                    | Capacitance of the Positive Input     | 5V / 214.65 / OFF / OFF / 1                  |             | 4           |             | pF    |
| CINN                                                    | Capacitance of the Negative Input     | 5V / 214.65 / OFF / OFF / 1                  |             | 4           |             | pF    |
| IIN                                                     | Input Leakage Current                 | 5V / 13.42 / ON / OFF / 1-8                  |             | 500         |             | pA    |
|                                                         |                                       | 5V / 13.42 / ON / OFF / 16 - 128             |             | 100         |             | pA    |
| DIGITAL INPUT CHARACTERISTICS at VA = VIO = VREF = 3.0V |                                       |                                              |             |             |             |       |
| VIH                                                     | Logical "1" Input Voltage             |                                              | 0.7 x VIO   |             |             | V     |
| VIL                                                     | Logical "0" Input Voltage             |                                              |             |             | 0.3 x VIO   | V     |
| IIL                                                     | Digital Input Leakage Current         |                                              | -10         |             | +10         | μA    |
| VHYST                                                   | Digital Input Hysteresis              |                                              |             | 0.1 x VIO   |             | V     |

(2) This parameter is specified by design and/or characterization and is not tested in production.

## Electrical Characteristics (continued)

Unless otherwise noted, the key for the condition is (VA = VIO = VREF) / ODR (SPS) / buffer / calibration / gain . Boldface limits apply for  $T_{MIN} \leq T_A \leq T_{MAX}$ ; the typical values apply for  $T_A = +25^{\circ}\text{C}$ .

| Symbol                                                          | Parameter                        | Conditions                                                   | Min | Typ                                                  | Max         | Units                   |
|-----------------------------------------------------------------|----------------------------------|--------------------------------------------------------------|-----|------------------------------------------------------|-------------|-------------------------|
| <b>DIGITAL OUTPUT CHARACTERISTICS at VA = VIO = VREF = 3.0V</b> |                                  |                                                              |     |                                                      |             |                         |
| VOH                                                             | Logical "1" Output Voltage       | Source 300 $\mu\text{A}$                                     | 2.6 |                                                      |             | V                       |
| VOL                                                             | Logical "0" Output Voltage       | Sink 300 $\mu\text{A}$                                       |     |                                                      | 0.4         | V                       |
| IOZH, IOZL                                                      | TRI-STATE Leakage Current        |                                                              | -10 |                                                      | 10          | $\mu\text{A}$           |
| COUT                                                            | TRI-STATE Capacitance            | See <sup>(2)</sup>                                           |     | 5                                                    |             | pF                      |
| <b>EXCITATION CURRENT SOURCES CHARACTERISTICS</b>               |                                  |                                                              |     |                                                      |             |                         |
| IB1, IB2                                                        | Excitation Current Source Output |                                                              |     | 0, 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000 |             | $\mu\text{A}$           |
|                                                                 | IB1/IB2 Tolerance                | VA = VREF = 5V                                               | -5  | 0.2                                                  | 5           | %                       |
|                                                                 | IB1/IB2 Output Compliance Range  | VA = 5.0V, IB1/IB2 = 100 $\mu\text{A}$ to 1000 $\mu\text{A}$ |     | VA - 0.8                                             |             | V                       |
|                                                                 | IB1/IB2 Regulation               | VA = 5.0V, IB1/IB2 = 100 $\mu\text{A}$ to 1000 $\mu\text{A}$ |     | 0.07                                                 |             | % / V                   |
| IBTC                                                            | IB1/IB2 Drift                    | VA = 5.0V                                                    |     | 60                                                   |             | ppm/ $^{\circ}\text{C}$ |
| IBMT                                                            | IB1/IB2 Matching                 | 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 100 $\mu\text{A}$     |     | 0.34                                                 | <b>1.53</b> | %                       |
|                                                                 |                                  | 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 200 $\mu\text{A}$     |     | 0.22                                                 | <b>1</b>    | %                       |
|                                                                 |                                  | 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 300 $\mu\text{A}$     |     | 0.2                                                  | <b>0.85</b> | %                       |
|                                                                 |                                  | 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 400 $\mu\text{A}$     |     | 0.15                                                 | <b>0.8</b>  | %                       |
|                                                                 |                                  | 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 500 $\mu\text{A}$     |     | 0.14                                                 | <b>0.7</b>  | %                       |
|                                                                 |                                  | 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 600 $\mu\text{A}$     |     | 0.13                                                 | <b>0.7</b>  | %                       |
|                                                                 |                                  | 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 700 $\mu\text{A}$     |     | 0.075                                                | <b>0.65</b> | %                       |
|                                                                 |                                  | 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 800 $\mu\text{A}$     |     | 0.085                                                | <b>0.6</b>  | %                       |
|                                                                 |                                  | 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 900 $\mu\text{A}$     |     | 0.11                                                 | <b>0.55</b> | %                       |
|                                                                 |                                  | 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 1000 $\mu\text{A}$    |     | 0.11                                                 | <b>0.45</b> | %                       |
| IBMTC                                                           | IB1/IB2 Matching Drift           | VA = 5.0V, IB1/IB2 = 100 $\mu\text{A}$ to 1000 $\mu\text{A}$ |     | 2                                                    |             | ppm/ $^{\circ}\text{C}$ |
| <b>INTERNAL/EXTERNAL CLK</b>                                    |                                  |                                                              |     |                                                      |             |                         |
| CLKIN                                                           | Internal Clock Frequency         |                                                              |     | 893                                                  |             | kHz                     |
| CLKEXT                                                          | External Clock Frequency         | See <sup>(3)</sup>                                           | 1.8 | 3.5717                                               | 7.2         | MHz                     |
|                                                                 | External Crystal Frequency       | Input Low Voltage                                            |     | 0                                                    |             | V                       |
|                                                                 |                                  | Input High Voltage                                           |     | 1                                                    |             | V                       |
|                                                                 |                                  | Frequency                                                    | 1.8 | 3.5717                                               | 7.2         | MHz                     |
|                                                                 |                                  | Start-up time                                                |     | 7                                                    |             | ms                      |

(3) This parameter is specified by design and/or characterization and is not tested in production.



## Electrical Characteristics (continued)

Unless otherwise noted, the key for the condition is ( $V_A = V_{IO} = V_{REF}$ ) / ODR (SPS) / buffer / calibration / gain . Boldface limits apply for  $T_{MIN} \leq T_A \leq T_{MAX}$ ; the typical values apply for  $T_A = +25^\circ\text{C}$ .

| Symbol | Parameter    | Conditions | Min | Typ | Max | Units |
|--------|--------------|------------|-----|-----|-----|-------|
| SCLK   | Serial Clock |            |     |     | 10  | MHz   |

**Table 1. ENOB (Noise Free Resolution) vs. Sampling Rate and Gain at  $V_A = V_{IO} = V_{REF} = 5\text{V}$**

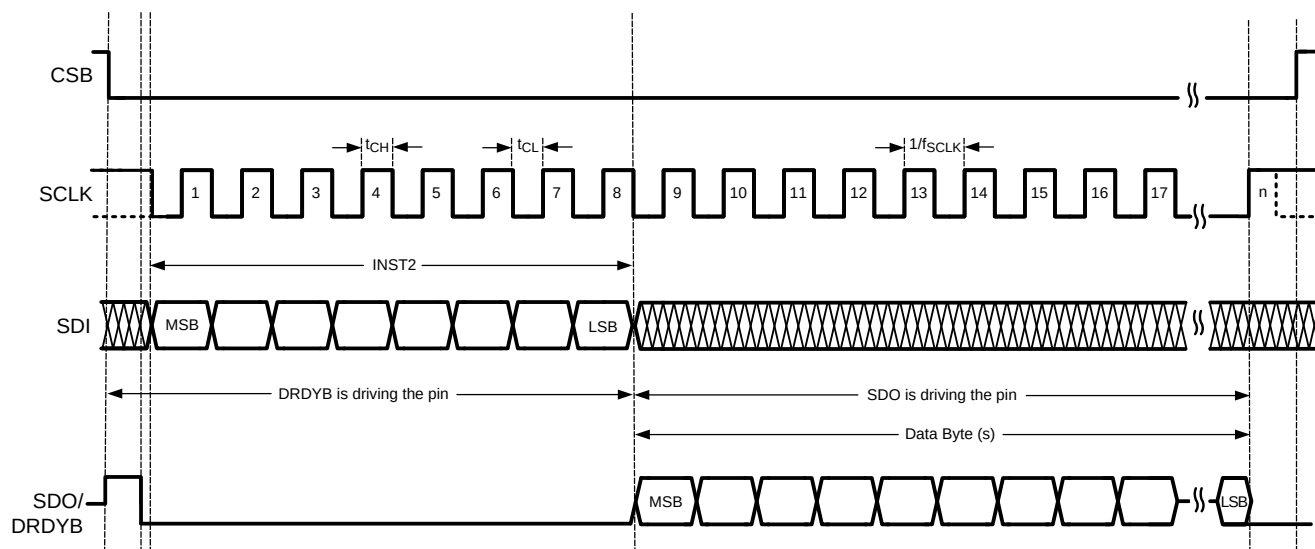
| SPS      | Gain of the ADC |         |         |         |         |         |           |           |
|----------|-----------------|---------|---------|---------|---------|---------|-----------|-----------|
|          | 1               | 2       | 4       | 8       | 16      | 32      | 64        | 128       |
| 1.6775   | 16 (16)         | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16)   | 16 (16)   |
| 3.355    | 16 (16)         | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16)   | 16 (15.5) |
| 6.71     | 16 (16)         | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16)   | 16 (15)   |
| 13.42    | 16 (16)         | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (15.5) | 16 (15)   |
| 26.83125 | 16 (16)         | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16)   | 16 (15.5) |
| 53.6625  | 16 (16)         | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16)   | 16 (15)   |
| 107.325  | 16 (16)         | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (15.5) | 16 (14.5) |
| 214.65   | 16 (16)         | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (16) | 16 (15)   | 16 (14)   |

**Table 2. RMS Noise ( $\mu\text{V}$ ) vs. Sampling Rate and Gain at  $V_A = V_{IO} = V_{REF} = 5\text{V}$**

| SPS      | Gain of the ADC |      |      |      |      |      |      |      |
|----------|-----------------|------|------|------|------|------|------|------|
|          | 1               | 2    | 4    | 8    | 16   | 32   | 64   | 128  |
| 1.6775   | 2.68            | 1.65 | 1.24 | 1.00 | 0.22 | 0.19 | 0.17 | 0.16 |
| 3.355    | 3.86            | 2.36 | 1.78 | 1.47 | 0.34 | 0.27 | 0.22 | 0.22 |
| 6.71     | 5.23            | 3.49 | 2.47 | 2.09 | 0.44 | 0.34 | 0.30 | 0.32 |
| 13.42    | 7.94            | 5.01 | 3.74 | 2.94 | 0.61 | 0.50 | 0.45 | 0.43 |
| 26.83125 | 2.90            | 1.86 | 1.34 | 1.08 | 0.29 | 0.24 | 0.23 | 0.23 |
| 53.6625  | 4.11            | 2.60 | 1.90 | 1.50 | 0.39 | 0.35 | 0.32 | 0.31 |
| 107.325  | 5.74            | 3.72 | 2.72 | 2.11 | 0.56 | 0.48 | 0.46 | 0.44 |
| 214.65   | 8.25            | 5.31 | 3.82 | 2.97 | 0.79 | 0.68 | 0.64 | 0.63 |

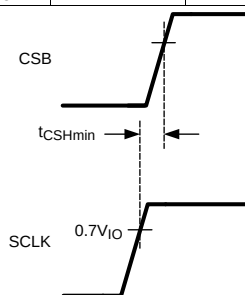
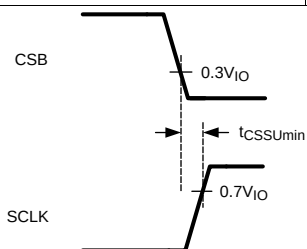
## Timing Diagrams

Unless otherwise noted, specified limits apply for  $V_A = 5V$ ,  $V_{IO} = 3.0V$ . Boldface limits apply for  $T_{MIN} \leq T_A \leq T_{MAX}$ ; the typical values apply for  $T_A = +25^\circ C$ .

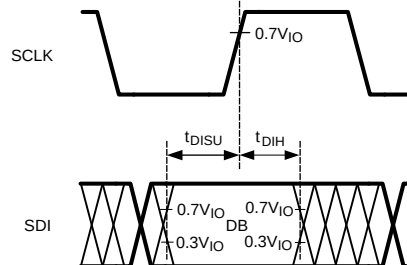
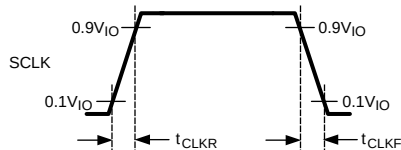


**Figure 3. Timing Diagram**

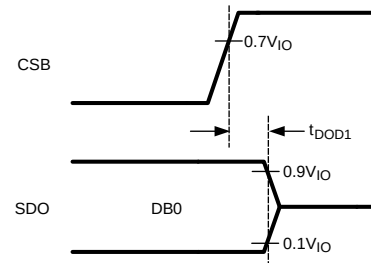
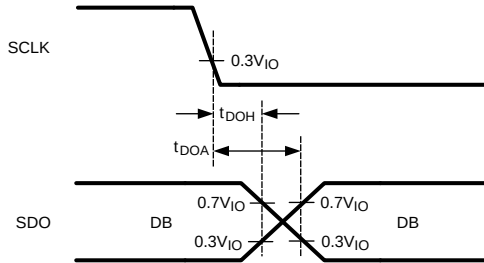
| Symbol     | Parameter      | Conditions | Min              | Typical | Max | Units |
|------------|----------------|------------|------------------|---------|-----|-------|
| $f_{SCLK}$ |                |            |                  |         | 10  | MHz   |
| $t_{CH}$   | SCLK High time |            | $0.4 / f_{SCLK}$ |         |     | ns    |
| $t_{CL}$   | SCLK Low time  |            | $0.4 / f_{SCLK}$ |         |     | ns    |



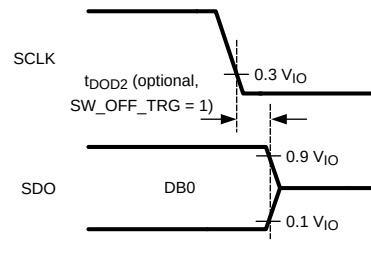
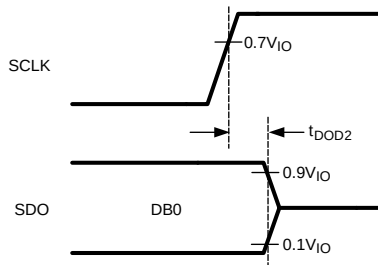
| Symbol     | Parameter                                        | Conditions | Min | Typical | Max | Units |
|------------|--------------------------------------------------|------------|-----|---------|-----|-------|
| $t_{CSSU}$ | CSB Setup time prior to an SCLK rising edge      |            | 10  |         |     | ns    |
| $t_{CSH}$  | CSB Hold time after the last rising edge of SCLK |            | 10  |         |     | ns    |



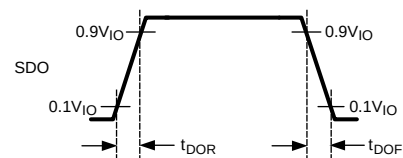
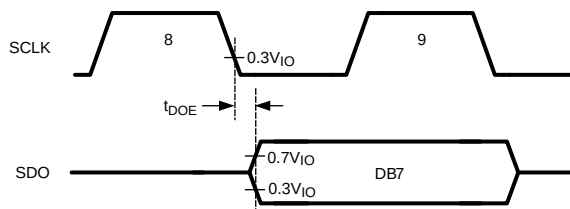
| Symbol     | Parameter                                   | Conditions | Min | Typical | Max | Units |
|------------|---------------------------------------------|------------|-----|---------|-----|-------|
| $t_{CLKR}$ | SCLK Rise time                              |            |     | 1.15    |     | ns    |
| $t_{CLKF}$ | SCLK Fall time                              |            |     | 1.15    |     | ns    |
| $t_{DISU}$ | SDI Setup time prior to an SCLK rising edge |            | 10  |         |     | ns    |
| $t_{DIH}$  | SDI Hold time after an SCLK rising edge     |            | 10  |         |     | ns    |



| Symbol     | Parameter                                     | Conditions | Min | Typical | Max | Units |
|------------|-----------------------------------------------|------------|-----|---------|-----|-------|
| $t_{DOA}$  | SDO Access time after an SCLK falling edge    |            |     |         | 35  | ns    |
| $t_{DOH}$  | SDO Hold time after an SCLK falling edge      |            | 0   |         |     | ns    |
| $t_{DOD1}$ | SDO Disable time after the rising edge of CSB |            |     | 5       |     | ns    |



| Symbol     | Parameter                                  | Conditions | Min | Typical | Max | Units |
|------------|--------------------------------------------|------------|-----|---------|-----|-------|
| $t_{DOD2}$ | SDO Disable time after either edge of SCLK |            |     | 27      |     | ns    |



| Symbol      | Parameter                                             | Conditions                    | Min | Typical | Max | Units   |
|-------------|-------------------------------------------------------|-------------------------------|-----|---------|-----|---------|
| $t_{DOE}$   | SDO Enable time from the falling edge of the 8th SCLK |                               |     |         | 35  | ns      |
| $t_{DOR}$   | SDO Rise time                                         | See <sup>(1)</sup>            |     | 7       |     | ns      |
| $t_{DOF}$   | SDO Fall time                                         | See <sup>(1)</sup>            |     | 7       |     | ns      |
| $t_{DRDYB}$ | Data Ready Bar pulse at every 1/ODR second            | $ODR \leq 13.42$ SPS          |     | 64      |     | $\mu$ s |
|             |                                                       | $13.42 < ODR \leq 214.65$ SPS |     | 4       |     | $\mu$ s |

(1) This parameter is specified by design and/or characterization and is not tested in production.

## Specific Definitions

**COMMON MODE REJECTION RATIO** is a measure of how well in-phase signals common to both input pins are rejected. To calculate CMRR, the change in output offset is measured while the common mode input voltage is changed.

$$\text{CMRR} = 20 \text{ LOG}(\Delta\text{Common Input} / \Delta\text{Output Offset})$$

**EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS)** – says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits. LMP90080-Q1's ENOB is a DC ENOB spec, not the dynamic ENOB that is measured using FFT and SINAD. Its equation is as follows:

$$\text{ENOB} = \log_2 \left( \frac{2 \times \text{VREF}/\text{Gain}}{\text{RMS Noise}} \right) \quad (1)$$

**GAIN ERROR** is the deviation from the ideal slope of the transfer function.

**INTEGRAL NON-LINEARITY (INL)** is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point fit method is used. INL for this product is specified over a limited range, per the Electrical Tables.

**NEGATIVE FULL-SCALE ERROR** is the difference between the differential input voltage at which the output code transitions to negative full scale and  $(-\text{VREF} + 1\text{LSB})$ .

**NEGATIVE GAIN ERROR** is the difference between the negative full-scale error and the offset error divided by  $(\text{VREF} / \text{Gain})$ .

**NOISE FREE RESOLUTION** is a method of specifying the number of bits for a converter with noise.

$$\text{NFR} = \log_2 \left( \frac{2 \times \text{VREF}/\text{Gain}}{\text{Peak-to-Peak Noise}} \right) \quad (2)$$

**ODR** Output Data Rate.

**OFFSET ERROR** is the difference between the differential input voltage at which the output code transitions from code 0000h to 0001h and 1 LSB.

**POSITIVE FULL-SCALE ERROR** is the difference between the differential input voltage at which the output code transitions to positive full scale and  $(\text{VREF} - 1\text{LSB})$ .

**POSITIVE GAIN ERROR** is the difference between the positive full-scale error and the offset error divided by  $(\text{VREF} / \text{Gain})$ .

**POWER SUPPLY REJECTION RATIO (PSRR)** is a measure of how well a change in the analog supply voltage is rejected. PSRR is calculated from the ratio of the change in offset error for a given change in supply voltage, expressed in dB.

$$\text{PSRR} = 20 \text{ LOG} (\Delta\text{VA} / \Delta\text{Output Offset})$$

## Typical Performance Characteristics

Unless otherwise noted, specified limits apply for  $V_A = 5V$ ,  $V_{IO} = V_{REF} = 3.0V$ . The maximum and minimum values apply for  $T_A = T_{MIN}$  to  $T_{MAX}$ ; the typical values apply for  $T_A = +25^\circ C$ .

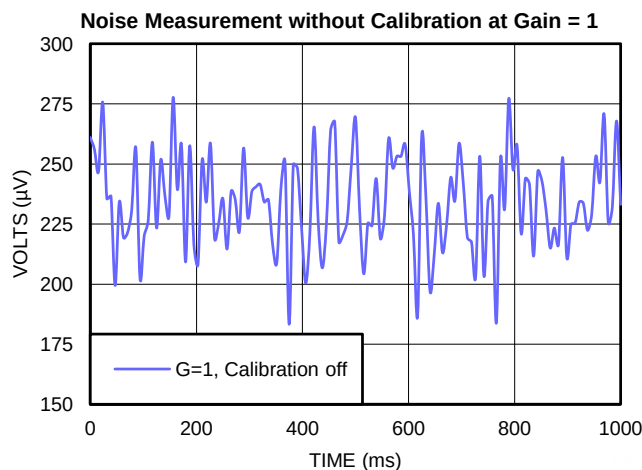


Figure 4.

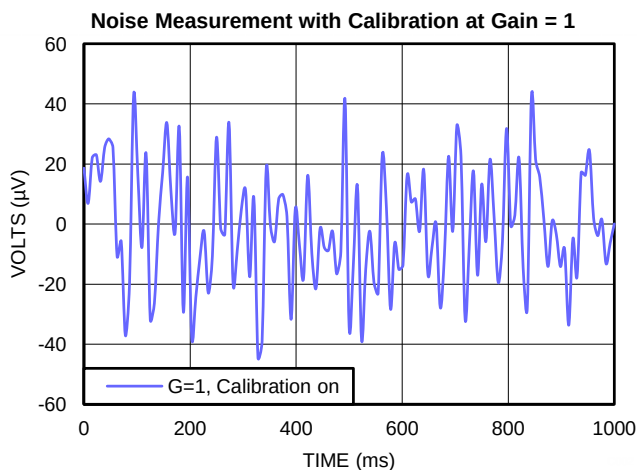


Figure 5.

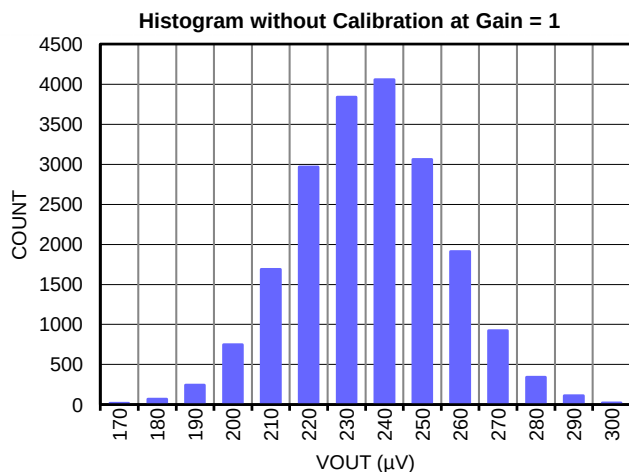


Figure 6.

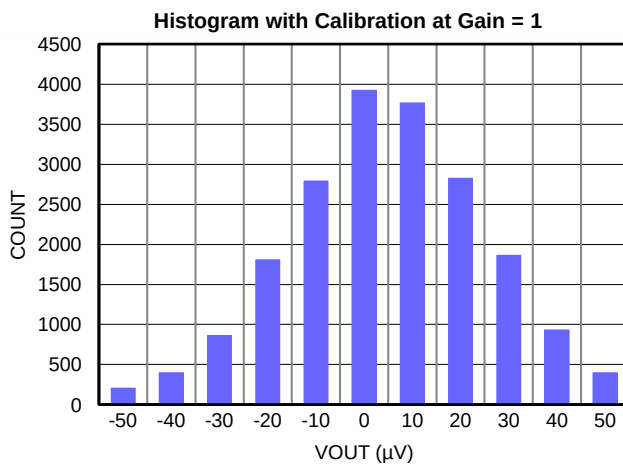


Figure 7.

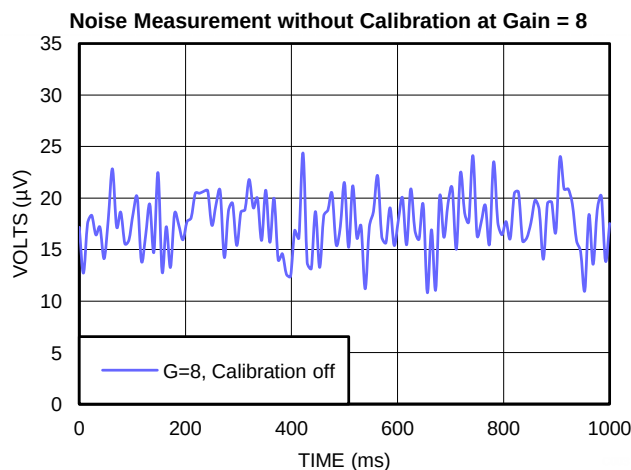


Figure 8.

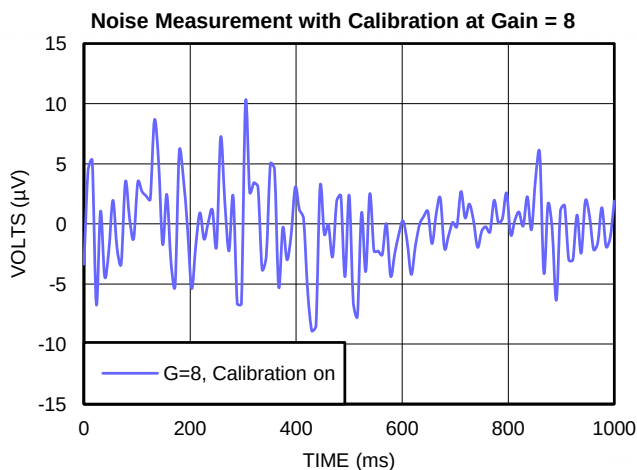
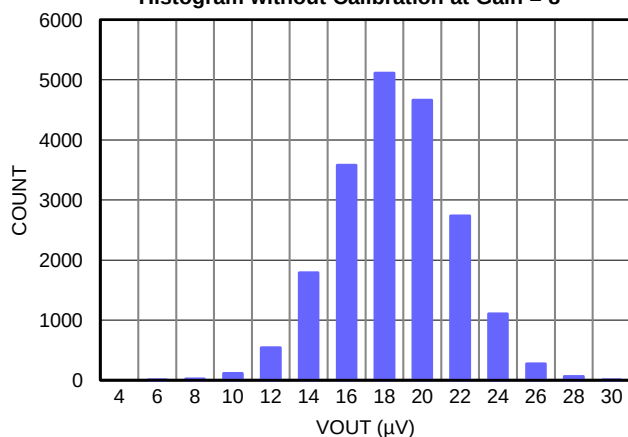


Figure 9.

### Typical Performance Characteristics (continued)

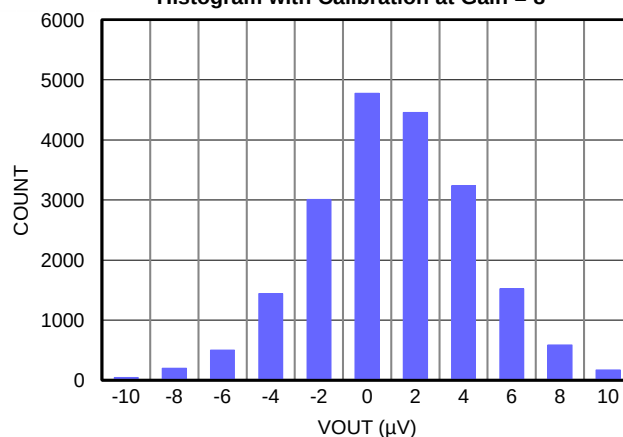
Unless otherwise noted, specified limits apply for  $V_A = 5V$ ,  $V_{IO} = V_{REF} = 3.0V$ . The maximum and minimum values apply for  $T_A = T_{MIN}$  to  $T_{MAX}$ ; the typical values apply for  $T_A = +25^\circ C$ .

**Histogram without Calibration at Gain = 8**



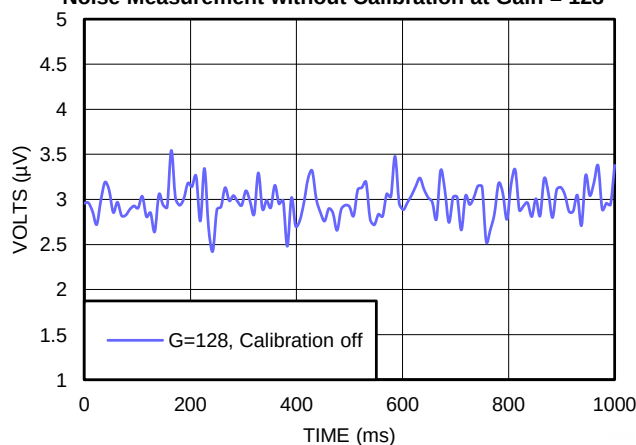
**Figure 10.**

**Histogram with Calibration at Gain = 8**



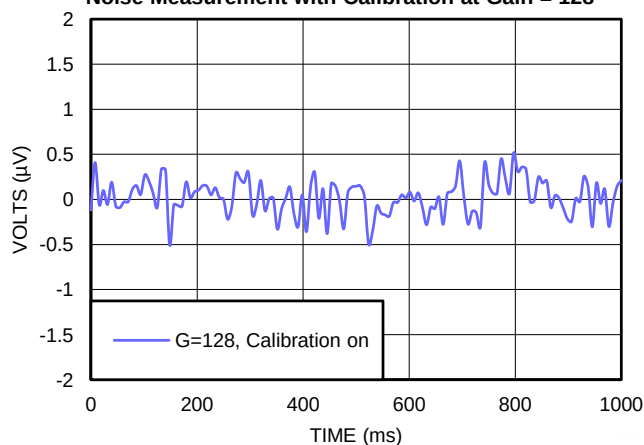
**Figure 11.**

**Noise Measurement without Calibration at Gain = 128**



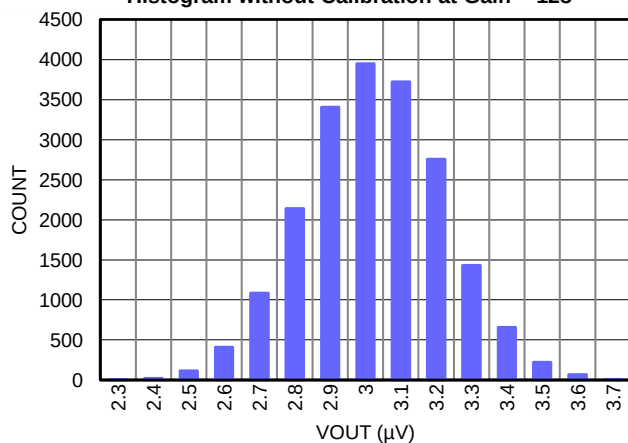
**Figure 12.**

**Noise Measurement with Calibration at Gain = 128**



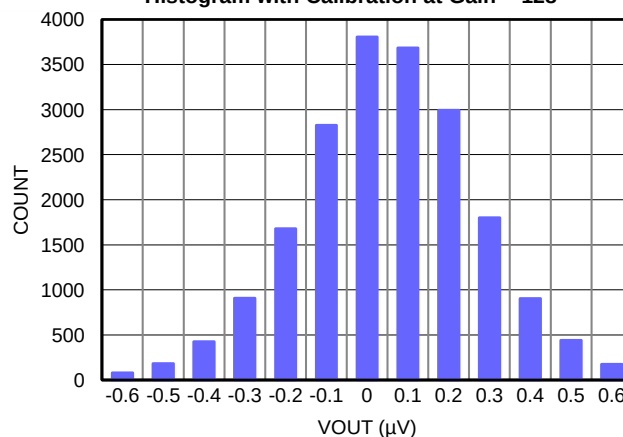
**Figure 13.**

**Histogram without Calibration at Gain = 128**



**Figure 14.**

**Histogram with Calibration at Gain = 128**



**Figure 15.**

## Typical Performance Characteristics (continued)

Unless otherwise noted, specified limits apply for  $V_A = 5V$ ,  $V_{IO} = V_{REF} = 3.0V$ . The maximum and minimum values apply for  $T_A = T_{MIN}$  to  $T_{MAX}$ ; the typical values apply for  $T_A = +25^\circ C$ .

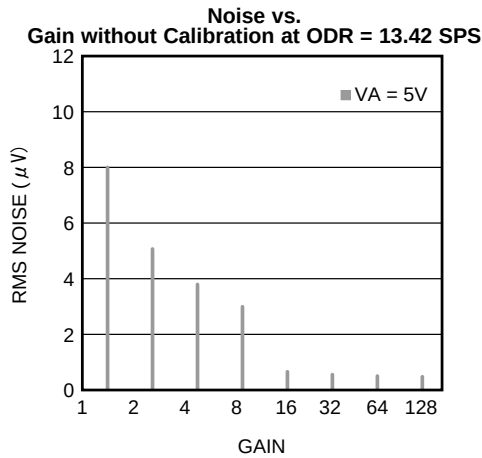


Figure 16.

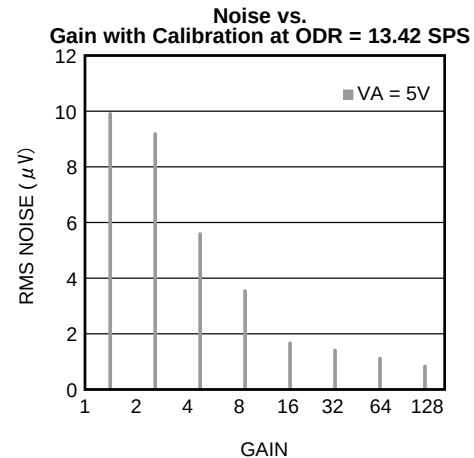


Figure 17.

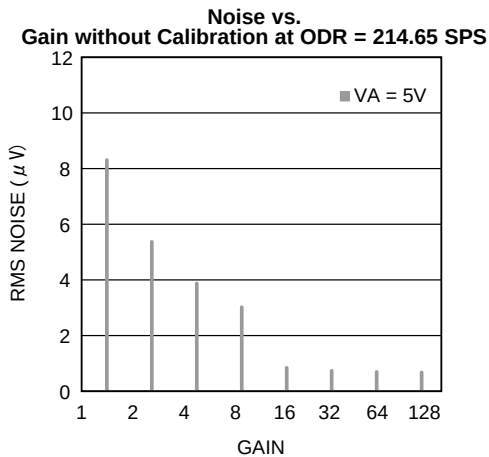


Figure 18.

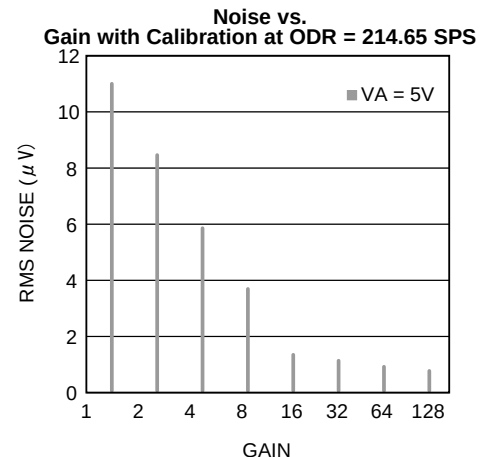


Figure 19.

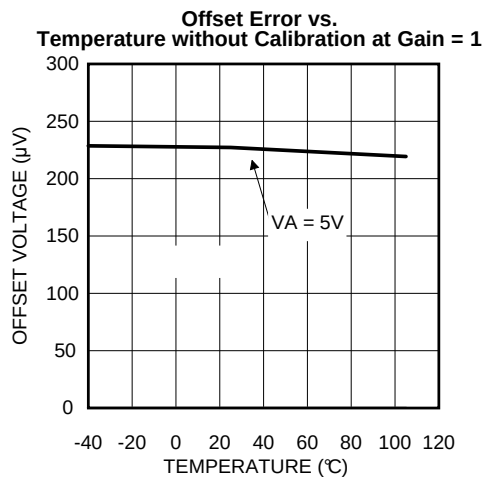


Figure 20.

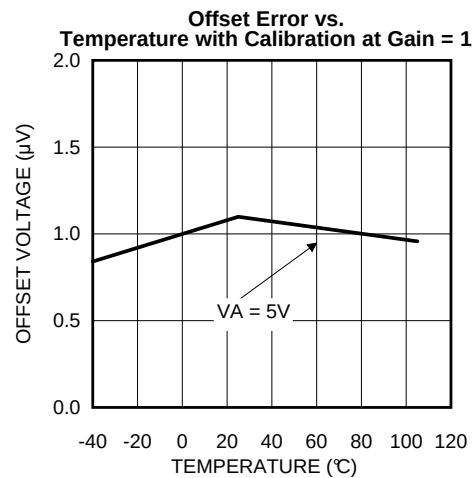


Figure 21.

### Typical Performance Characteristics (continued)

Unless otherwise noted, specified limits apply for  $V_A = 5V$ ,  $V_{IO} = V_{REF} = 3.0V$ . The maximum and minimum values apply for  $T_A = T_{MIN}$  to  $T_{MAX}$ ; the typical values apply for  $T_A = +25^\circ C$ .

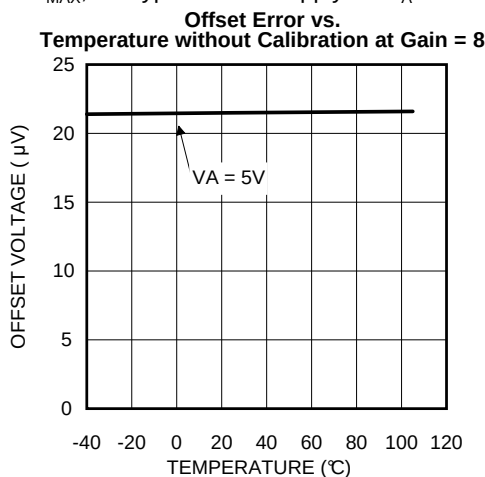


Figure 22.

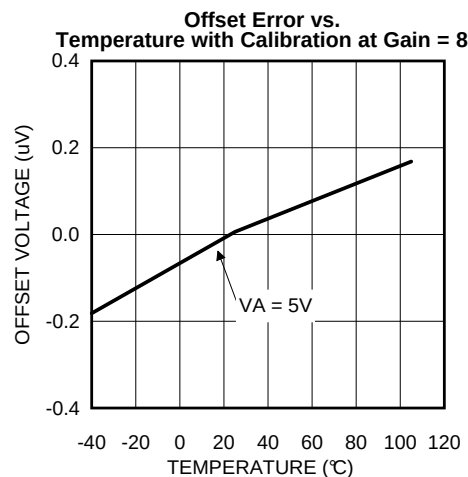


Figure 23.

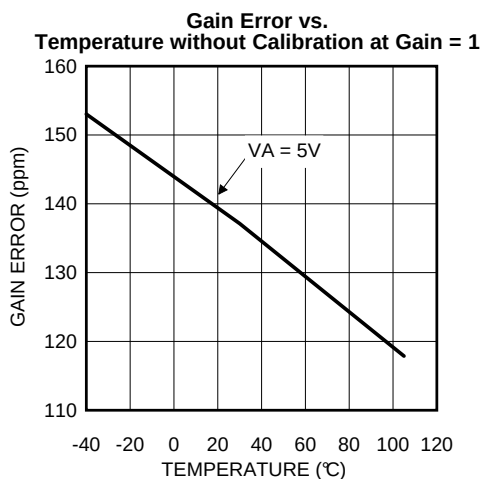


Figure 24.

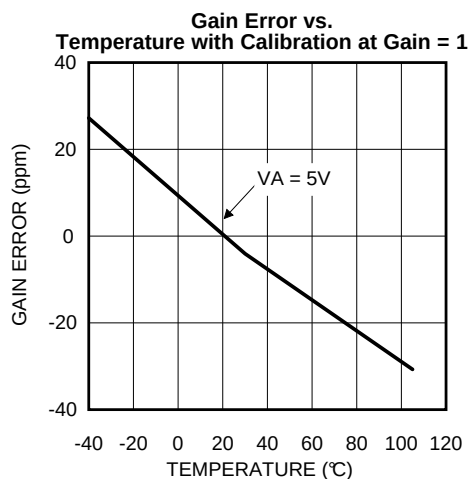


Figure 25.

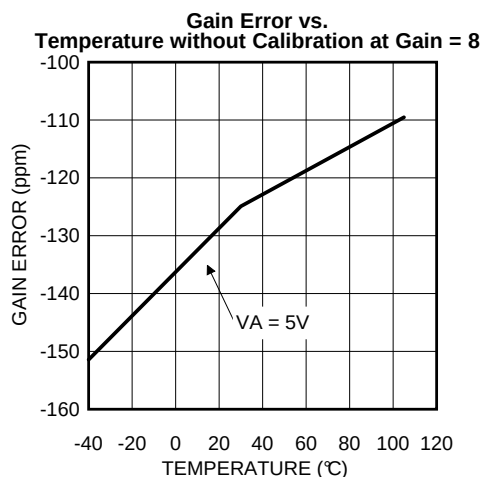


Figure 26.

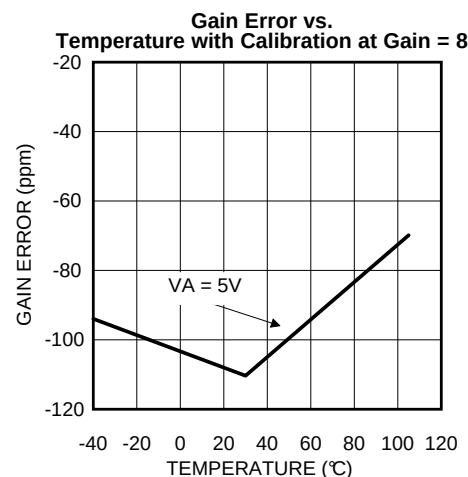


Figure 27.



## Typical Performance Characteristics (continued)

Unless otherwise noted, specified limits apply for  $V_A = 5V$ ,  $V_{IO} = V_{REF} = 3.0V$ . The maximum and minimum values apply for  $T_A = T_{MIN}$  to  $T_{MAX}$ ; the typical values apply for  $T_A = +25^\circ C$ .

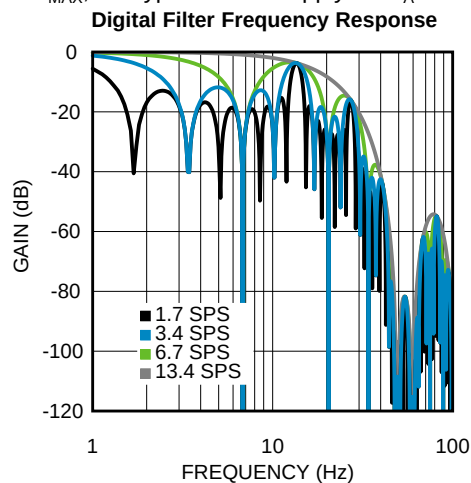


Figure 28.

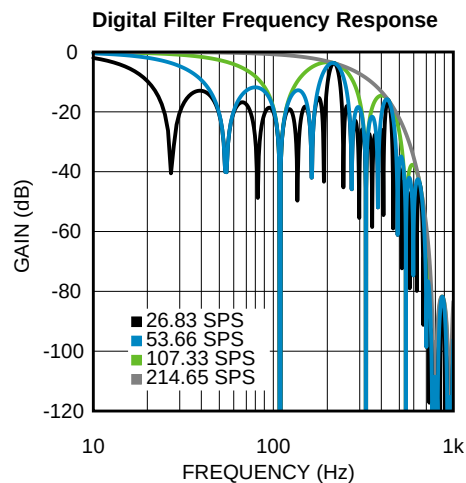


Figure 29.

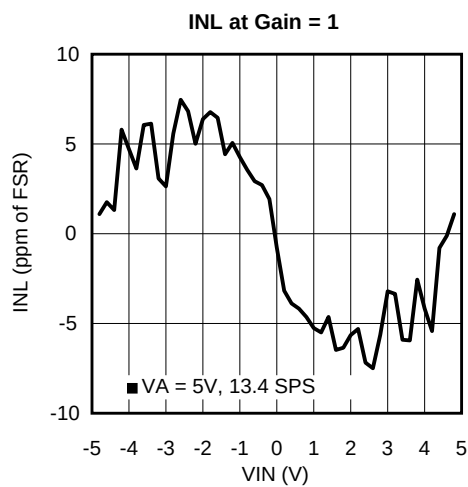


Figure 30.

## Functional Description

The LMP90080-Q1 is a low-power 16-Bit  $\Sigma\Delta$  ADC with 4 fully differential / 7 single-ended analog channels. Its serial data output is two's complement format. The output data rate (ODR) ranges from 1.6775 SPS to 214.65 SPS.

The serial communication for LMP90080-Q1 is SPI, a synchronous serial interface that operates using 4 pins: chip select bar (CSB), serial clock (SCLK), serial data in (SDI), and serial data out / data ready bar (SDO/DRYDYB).

True continuous built-in offset and gain background calibration is also available to improve measurement accuracy. Unlike other ADCs, the LMP90080-Q1's background calibration can run without heavily impacting the input signal. This unique technique allows for positive as well as negative gain calibration and is available at all gain settings.

The registers can be found in [Registers](#), and a detailed description of the LMP90080-Q1 are provided in the following sections.

## Signal Path

### Reference Input ( $V_{REF}$ )

The differential reference voltage  $V_{REF}$  ( $V_{REFP} - V_{REFN}$ ) sets the range for  $V_{IN}$ .

The muxed  $V_{REF}$  allows the user to choose between  $V_{REF1}$  or  $V_{REF2}$  for each channel. This selection can be made by programming the  $V_{REF\_SEL}$  bit in the  $CHx\_INPUTCN$  registers ( $CHx\_INPUTCN: V_{REF\_SEL}$ ). The default mode is  $V_{REF1}$ . If  $V_{REF2}$  is used, then  $V_{IN6}$  and  $V_{IN7}$  cannot be used as inputs because they share the same pin.

Refer to [V<sub>REF</sub>](#) for  $V_{REF}$  applications information.

### Flexible Input MUX ( $V_{IN}$ )

LMP90080-Q1 provides a flexible input MUX as shown in [Figure 31](#). The input that is digitized is  $V_{IN} = V_{INP} - V_{INN}$ ; where  $V_{INP}$  and  $V_{INN}$  can be any available input.

The digitized input is also known as a channel, where  $CH = V_{IN} = V_{INP} - V_{INN}$ . Thus, there are a maximum of 4 differential channels: CH0, CH1, CH2, and CH3.

LMP90080-Q1 can also be configured single-endedly, where the common ground is any one of the inputs. There are a maximum of 7 single-ended channels: CH0, CH1, CH2, CH3, CH4, CH5, and CH6 for the LMP90080-Q1.

The input MUX can be programmed in the  $CHx\_INPUTCN$  registers. For example, to program  $CH0 = V_{IN} = V_{IN4} - V_{IN1}$ , go to the  $CH0\_INPUTCN$  register and set:

1.  $V_{INP} = 0x4$
2.  $V_{INN} = 0x1$

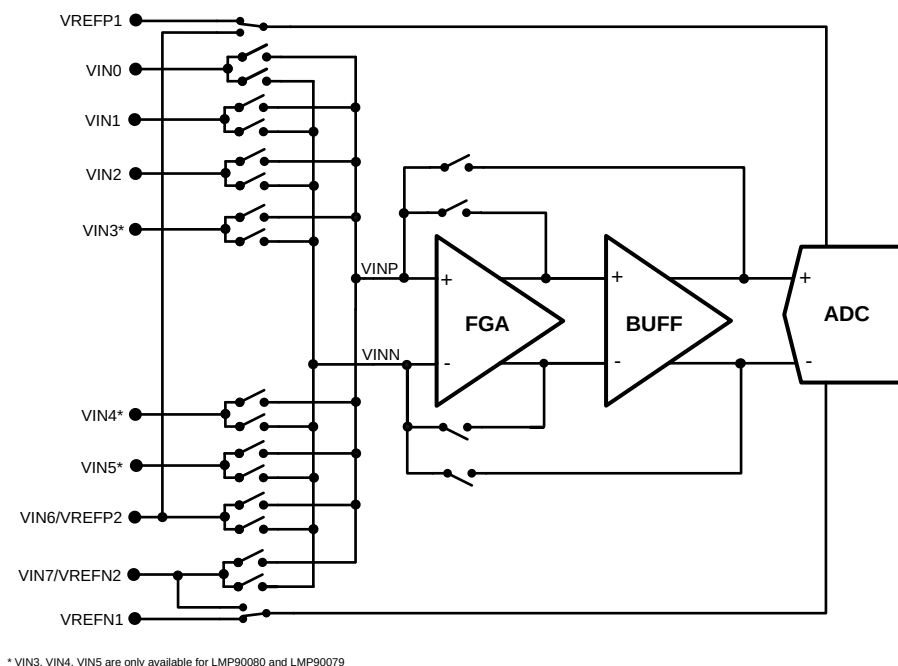


Figure 31. Simplified VIN Circuitry

### Selectable Gains (FGA & PGA)

LMP90080-Q1 provides two types of gain amplifiers: a fixed gain amplifier (FGA) and a programmable gain amplifier (PGA). FGA has a fixed gain of 16x or it can be bypassed, while the PGA has programmable gain settings of 1x, 2x, 4x, or 8x.

Total gain is defined as FGA x PGA. Thus, the LMP90080-Q1 provides gain settings of 1x, 2x, 4x, 8x, 16x, 32x, 64x, or 128x with true continuous background calibration.

The gain is channel specific, which means that one channel can have one gain, while another channel can have the same or a different gain.

The gain can be selected by programming the CHx\_CONFIG: GAIN\_SEL bits.

### Buffer (BUFF)

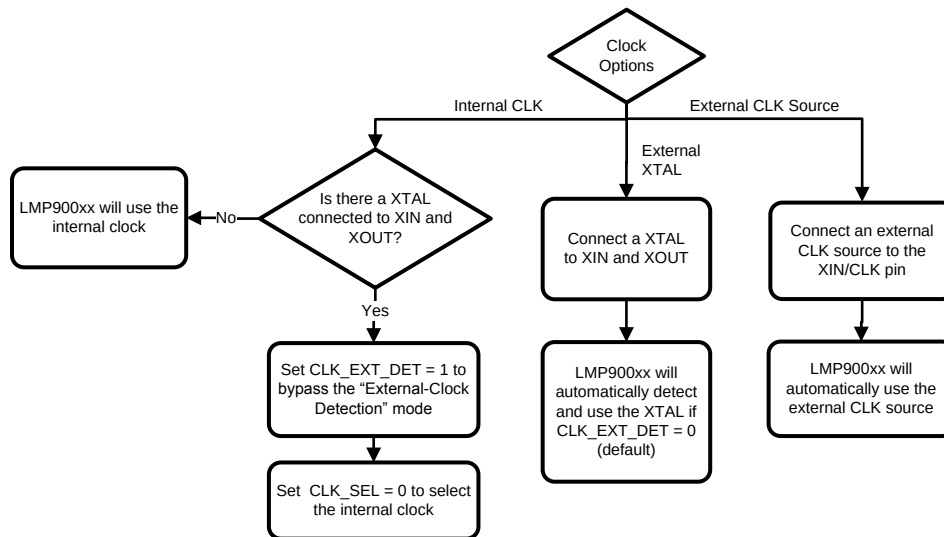
There is an internal unity gain buffer that can be included or excluded from the signal path. Including the buffer provides a high input impedance but increases the power consumption.

When gain  $\geq 16$ , the buffer is automatically included in the signal path. When gain  $< 16$ , including or excluding the buffer from the signal path can be done by programming the CHX\_CONFIG: BUF\_EN bit.

### Internal/External CLK Selection

The LMP90080-Q1 allows two clock options: internal CLK or external CLK (crystal (XTAL) or clock source).

There is an "External Clock Detection" mode, which detects the external XTAL if it is connected to XOUT and XIN. When operating in this mode, the LMP90080-Q1 shuts off the internal clock to reduce power consumption. Below is a flow chart to help set the appropriate clock registers.

**Figure 32. CLK Register Settings**

The recommended value for the external CLK is discussed in the next sections.

### Programmable ODRs

If using the internal CLK or external CLK of 3.5717 MHz, then the output date rates (ODR) can be selected (using the ODR\_SEL bit) as:

1.  $13.42/8 = 1.6775$  SPS
2.  $13.42/4 = 3.355$  SPS
3.  $13.42/2 = 6.71$ SPS
4. 13.42 SPS
5.  $214.65/8 = 26.83125$  SPS
6.  $214.65/4 = 53.6625$  SPS
7.  $214.65/2 = 107.325$  SPS
8. 214.65 SPS (default)

If the internal CLK is not being used and the external CLK is not 3.5717 MHz, then the ODR will be different. If this is the case, use the equation below to calculate the new ODR values.

$$\text{ODR\_Base1} = (\text{CLK}_{\text{EXT}}) / (266,240) \quad (3)$$

$$\text{ODR\_Base2} = (\text{CLK}_{\text{EXT}}) / (16,640) \quad (4)$$

$$\text{ODR1} = (\text{ODR\_Base1}) / n, \text{ where } n = 1,2,4,8 \quad (5)$$

$$\text{ODR2} = (\text{ODR\_Base2}) / n, \text{ where } n = 1,2,4,8 \quad (6)$$

For example, a 3.6864 MHz XTAL or external clock has the following ODR values:

$$\text{ODR\_Base1} = (3.6864 \text{ MHz}) / (266,240) = 13.85 \text{ SPS} \quad (7)$$

$$\text{ODR\_Base2} = (3.6864 \text{ MHz}) / (16,640) = 221.54 \text{ SPS} \quad (8)$$

$$\text{ODR1} = (13.85 \text{ SPS}) / n = 13.85, 6.92, 3.46, 1.73 \text{ SPS} \quad (9)$$

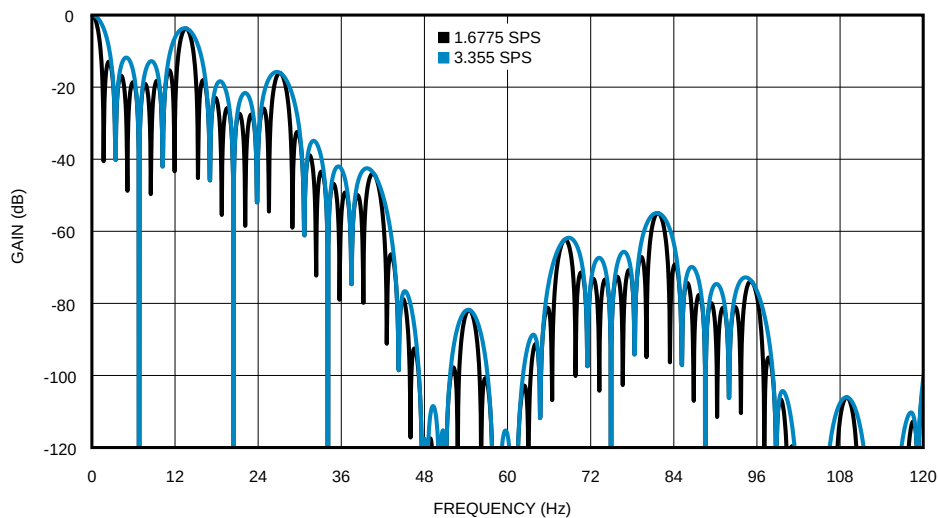
$$\text{ODR2} = (221.54 \text{ SPS}) / n = 221.54, 110.77, 55.38, 27.69 \text{ SPS} \quad (10)$$

The ODR is channel specific, which means that one channel can have one ODR, while another channel can have the same or a different ODR.

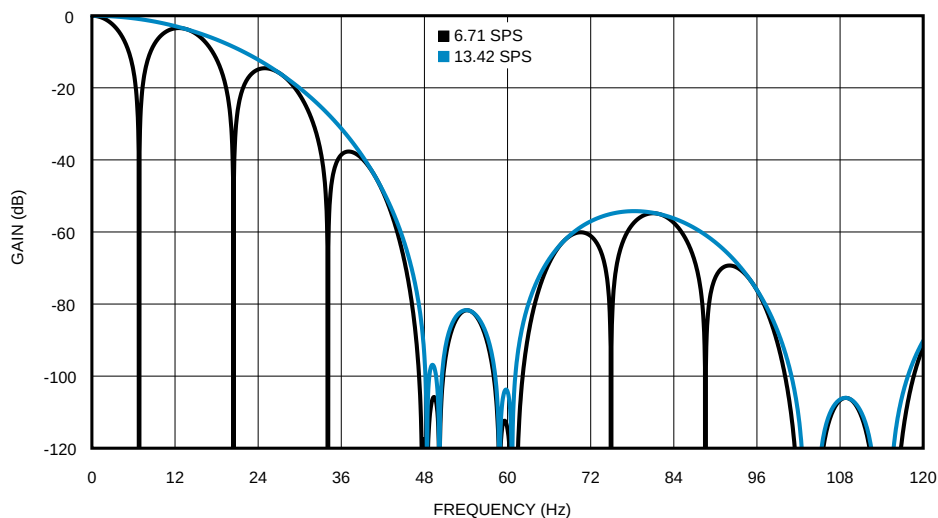
Note that these ODRs are meant for a single channel conversion; the ODR needs to be divided by n for n channels scanning. For example, if the ADC were running at 214.65 SPS and four channels are being scanned, then the ODR per channel would be  $214.65/4 = 53.6625$  SPS.

### Digital Filter

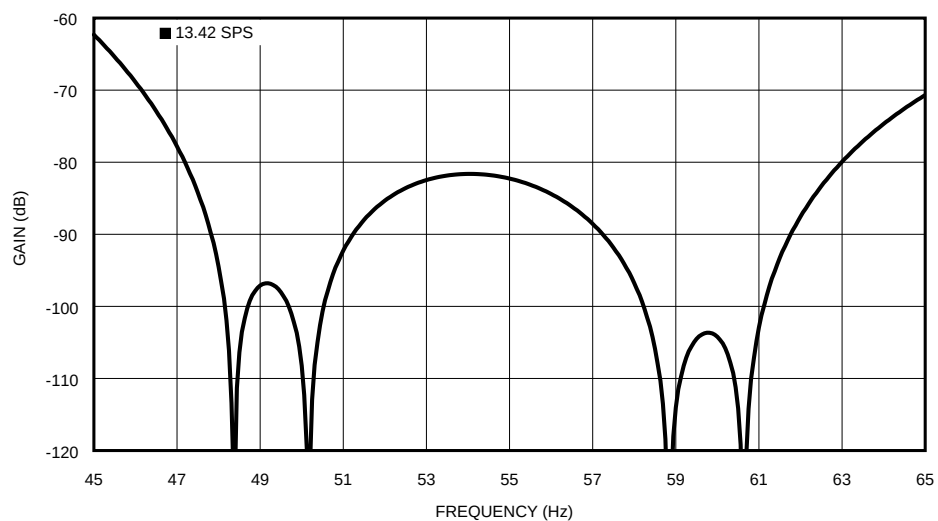
The LMP90080-Q1 has a fourth order rotated sinc filter that is used to configure various ODRs and to reject power supply frequencies of 50Hz and 60Hz. The 50/60 Hz rejection is only effective when the device is operating at  $ODR \leq 13.42$  SPS. If the internal CLK or the external CLK of 3.5717 MHz is used, then the LMP90080-Q1 will have the frequency response shown in [Figure 33](#) through [Figure 37](#).



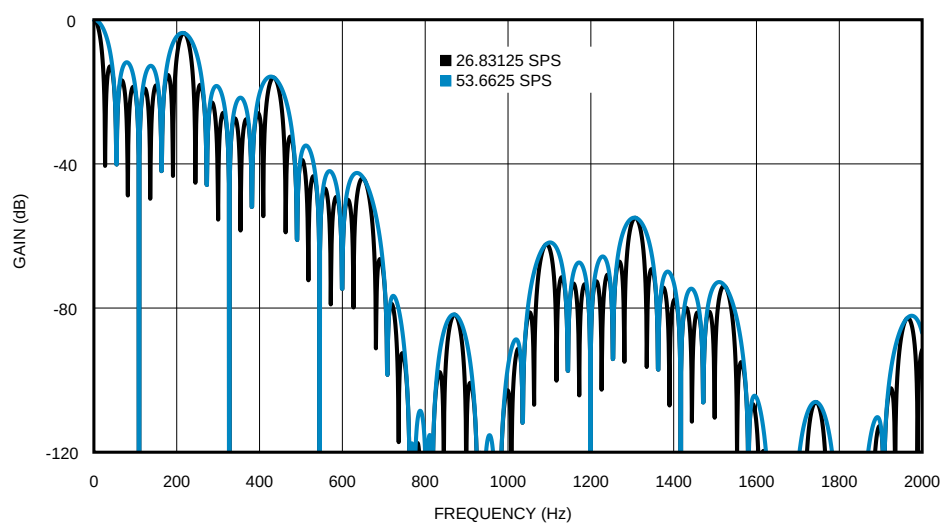
**Figure 33. Digital Filter Response, 1.6775 SPS and 3.355 SPS**



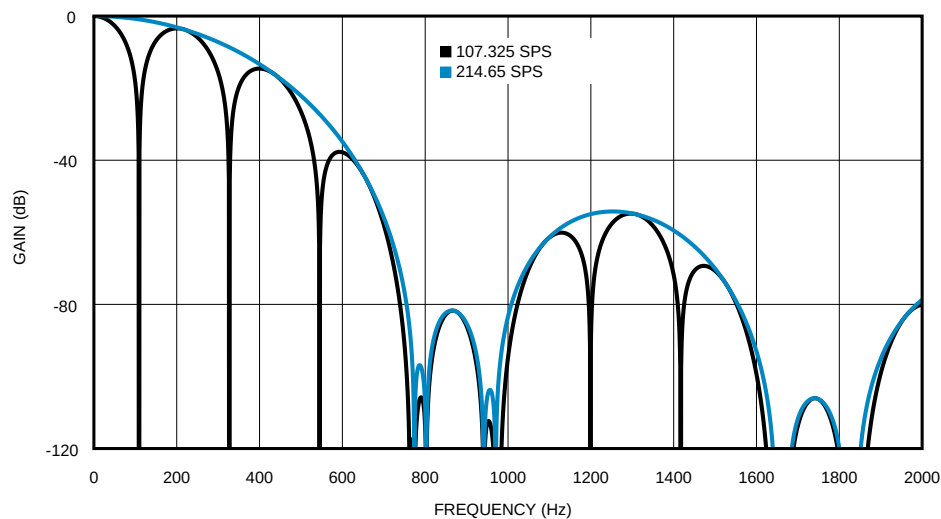
**Figure 34. Digital Filter Response, 6.71 SPS and 13.42 SPS**



**Figure 35. Digital Filter Response at 13.42 SPS**



**Figure 36. Digital Filter Response, 26.83125 SPS and 53.6625 SPS**

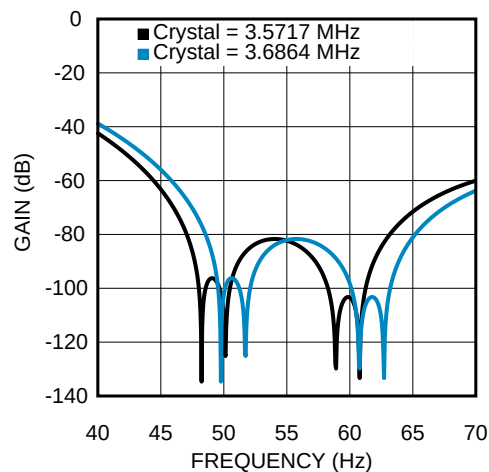


**Figure 37. Digital Filter Response 107.325 SPS and 214.65 SPS**

If the internal CLK is not being used and the external CLK is not 3.5717 MHz, then the filter response would be the same as the response shown above, but the frequency will change according to the equation:

$$f_{\text{NEW}} = [(\text{CLK}_{\text{EXT}}) / 256] \times (f_{\text{OLD}} / 13.952\text{k}) \quad (11)$$

Using the equation above, an example of the filter response for a 3.5717 MHz XTAL versus a 3.6864 MHz XTAL can be seen in Figure 38.



**Figure 38. Digital Filter Response for a 3.5717MHz versus 3.6864 MHz XTAL**

## GPIO (D0–D6)

Pins D0-D6 are general purpose input/output (GPIO) pins that can be used to control external LEDs or switches. Only a high or low value can be sourced to or read from each pin.

Figure 39 shows a flowchart how these GPIOs can be programmed.

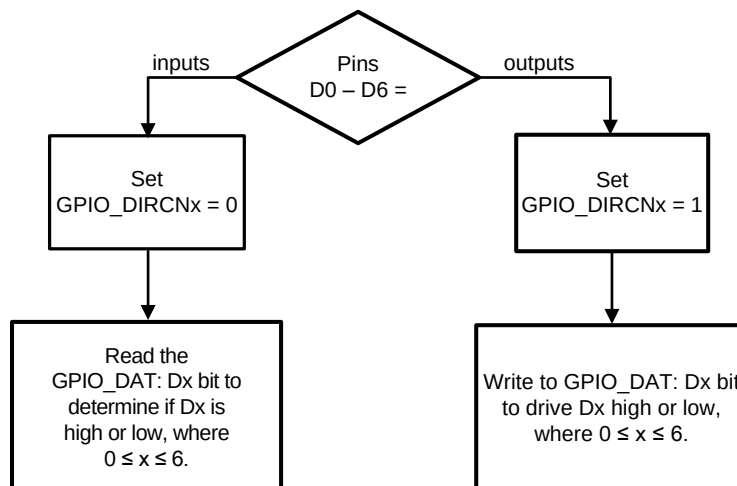


Figure 39. GPIO Register Settings

## Calibration

As seen in [Figure 40](#), there are two types of calibration: background calibration and system calibration. These calibrations are further described in the next sections.

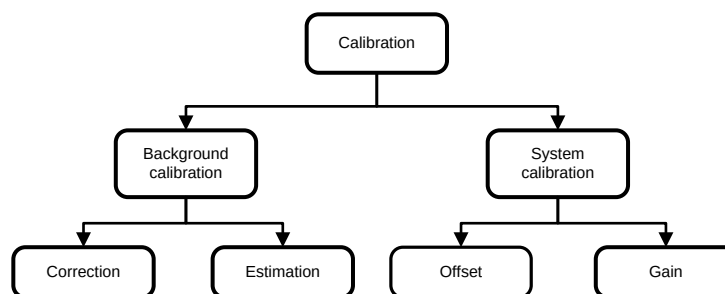


Figure 40. Types of Calibration

## Background Calibration

Background calibration is the process of continuously determining and applying the offset and gain calibration coefficients to the output codes to minimize the LMP90080-Q1's offset and gain errors. Background calibration is a feature built into the LMP90080-Q1 and is automatically done by the hardware without interrupting the input signal.

Four differential channels, CH0-CH3, each with its own gain and ODRs, can be calibrated to improve the accuracy.

### Types of Background Calibration:

[Figure 40](#) also shows that there are two types of background calibration:

1. Type 1: Correction - the process of continuously determining and applying the offset and gain calibration coefficients to the output codes to minimize the LMP90080-Q1's offset and gain errors. This method keeps track of changes in the LMP90080-Q1's gain and offset errors due to changes in the operating condition such as voltage, temperature, or time.
2. Type 2: Estimation - the process of determining and continuously applying the last known offset and gain calibration coefficients to the output codes to minimize the LMP90080-Q1's offset and gain errors. The last known offset or gain calibration coefficients can come from two sources. The first source is the default coefficient which is pre-determined and burnt in the device's non-volatile memory. The second source is from a previous calibration run of Type 1: Correction.

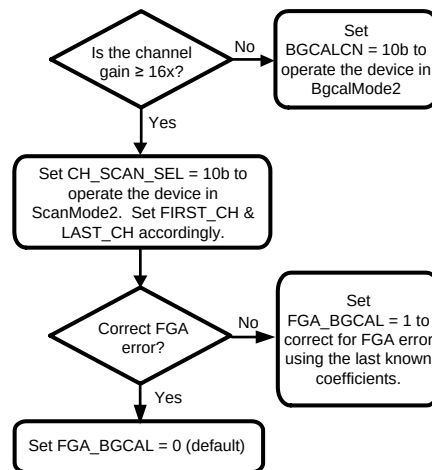


The benefits of using type 2 calibration is a higher throughput, lower power consumption, and slightly better noise. The exact savings would depend on the number of channels being scanned, and the ODR and gain of each channel.

### Using Background Calibration:

There are four modes of background calibration, which can be programmed using the BGCALCN bits. They are as follows:

1. BgcalMode0: Background Calibration OFF
2. BgcalMode1: Offset Correction / Gain Estimation
3. BgcalMode2: Offset Correction / Gain Correction. Follow [Figure 41](#) to set other appropriate registers when using this mode.
4. BgcalMode3: Offset Estimation / Gain Estimation



**Figure 41. BgcalMode2 Register Settings**

If operating in BgcalMode2, four channels (with the same ODR) are being converted, and FGA\_BGCAL = 0 (default), then the ODR is reduced by:

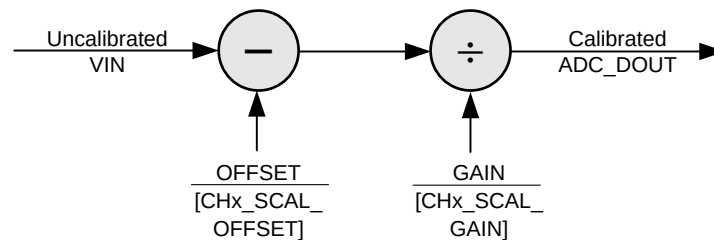
1. 0.19% of 1.6775 SPS
2. 0.39% of 3.355 SPS
3. 0.78% of 6.71 SPS
4. 1.54% of 13.42 SPS
5. 3.03% of 26.83125 SPS
6. 5.88% of 53.6625 SPS
7. 11.11% of 107.325 SPS
8. 20% of 214.65 SPS

## System Calibration

The LMP90080-Q1 provides some unique features to support easy system offset and system gain calibrations.

The System Calibration Offset Registers (CHx\_SCAL\_OFFSET) hold the System Calibration Offset Coefficients in 16-bit, two's complement binary format. The System Calibration Gain Registers (CHx\_SCAL\_GAIN) hold the System Calibration Gain Coefficient in 16-bit, 1.15, unsigned, fixed-point binary format. For each channel, the System Calibration Offset coefficient is subtracted from the conversion result prior to the division by the System Calibration Gain coefficient.

A data-flow diagram of these coefficients can be seen in [Figure 42](#).



**Figure 42. System Calibration Data-Flow Diagram**

There are four distinct sets of System Calibration Offset and System Calibration Gain Registers for use with CH0-CH3. CH4-CH6 reuse the registers of CH0-CH2, respectively.

The LMP90080-Q1 provides two system calibration modes that automatically fill the Offset and Gain coefficients for each channel. These modes are the System Calibration Offset Coefficient Determination mode and the System Calibration Gain Coefficient Determination mode. The System Calibration Offset Coefficient Determination mode must be entered prior to the System Calibration Gain Coefficient Determination mode, for each channel.

The system zero-scale condition is a system input condition (sensor loading) for which zero (0x0000) system-calibrated output code is desired. It may not, however, cause a zero input voltage at the input of the ADC.

The system reference-scale condition is usually the system full-scale condition in which the system's input (or sensor's loading) would be full-scale and the desired system-calibrated output code would be 0x8000 (unsigned 16-bit binary). However, system full-scale condition need not cause full-scale input voltage at the input of the ADC.

The system reference-scale condition is not restricted to just the system full-scale condition. In fact, it can be any arbitrary fraction of full-scale (up to 1.25 times) and the desired system-calibrated output code can be any appropriate value (up to 0xA000). The CHx\_SCAL\_GAIN register must be written with the desired system-calibrated output code (default: 0x8000) before entering the System Calibration Gain Coefficient Determination mode. This helps in in-place system calibration.

Below are the detailed procedures for using the System Calibration Offset Coefficient Determination and System Calibration Gain Coefficient Determination modes.

### System Calibration Offset Coefficient Determination mode

1. Apply system zero-scale condition to the channel (CH0/CH1/CH2/CH3).
2. Enter the System Calibration Offset Coefficient Determination mode by programming 0x1 in the SCALCN register.
3. The LMP90080-Q1 starts a fresh conversion at the selected output data rate for the selected channel. At the end of the conversion, the CHx\_SCAL\_OFFSET register is filled-in with the System Calibration Offset coefficient.
4. The System Calibration Offset Coefficient Determination mode is automatically exited.
5. The computed calibration coefficient is accurate only to the effective resolution of the device and will probably contain some noise. The noise factor can be minimized by computing over many times, averaging (externally) and putting the resultant value back into the register. Alternatively, select the output data rate to be 26.83 sps or 1.67 sps.

### System Calibration Gain Coefficient Determination mode

1. Repeat the System Calibration Offset Coefficient Determination to calibrate the System offset for the channel.
2. Apply the system reference-scale condition to the channel CH0/CH1/CH2/CH3.
3. In the CHx\_SCAL\_GAIN register, program the expected (desired) system-calibrated output code for this condition in 16-bit unsigned format.
4. Enter the System Calibration Gain Coefficient Determination mode by programming 0x3 in the SCALCN register.
5. The LMP90080-Q1 starts a fresh conversion at the selected output data rate for the channel. At the end of the conversion, the CHx\_SCAL\_GAIN is filled-in (or overwritten) with the System Calibration Gain coefficient.
6. The System Calibration Gain Coefficient Determination mode is automatically exited.
7. The computed calibration coefficient is accurate only to the effective resolution of the device and will probably contain some noise. The noise factor can be minimized by computing over many times, averaging (externally) and putting the resultant value back into the register. Alternatively, select the output data rate to be 26.83 sps or 1.67 sps.

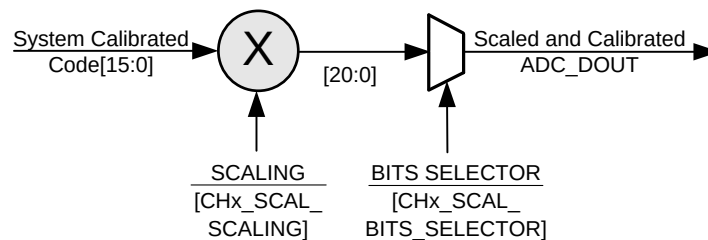
### Post-calibration Scaling

The LMP90080-Q1 allows scaling (multiplication and shifting) for the System Calibrated result. This eases downstream processing, if any. Multiplication is done using the System Calibration Scaling Coefficient in the CHx\_SCAL\_SCALING register and shifting is done using the System Calibration Bits Selector in the CHx\_SCAL\_BITS\_SELECTOR register.

The System Calibration Bits Selector value should ideally be the logarithm (to the base 2) of the System Calibration Scaling Coefficient value.

There are four distinct sets of System Calibration Scaling and System Calibration Bits Selector Registers for use with CH0-CH3. CH4-CH6 reuse the registers of CH0-CH2, respectively.

A data-flow diagram of these coefficients can be seen in [Figure 43](#).



**Figure 43. Post-calibration Scaling Data-Flow Diagram**

### Channels Scan Mode

There are four scan modes. These scan modes are selected using the CH\_SCAN: CH\_SCAN\_SEL bit. The first scanned channel is FIRST\_CH, and the last scanned channel is LAST\_CH; they are both located in the CH\_SCAN register.

The CH\_SCAN register is double buffered. That is, user inputs are stored in a slave buffer until the start of the next conversion during which time they are transferred to the master buffer. Once the slave buffer is written, subsequent updates are disregarded until a transfer to the master buffer happens. Hence, it may be appropriate to check the CH\_SCAN\_NRDY bit before programming the CH\_SCAN register.

### ScanMode0: Single-Channel Continuous Conversion

The LMP90080-Q1 continuously converts the selected FIRST\_CH.

Do not operate in this scan mode if gain  $\geq 16$  and the LMP90080-Q1 is running in background calibration modes BgcalMode1 or BgcalMode2. If this is the case, then it is more suitable to operate the device in ScanMode2 instead.

**ScanMode1: Multiple-Channels Single Scan**

The LMP90080-Q1 converts one or more channels starting from FIRST\_CH to LAST\_CH, and then enters the stand-by state.

**ScanMode2: Multiple-Channels Continuous Scan**

The LMP90080-Q1 continuously converts one or more channels starting from FIRST\_CH to LAST\_CH, and then it repeats this process.

**ScanMode3: Multiple-Channels Continuous Scan with Burnout Currents**

This mode is the same as ScanMode2 except that the burnout current is provided in a serially scanned fashion (injected in a channel after it has undergone a conversion). Thus it avoids burnout current injection from interfering with the conversion result for the channel.

The sensor diagnostic burnout currents are available for all four scan modes. The burnout current is further gated by the BURNOUT\_EN bit for each channel. ScanMode3 is the only mode that scans multiple channels while injecting burnout currents without interfering with the signal. This is described in details in [Burnout Currents](#).

**Sensor Interface**

The LMP90080-Q1 contains two excitation currents (IB1 & IB2) for sourcing external sensors, and two burnout currents for sensor diagnostics. They are described in the next sections.

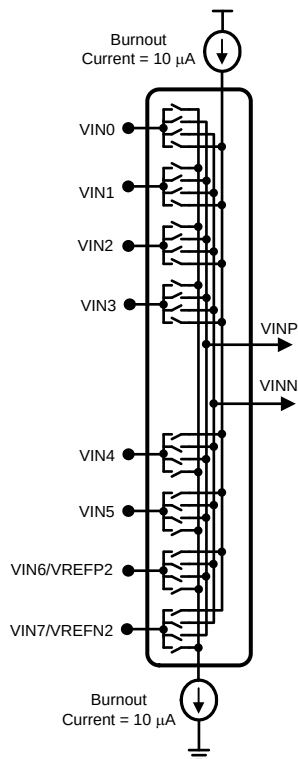
**IB1 & IB2 - Excitation Currents**

IB1 and IB2 can be used for providing currents to external sensors, such as RTDs or bridge sensors. 100µA to 1000µA, in steps of 100µA, can be sourced by programming the ADC\_AUXCN: RTD\_CUR\_SEL bits.

Refer to [3-Wire RTD](#) to see how IB1 and IB2 can be used to source a 3-wire RTD.

**Burnout Currents**

As shown in [Figure 44](#), the LMP90080-Q1 contains two internal 10 µA burnout current sources, one sourcing current from  $V_A$  to  $V_{INP}$ , and the other sinking current from  $V_{INN}$  to ground. These currents are used for sensor diagnostics and can be enabled for each channel using the CHx\_INPUTCN: BURNOUT\_EN bit.



\* VIN3, VIN4, VIN5 are only available for LMP90080 and LMP90079

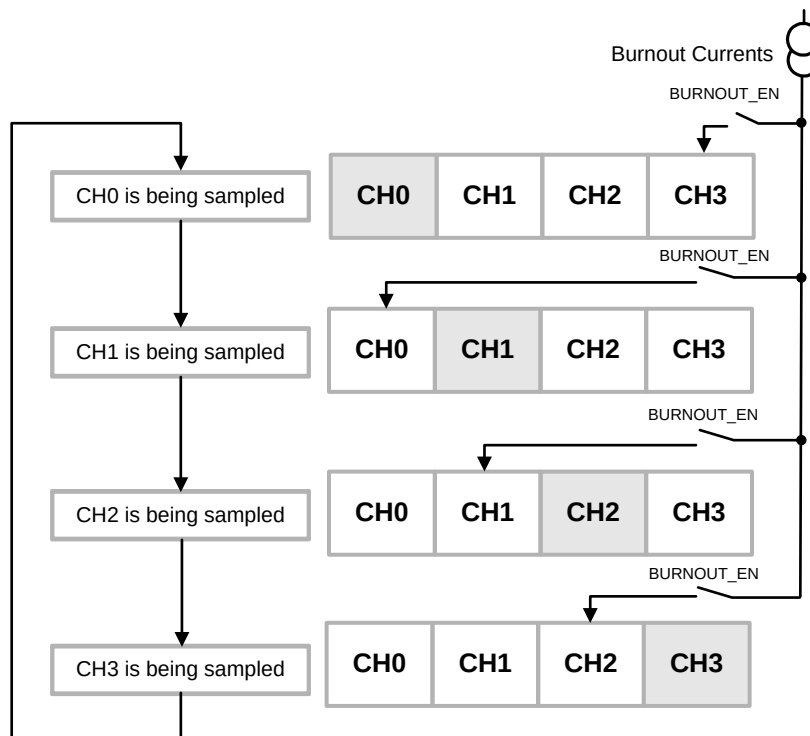
**Figure 44. Burnout Currents**

### Burnout Current Injection:

Burnout currents are injected differently depending on the channel scan mode selected.

When BURNOUT\_EN = 1 and the device is operating in ScanMode0, 1, or 2, the burnout currents are injected into all the channels for which the BURNOUT\_EN bit is selected. This will cause problems and hence in this mode, more than one channel should not have its BURNOUT\_EN bit selected. Also, the burnout current will interfere with the signal and introduce a fixed error depending on the particular external sensor.

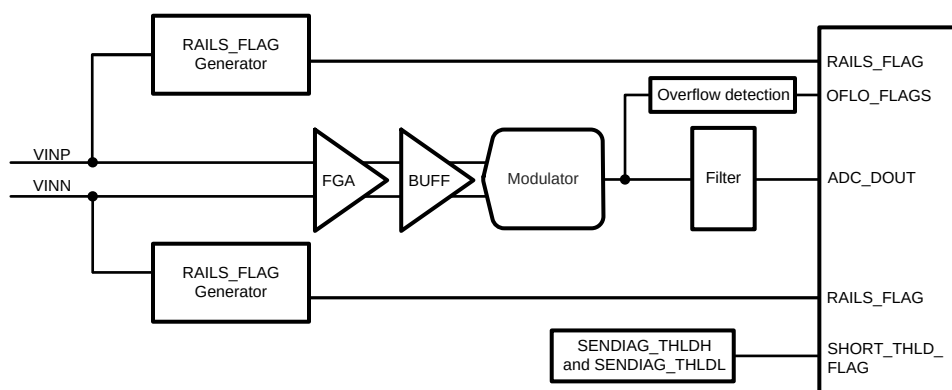
When BURNOUT\_EN = 1 and the device is operating in ScanMode3, burnout currents are injected into the last sampled channel on a cyclical basis (Figure 45). In this mode, burnout currents injection is truly done in the background without affecting the accuracy of the on-going conversion. Operating in this mode is recommended.



**Figure 45. Burnout Currents Injection for ScanMode3**

### Sensor Diagnostic Flags

Burnout currents can be used to verify that an external sensor is still operational before attempting to make measurements on that channel. A non-operational sensor means that there is a possibility the connection between the sensor and the LMP90080-Q1 is open circuited, short circuited, shorted to  $V_A$  or GND, overloaded, or the reference may be absent. The sensor diagnostic flags diagram can be seen in [Figure 46](#).



**Figure 46. Sensor Diagnostic Flags Diagram**

The sensor diagnostic flags are located in the SENDIAG\_FLAGS register and are described in further details below.

### SHORT\_THLD\_FLAG:

The short circuit threshold flag is used to report a short-circuit condition. It is set when the output voltage ( $V_{OUT}$ ) is within the absolute  $V_{threshold}$ .  $V_{threshold}$  can be programmed using the 8-bit SENDIAG\_THLDH register.

For example, assume  $V_{REF} = 5V$ , gain = 1, SENDIAG\_THLD = 0xDA (218d). In this case,  $V_{threshold}$  can be calculated as:

$$V_{threshold} = [(SENDIAG\_THLD)(2)(V_{REF})] / [(Gain)(2^{16})] \quad (12)$$

$$V_{threshold} = [(218)(2)(5V)] / [(1)(2^{16})] \quad (13)$$

$$V_{threshold} = 33.3 \text{ mV} \quad (14)$$

When  $(-33.3\text{mV}) \leq V_{OUT} \leq (33.3\text{mV})$ , then SHORT\_THLD\_FLAG = 1; otherwise, SHORT\_THLD\_FLAG = 0.

### RAILS\_FLAG:

The rails flag is used to detect if one of the sampled channels is within 50mV of the rails potential ( $V_A$  or  $V_{SS}$ ). This can be further investigated to detect an open-circuit or short-circuit condition. If the sampled channel is near a rail, then RAILS\_FLAG = 1; otherwise, RAILS\_FLAG = 0.

### POR\_AFT\_LST\_RD:

If POR\_AFT\_LST\_READ = 1, then there was a power-on reset since the last time the SENDIAG\_FLAGS register was read. This flag's status is cleared when this bit is read, unless this bit is set again on account of another power-on-reset event in the intervening period.

### OFLO\_FLAGS:

OFLO\_FLAGS is used to indicate whether the modulator is over-ranged or under-ranged. The following conditions are possible:

1. OFLO\_FLAGS = 0x0: Normal Operation
2. OFLO\_FLAGS = 0x1: The differential input is more than  $(\pm V_{REF}/Gain)$  but is not more than  $\pm(1.3*V_{REF}/Gain)$  to cause a modulator over-range.
3. OFLO\_FLAGS = 0x2: The modulator was over-ranged towards  $+V_{REF}/Gain$ .
4. OFLO\_FLAGS = 0x3: The modulator was over-ranged towards  $-V_{REF}/Gain$ .

The condition of OFLO\_FLAGS = 10b or 11b can be used in conjunction with the RAILS\_FLAG to determine the fault condition.

### SAMPLED\_CH:

These three bits show the channel number for which the ADC\_DOUT and SENDIAG\_FLAGS are available. This does not necessarily indicate the current channel under conversion because the conversion frame and computation of results from the channels are pipelined. That is, while the conversion is going on for a particular channel, the results for the previous conversion (of the same or a different channel) are available.

## Serial Digital Interface

A synchronous 4-wire serial peripheral interface (SPI) provides access to the internal registers of LMP90080-Q1 via CSB, SCLK, SDI, SDO/DRDYB.

### Register Address (ADDR)

All registers are memory-mapped. A register address (ADDR) is composed of an upper register address (URA) and lower register address (LRA) as shown in Table 3. For example, ADDR 0x3A has URA=0x3 and LRA=0xA.

**Table 3. ADDR Map**

| Bit  | [6:4] | [3:0] |
|------|-------|-------|
| Name | URA   | LRA   |

## Register Read/Write Protocol

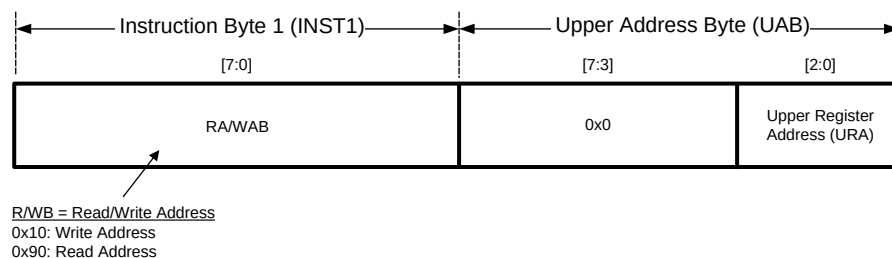
Figure 47 shows the protocol how to write to or read from a register.

Transaction 1 sets up the upper register address (URA) where the user wants to start the register-write or register-read.

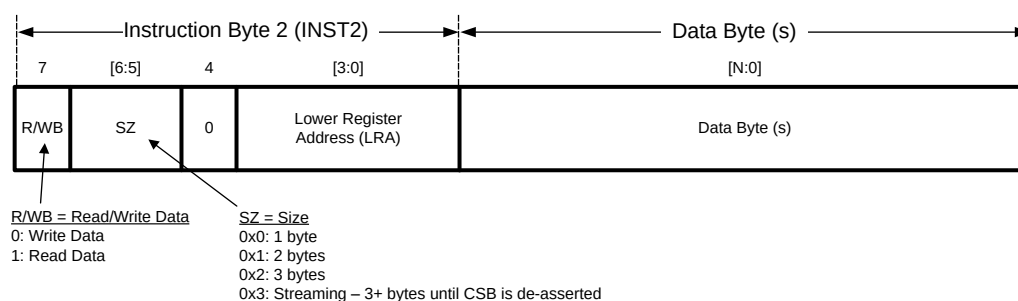
Transaction 2 sets the lower register address (LRA) and includes the Data Byte(s), which contains the incoming data from the master or outgoing data from the LMP90080-Q1.

Examples of register-reads or register-writes can be found in [Register Read/Write Examples](#).

**Transaction 1 – URA Setup** – necessary only when the previous URA is different than the desired URA.



### Transaction 2 – Data Access



**Figure 47. Register Read/Write Protocol**

## Streaming

When writing/reading 3+ bytes, the user must operate the device in Normal Streaming mode or Controlled Streaming mode. In the Normal Streaming mode, which is the default mode, data runs continuously starting from ADDR until CSB deasserts. This mode is especially useful when programming all the configuration registers in a single transaction. See [Normal Streaming Example](#) for an example of the Normal Streaming mode.

In the Controlled Streaming mode, data runs continuously starting from ADDR until the data has run through all (STRM\_RANGE + 1) registers. For example, if the starting ADDR is 0x1C, STRM\_RANGE = 5, then data will be written to or read from the following ADDRs: 0x1C, 0x1D, 0x1E, 0x1F, 0x20, 0x21. Once the data reaches ADDR 0x21, LMP90080-Q1 will wrap back to ADDR 0x1C and repeat this process until CSB deasserts. See [Controlled Streaming Example](#) for an example of the Controlled Streaming mode.

If streaming reaches ADDR 0x7F, then it will wrap back to ADDR 0x00. Furthermore, reading back the Upper Register Address after streaming will report the Upper Register Address at the start of streaming, not the Upper Register Address at the end of streaming.

To stream, write 0x3 to INST2's SZ bits as seen in [Figure 47](#). To select the stream type, program the SPI\_STREAMCN: STRM\_TYPE bit. The STRM\_RANGE can also be programmed in the same register.



## CSB - Chip Select Bar

An SPI transaction begins when the master asserts (active low) CSB and ends when the master deasserts (active high) CSB. Each transaction might be separated by a subsequent one with a CSB deassertion, but this is optional. Once CSB is asserted, it must not pulse (deassert and assert again) during a (desired) transaction.

CSB can be grounded in systems where the LMP90080-Q1 is the only SPI slave. This frees the software from handling the CSB. Care has to be taken to avoid any false edge on SCLK, and while operating in this mode, the streaming transaction should not be used because exiting from this mode can only be done through a CSB deassertion.

## SPI Reset

SPI Reset resets the SPI-Protocol State Machine by monitoring the SDI for at least 73 consecutive 1's at each SCLK rising edge. After an SPI Reset, SDI is monitored for a possible Write Instruction at each SCLK rising edge.

SPI Reset will reset the Upper Address Register (URA) to 0, but the register contents are not reset.

By default, SPI reset is disabled, but it can be enabled by writing 0x01 to SPI Reset Register (ADDR 0x02).

## DRDYB - Data Ready Bar

DRDYB is a signal generated by the LMP90080-Q1 that indicates a fresh conversion data is available in the ADC\_DOUT registers.

DRDYB is automatically asserted every (1/ODR) second as seen in Figure 48. Before the next assertion, DRDYB will pulse for  $t_{DRDYB}$  second. The value for  $t_{DRDYB}$  can be found in Timing Diagrams.



Figure 48. DRDYB Behavior

If ADC\_DOUT is being read while a new ADC\_DOUT becomes available, then the ADC\_DOUT that is being read is still valid (Figure 49). DRDYB will still be deasserted every 1/ODR second, but a consecutive read on the ADC\_DOUT register will fetch the newly converted data available.

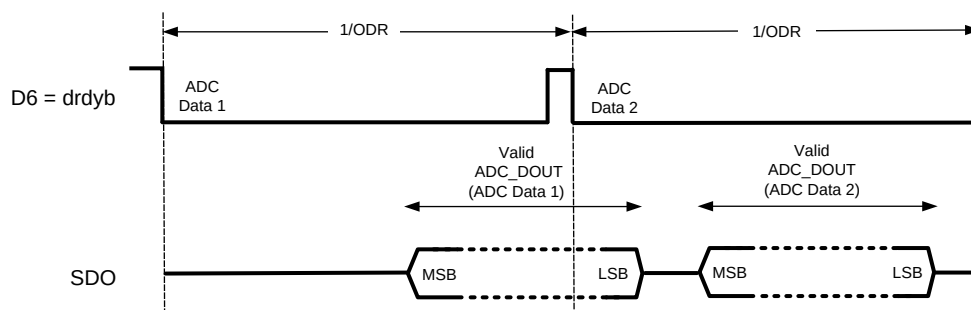
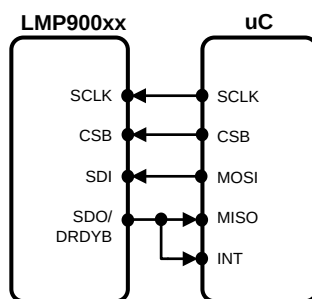


Figure 49. DRDYB Behavior for an Incomplete ADC\_DOUT Reading

DRDYB can also be accessed via registers using the DT\_AVAIL\_B bit. This bit indicates when fresh conversion data is available in the ADC\_DOUT registers. If new conversion data is available, then DT\_AVAIL\_B = 0; otherwise, DT\_AVAIL\_B = 1.

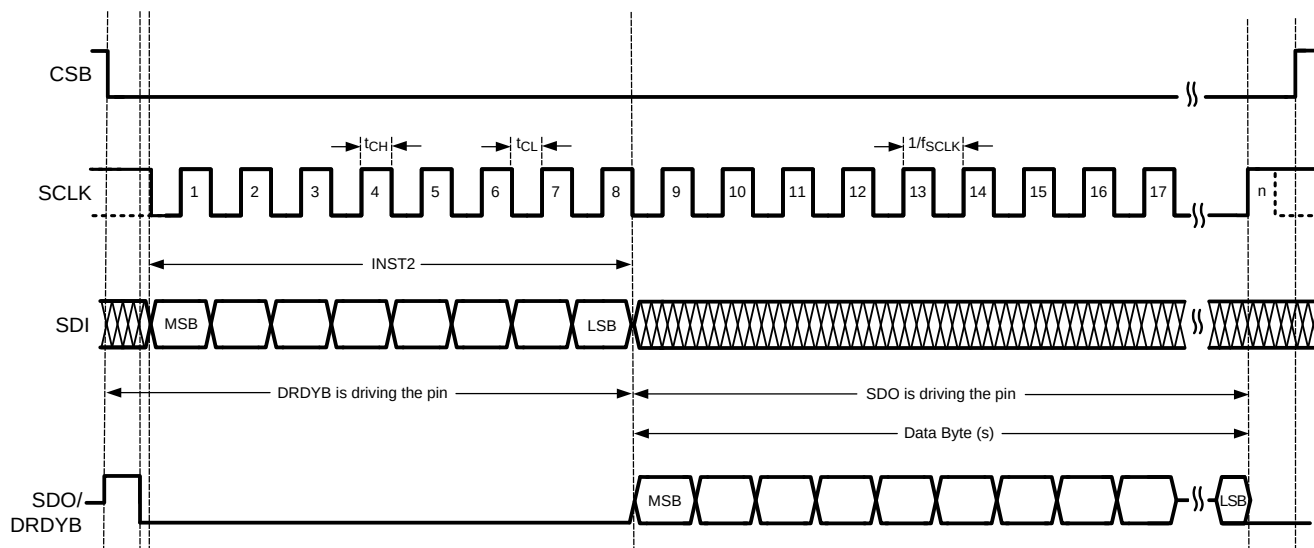
A complete reading for DT\_AVAIL\_B occurs when the MSB of ADC\_DOUTH is read out. This bit cannot be reset even if REG\_AND\_CNVRST = 0xC3.

**DrdybCase1: Combining SDO/DRDYB with SDO\_DRDYB\_DRIVER = 0x00****Figure 50. DrdybCase1 Connection Diagram**

As shown in [Figure 50](#), the drdyb signal and SDO can be multiplexed on the same pin as their functions are mostly complementary. In fact, this is the default mode for the SDO/DRDYB pin.

[Figure 51](#) shows a timing protocol for DrdybCase1. In this case, start by asserting CSB first to monitor a drdyb assertion. When the drdyb signal asserts, begin writing the Instruction Bytes (INST1, UAB, INST2) to read from or write to registers. Note that INST1 and UAB are omitted from the figure below because this transaction is only required if a new UAB needs to be implemented.

While the CSB is asserted, DRDYB is driving the SDO/DRDYB pin unless the device is reading data, in which case, SDO will be driving the pin. If CSB is deasserted, then the SDO/DRDYB pin is High-Z.

**Figure 51. Timing Protocol for DrdybCase1**

## DrdybCase2: Combining SDO/DRDYB with SDO\_DRDYB\_DRIVER = 0x03

SDO/DRDYB can be made independent of CSB by setting SDO\_DRDYB\_DRIVER = 0x03 in the SPI Handshake Control register. In this case, DRDYB will drive the pin unless the device is reading data, independent of the state of CSB. SDO will drive the pin when CSB is asserted and the device is reading data.

With this scheme, one can use SDO/DRDYB as a true interrupt source, independent of the state of CSB. But this scheme can only be used when the LMP90080-Q1 is the only device connected to the master's SPI bus because the SDO/DRDYB pin will be DRDYB even when CSB is deasserted.

The timing protocol for this case can be seen in Figure 52. When drdyb asserts, assert CSB to start the SPI transaction and begin writing the Instruction Bytes (INST1, UAB, INST2) to read from or write to registers.

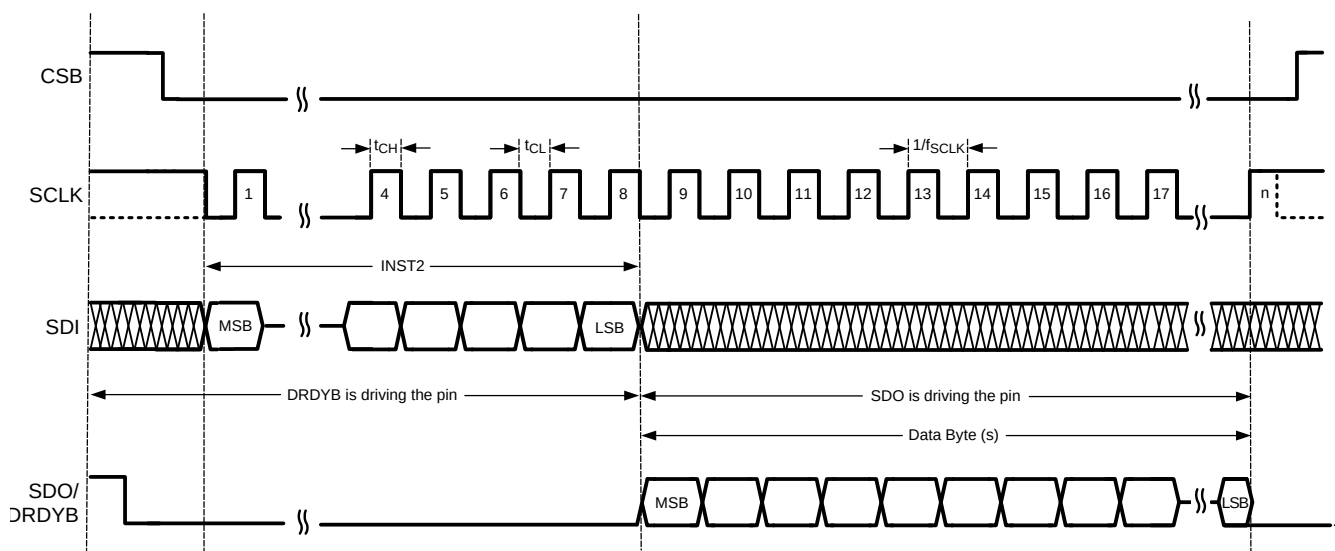


Figure 52. Timing Protocol for DrdybCase2

## DrdybCase3: Routing DRDYB to D6

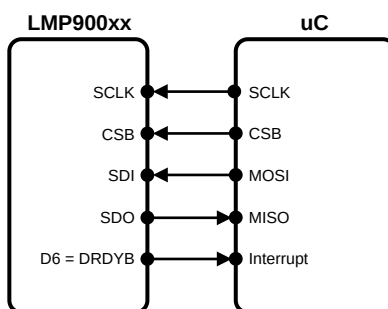


Figure 53. DrdybCase3 Connection Diagram

The drdyb signal can be routed to pin D6 by setting SPI\_DRDYB\_D6 high and SDO\_DRDYB\_DRIVER to 0x4. This is the behavior for DrdybCase3 as shown in Figure 53.

The timing protocol for this case can be seen in Figure 54. Since DRDYB is separated from SDO, it can be monitored using the interrupt or polling method. If polled, the drdyb signal needs to be polled faster than  $t_{DRDYB}$  to detect a drdyb assertion. When drdyb asserts, assert CSB to start the SPI transaction and begin writing the Instruction Bytes (INST1, UAB, INST2) to read from or write to registers.

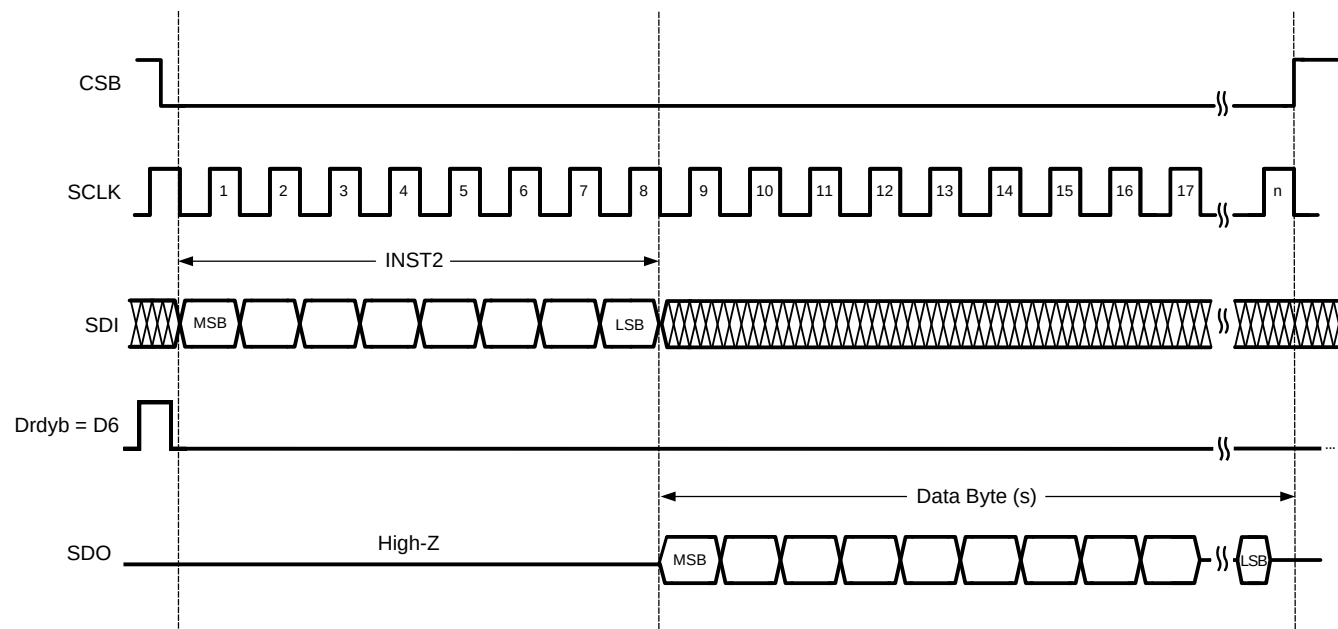


Figure 54. Timing Protocol for DrdybCase3

### Data Only Read Transaction

In a data only read transaction, one can directly access the data byte(s) as soon as the CSB is asserted without having to send any instruction byte. This is useful as it brings down the latency as well as the overhead associated with the instruction byte (as well as the Upper Address Byte, if any).

In order to use the data only transaction, the device must be placed in the data first mode. The following table lists transaction formats for placing the device in and out of the data first mode and reading the mode status.

Table 4. Data First Mode Transactions

|                                     | Bit[7] | Bits[6:5] | Bit[4] | Bits[3:0] | Data Bytes |
|-------------------------------------|--------|-----------|--------|-----------|------------|
| Enable Data First Mode Instruction  | 1      | 11        | 1      | 1010      | None       |
| Disable Data First Mode Instruction | 1      | 11        | 1      | 1011      | None       |
| Read Mode Status Transaction        | 1      | 00        | 1      | 1111      | One        |

Note that while being in the data first mode, once the data bytes in the data only read transaction are sent out, the device is ready to start on any normal (non-data-only) transaction including the Disable Data First Mode Instruction. The current status of the data first mode (enabled/disabled status) can be read back using the Read Mode Status Transaction. This transaction consists of the Read Mode Status Instruction followed by a single data byte (driven by the device). The data first mode status is available on bit [1] of this data byte.

The data only read transaction allows reading up to eight consecutive registers, starting from any start address. Usually, the start address will be the address of the most significant byte of conversion data, but it could just as well be any other address. The start address and number of bytes to be read during the data only read transaction can be programmed using the DATA\_ONLY\_1 AND DATA\_ONLY\_2 registers respectively.

The upper register address is unaffected by a data only read transaction. That is, it retains its setting even after encountering a data only transaction. The data only transaction uses its own address (including the upper address) from the DATA\_ONLY\_1 register. When in the data first mode, the SCLK must stop high before entering the Data Only Read Transaction; this transaction should be completed before the next scheduled DRDYB deassertion.

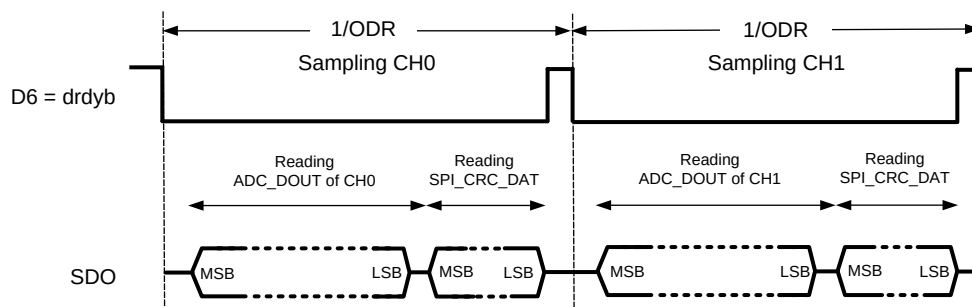
## Cyclic Redundancy Check (CRC)

CRC can be used to ensure integrity of data read from LMP90080-Q1. To enable CRC, set EN\_CRC high. Once CRC is enabled, the CRC value is calculated and stored in SPI\_CRC\_DAT so that the master device can periodically read for data comparison. The CRC is automatically reset when CSB or DRDYB is deasserted.

The CRC polynomial is  $x^8 + x^5 + x^4 + 1$ . The reset value of the SPI\_CRC\_DAT register is zero, and the final value is ones-complemented before it is sent out. Note that CRC computation only includes the bits sent out on SDO and does not include the bits of the SPI\_CRC\_DAT itself; thus it is okay to read SPI\_CRC\_DAT repeatedly.

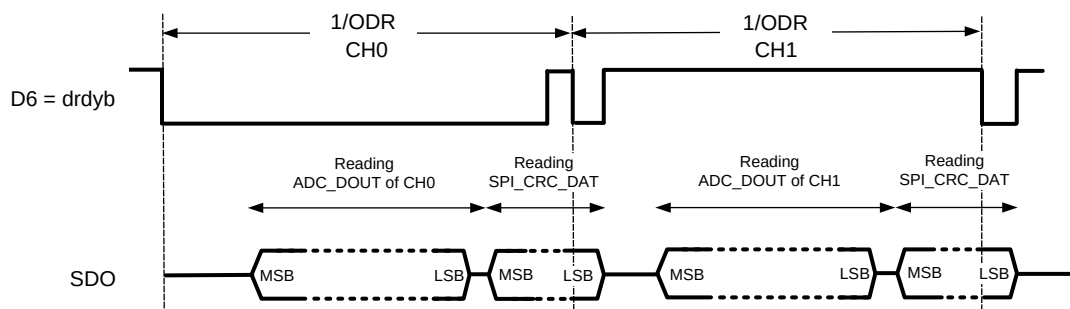
The drdyb signal normally deasserts (active high) every 1/ODR second. However, this behavior can be changed so that drdyb deassertion can occur after SPI\_CRC\_DAT is read, but not later than normal DRDYB deassertion which occurs at every 1/ODR seconds. This is done by setting bit DRDYB\_AFT\_CRC high.

The timing protocol for CRC can be found in [Figure 55](#).



**Figure 55. Timing Protocol for Reading SPI\_CRC\_DAT**

If SPI\_CRC\_DAT read extends beyond the normal DRDYB deassertion at every 1/ODR seconds, then CRC\_RST has to be set in the SPI Data Ready Bar Control Register. This is done to avoid a CRC reset at the DRDYB deassertion. Timing protocol for reading CRC with CRC\_RST set is shown in [Figure 56](#).



**Figure 56. Timing Protocol for Reading SPI\_CRC\_DAT beyond normal DRDYB deassertion at every 1/ODR seconds**

Follow the steps below to enable CRC:

1. Set SPI\_CRC\_CN = 1 (register 0x13, bit 4) to enable CRC.
2. Set DRDYB\_AFT\_CRC = 1 (register 0x13, bit 2) to deassert the DRDYB after CRC.
3. Compute the CRC externally, which should include ADC\_DOUTH and ADC\_DOUTL.
4. Collect the data and verify the reported CRC matches with the computed CRC (step above).

## Power Management

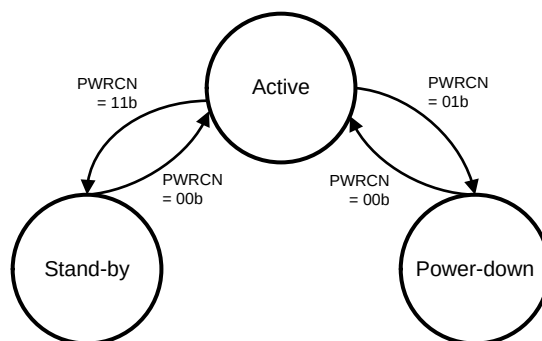
The device can be placed in Active, Power-Down, or Stand-By state.

In Power-Down, the ADC is not converting data, contents of the registers are unaffected, and there is a drastic power reduction. In Stand-By, the ADC is not converting data, but the power is only slightly reduced so that the device can quickly transition into the active state if desired.

These states can be selected using the PWRCN register. When written, PWRCN brings the device into the Active, Power-Down, or Stand-By state. When read, PWRCN indicates the state of the device.

The read value would confirm the write value after a small latency (approximately 15  $\mu$ s with the internal CLK). It may be appropriate to wait for this latency to confirm the state change. Requests not adhering to this latency requirement may be rejected.

It is not possible to make a direct transition from the power-down state to the stand-by state. This state diagram is shown below.



**Figure 57. Active, Power-Down, Stand-by State Diagram**

## Reset and Restart

Writing 0xC3 to the REG\_AND\_CNV\_RST field will reset the conversion and most of the programmable registers to their default values. The only registers that will not be reset are the System Calibration Registers (CHx\_SCAL\_OFFSET, CHx\_SCAL\_GAIN) and the DT\_AVAIL\_B bit.

If it is desirable to reset the System Calibration Coefficient Registers, then set RESET\_SYSCAL = 1 before writing 0xC3 to REG\_AND\_CNV\_RST. If the device is operating in the "System Calibration Offset/Gain Coefficient Determination" mode (SCALCN register), then write REG\_AND\_CNV\_RST = 0xC3 twice to get out of this mode.

After a register reset, any on-going conversions will be aborted and restarted. If the device is in the power-down state, then a register reset will bring it out of the power-down state.

To restart a conversion, write 1 to the RESTART bit. This bit can be used to synchronize the conversion to an external event.

After a restart conversion, the first sample is not valid. To restart with a valid first sample, issue a stand-by command followed by an active command.

## APPLICATIONS INFORMATION

### Quick Start

This section shows step-by-step instructions to configure the LMP90080-Q1 to perform a simple DC reading from CH0.

1. Apply  $V_A = V_{IO} = V_{REFP1} = 5V$ , and ground  $V_{REFN1}$
2. Apply  $V_{INP} = \frac{3}{4}V_{REF}$  and  $V_{INN} = \frac{1}{4}V_{REF}$  for CH0. Thus, set  $CH0 = V_{IN} = V_{INP} - V_{INN} = \frac{1}{2}V_{REF}$  (CH0\_INPUTCN register)
3. Set gain = 1 (CH0\_CONFIG: GAIN\_SEL = 0x0)
4. Exclude the buffer from the signal path (CH0\_CONFIG: BUF\_EN = 1)
5. Set the background to BgcalMode2 (BGCALCN = 0x2)
6. Select  $V_{REF1}$  (CH0\_INPUTCN:  $V_{REF\_SEL} = 0$ )
7. To use the internal CLK, set CLK\_EXT\_DET = 1 and CLK\_SEL = 0.
8. Follow the register read/write protocol (Figure 47) to capture ADC\_DOUT from CH0.

### Connecting the Supplies

#### $V_A$ and $V_{IO}$

Any ADC architecture is sensitive to spikes on the analog voltage,  $V_A$ , digital input/output voltage,  $V_{IO}$ , and ground pins. These spikes may originate from switching power supplies, digital logic, high power devices, and other sources. To diminish these spikes, the LMP90080-Q1's  $V_A$  and  $V_{IO}$  pins should be clean and well bypassed. A 0.1  $\mu F$  ceramic bypass capacitor and a 1  $\mu F$  tantalum capacitor should be used to bypass the LMP90080-Q1 supplies, with the 0.1  $\mu F$  capacitor placed as close to the LMP90080-Q1 as possible.

Since the LMP90080-Q1 has both external  $V_A$  and  $V_{IO}$  pins, the user has two options on how to connect these pins. The first option is to tie  $V_A$  and  $V_{IO}$  together and power them with the same power supply. This is the most cost effective way of powering the LMP90080-Q1 but is also the least ideal because noise from  $V_{IO}$  can couple into  $V_A$  and negatively affect performance. The second option involves powering  $V_A$  and  $V_{IO}$  with separate power supplies. These supply voltages can have the same amplitude or they can be different.

#### $V_{REF}$

Operation with  $V_{REF}$  below  $V_A$  is also possible with slightly diminished performance. As  $V_{REF}$  is reduced, the range of acceptable analog input voltages is also reduced. Reducing the value of  $V_{REF}$  also reduces the size of the LSB. When the LSB size goes below the noise floor of the LMP90080-Q1, the noise will span an increasing number of codes and performance will degrade. For optimal performance,  $V_{REF}$  should be the same as  $V_A$  and sourced with a clean source that is bypassed with a ceramic capacitor value of 0.1  $\mu F$  and a tantalum capacitor of 10  $\mu F$ .

LMP90080-Q1 also allows ratiometric connection for noise immunity reasons. A ratiometric connection is when the ADC's  $V_{REFP}$  and  $V_{REFN}$  are used to excite the input device's (i.e. a bridge sensor) voltage references. This type of connection severely attenuates any  $V_{REF}$  ripple seen the ADC output, and is thus strongly recommended.

### ADC\_DOUT Calculation

The output code of the LMP90080-Q1 can be calculated as:

$$ADC\_DOUT = \pm \left( \frac{(VINP - VINN) \times GAIN}{VREFP - VREFN} \right) \times (2^{15}) \quad (15)$$

Output Code

ADC\_DOUT is in 16-bit two's complement binary format. The largest positive value is 0x7FFF (or 32767 in decimal), while the largest negative value is 0x8000 (or 32768 in decimal). In case of an over range the value is automatically clamped to one of these two values.

Figure 58 shows the theoretical output code, ADC\_DOUT, vs. analog input voltage,  $V_{IN}$ , using the equation above.

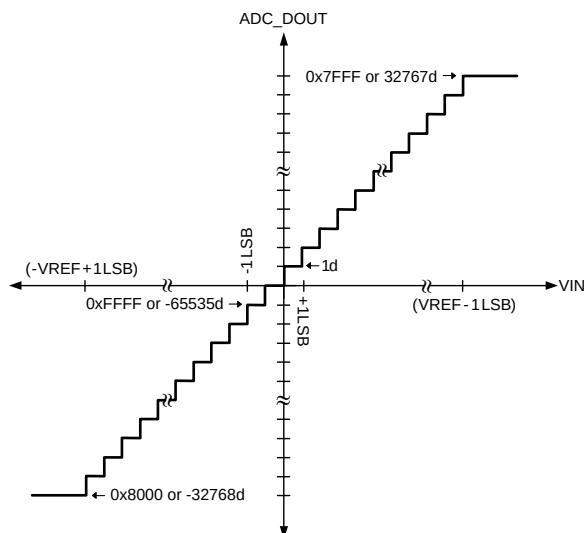


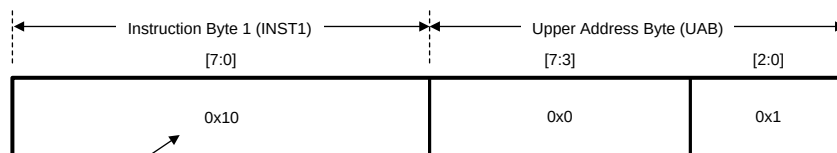
Figure 58. ADC\_DOUT vs. VIN of a 16-Bit Resolution (VREF = 5.5V, Gain = 1).

## Register Read/Write Examples

### Writing to Register Examples

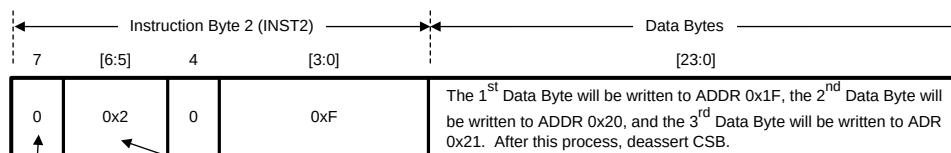
Using the register read/write protocol shown in Figure 47, the following example shows how to write three data bytes starting at register address (ADDR) 0x1F. After the last byte has been written to ADDR 0x21, deassert CSB to end the register-write.

**Transaction 1 – URA Setup** – necessary only when the previous URA is different than the desired URA.



R/WB = Read/Write Address  
 0x10: Write Address  
 0x90: Read Address

**Transaction 2 – Data Access**



R/WB = Read/Write Data  
 0: Write Data  
 1: Read Data

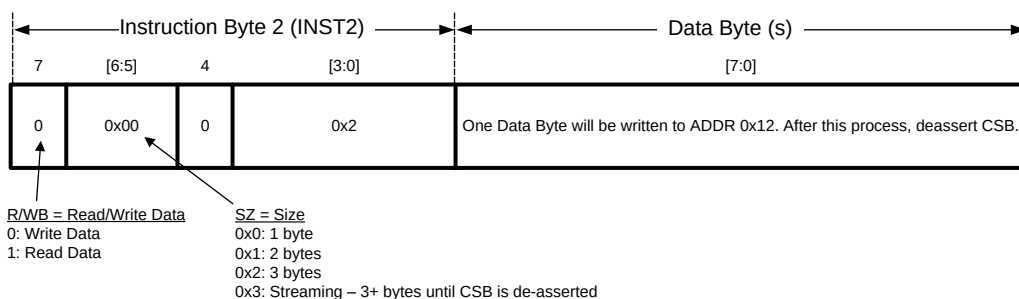
SZ = Size  
 0x0: 1 byte  
 0x1: 2 bytes  
 0x2: 3 bytes  
 0x3: Streaming – 3+ bytes until CSB is de-asserted

Figure 59. Register-Write Example 1



The next example shows how to write one data byte to ADDR 0x12. Since the URA for this example is the same as the last example, transaction 1 can be omitted.

### Transaction 2 – Data Access

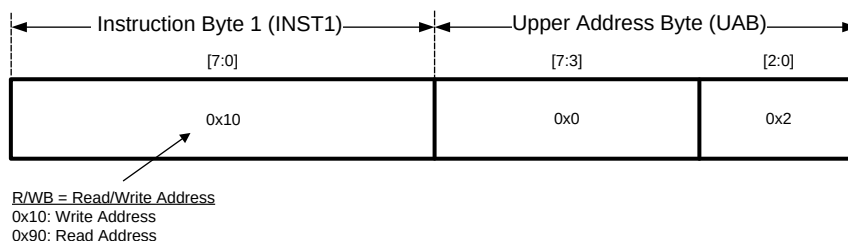


**Figure 60. Register-Write Example 2**

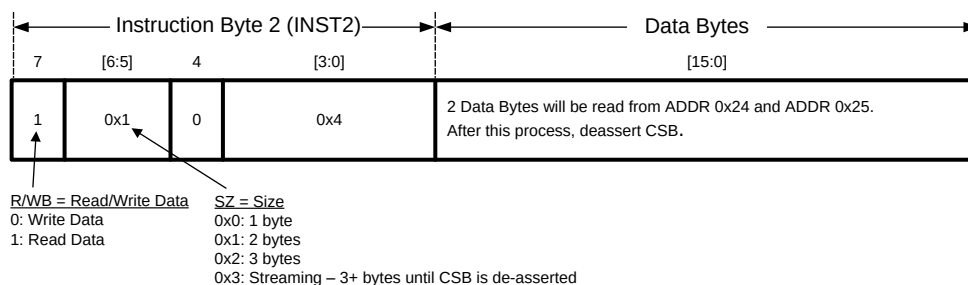
### Reading from Register Example

The following example shows how to read two bytes. The first byte will be read from starting ADDR 0x24, and the second byte will be read from ADDR 0x25.

**Transaction 1 – URA Setup** – necessary only when the previous URA is different than the desired URA.



### Transaction 2 – Data Access



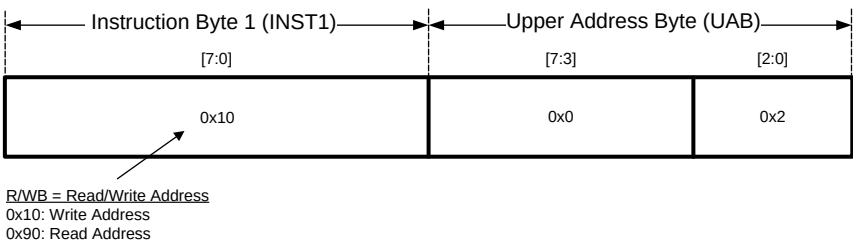
**Figure 61. Register-Read Example**

## Streaming Examples

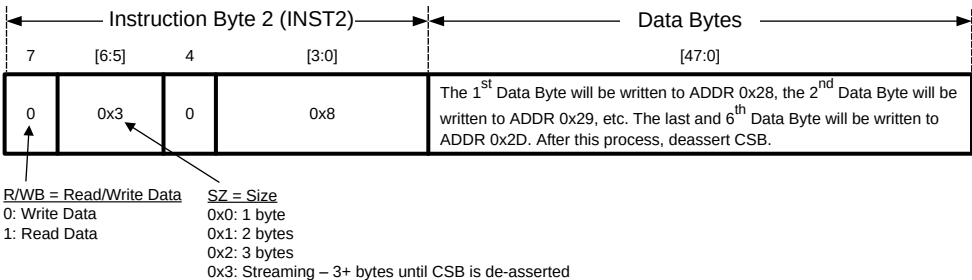
### Normal Streaming Example

This example shows how to write six data bytes starting at ADDR 0x28 using the Normal Streaming mode. Because the default STRM\_TYPE is the Normal Streaming mode, setting up the SPI\_STREAMCN register can be omitted.

**Transaction 1 – URA Setup** – necessary only when the previous URA is different than the desired URA.



### Transaction 2 – Data Access



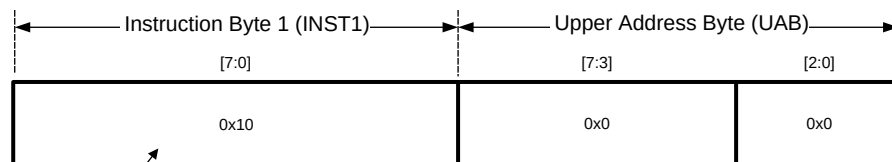
**Figure 62. Normal Streaming Example**

### Controlled Streaming Example

This example shows how to read the 16-bit conversion data (ADC\_DOUT) four times using the Controlled Streaming mode. The ADC\_DOUT registers consist of ADC\_DOUTH at ADDR 0x1A and ADC\_DOUTL at ADDR 0x1B.

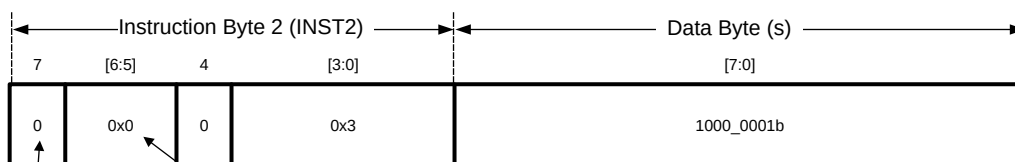
The first step ([Figure 63](#)) sets up the SPI\_STREAMCN register. This step enters the Controlled Streaming mode by setting STRM\_TYPE high in ADDR 0x03. Since two registers (ADDR 0x1A - 0x1B) need to be read, the STRM\_RANGE is 1.

**Transaction 1 – URA Setup** – necessary only when the previous URA is different than the desired URA.



R/WB = Read/Write Address  
0x10: Write Address  
0x90: Read Address

**Transaction 2 – Data Access**



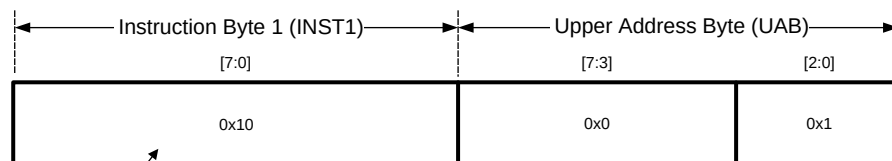
R/WB = Read/Write Data  
0: Write Data  
1: Read Data

SZ = Size  
0x0: 1 byte  
0x1: 2 bytes  
0x2: 3 bytes  
0x3: Streaming – 3+ bytes until CSB is de-asserted

**Figure 63. Setting up SPI\_STREAMCN**

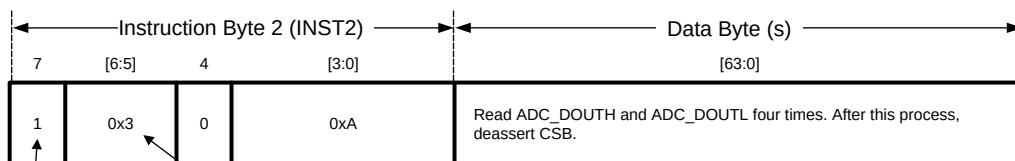
The next step shows how to perform the Controlled Streaming mode so that the master device will read ADC\_DOUT from ADDR 0x1A and 0x1B, then wrap back to ADDR 0x1A, and repeat this process for four times. After this process, deassert CSB to end the Controlled Streaming mode.

**Transaction 1 – URA Setup** – necessary only when the previous URA is different than the desired URA.



R/WB = Read/Write Address  
0x10: Write Address  
0x90: Read Address

**Transaction 2 – Data Access**



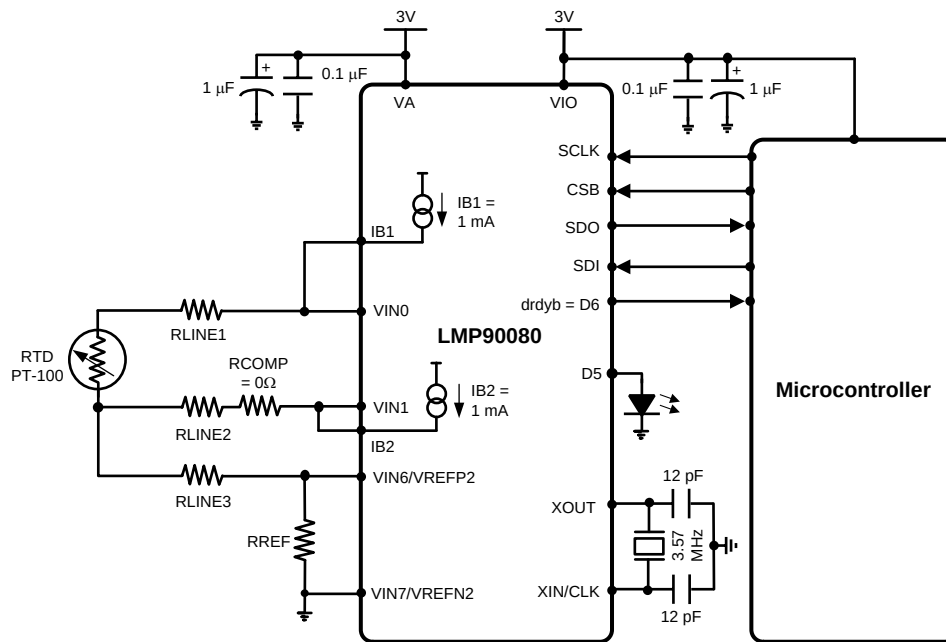
R/WB = Read/Write Data  
0: Write Data  
1: Read Data

SZ = Size  
0x0: 1 byte  
0x1: 2 bytes  
0x2: 3 bytes  
0x3: Streaming – 3+ bytes until CSB is de-asserted

**Figure 64. Controlled Streaming Example**

## Example Applications

### 3-Wire RTD



**Figure 65. Topology #1: 3-wire RTD Using 2 Current Sources**

Figure 65 shows the first topology for a 3-wire resistive temperature detector (RTD) application. Topology #1 uses two excitation current sources, IB1 and IB2, to create a differential voltage across VIN0 and VIN1. As a result of using both IB1 and IB2, only one channel (VIN0-VIN1) needs to be measured. As shown in Equation 16, the equation for this channel is  $IB1 \times (RTD - RCOMP)$  assuming that  $RLINE1 = RLINE2$ .

$$\begin{aligned} VIN0 &= IB1 (RLINE1 + RTD) + (IB1 + IB2) (RLINE3 + RREF) \\ VIN1 &= IB2 (RLINE2 + RCOMP) + (IB1 + IB2) (RLINE3 + RREF) \\ \text{If } RLINE1 &= RLINE2, \text{ then:} \\ VIN &= (VIN0 - VIN1) = IB1 (RTD - RCOMP) \end{aligned}$$

VIN Equation for Topology #1

(16)

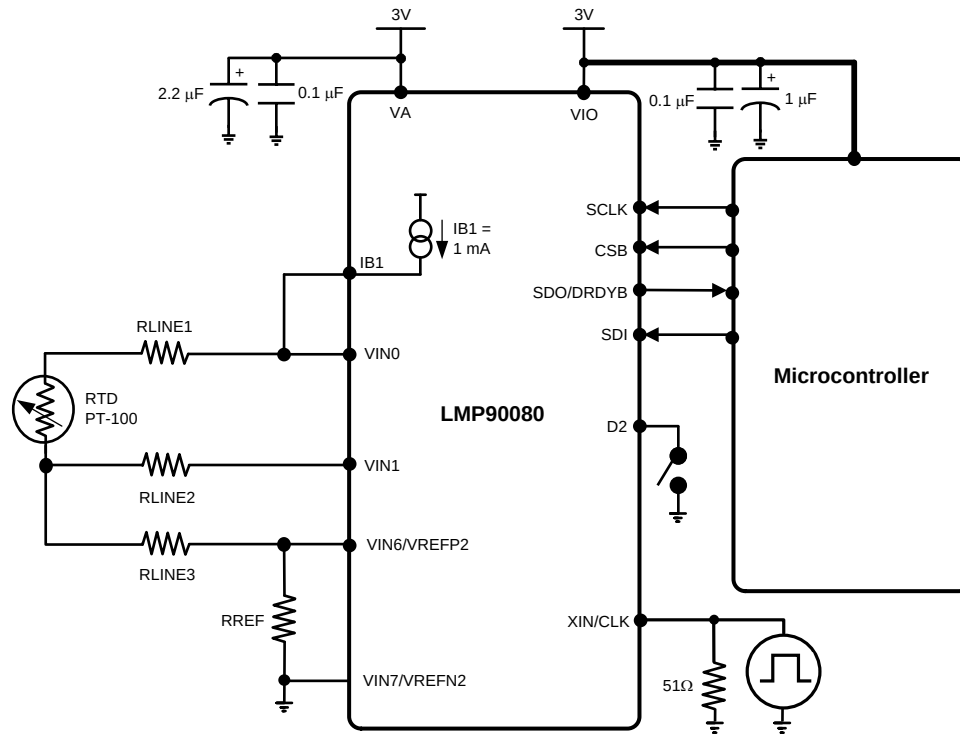
The PT-100 changes linearly from 100 Ohm at 0°C to 146.07 Ohm at 120°C. If desired, choose a suitable compensating resistor (RCOMP) so that VIN can be virtually 0V at any desirable temperature. For example, if RCOMP = 100 Ohm, then at 0°C, VIN = 0V and thus a higher gain can be used.

The advantage of this circuit is its ratiometric configuration, where  $VREF = (IB1 + IB2) \times (RREF)$ . Equation 17 shows that a ratiometric configuration eliminates IB1 and IB2 from the output equation, thus increasing the overall performance.

$$\begin{aligned} ADC\_DOUT &= \frac{VIN(Gain)}{2VREF} (2^n) \\ ADC\_DOUT &= \frac{[IB1(RTD - RCOMP)Gain]}{2(IB1+IB2)RREF} (2^n) \\ ADC\_DOUT &= \frac{[(RTD - RCOMP)Gain]}{2(2)RREF} (2^n) \end{aligned}$$

ADC\_DOUT Showing IB1 & IB2 Elimination

(17)



**Figure 66. Topology #2: 3-wire RTD Using 1 Current Source**

Figure 66 shows the second topology for a 3-wire RTD application. Topology #2 shows the same connection as topology #1, but without IB2. Although this topology eliminates a current source, it requires two channel measurements as shown in Equation 18.

$$\begin{aligned} \text{VIN0} &= \text{IB1} (\text{RLINE1} + \text{RTD} + \text{RLINE3} + \text{RREF}) \\ \text{VIN1} &= \text{IB1} (\text{RLINE3} + \text{RREF}) \\ \text{VIN6} &= \text{IB1} (\text{RREF}) \end{aligned}$$

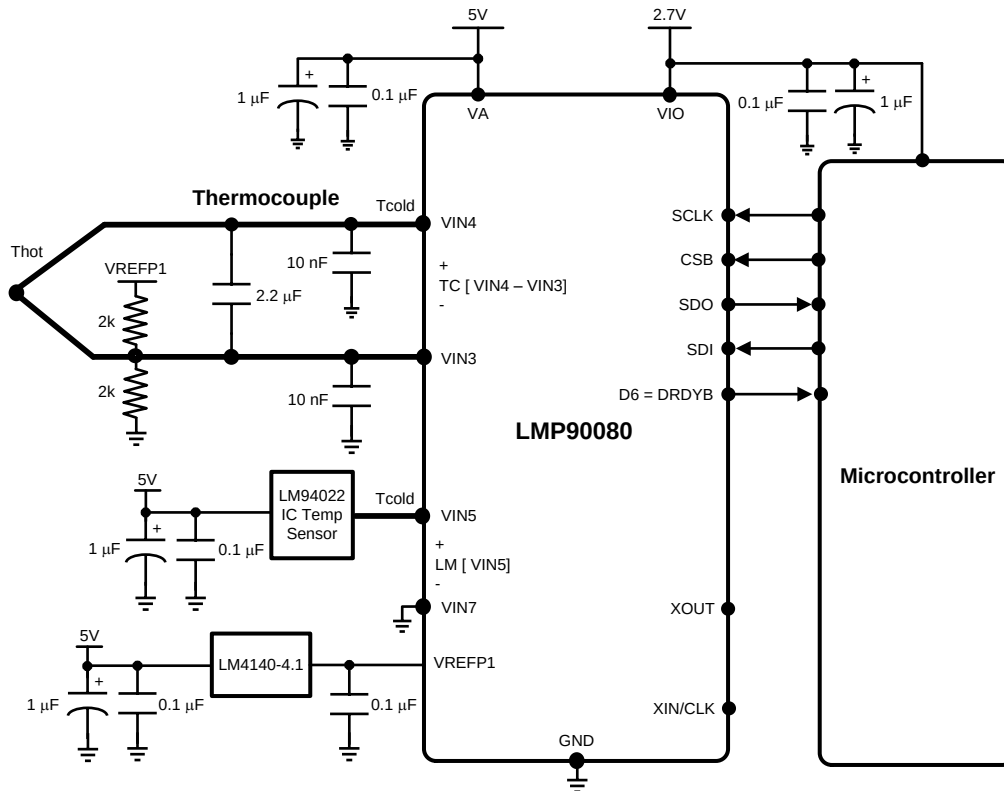
$$\begin{aligned} \text{CH0} &= \text{VIN0} - \text{VIN1} = \text{IB1} (\text{RLINE1} + \text{RTD}) \\ \text{CH1} &= \text{VIN1} - \text{VIN6} = \text{IB1} (\text{RLINE3}) \end{aligned}$$

$$\begin{aligned} \text{Assume } \text{RLINE1} &= \text{RLINE3, thus:} \\ \text{CH0} - \text{CH1} &= \text{IB1} (\text{RTD}) \end{aligned}$$

$$\text{VIN Equation for Topology \#2}$$

(18)

## Thermocouple and IC Analog Temperature



**Figure 67. Thermocouple with CJC**

The LMP90080-Q1 is also ideal for thermocouple temperature applications. Thermocouples have several advantages that make them popular in many industrial and medical applications. Compare to RTDs, thermistors, and IC sensors, thermocouples are the most rugged, least expensive, and can operate over the largest temperature range.

A thermocouple is a sensor whose junction generates a differential voltage,  $V_{IN}$ , that is relative to the temperature difference ( $T_{hot} - T_{cold}$ ).  $T_{hot}$  is also known as the measuring junction or “hot” junction, which is placed at the measured environment.  $T_{cold}$  is also known as the reference or “cold” junction, which is placed at the measuring system environment.

Because a thermocouple can only measure a temperature difference, it does not have the ability to measure absolute temperature. To determine the absolute temperature of the measured environment ( $T_{hot}$ ), a technique known as cold junction compensation (CJC) must be used.

In a CJC technique, the “cold” junction temperature,  $T_{cold}$ , is sensed by using an IC temperature sensor, such as the LM94022. The temperature sensor should be placed within close proximity of the reference junction and should have an isothermal connection to the board to minimize any potential temperature gradients.

Once  $T_{cold}$  is obtained, use a standard thermocouple look-up-table to find its equivalent voltage. Next, measure the differential thermocouple voltage and add the equivalent cold junction voltage. Lastly, convert the resulting voltage to temperature using a standard thermocouple look-up-table.

For example, assume  $T_{cold} = 20^{\circ}\text{C}$ . The equivalent voltage from a type K thermocouple look-up-table is 0.798 mV. Next, add the measured differential thermocouple voltage to the  $T_{cold}$  equivalent voltage. For example, if the thermocouple voltage is 4.096 mV, the total would be 0.798 mV + 4.096 mV = 4.894 mV. Referring to the type K thermocouple table gives a temperature of 119.37°C for 4.894 mV.

## Registers

1. If written to, RESERVED bits must be written to only 0 unless otherwise indicated.
2. Read back value of RESERVED bits and registers is unspecified and should be discarded.
3. Recommended values must be programmed and forbidden values must not be programmed where they are indicated in order to avoid unexpected results.
4. If written to, registers indicated as Reserved must have the indicated default value as shown below. Any other value can cause unexpected results.

**Table 5. Register Map**

| Register Name                          |                                | ADDR (URA & LRA) | Type    | Default |
|----------------------------------------|--------------------------------|------------------|---------|---------|
| RESETCN                                | Reset Control                  | 0x00             | WO      | -       |
| SPI_HANDSHAKECN                        | SPI Handshake Control          | 0x01             | R/W     | 0x00    |
| SPI_RESET                              | SPI Reset Control              | 0x02             | R/W     | 0x00    |
| SPI_STREAMCN                           | SPI Stream Control             | 0x03             | R/W     | 0x00    |
| Reserved                               | -                              | 0x04 - 0x07      | -       | 0x00    |
| PWRCN                                  | Power Mode Control and Status  | 0x08             | RO & WO | 0x00    |
| DATA_ONLY_1                            | Data Only Read Control 1       | 0x09             | R/W     | 0x1A    |
| DATA_ONLY_2                            | Data Only Read Control 2       | 0x0A             | R/W     | 0x02    |
| ADC_RESTART                            | ADC Restart Conversion         | 0x0B             | WO      | -       |
| Reserved                               | -                              | 0x0C - 0x0D      | -       | 0x00    |
| GPIO_DIRCN                             | GPIO Direction Control         | 0x0E             | R/W     | 0x00    |
| GPIO_DAT                               | GPIO Data                      | 0x0F             | RO & WO | -       |
| BGCALCN                                | Background Calibration Control | 0x10             | R/W     | 0x00    |
| SPI_DRDYBCN                            | SPI Data Ready Bar Control     | 0x11             | R/W     | 0x03    |
| ADC_AUXCN                              | ADC Auxiliary Control          | 0x12             | R/W     | 0x00    |
| SPI_CRC_CN                             | CRC Control                    | 0x13             | R/W     | 0x02    |
| SENDIAG_THLD                           | Sensor Diagnostic Threshold    | 0x14             | R/W     | 0x00    |
| Reserved                               | -                              | 0x15-0x16        | -       | 0x0000  |
| SCALCN                                 | System Calibration Control     | 0x17             | R/W     | 0x00    |
| ADC_DONE                               | ADC Data Available             | 0x18             | RO      | -       |
| SENDIAG_FLAGS                          | Sensor Diagnostic Flags        | 0x19             | RO      | -       |
| ADC_DOUT                               | Conversion Data 1 and 0        | 0x1A - 0x1B      | RO      | -       |
| Reserved                               | -                              | 0x1C             | -       | -       |
| SPI_CRC_DAT                            | CRC Data                       | 0x1D             | RO & WO | -       |
| <b>CHANNEL CONFIGURATION REGISTERS</b> |                                |                  |         |         |
| CH_STS                                 | Channel Status                 | 0x1E             | RO      | 0x00    |
| CH_SCAN                                | Channel Scan Mode              | 0x1F             | R/W     | 0x30    |
| CH0_INPUTCN                            | CH0 Input Control              | 0x20             | R/W     | 0x01    |
| CH0_CONFIG                             | CH0 Configuration              | 0x21             | R/W     | 0x70    |
| CH1_INPUTCN                            | CH1 Input Control              | 0x22             | R/W     | 0x13    |
| CH1_CONFIG                             | CH1 Configuration              | 0x23             | R/W     | 0x70    |
| CH2_INPUTCN                            | CH2 Input Control              | 0x24             | R/W     | 0x25    |
| CH2_CONFIG                             | CH2 Configuration              | 0x25             | R/W     | 0x70    |
| CH3_INPUTCN                            | CH3 Input Control              | 0x26             | R/W     | 0x37    |
| CH3_CONFIG                             | CH3 Configuration              | 0x27             | R/W     | 0x70    |
| CH4_INPUTCN                            | CH4 Input Control              | 0x28             | R/W     | 0x01    |
| CH4_CONFIG                             | CH4 Configuration              | 0x29             | R/W     | 0x70    |
| CH5_INPUTCN                            | CH5 Input Control              | 0x2A             | R/W     | 0x13    |
| CH5_CONFIG                             | CH5 Configuration              | 0x2B             | R/W     | 0x70    |
| CH6_INPUTCN                            | CH6 Input Control              | 0x2C             | R/W     | 0x25    |

**Table 5. Register Map (continued)**

| Register Name                       |                                             | ADDR (URA & LRA) | Type | Default |
|-------------------------------------|---------------------------------------------|------------------|------|---------|
| CH6_CONFIG                          | CH6 Configuration                           | 0x2D             | R/W  | 0x70    |
| Reserved                            | -                                           | 0x2E - 0x2F      | -    | 0x00    |
| <b>SYSTEM CALIBRATION REGISTERS</b> |                                             |                  |      |         |
| CH0_SCAL_OFFSET                     | CH0 System Calibration Offset Coefficients  | 0x30 - 0x31      | R/W  | 0x0000  |
| Reserved                            | -                                           | 0x32             | -    | 0x00    |
| CH0_SCAL_GAIN                       | CH0 System Calibration Gain Coefficients    | 0x33 - 0x34      | R/W  | 0x8000  |
| Reserved                            | -                                           | 0x35             | -    | 0x00    |
| CH0_SCAL_SCALING                    | CH0 System Calibration Scaling Coefficients | 0x36             | R/W  | 0x01    |
| CH0_SCAL_BITS_SELECTOR              | CH0 System Calibration Bit Selector         | 0x37             | R/W  | 0x00    |
| CH1_SCAL_OFFSET                     | CH1 System Calibration Offset Coefficients  | 0x38 - 0x39      | R/W  | 0x0000  |
| Reserved                            | -                                           | 0x3A             | -    | 0x00    |
| CH1_SCAL_GAIN                       | CH1 System Calibration Gain Coefficient     | 0x3B - 0x3C      | R/W  | 0x8000  |
| Reserved                            | -                                           | 0x3D             | -    | 0x00    |
| CH1_SCAL_SCALING                    | CH1 System Calibration Scaling Coefficients | 0x3E             | R/W  | 0x01    |
| CH1_SCAL_BITS_SELECTOR              | CH1 System Calibration Bit Selector         | 0x3F             | R/W  | 0x00    |
| CH2_SCAL_OFFSET                     | CH2 System Calibration Offset Coefficients  | 0x40 - 0x41      | R/W  | 0x0000  |
| Reserved                            | -                                           | 0x42             | -    | 0x00    |
| CH2_SCAL_GAIN                       | CH2 System Calibration Gain Coefficient     | 0x43 - 0x44      | R/W  | 0x8000  |
| Reserved                            | -                                           | 0x45             | -    | 0x00    |
| CH2_SCAL_SCALING                    | CH2 System Calibration Scaling Coefficients | 0x46             | R/W  | 0x01    |
| CH2_SCAL_BITS_SELECTOR              | CH2 System Calibration Bit Selector         | 0x47             | R/W  | 0x00    |
| CH3_SCAL_OFFSET                     | CH3 System Calibration Offset Coefficients  | 0x48 - 0x49      | R/W  | 0x0000  |
| Reserved                            | -                                           | 0x4A             | -    | 0x00    |
| CH3_SCAL_GAIN                       | CH3 System Calibration Gain Coefficient     | 0x4B - 0x4C      | R/W  | 0x8000  |
| Reserved                            | -                                           | 0x4D             | -    | 0x00    |
| CH3_SCAL_SCALING                    | CH3 System Calibration Scaling Coefficients | 0x4E             | R/W  | 0x01    |
| CH3_SCAL_BITS_SELECTOR              | CH3 System Calibration Bit Selector         | 0x4F             | R/W  | 0x00    |
| Reserved                            | -                                           | 0x50 - 0x7F      | -    | 0x00    |

**Power and Reset Registers****Table 6. RESETCN**

| Reset Control (Address 0x00) |                 |                                                                                                         |
|------------------------------|-----------------|---------------------------------------------------------------------------------------------------------|
| Bit                          | Bit Symbol      | Bit Description                                                                                         |
| [7:0]                        | REG_AND_CNV_RST | Register and Conversion Reset<br><b>0xC3:</b> Register and conversion reset<br><b>Others:</b> Neglected |

**Table 7. SPI\_RESET**

| SPI Reset Control (Address 0x02) |            |                                                                                                              |
|----------------------------------|------------|--------------------------------------------------------------------------------------------------------------|
| Bit                              | Bit Symbol | Bit Description                                                                                              |
| [0]                              | SPI_RST    | SPI Reset Enable<br><b>0x0 (default):</b> SPI Reset Disabled<br><b>0x1:</b> SPI Reset Enabled <sup>(1)</sup> |

- (1) Once written, the contents of this register are sticky. That is, the content of this register cannot be changed with subsequent write. However, a Register reset clears the register as well as the sticky status.



**Table 8. PWRCN**

| Power Mode Control and Status (Address 0x08) |            |                                                                                                                                                                                                                                                                                                                          |
|----------------------------------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                                          | Bit Symbol | Bit Description                                                                                                                                                                                                                                                                                                          |
| [7:2]                                        | Reserved   | -                                                                                                                                                                                                                                                                                                                        |
| [1:0]                                        | PWRCN      | <p>Power Control</p> <p>Write Only – power down mode control</p> <p><b>0x0:</b> Active Mode</p> <p><b>0x1:</b> Power-down Mode</p> <p><b>0x3:</b> Stand-by Mode</p> <p>Read Only – the present mode is:</p> <p><b>0x0 (default):</b> Active Mode</p> <p><b>0x1:</b> Power-down Mode</p> <p><b>0x3:</b> Stand-by Mode</p> |

## ADC Registers

**Table 9. ADC\_RESTART**

| ADC Restart Conversion (Address 0x0B) |            |                                                                |
|---------------------------------------|------------|----------------------------------------------------------------|
| Bit                                   | Bit Symbol | Bit Description                                                |
| [7:1]                                 | Reserved   | -                                                              |
| 0                                     | RESTART    | <p>Restart conversion</p> <p><b>1:</b> Restart conversion.</p> |

**Table 10. ADC\_AUXCN**

| ADC Auxiliary Control (Address 0x12) |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------------------------------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                                  | Bit Symbol   | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 7                                    | Reserved     | -                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 6                                    | RESET_SYSCAL | <p>The System Calibration registers (CHx_SCAL_OFFSET and CHx_SCAL_GAIN) are:</p> <p><b>0 (default):</b> preserved even when "REG_AND_CNV_RST" = 0xC3.</p> <p><b>1:</b> reset by setting "REG_AND_CNV_RST" = 0xC3.</p>                                                                                                                                                                                                                                                                                              |
| 5                                    | CLK_EXT_DET  | <p>External clock detection</p> <p><b>0 (default):</b> "External Clock Detection" is operational</p> <p><b>1:</b> "External-Clock Detection" is bypassed</p>                                                                                                                                                                                                                                                                                                                                                       |
| 4                                    | CLK_SEL      | <p>Clock select – only valid if CLK_EXT_DET = 1</p> <p><b>0 (default):</b> Selects internal clock</p> <p><b>1:</b> Selects external clock</p>                                                                                                                                                                                                                                                                                                                                                                      |
| [3:0]                                | RTD_CUR_SEL  | <p>Selects RTD Current as follows:</p> <p><b>0x0 (default):</b> 0 <math>\mu</math>A</p> <p><b>0x1:</b> 100 <math>\mu</math>A</p> <p><b>0x2:</b> 200 <math>\mu</math>A</p> <p><b>0x3:</b> 300 <math>\mu</math>A</p> <p><b>0x4:</b> 400 <math>\mu</math>A</p> <p><b>0x5:</b> 500 <math>\mu</math>A</p> <p><b>0x6:</b> 600 <math>\mu</math>A</p> <p><b>0x7:</b> 700 <math>\mu</math>A</p> <p><b>0x8:</b> 800 <math>\mu</math>A</p> <p><b>0x9:</b> 900 <math>\mu</math>A</p> <p><b>0xA:</b> 1000 <math>\mu</math>A</p> |

**Table 11. ADC\_DONE**

| ADC Data Available (Address 0x18) |            |                                                                                                                               |
|-----------------------------------|------------|-------------------------------------------------------------------------------------------------------------------------------|
| Bit                               | Bit Symbol | Bit Description                                                                                                               |
| [7:0]                             | DT_AVAIL_B | Data Available – indicates if new conversion data is available<br><b>0x00 – 0xFE:</b> Available<br><b>0xFF:</b> Not available |

**Table 12. ADC\_DOUT<sup>(1)</sup>**

| 16-bit Conversion Data (two's complement) (Address 0x1A - 0x1B) |           |                            |
|-----------------------------------------------------------------|-----------|----------------------------|
| Address                                                         | Name      | Register Description       |
| 0x1A                                                            | ADC_DOUTH | ADC Conversion Data [15:8] |
| 0x1B                                                            | ADC_DOUTL | ADC Conversion Data [7:0]  |
| 0x1C                                                            | Reserved  | Reserved                   |

(1) Repeat reads of these registers are allowed as long as such reads are spaced apart by at least 72  $\mu$ s.

## Channel Configuration Registers

**Table 13. CH\_STS**

| Channel Status (Address 0x1E) |                   |                                                                                                                                                                                                        |
|-------------------------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                           | Bit Symbol        | Bit Description                                                                                                                                                                                        |
| [7:2]                         | Reserved          | -                                                                                                                                                                                                      |
| 1                             | CH_SCAN_NRDY      | Channel Scan Not Ready – indicates if it is okay to program CH_SCAN<br>0: Update not pending, CH_SCAN register is okay to program<br>1: Update pending, CH_SCAN register is not ready to be programmed |
| 0                             | INV_OR_RPT_RD_STS | Invalid or Repeated Read Status<br>0: ADC_DOUT just read was valid and hitherto unread<br>1: ADC_DOUT just read was either invalid (not ready) or there was a repeated read.                           |

**Table 14. CH\_SCAN<sup>(1)</sup>**

| Channel Scan Mode (Address 0x1F) |             |                                                                                                                                                                                                                                                                                                             |
|----------------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                              | Bit Symbol  | Bit Description                                                                                                                                                                                                                                                                                             |
| [7:6]                            | CH_SCAN_SEL | Channel Scan Select<br><b>0x0 (default):</b> ScanMode0: Single-Channel Continuous Conversion<br><b>0x1:</b> ScanMode1: One or more channels Single Scan<br><b>0x2:</b> ScanMode2: One or more channels Continuous Scan<br><b>0x3:</b> ScanMode3: One or more channels Continuous Scan with Burnout Currents |
| [5:3]                            | LAST_CH     | Last channel for conversion<br><b>0x0:</b> CH0<br><b>0x1:</b> CH1<br><b>0x2:</b> CH2<br><b>0x3:</b> CH3<br><b>0x4:</b> CH4<br><b>0x5:</b> CH5<br><b>0x6 (default):</b> CH6 <sup>(2)</sup>                                                                                                                   |

(1) While writing to the CH\_SCAN register, if 0x7 is written to FIRST\_CH or LAST\_CH the write to the entire CH\_SCAN register is ignored.

(2) LAST\_CH cannot be smaller than FIRST\_CH. For example, if LAST\_CH = CH5, then FIRST\_CH cannot be CH6. If 0x7 is written it is ignored.

**Table 14. CH\_SCAN<sup>(1)</sup> (continued)**

| Channel Scan Mode (Address 0x1F) |            |                                                                                                                                                                                               |
|----------------------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                              | Bit Symbol | Bit Description                                                                                                                                                                               |
| [2:0]                            | FIRST_CH   | Starting channel for conversion<br><b>0x0 (default):</b> CH0<br><b>0x1:</b> CH1<br><b>0x2:</b> CH2<br><b>0x3:</b> CH3<br><b>0x4:</b> CH4<br><b>0x5:</b> CH5<br><b>0x6:</b> CH6 <sup>(3)</sup> |

(3) FIRST\_CH cannot be greater than LAST\_CH. For example, if FIRST\_CH = CH1, then LAST\_CH cannot be CH0. If 0x7 is written it is ignored.

**Table 15. CHx\_INPUTCN**

| Channel Input Control                                                                               |            |                                                                                                                                                                                                      |
|-----------------------------------------------------------------------------------------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Register Address (hex): CH0: 0x20, CH1: 0x22, CH2: 0x24, CH3: 0x26, CH4: 0x28, CH5: 0x2A, CH6: 0x2C |            |                                                                                                                                                                                                      |
| Bit                                                                                                 | Bit Symbol | Bit Description                                                                                                                                                                                      |
| 7                                                                                                   | BURNOUT_EN | Enable sensor diagnostic<br><b>0 (default):</b> Disable Sensor Diagnostics current injection for this Channel<br><b>1:</b> Enable Sensor Diagnostics current injection for this Channel              |
| 6                                                                                                   | VREF_SEL   | Select the reference<br><b>0 (Default):</b> Select VREFP1 and VREFN1<br><b>1:</b> Select VREFP2 and VREFN2                                                                                           |
| [5:3]                                                                                               | VINP       | Positive input select<br><b>0x0:</b> VIN0<br><b>0x1:</b> VIN1<br><b>0x2:</b> VIN2<br><b>0x3:</b> VIN3<br><b>0x4:</b> VIN4<br><b>0x5:</b> VIN5<br><b>0x6:</b> VIN6<br><b>0x7:</b> VIN7 <sup>(1)</sup> |
| [2:0]                                                                                               | VINN       | Negative input select<br><b>0x0:</b> VIN0<br><b>0x1:</b> VIN1<br><b>0x2:</b> VIN2<br><b>0x3:</b> VIN3<br><b>0x4:</b> VIN4<br><b>0x5:</b> VIN5<br><b>0x6:</b> VIN6<br><b>0x7:</b> VIN7 <sup>(1)</sup> |

(1) To see the default values for each channel, refer to the table below.

**Table 16. Default VINx for CH0-CH6**

|     | VINP | VINN |
|-----|------|------|
| CH0 | VIN0 | VIN1 |
| CH1 | VIN2 | VIN3 |
| CH2 | VIN4 | VIN5 |
| CH3 | VIN6 | VIN7 |
| CH4 | VIN0 | VIN1 |
| CH5 | VIN2 | VIN3 |
| CH6 | VIN4 | VIN5 |

**Table 17. CHx\_CONFIG**

| Channel Configuration                                                                               |            |                                                                                                                                                                                                                                                                                                                |
|-----------------------------------------------------------------------------------------------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Register Address (hex): CH0: 0x21, CH1: 0x23, CH2: 0x25, CH3: 0x27, CH4: 0x29, CH5: 0x2B, CH6: 0x2D |            |                                                                                                                                                                                                                                                                                                                |
| Bit                                                                                                 | Bit Symbol | Bit Description                                                                                                                                                                                                                                                                                                |
| 7                                                                                                   | Reserved   | -                                                                                                                                                                                                                                                                                                              |
| [6:4]                                                                                               | ODR_SEL    | ODR Select<br><b>0x0:</b> 13.42 / 8 = 1.6775 SPS<br><b>0x1:</b> 13.42 / 4 = 3.355 SPS<br><b>0x2:</b> 13.42 / 2 = 6.71 SPS<br><b>0x3:</b> 13.42 SPS<br><b>0x4:</b> 214.65 / 8 = 26.83125 SPS<br><b>0x5:</b> 214.65 / 4 = 53.6625 SPS<br><b>0x6:</b> 214.65 / 2 = 107.325 SPS<br><b>0x7(default):</b> 214.65 SPS |
| [3:1]                                                                                               | GAIN_SEL   | Gain Select<br><b>0x0 (default):</b> 1 (FGA OFF)<br><b>0x1:</b> 2 (FGA OFF)<br><b>0x2:</b> 4 (FGA OFF)<br><b>0x3:</b> 8 (FGA OFF)<br><b>0x4:</b> 16 (FGA ON)<br><b>0x5:</b> 32 (FGA ON)<br><b>0x6:</b> 64 (FGA ON)<br><b>0x7:</b> 128 (FGA ON)                                                                 |
| 0                                                                                                   | BUF_EN     | Enable/Disable the buffer<br><b>0 (default):</b> Include the buffer in the signal path<br><b>1:</b> Exclude the buffer from the signal path <sup>(1)</sup>                                                                                                                                                     |

(1) When gain  $\geq 16$ , the buffer is automatically included in the signal path irrespective of this bit.

## Calibration Registers

**Table 18. BGCALCN**

| Background Calibration Control (Address 0x10) |            |                                                                                                                                                                                                                                                                                                                                                     |
|-----------------------------------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                                           | Bit Symbol | Bit Description                                                                                                                                                                                                                                                                                                                                     |
| [7:2]                                         | Reserved   | -                                                                                                                                                                                                                                                                                                                                                   |
| [1:0]                                         | BGCALN     | Background calibration control – selects scheme for continuous background calibration.<br><b>0x0 (default):</b> BgcalMode0: Background Calibration OFF<br><b>0x1:</b> BgcalMode1: Offset Correction / Gain Estimation<br><b>0x2:</b> BgcalMode2: Offset Correction / Gain Correction<br><b>0x3:</b> BgcalMode3: Offset Estimation / Gain Estimation |

**Table 19. SCALCN**

| System Calibration Control (Address 0x17) |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------------------------------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                                       | Bit Symbol | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| [7:2]                                     | Reserved   | -                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| [1:0]                                     | SCALCN     | <p>System Calibration Control</p> <p>When written, set SCALCN to:</p> <p><b>0x0 (default):</b> Normal Mode</p> <p><b>0x1:</b> "System Calibration Offset Coefficient Determination" mode</p> <p><b>0x2:</b> "System Calibration Gain Coefficient Determination" mode</p> <p><b>0x3:</b> Reserved</p> <p>When read, this bit indicates the system calibration mode is in:</p> <p><b>0x0:</b> Normal Mode</p> <p><b>0x1:</b> "System Calibration Offset Coefficient Determination" mode</p> <p><b>0x2:</b> "System Calibration Gain Coefficient Determination" mode</p> <p><b>0x3:</b> Reserved<sup>(1)</sup></p> |

- (1) When read, this bit will indicate the current System Calibration status. Since this coefficient determination mode will only take 1 conversion cycle, reading this register will only return 0x00, unless this register is read within 1 conversion window.

**Table 20. CHx\_SCAL\_OFFSET**

| CH0-CH3 System Calibration Offset Registers (Two's-Complement) |      |      |      |                  |                                                   |
|----------------------------------------------------------------|------|------|------|------------------|---------------------------------------------------|
| ADDR                                                           |      |      |      | Name             | Description                                       |
| CH0                                                            | CH1  | CH2  | CH3  |                  |                                                   |
| 0x30                                                           | 0x38 | 0x40 | 0x48 | CHx_SCAL_OFFSETH | System Calibration Offset Coefficient Data [15:8] |
| 0x31                                                           | 0x39 | 0x41 | 0x49 | CHx_SCAL_OFFSETM | System Calibration Offset Coefficient Data [7:0]  |
| 0x32                                                           | 0x3A | 0x42 | 0x4A | Reserved         | -                                                 |

**Table 21. CHx\_SCAL\_GAIN**

| CH0-CH3 System Calibration Gain Registers (Fixed Point 1.23 Format) |      |      |      |                |                                                 |
|---------------------------------------------------------------------|------|------|------|----------------|-------------------------------------------------|
| ADDR                                                                |      |      |      | Name           | Description                                     |
| CH0                                                                 | CH1  | CH2  | CH3  |                |                                                 |
| 0x33                                                                | 0x3B | 0x43 | 0x4B | CHx_SCAL_GAINH | System Calibration Gain Coefficient Data [15:8] |
| 0x34                                                                | 0x3C | 0x44 | 0x4C | CHx_SCAL_GAINL | System Calibration Gain Coefficient Data [7:0]  |
| 0x35                                                                | 0x3D | 0x45 | 0x4D | Reserved       | -                                               |

**Table 22. CHx\_SCAL\_SCALING**

| CH0-CH3 System Calibration Scaling Coefficient Registers |      |      |      |                  |                                                   |
|----------------------------------------------------------|------|------|------|------------------|---------------------------------------------------|
| ADDR                                                     |      |      |      | Name             | Description                                       |
| CH0                                                      | CH1  | CH2  | CH3  |                  |                                                   |
| 0x36                                                     | 0x3E | 0x46 | 0x4E | CHx_SCAL_SCALING | System Calibration Scaling Coefficient Data [5:0] |

**Table 23. CHx\_SCAL\_BITS\_SELECTOR**

| CH0-CH3 System Calibration Bit Selector Registers |      |      |      |                        |                                             |
|---------------------------------------------------|------|------|------|------------------------|---------------------------------------------|
| ADDR                                              |      |      |      | Name                   | Description                                 |
| CH0                                               | CH1  | CH2  | CH3  |                        |                                             |
| 0x37                                              | 0x3F | 0x47 | 0x4F | CHx_SCAL_BITS_SELECTOR | System Calibration Bit Selection Data [2:0] |

## Sensor Diagnostic Registers

**Table 24. SENDIAG\_THLD**

| Sensor Diagnostic Threshold (Address 0x14) |              |                             |
|--------------------------------------------|--------------|-----------------------------|
| Address                                    | Name         | Register Description        |
| 0x14                                       | SENDIAG_THLD | Sensor Diagnostic threshold |

**Table 25. SENDIAG\_FLAGS**

| Sensor Diagnostic Flags (Address 0x19) |                 |                                                                                                                                                                                                                                                                                                                                                          |
|----------------------------------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                                    | Bit Symbol      | Bit Description                                                                                                                                                                                                                                                                                                                                          |
| 7                                      | SHORT_THLD_FLAG | Short Circuit Threshold Flag = 1 when the absolute value of VOUT is within the absolute threshold voltage set by the SENDIAG_THLD register.                                                                                                                                                                                                              |
| 6                                      | RAILS_FLAG      | Rails Flag = 1 when at least one of the inputs is near rail (VA or GND).                                                                                                                                                                                                                                                                                 |
| 5                                      | POR_AFT_LST_RD  | Power-on-reset after last read = 1 when there was a power-on-reset event since the last time the SENDIAG_FLAGS register was read.                                                                                                                                                                                                                        |
| [4:3]                                  | OFLO_FLAGS      | Overflow flags<br><b>0x0:</b> Normal operation<br><b>0x1:</b> The modulator was not overranged, but ADC_DOUT got clamped to 0x7f_ffff (positive fullscale) or 0x80_0000 (negative full scale)<br><b>0x2:</b> The modulator was over-ranged ( $VIN > 1.2 \cdot VREF/GAIN$ )<br><b>0x3:</b> The modulator was over-ranged ( $VIN < -1.2 \cdot VREF/GAIN$ ) |
| [2:0]                                  | SAMPLED_CH      | Channel Number – the sampled channel for ADC_DOUT and SENDIAG_FLAGS.                                                                                                                                                                                                                                                                                     |

## SPI Registers

**Table 26. SPI\_HANDSHAKECN**

| SPI Handshake Control (Address 0x01) |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                             |                                                                 |                   |
|--------------------------------------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------|-----------------------------------------------------------------|-------------------|
| Bit                                  | Bit Symbol       | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                             |                                                                 |                   |
| [7:4]                                | Reserved         | -                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                             |                                                                 |                   |
| [3:1]                                | SDO_DRDYB_DRIVER | SDO/DRDYB Driver – sets who is driving the SDO/DRYB pin                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                                             |                                                                 |                   |
|                                      |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Whenever CSB is Asserted and the Device is Reading ADC_DOUT | Whenever CSB is Asserted and the Device is Not Reading ADC_DOUT | CSB is Deasserted |
|                                      |                  | 0x0 (default)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | SDO is driving                                              | DRDYB is driving                                                | High-Z            |
|                                      |                  | 0x3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | SDO is driving                                              | DRDYB is driving                                                | DRDYB is driving  |
|                                      |                  | 0x4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | SDO is driving                                              | High-Z                                                          | High-Z            |
|                                      |                  | Others                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Forbidden                                                   |                                                                 |                   |
| 0                                    | SW_OFF_TRG       | Switch-off trigger - refers to the switching of the output drive from the slave to the master.<br><b>0 (default):</b> SDO will be high-Z after the last (16th, 24th, 32nd, etc) rising edge of SCLK. This option allows time for the slave to transfer control back to the master at the end of the frame.<br><b>1:</b> SDO's high-Z is postponed to the subsequent falling edge following the last (16th, 24th, 32nd, etc) rising edge of SCLK. This option provides additional hold time for the last bit, DB0, in non-streaming read transfers. |                                                             |                                                                 |                   |

**Table 27. SPI\_STREAMCN**

| SPI Streaming Control (Address 0x03) |            |                                                                                                 |
|--------------------------------------|------------|-------------------------------------------------------------------------------------------------|
| Bit                                  | Bit Symbol | Bit Description                                                                                 |
| 7                                    | STRM_TYPE  | Stream type<br><b>0 (default):</b> Normal Streaming mode<br><b>1:</b> Controlled Streaming mode |
| [6:0]                                | STRM_RANGE | Stream range – selects Range for Controlled Streaming mode<br><b>Default:</b> 0x00              |

**Table 28. DATA\_ONLY\_1**

| Data Only Read Control 1 (Address 0x09) |               |                                                                                                                                                                 |
|-----------------------------------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                                     | Bit Symbol    | Bit Description                                                                                                                                                 |
| 7                                       | Reserved      | -                                                                                                                                                               |
| [6:0]                                   | DATA_ONLY_ADR | Start address for the Data Only Read Transaction<br><b>Default:</b> 0x1A<br>Please refer to the description of DT_ONLY_SZ in <a href="#">Table 29</a> register. |

**Table 29. DATA\_ONLY\_2**

| Data Only Read Control 2 (Address 0x0A) |              |                                                                                                                                         |
|-----------------------------------------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Bit                                     | Bit Symbol   | Bit Description                                                                                                                         |
| [7:3]                                   | Reserved     | -                                                                                                                                       |
| [2:0]                                   | DATA_ONLY_SZ | Number of bytes to be read out in Data Only mode. A value of 0x0 means read one byte and 0x7 means read 8 bytes.<br><b>Default:</b> 0x2 |

**Table 30. SPI\_DRDYBCN**

| SPI Data Ready Bar Control (Address 0x11) |              |                                                                                                                                                                                                                                            |
|-------------------------------------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                                       | Bit Symbol   | Bit Description                                                                                                                                                                                                                            |
| 7                                         | SPI_DRDYB_D6 | Enable DRDYB on D6<br><b>0 (default):</b> D6 is a GPIO<br><b>1:</b> D6 = drdyb signal                                                                                                                                                      |
| 6                                         | Reserved     | -                                                                                                                                                                                                                                          |
| 5                                         | CRC_RST      | CRC Reset<br><b>0 (default):</b> Enable CRC reset on DRDYB deassertion<br><b>1:</b> Disbale CRC reset on DRDYB deassertion                                                                                                                 |
| 4                                         | Reserved     | -                                                                                                                                                                                                                                          |
| 3                                         | FGA_BGCAL    | Gain background calibration<br><b>0 (default):</b> Correct FGA gain error. This is useful only if the device is operating in BgcalMode2 and ScanMode2 or ScanMode3.<br><b>1:</b> Correct FGA gain error using the last known coefficients. |
| [2:0]                                     | Reserved     | Default - 0x3 (do not change this value)                                                                                                                                                                                                   |

**Table 31. SPI\_CRC\_CN**

| CRC Control (Address 0x13) |               |                                                                                                                                                                                          |
|----------------------------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                        | Bit Symbol    | Bit Description                                                                                                                                                                          |
| [7:5]                      | Reserved      | -                                                                                                                                                                                        |
| 4                          | EN_CRC        | Enable CRC<br><b>0 (default):</b> Disable CRC<br><b>1:</b> Enable CRC                                                                                                                    |
| 3                          | Reserved      | Default - 0x0 (do not change this value)                                                                                                                                                 |
| 2                          | DRDYB_AFT_CRC | DRDYB After CRC<br><b>0 (default):</b> DRDYB is deasserted (active high) after ADC_DOUTL is read.<br><b>1:</b> DRDYB is deasserted after SPI_CRC_DAT (which follows ADC_DOUTL), is read. |
| [1:0]                      | Reserved      | -                                                                                                                                                                                        |

**Table 32. SPI\_CRC\_DAT**

| CRC Data (Address 0x1D) |            |                                                                                                                                       |
|-------------------------|------------|---------------------------------------------------------------------------------------------------------------------------------------|
| Bit                     | Bit Symbol | Bit Description                                                                                                                       |
| [7:0]                   | CRC_DAT    | CRC Data<br>When written, this register reset CRC:<br><b>Any Value:</b> Reset CRC<br>When read, this register indicates the CRC data. |

**GPIO Registers****Table 33. GPIO\_DIRCN**

| GPIO Direction (Address 0x0E) |             |                                                                                                                                                                                                                                                                                                           |
|-------------------------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                           | Bit Symbol  | Bit Description                                                                                                                                                                                                                                                                                           |
| 7                             | Reserved    | -                                                                                                                                                                                                                                                                                                         |
| x                             | GPIO_DIRCNx | GPIO direction control – these bits are used to control the direction of each General Purpose Input/Outputs (GPIO) pins D0 - D6.<br><b>0 (default):</b> Dx is an Input<br><b>1:</b> Dx is an Output<br>where $0 \leq x \leq 6$<br>For example, writing a 1 to bit 6 means D6 is an Output. <sup>(1)</sup> |

(1) If D6 is used for DRDYB, then it cannot be used for GPIO.

**Table 34. GPIO\_DAT**

| GPIO Data (Address 0x0F) |            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                      | Bit Symbol | Bit Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 7                        | Reserved   | -                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| x                        | Dx         | Write Only - when GPIO_DIRCNx = 0<br>0: Dx is LO<br>1: Dx is HI<br>Read Only - when GPIO_DIRCNx = 1<br>0: Dx driven LO<br>1: Dx driven HI<br>where $0 \leq x \leq 6$<br><br>For example, writing a 0 to bit 4 means D4 is LO.<br>It is okay to Read the GPIOs that are configured as outputs and write to GPIOs that are configured as inputs. Reading the GPIOs that are outputs would return the current value on those GPIOs, and writing to the GPIOs that are inputs are neglected. |



## REVISION HISTORY

| Changes from Revision (May 2013) to Revision A                                                                                                                                                               | Page                                     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|
| <ul style="list-style-type: none"> <li>Deleted CH_STS and ADC_DOUTM from the sentence: Compute the CRC externally... ..</li> <li>Added sentence to the end of the RESET and RESTART section .....</li> </ul> | <a href="#">37</a><br><a href="#">38</a> |

## PACKAGING INFORMATION

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LMP90080QMH/NOPB</a>  | Active        | Production           | HTSSOP (PWP)   28 | 48   TUBE             | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 150   | LMP90080Q<br>MH     |
| LMP90080QMH/NOPB.A                | Active        | Production           | HTSSOP (PWP)   28 | 48   TUBE             | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 150   | LMP90080Q<br>MH     |
| <a href="#">LMP90080QMHE/NOPB</a> | Active        | Production           | HTSSOP (PWP)   28 | 250   SMALL T&R       | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 150   | LMP90080Q<br>MH     |
| LMP90080QMHE/NOPB.A               | Active        | Production           | HTSSOP (PWP)   28 | 250   SMALL T&R       | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 150   | LMP90080Q<br>MH     |
| <a href="#">LMP90080QMHX/NOPB</a> | Active        | Production           | HTSSOP (PWP)   28 | 2500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 150   | LMP90080Q<br>MH     |
| LMP90080QMHX/NOPB.A               | Active        | Production           | HTSSOP (PWP)   28 | 2500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 150   | LMP90080Q<br>MH     |
| LMP90080QMHX/NOPB.B               | Active        | Production           | HTSSOP (PWP)   28 | 2500   LARGE T&R      | -           | Call TI                              | Call TI                           | -40 to 150   |                     |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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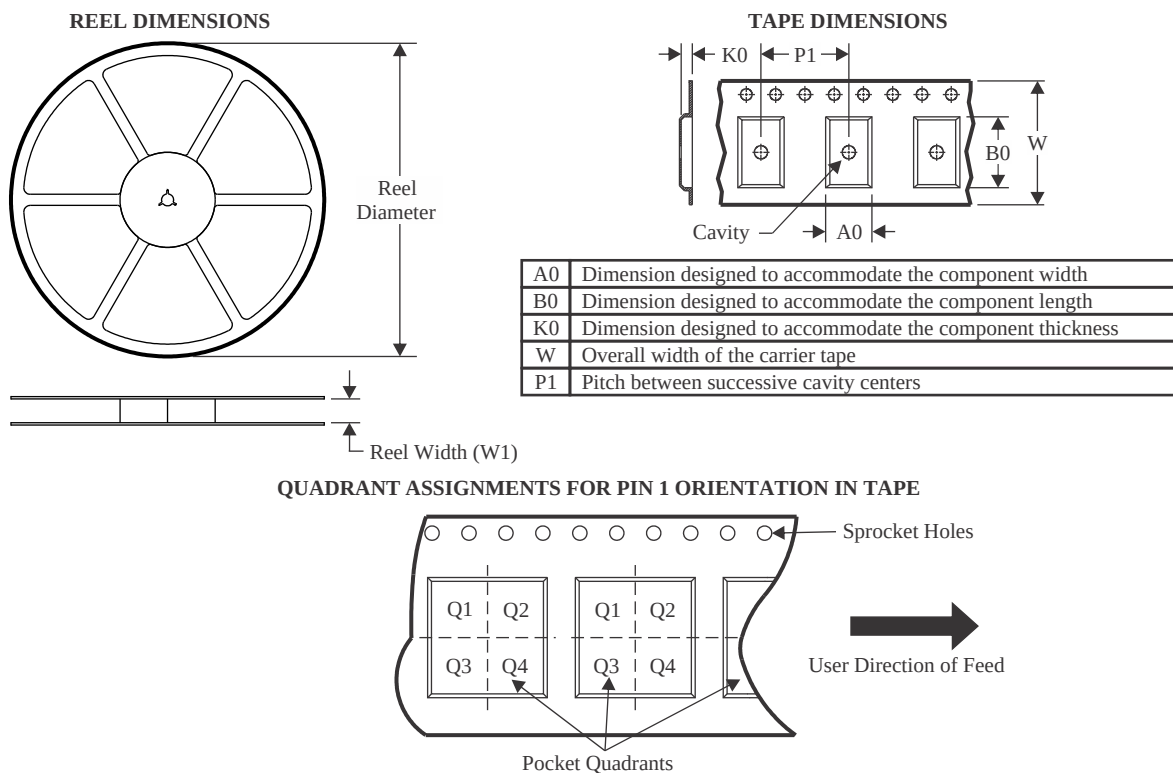
**OTHER QUALIFIED VERSIONS OF LMP90080-Q1 :**

- Catalog : [LMP90080](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

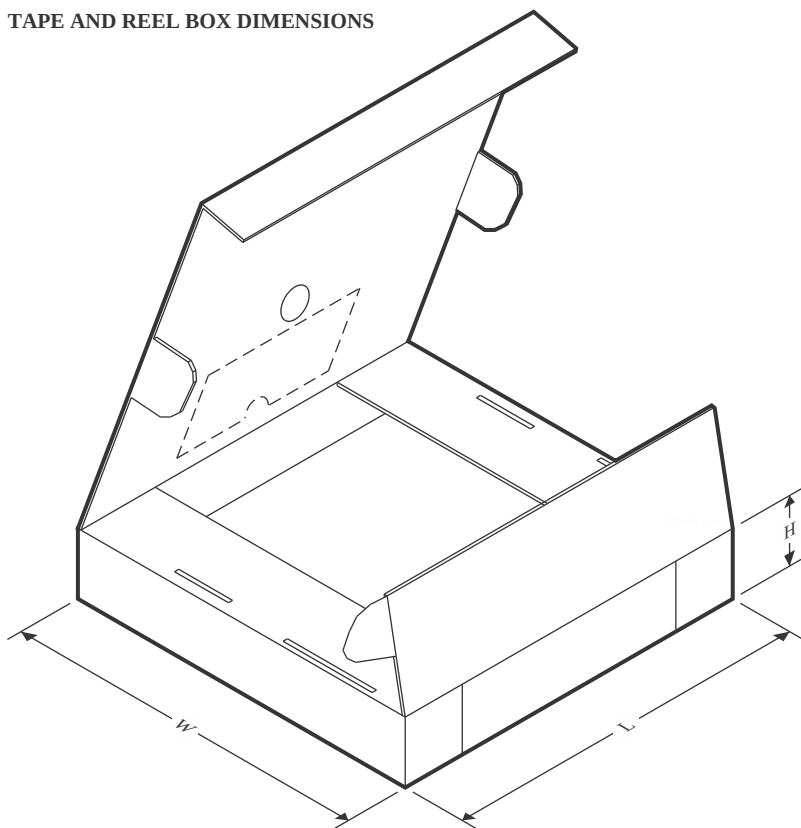
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMP90080QMHE/NOPB | HTSSOP       | PWP             | 28   | 250  | 178.0              | 16.4               | 6.95    | 10.0    | 1.7     | 8.0     | 16.0   | Q1            |
| LMP90080QMHX/NOPB | HTSSOP       | PWP             | 28   | 2500 | 330.0              | 16.4               | 6.95    | 10.0    | 1.7     | 8.0     | 16.0   | Q1            |

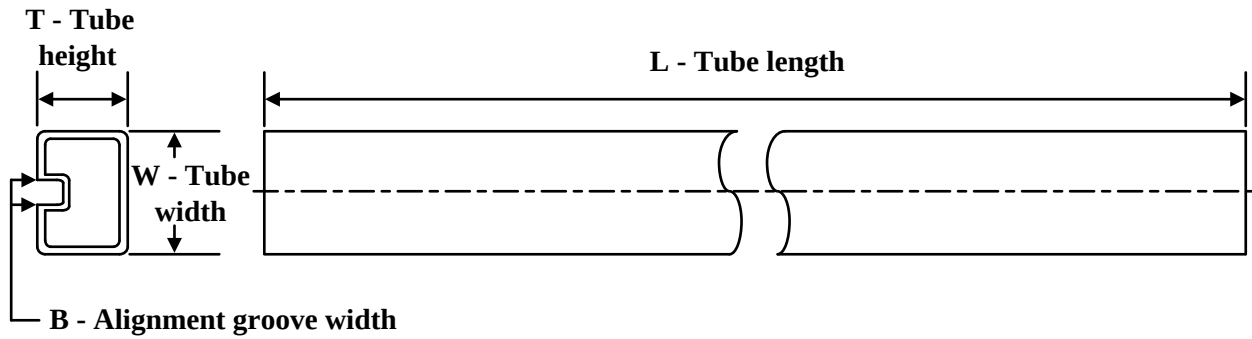
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

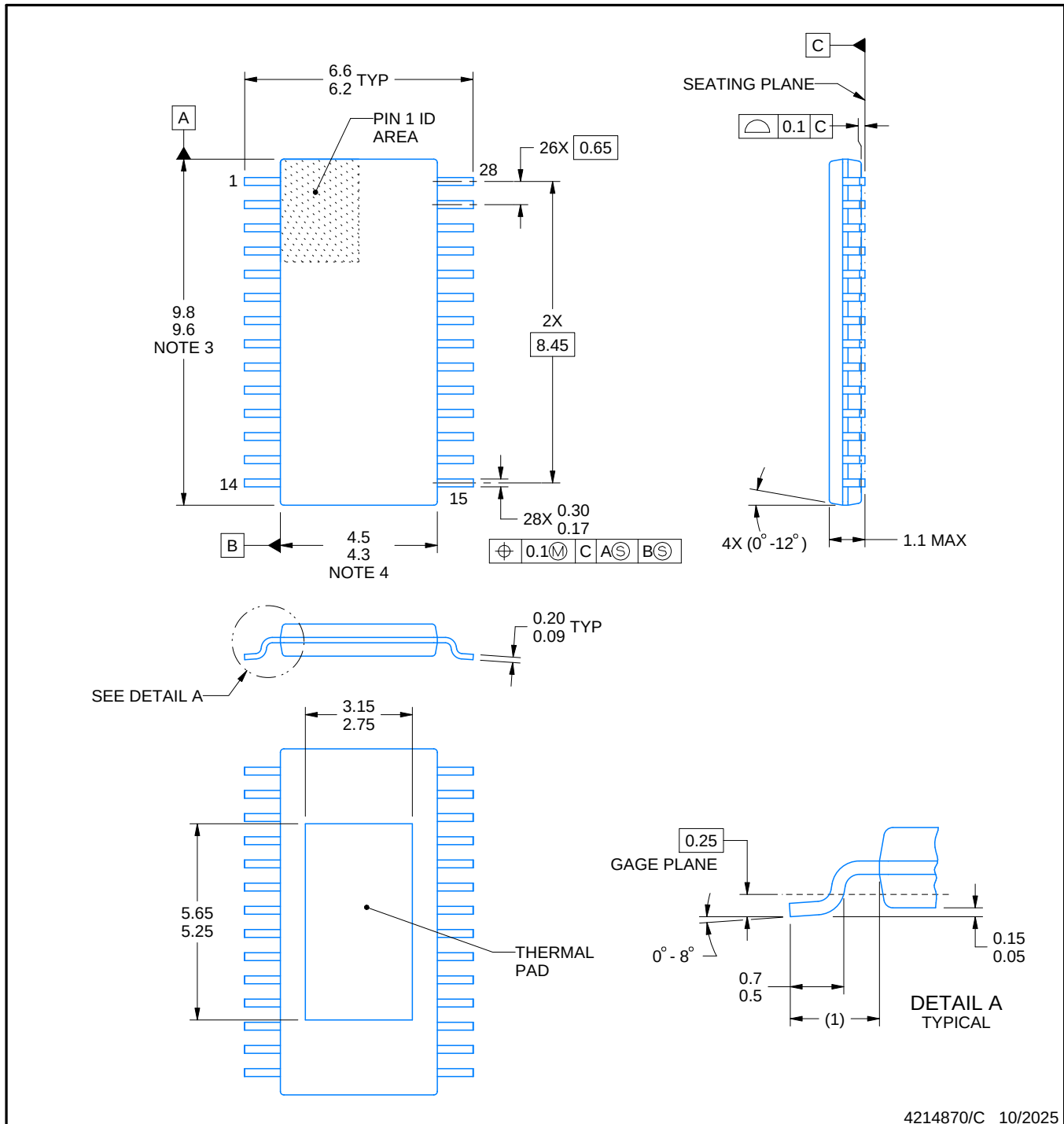
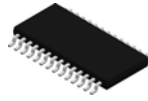
| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMP90080QMHE/NOPB | HTSSOP       | PWP             | 28   | 250  | 208.0       | 191.0      | 35.0        |
| LMP90080QMHX/NOPB | HTSSOP       | PWP             | 28   | 2500 | 356.0       | 356.0      | 36.0        |

## TUBE



\*All dimensions are nominal

| Device             | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LMP90080QMH/NOPB   | PWP          | HTSSOP       | 28   | 48  | 495    | 8      | 2514.6 | 4.06   |
| LMP90080QMH/NOPB.A | PWP          | HTSSOP       | 28   | 48  | 495    | 8      | 2514.6 | 4.06   |



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## NOTES:

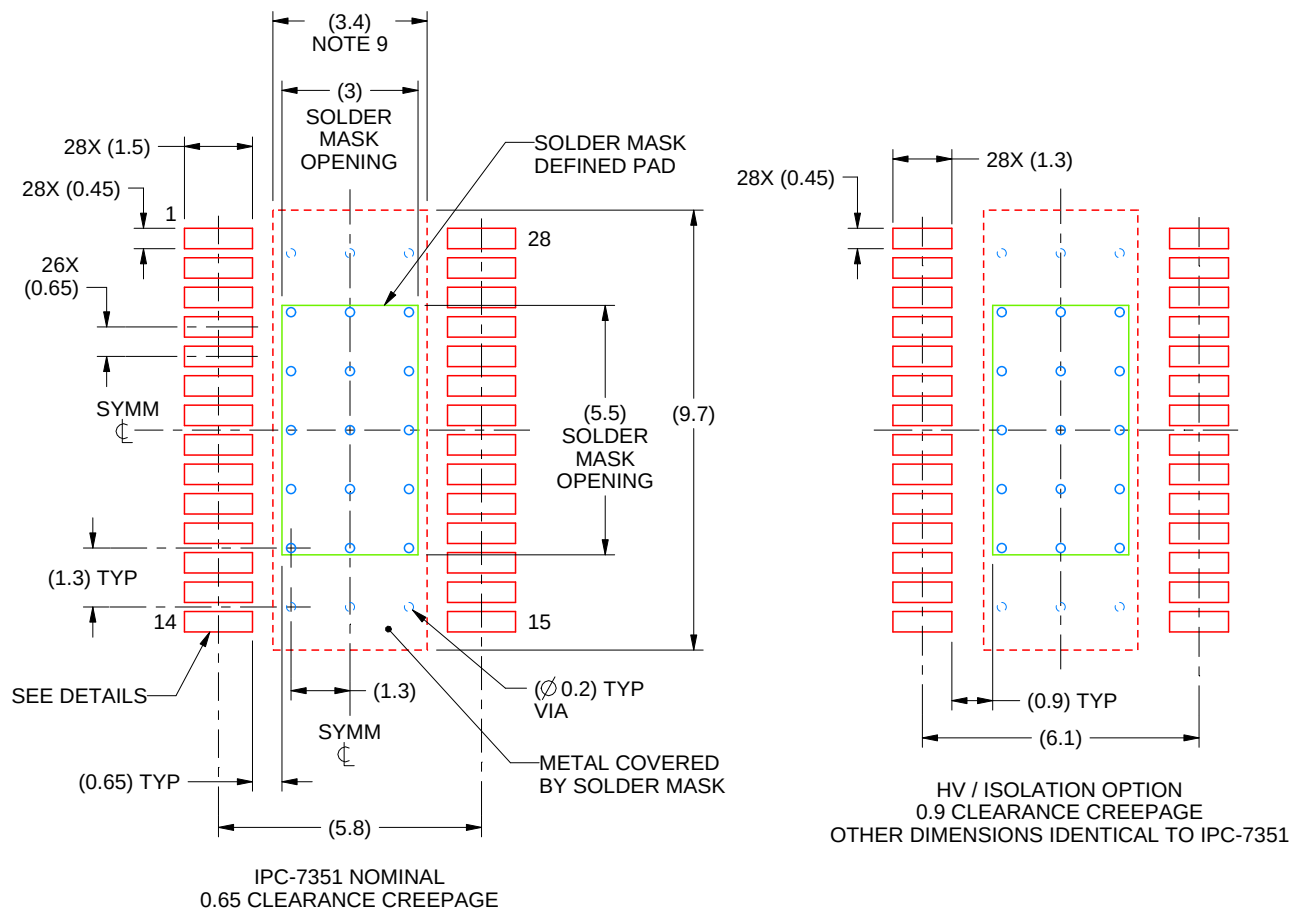
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.

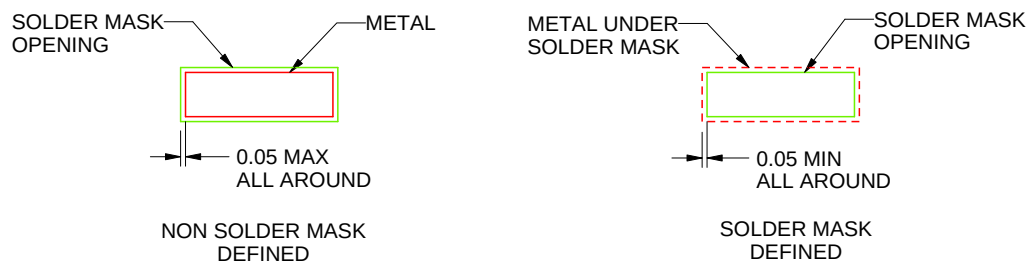
**PWP0028A**

## PowerPAD™ - 1.1 mm max height

## PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.

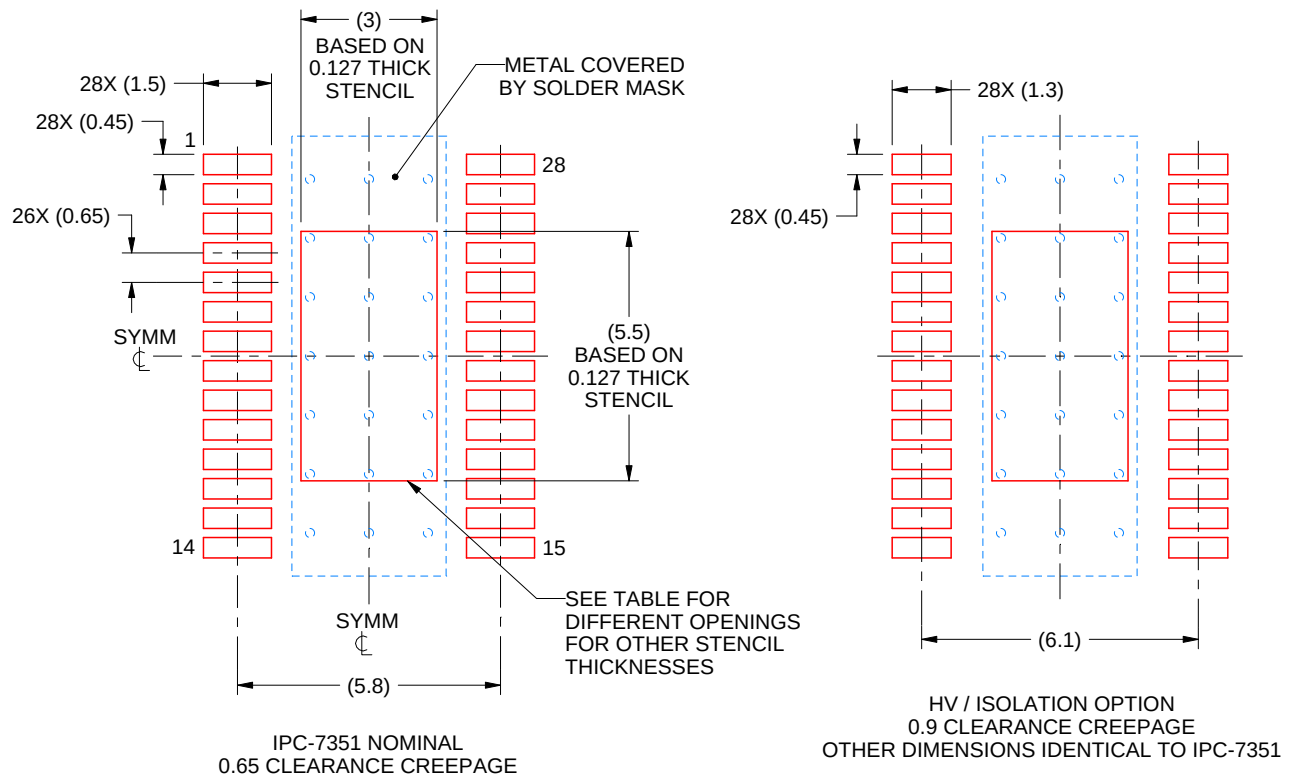


# EXAMPLE STENCIL DESIGN

PWP0028A

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE AREA  
SCALE:6X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 3.55 X 6.37            |
| 0.127             | 3.0 X 5.5 (SHOWN)      |
| 0.152             | 2.88 X 5.16            |
| 0.178             | 2.66 X 4.77            |

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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