88 MHz, Precision, Low Noise, 1.8V CMOS Input, Decompensated Operational Amplifier

Check for Samples: LMP7717, LMP7718

FEATURES

- **(Typical 5V Supply, Unless Otherwise Noted)**
- **Input Offset Voltage: ±150 µV (max)**
- **Input Referred Voltage Noise: 5.8 nV/√Hz**
- **Input Bias Current: 100 fA**
- **Gain Bandwidth Product: 88 MHz**
- **Supply Voltage Range: 1.8V to 5.5V**
- **Supply Current Per Channel**
  - **LMP7717: 1.15 mA**
  - **LMP7718: 1.30 mA**
- **Rail-to-Rail Output Swing**
  - **@ 10 kΩ Load: 25 mV from Rail**
  - **@ 2 kΩ Load: 45 mV from Rail**
- **Ensured 2.5V and 5.0V Performance**
- **Total Harmonic Distortion: 0.04% @1 kHz, 600Ω**
- **Temperature Range: −40°C to 125°C**

APPLICATIONS

- **ADC Interface**
- **Photodiode Amplifiers**
- **Active Filters and Buffers**
- **Low Noise Signal Processing**
- **Medical Instrumentation**
- **Sensor Interface Applications**

DESCRIPTION

The LMP7717 (single) and the LMP7718 (dual) low noise, CMOS input operational amplifiers offer a low input voltage noise density of 5.8 nV/√Hz while consuming only 1.15 mA (LMP7717) of quiescent current. The LMP7717/LMP7718 are stable at a gain of 10 and have a gain bandwidth (GBW) product of 88 MHz. The LMP7717/LMP7718 have a supply voltage range of 1.8V to 5.5V and can operate from a single supply. The LMP7717/LMP7718 each feature a rail-to-rail output stage. Both amplifiers are part of the LMP™ precision amplifier family and are ideal for a variety of instrumentation applications.

The LMP7717 family provides optimal performance in low voltage and low noise systems. A CMOS input stage, with typical input bias currents in the range of a few femto-Amperes, and an input common mode voltage range, which includes ground, make the LMP7717/LMP7718 ideal for low power sensor applications where high speeds are needed.

The LMP7717/LMP7718 are manufactured using TI's advanced VIP50 process. The LMP7717 is offered in either a 5-Pin SOT-23 or an 8-Pin SOIC package. The LMP7718 is offered in either the 8-Pin SOIC or the 8-Pin VSSOP.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Typical Application

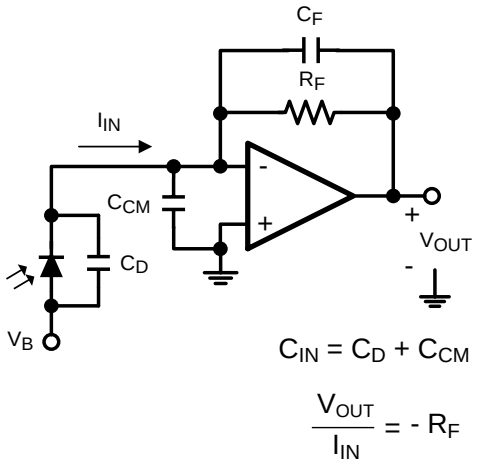


Figure 1. Photodiode Transimpedance Amplifier

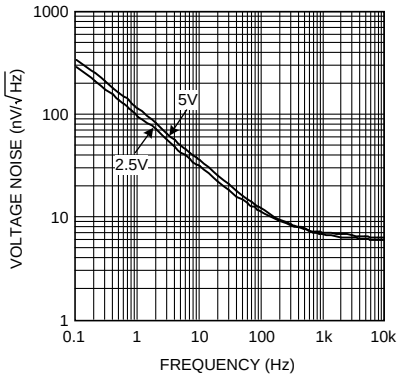


Figure 2. Input Referred Voltage Noise vs. Frequency

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)(2)

ESD Tolerance (3)	
Human Body Model	2000V
Machine Model	200V
Charge-Device Model	1000V
V_{IN} Differential	±0.3V
Supply Voltage ($V^+ - V^-$)	6.0V
Input/Output Pin Voltage	V^+ +0.3V, V^- −0.3V
Storage Temperature Range	−65°C to 150°C
Junction Temperature(4)	+150°C
For soldering specifications: see product folder at www.ti.com/ and http://www.ti.com/lit/SNOA549	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see 5V Electrical Characteristics().

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings(1)

Temperature Range(2)	−40°C to 125°C
Supply Voltage ($V^+ - V^-$) −40°C ≤ T_A ≤ 125°C	2.0V to 5.5V
0°C ≤ T_A ≤ 125°C	1.8V to 5.5V
Package Thermal Resistance (θ_{JA}(2))	
5-Pin SOT-23	180°C/W
8-Pin SOIC	190°C/W
8-Pin VSSOP	236°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see 5V Electrical Characteristics().

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

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2.5V Electrical Characteristics[1]

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 2.5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min[2]	Typ[3]	Max[2]	Units
V_{OS}	Input Offset Voltage				±20	±180 **±480**	µV
TC V_{OS}	Input Offset Voltage Temperature Drift[4] [5]	LMP7717			−1.0	±4	µV/°C
		LMP7718			−1.8		
I_B	Input Bias Current	V_{CM} = 1.0V See [6] and [5]	−40°C ≤ T_A ≤ 85°C		0.05	1 **25**	pA
			−40°C ≤ T_A ≤ 125°C		0.05	1 **100**	
I_{OS}	Input Offset Current	V_{CM} = 1.0V See[5]			.006	0.5 **50**	pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.4V		83 **80**	94		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		85 **80**	100		dB
		1.8V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		85	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 60 dB CMRR ≥ 55 dB		−0.3 **−0.3**		1.5 **1.5**	V
A_{VOL}	Open Loop Voltage Gain	V_{OUT} = 0.15V to 2.2V, R_L = 2 kΩ to $V^+/2$	LMP7717	88 **82**	98		dB
			LMP7718	84 **80**	92		
		V_{OUT} = 0.15V to 2.2V, R_L = 10 kΩ to $V^+/2$	LMP7717	92 **88**	110		
			LMP7718	90 **86**	95		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to $V^+/2$			25	70 **77**	mV from either rail
		R_L = 10 kΩ to $V^+/2$			20	60 **66**	
	Output Voltage Swing Low	R_L = 2 kΩ to $V^+/2$			30	70 **73**	
		R_L = 10 kΩ to $V^+/2$			15	60 **62**	
I_{OUT}	Output Current	Sourcing to V^- V_{IN} = 200 mV See[7]		36 **30**	47		mA
		Sinking to V^+ V_{IN} = –200 mV See[7]		7.5 **5**	15		
I_S	Supply Current per Amplifier	LMP7717			0.95	1.30 **1.65**	mA
		LMP7718 per channel			1.1	1.5 **1.85**	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Offset voltage average drift is determined by dividing the change in V_{OS} by temperature change.
(5) Parameter is specified by design and/or characterization and is not test in production.
(6) Positive current corresponds to current flowing into the device.
(7) The short circuit test is a momentary test, the short circuit duration is 1.5 ms.

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2.5V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 2.5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
SR	Slew Rate	A_V = +10, Rising (10% to 90%)		32		V/µs
		A_V = +10, Falling (90% to 10%)		24		
GBW	Gain Bandwidth	A_V = +10, R_L = 10 kΩ		88		MHz
e_n	Input Referred Voltage Noise Density	f = 1 kHz		6.2		nV/√Hz
i_n	Input Referred Current Noise Density	f = 1 kHz		0.01		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 600Ω		0.01		%

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5V Electrical Characteristics[1]

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min[2]	Typ[3]	Max[2]	Units
V_{OS}	Input Offset Voltage				±10	±150 **±450**	µV
TC V_{OS}	Input Offset Voltage Temperature Drift[4] [5]	LMP7717			−1.0	±4	µV/°C
		LMP7718			−1.8		
I_B	Input Bias Current	V_{CM} = 2.0V See [6]and [5]	−40°C ≤ T_A ≤ 85°C		0.1	1 **25**	pA
			−40°C ≤ T_A ≤ 125°C		0.1	1 **100**	
I_{OS}	Input Offset Current	V_{CM} = 2.0V See[5]			.01	0.5 **50**	pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.7V		85 **80**	100		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		85 **80**	100		dB
		1.8V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		85	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 60 dB CMRR ≥ 55 dB		−0.3 **−0.3**		4 **4**	V
A_{VOL}	Open Loop Voltage Gain	V_{OUT} = 0.3V to 4.7V, R_L = 2 kΩ to $V^+/2$	LMP7717	88 **82**	107		dB
			LMP7718	84 **80**	90		
		V_{OUT} = 0.3V to 4.7V, R_L = 10 kΩ to $V^+/2$	LMP7717	92 **88**	110		
			LMP7718	90 **86**	95		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to $V^+/2$	LMP7717		35	70 **77**	mV from either rail
			LMP7718		45	80 **83**	
		R_L = 10 kΩ to $V^+/2$			25	60 **66**	
	Output Voltage Swing Low	R_L = 2 kΩ to $V^+/2$	LMP7717		42	70 **73**	
			LMP7718		45	80 **83**	
		R_L = 10 kΩ to $V^+/2$			25	60 **66**	
I_{OUT}	Output Short Circuit Current	Sourcing to V^- V_{IN} = 200 mV See[7]		46 **38**	60		mA
		Sinking to V^+ V_{IN} = –200 mV See[7]		10.5 **6.5**	21		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) Offset voltage average drift is determined by dividing the change in V_{OS} by temperature change.
(5) Parameter is specified by design and/or characterization and is not test in production.
(6) Positive current corresponds to current flowing into the device.
(7) The short circuit test is a momentary test, the short circuit duration is 1.5 ms.

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5V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
I_S	Supply Current per Amplifier	LMP7717		1.15	1.40 **1.75**	mA
		LMP7718 per channel		1.30	1.70 **2.05**	
SR	Slew Rate	A_V = +10, Rising (10% to 90%)		35		V/µs
		A_V = +10, Falling (90% to 10%)		28		
GBW	Gain Bandwidth	A_V = +10, R_L = 10 kΩ		88		MHz
e_n	Input Referred Voltage Noise Density	f = 1 kHz		5.8		nV/√Hz
i_n	Input Referred Current Noise Density	f = 1 kHz		0.01		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 600Ω		0.01		%

CONNECTION DIAGRAMS

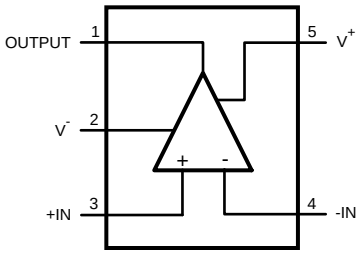


Figure 3. 5-Pin SOT-23 (LMP7717)
Top View

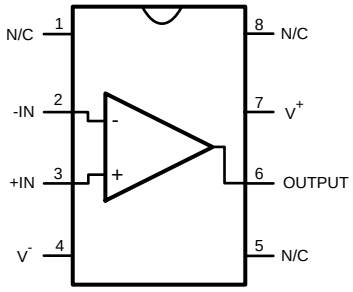


Figure 4. 8-Pin SOIC (LMP7717)
Top View

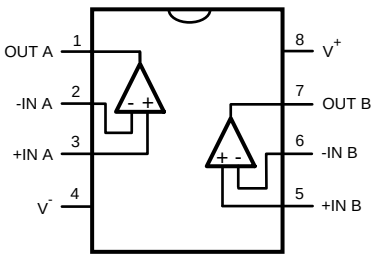


Figure 5. 8-Pin SOIC/VSSOP (LMP7718)

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = 5V, $V_S = V^+ - V^-$, $V_{CM} = V_S/2$.

TCV_{OS} Distribution (LMP7717)

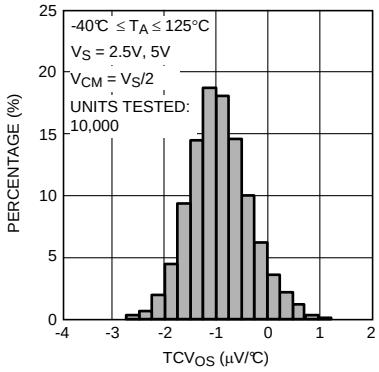


Figure 6.

Offset Voltage Distribution

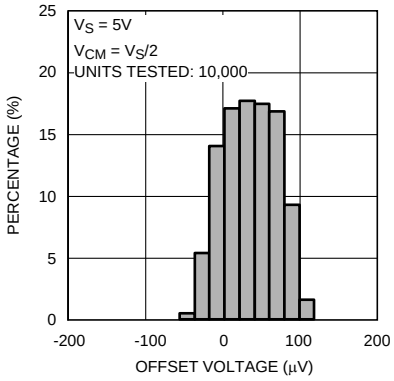


Figure 7.

TCV_{OS} Distribution (LMP7717)

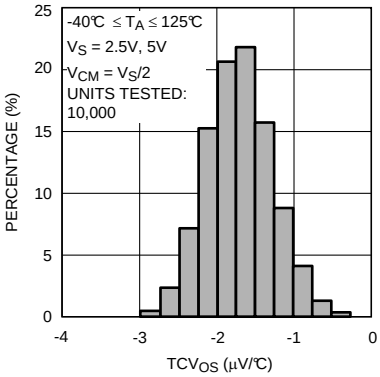


Figure 8.

Offset Voltage Distribution

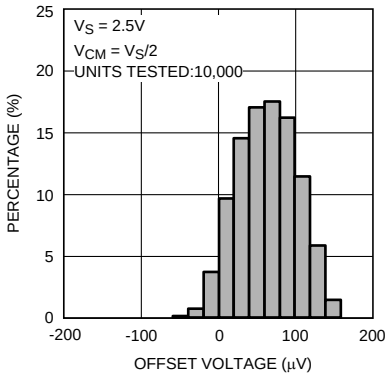


Figure 9.

Supply Current vs. Supply Voltage (LMP7717)

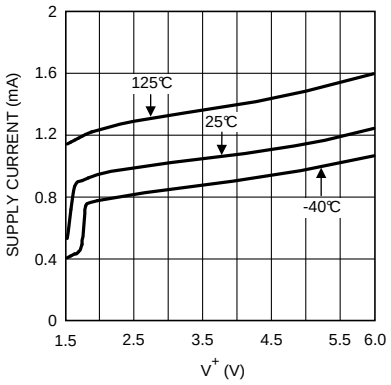


Figure 10.

Offset Voltage vs. V_{CM}

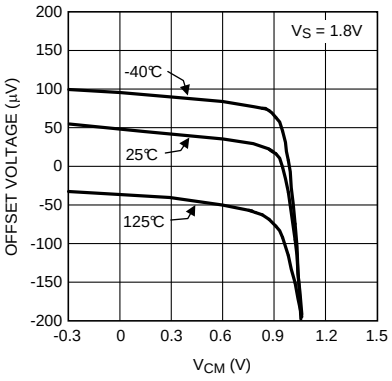


Figure 11.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = 5V, $V_S = V^+ - V^-$, $V_{CM} = V_S/2$.

Offset Voltage vs. V_{CM}

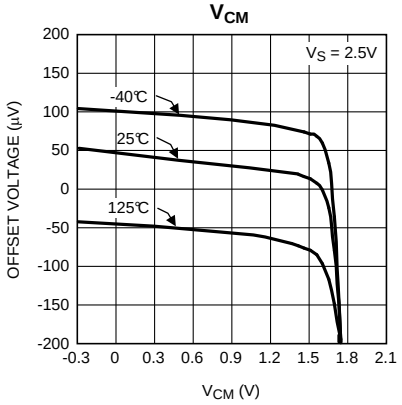


Figure 12.

Offset Voltage vs. V_{CM}

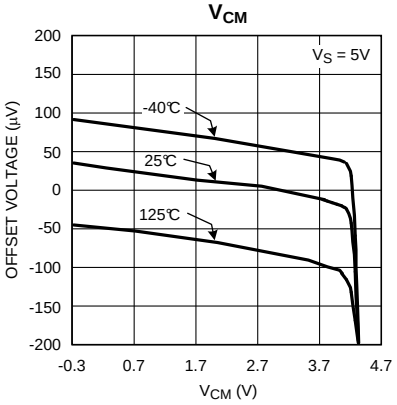


Figure 13.

Offset Voltage vs. Temperature

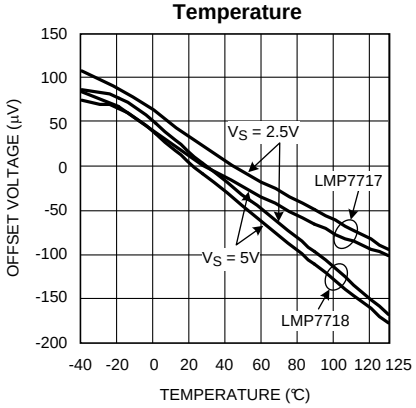


Figure 14.

Slew Rate vs. Supply Voltage

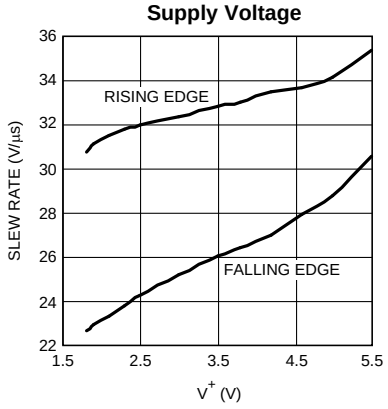


Figure 15.

Input Bias Current Over Temperature

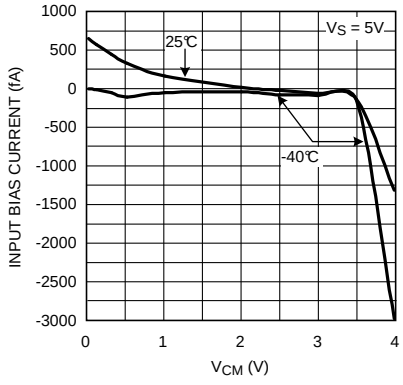


Figure 16.

Input Bias Current vs. V_{CM}

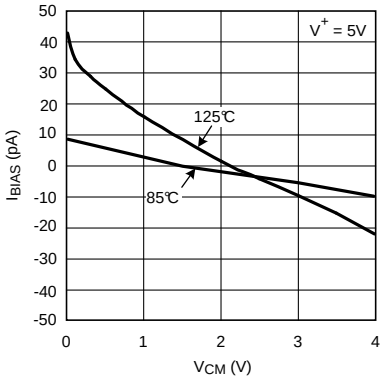


Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = 5V, $V_S = V^+ - V^-$, $V_{CM} = V_S/2$.

Offset Voltage vs. Supply Voltage

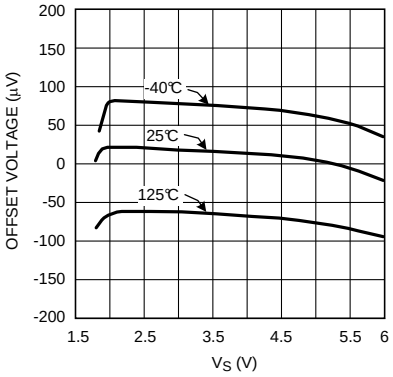


Figure 18.

Sourcing Current vs. Supply Voltage

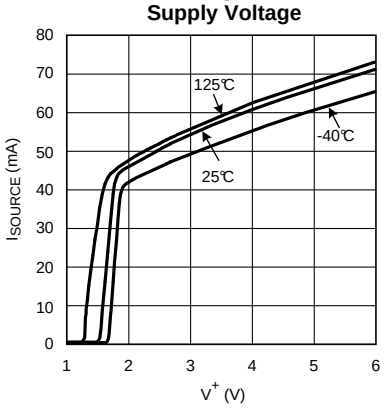


Figure 19.

Sinking Current vs. Supply Voltage

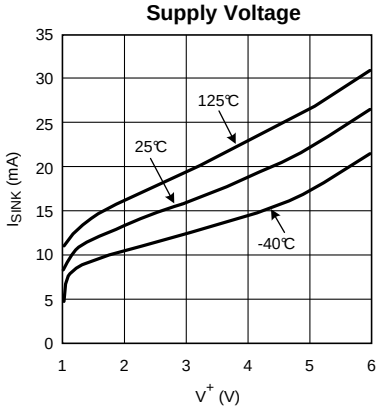


Figure 20.

Sourcing Current vs. Output Voltage

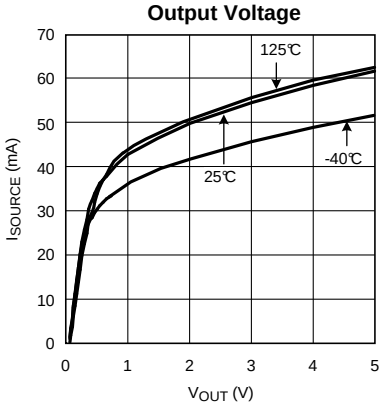


Figure 21.

Sinking Current vs. Output Voltage

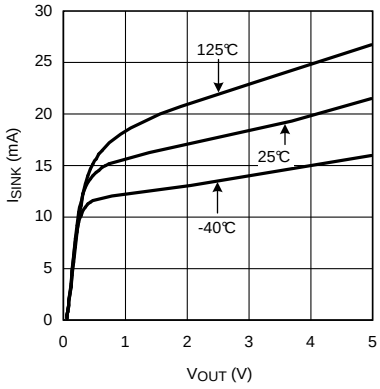


Figure 22.

Positive Output Swing vs. Supply Voltage

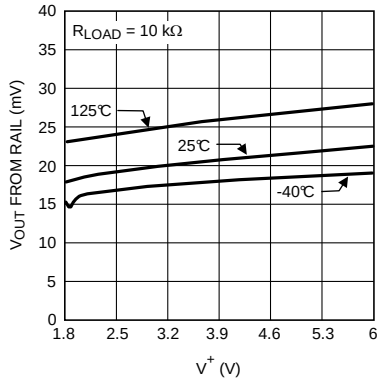


Figure 23.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = 5V, $V_S = V^+ - V^-$, $V_{CM} = V_S/2$.

Negative Output Swing vs. Supply Voltage

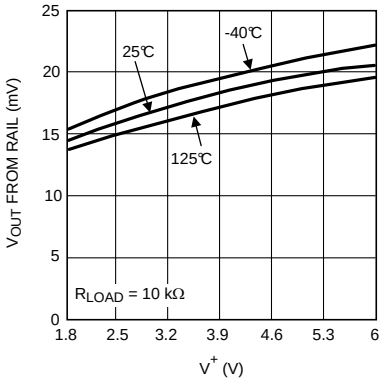


Figure 24.

Positive Output Swing vs. Supply Voltage

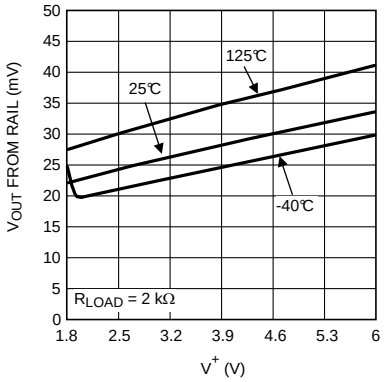


Figure 25.

Negative Output Swing vs. Supply Voltage

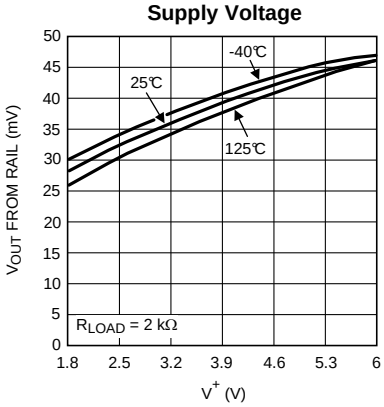


Figure 26.

Positive Output Swing vs. Supply Voltage

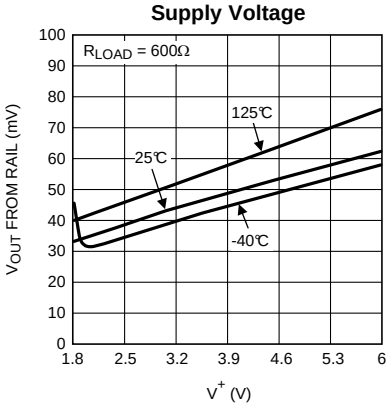


Figure 27.

Negative Output Swing vs. Supply Voltage

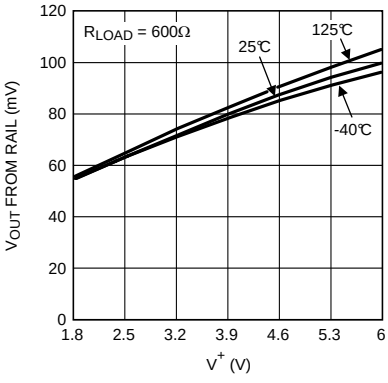


Figure 28.

Input Referred Voltage Noise vs. Frequency

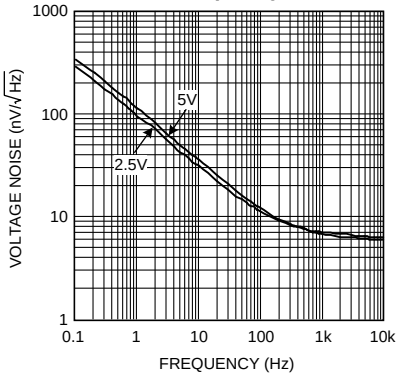


Figure 29.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = 5V, $V_S = V^+ - V^-$, $V_{CM} = V_S/2$.

Time Domain Voltage Noise

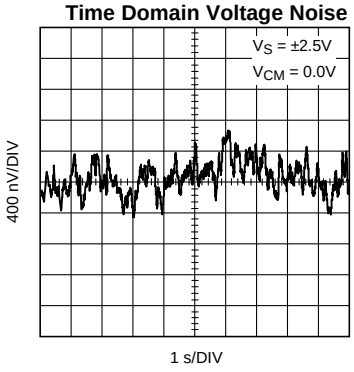


Figure 30.

Overshoot and Undershoot vs. C_{LOAD}

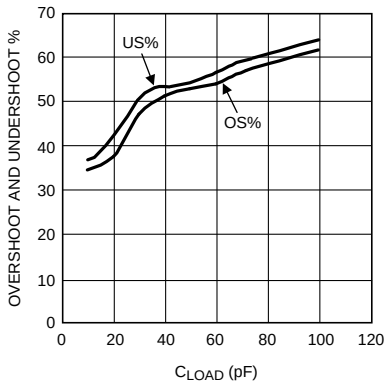


Figure 31.

THD+N vs. Frequency

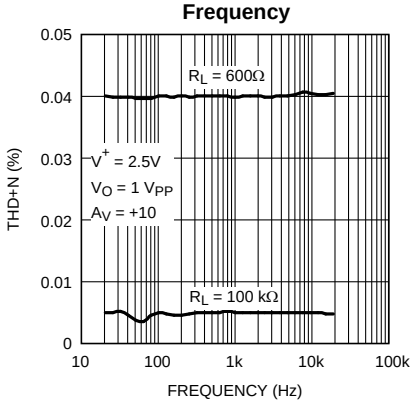


Figure 32.

THD+N vs. Frequency

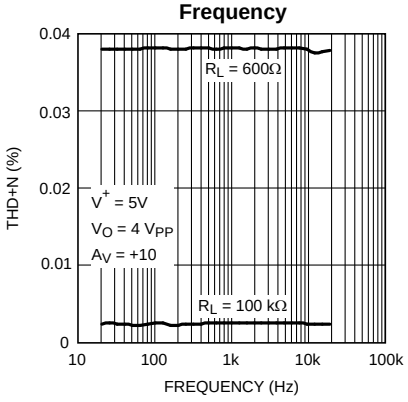


Figure 33.

THD+N vs. Peak-to-Peak Output Voltage (V_{OUT})

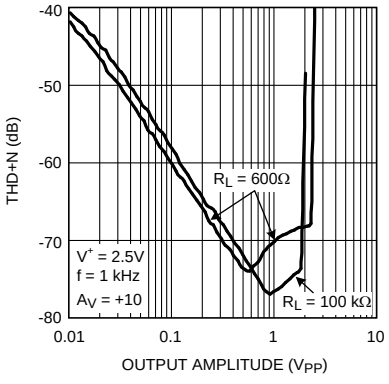


Figure 34.

THD+N vs. Peak-to-Peak Output Voltage (V_{OUT})

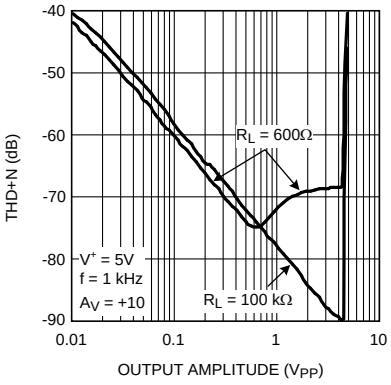


Figure 35.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = 5V, $V_S = V^+ - V^-$, $V_{CM} = V_S/2$.

Open Loop Gain and Phase

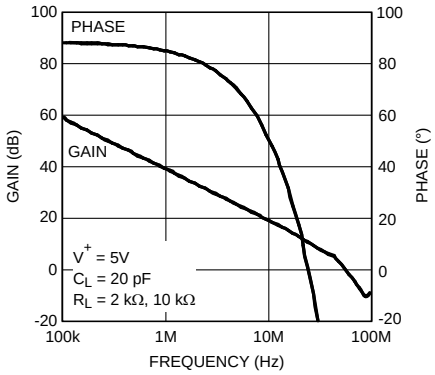


Figure 36.

Closed Loop Output Impedance vs. Frequency

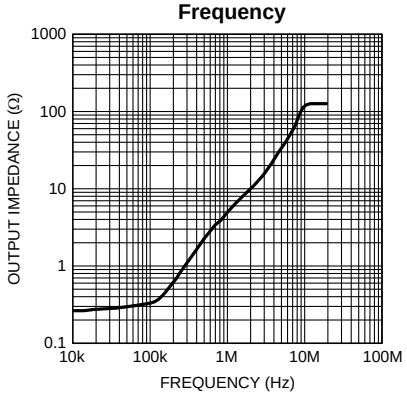


Figure 37.

Crosstalk Rejection

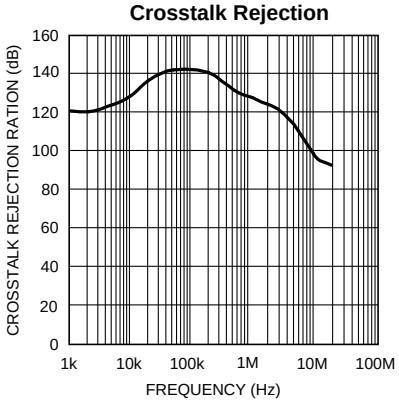


Figure 38.

Small Signal Transient Response, A_V = +10

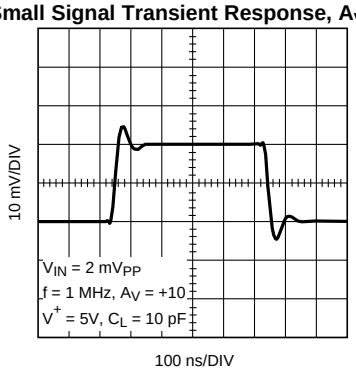


Figure 39.

Large Signal Transient Response, A_V = +10

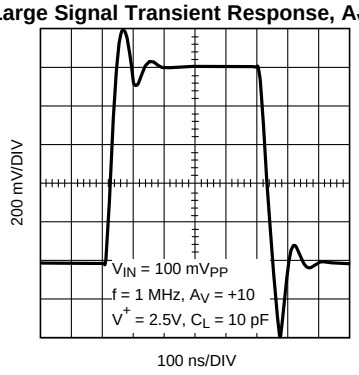


Figure 40.

Small Signal Transient Response, A_V = +10

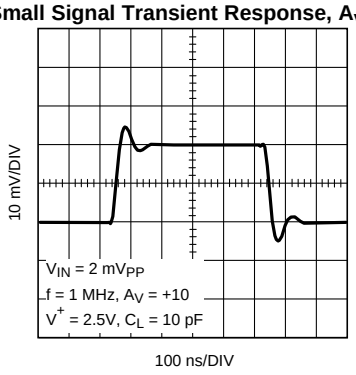


Figure 41.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = 5V, $V_S = V^+ - V^-$, $V_{CM} = V_S/2$.

Large Signal Transient Response, A_V = +10

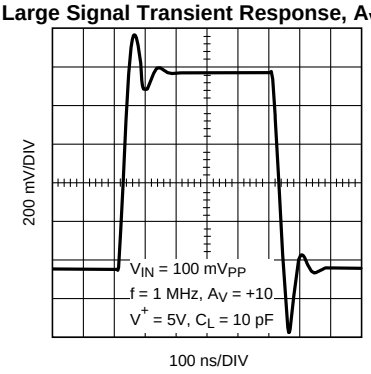


Figure 42.

PSRR vs. Frequency

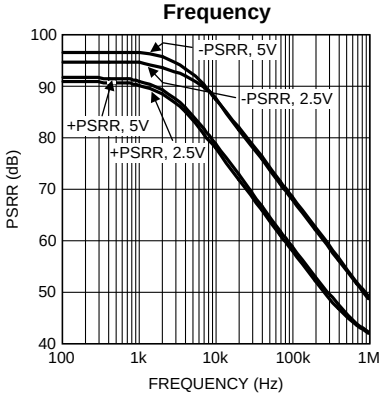


Figure 43.

CMRR vs. Frequency

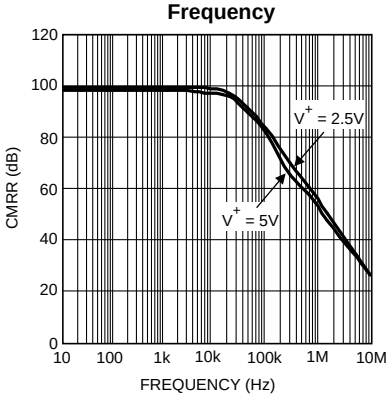


Figure 44.

Input Common Mode Capacitance vs. V_{CM}

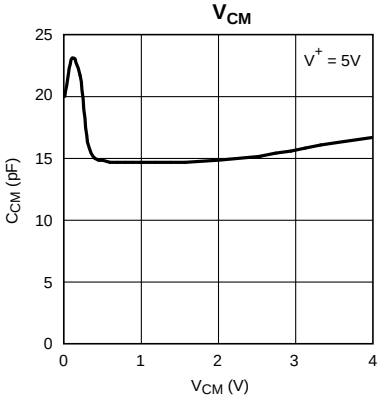


Figure 45.

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APPLICATION INFORMATION

ADVANTAGES OF THE LMP7717/LMP7718

Wide Bandwidth at Low Supply Current

The LMP7717/LMP7718 are high performance op amps that provide a GBW of 88 MHz with a gain of 10 while drawing a low supply current of 1.15 mA. This makes them ideal for providing wideband amplification in data acquisition applications.

With the proper external compensation the LMP7717 can be operated at gains of ±1 and still maintain much faster slew rates than comparable unity gain stable amplifiers. The increase in bandwidth and slew rate is obtained without any additional power consumption over the LMP7715.

Low Input Referred Noise and Low Input Bias Current

The LMP7717/LMP7718 have a very low input referred voltage noise density (5.8 nV/$\sqrt{\text{Hz}}$ at 1 kHz). A CMOS input stage ensures a small input bias current (100 fA) and low input referred current noise (0.01 pA/$\sqrt{\text{Hz}}$). This is very helpful in maintaining signal integrity, and makes the LMP7717/LMP7718 ideal for audio and sensor based applications.

Low Supply Voltage

The LMP7717 and the LMP7718 have performance ensured at 2.5V and 5V supply. These parts are ensured to be operational at all supply voltages between 2.0V and 5.5V, for ambient temperatures ranging from −40°C to 125°C, thus utilizing the entire battery lifetime. The LMP7717/LMP7718 are also ensured to be operational at 1.8V supply voltage, for temperatures between 0°C and 125°C optimizing their usage in low-voltage applications.

RRO and Ground Sensing

Rail-to-Rail output swing provides the maximum possible dynamic range. This is particularly important when operating at low supply voltages. An innovative positive feedback scheme is used to boost the current drive capability of the output stage. This allows the LMP7717/LMP7718 to source more than 40 mA of current at 1.8V supply. This also limits the performance of the these parts as comparators, and hence the usage of the LMP7717 and the LMP7718 in an open-loop configuration is not recommended. The input common-mode range includes the negative supply rail which allows direct sensing at ground in single supply operation.

Small Size

The small footprints of the LMP7717 packages and the LMP7718 packages save space on printed circuit boards, and enable the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. Long traces between the signal source and the op amp make the signal path more susceptible to noise pick up.

The physically smaller LMP7717 or LMP7718 packages allow the op amp to be placed closer to the signal source, thus reducing noise pickup and maintaining signal integrity.

USING THE DECOMPENSATED LMP7717

Advantages of Decompensated Op Amp

A unity gain stable op amp, which is fully compensated, is designed to operate with good stability down to gains of ±1. The large amount of compensation does provide an op amp that is relatively easy to use; however, a decompensated op amp is designed to maximize the bandwidth and slew rate without any additional power consumption. This can be very advantageous.

The LMP7717/LMP7718 require a gain of ±10 to be stable. However, with an external compensation network (a simple RC network) these parts can be stable with gains of ±1 and still maintain the higher slew rate. Looking at the Bode plots for the LMP7717 and its closest equivalent unity gain stable op amp, the LMP7715, one can clearly see the increased bandwidth of the LMP7717. Both plots are taken with a parallel combination of 20 pF and 10 kΩ for the output load.

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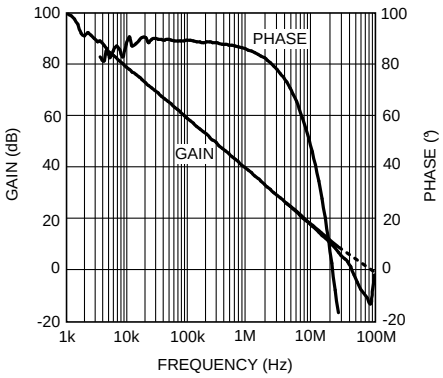


Figure 46. LMP7717 A_{VOL} vs. Frequency

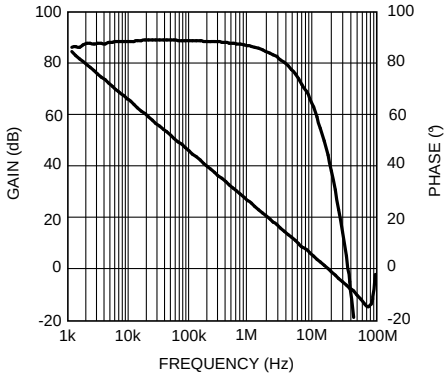


Figure 47. LMP7715 A_{VOL} vs. Frequency

Figure 46 shows the much larger 88 MHz bandwidth of the LMP7717 as compared to the 17 MHz bandwidth of the LMP7715 shown in Figure 47. The decompensated LMP7717 has five times the bandwidth of the LMP7715.

What is a Decompensated Op Amp?

The differences between the unity gain stable op amp and the decompensated op amp are shown in Figure 48. This Bode plot assumes an ideal two pole system. The dominant pole of the decompensated op amp is at a higher frequency, f_1, as compared to the unity gain stable op amp which is at f_d as shown in Figure 48. This is done in order to increase the speed capability of the op amp while maintaining the same power dissipation of the unity gain stable op amp. The LMP7717/LMP7718 have a dominant pole at 1.6 kHz. The unity gain stable LMP7715/LMP7716 have their dominant pole at 300 Hz.

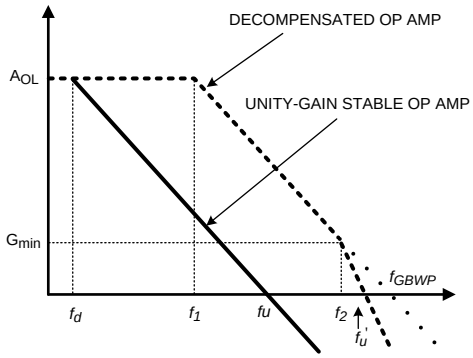


Figure 48. Open Loop Gain for Unity Gain Stable Op Amp and Decompensated Op Amp

Having a higher frequency for the dominate pole will result in:

1. The DC open loop gain (A_{VOL}) extending to a higher frequency.
2. A wider closed loop bandwidth.
3. Better slew rate due to reduced compensation capacitance within the op amp.

The second open loop pole (f_2) for the LMP7717/LMP7718 occurs at 45 MHz. The unity gain (f_u') occurs after the second pole at 51 MHz. An ideal two pole system would give a phase margin of 45° at the location of the second pole. The LMP7717/LMP7718 have parasitic poles close to the second pole, giving a phase margin closer to 0°. Therefore it is necessary to operate the LMP7717/LMP7718 at a closed loop gain of 10 or higher, or to add external compensation in order to assure stability.

For the LMP7715, the gain bandwidth product occurs at 17 MHz. The curve is constant from f_d to f_u which occurs before the second pole.

For the LMP7717/LMP7718 the GBW = 88 MHz and is constant between f_1 and f_2. The second pole at f_2 occurs before A_{VOL} =1. Therefore f_u' occurs at 51 MHz, well before the GBW frequency of 88 MHz. For decompensated op amps the unity gain frequency and the GBW are no longer equal. G_{min} is the minimum gain for stability and for the LMP7717/LMP7718 this is a gain of 18 to 20 dB.

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Input Lead-Lag Compensation

The recommended technique which allows the user to compensate the LMP7717/LMP7718 for stable operation at any gain is lead-lag compensation. The compensation components added to the circuit allow the user to shape the feedback function to make sure there is sufficient phase margin when the loop gain is as low as 0 dB and still maintain the advantages over the unity gain op amp. Figure 49 shows the lead-lag configuration. Only R_C and C are added for the necessary compensation.

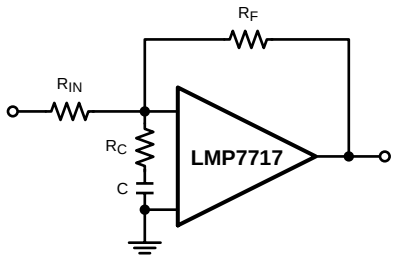


Figure 49. LMP7717 with Lead-Lag Compensation for Inverting Configuration

To cover how to calculate the compensation network values it is necessary to introduce the term called the feedback factor or F. The feedback factor F is the feedback voltage V_A-V_B across the op amp input terminals relative to the op amp output voltage V_{OUT}.

$$F = \frac{V_A - V_B}{V_{OUT}} \tag{1}$$

From feedback theory the classic form of the feedback equation for op amps is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + AF} \tag{2}$$

A is the open loop gain of the amplifier and AF is the loop gain. Both are highly important in analyzing op amps. Normally AF >>1 and so the above equation reduces to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{F} \tag{3}$$

Deriving the equations for the lead-lag compensation is beyond the scope of this datasheet. The derivation is based on the feedback equations that have just been covered. The inverse of feedback factor for the circuit in Figure 49 is:

$$\frac{1}{F} = \left(1 + \frac{R_F}{R_{IN}}\right)\left(\frac{1 + s(R_c + R_{IN} \parallel R_F)\, C}{1 + sR_cC}\right) \tag{4}$$

where 1/F's pole is located at

$$f_p = \frac{1}{2\pi R_cC} \tag{5}$$

1/F's zero is located at

$$f_z = \frac{1}{2\pi(R_c + R_{IN} \parallel R_F)C} \tag{6}$$

$$\left.\frac{1}{F}\right|_{f=0} = 1 + \frac{R_F}{R_{IN}} \tag{7}$$

The circuit gain for Figure 49 at low frequencies is $-R_F/R_{IN}$, but F, the feedback factor is not equal to the circuit gain. The feedback factor is derived from feedback theory and is the same for both inverting and non-inverting configurations. Yes, the feedback factor at low frequencies is equal to the gain for the non-inverting configuration.

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$$\left.\frac{1}{F}\right|_{f=\infty} = \left(1 + \frac{R_F}{R_{IN}}\right)\left(1 + \frac{R_{IN} \parallel R_F}{R_C}\right) \quad (8)$$

From this formula, we can see that

- 1/F's zero is located at a lower frequency compared with 1/F's pole.
- 1/F's value at low frequency is $1 + R_F/R_{IN}$.
- This method creates one additional pole and one additional zero.
- This pole-zero pair will serve two purposes:
  - To raise the 1/F value at higher frequencies prior to its intercept with A, the open loop gain curve, in order to meet the $G_{min} = 10$ requirement. For the LMP7717 some overcompensation will be necessary for good stability.
  - To achieve the previous purpose above with no additional loop phase delay.

Please note the constraint $1/F \geq G_{min}$ needs to be satisfied only in the vicinity where the open loop gain A and 1/F intersect; 1/F can be shaped elsewhere as needed. The 1/F pole must occur before the intersection with the open loop gain A.

In order to have adequate phase margin, it is desirable to follow these two rules:

Rule 1 1/F and the open loop gain A should intersect at the frequency where there is a minimum of 45° of phase margin. When over-compensation is required the intersection point of A and 1/F is set at a frequency where the phase margin is above 45°, therefore increasing the stability of the circuit.

Rule 2 1/F's pole should be set at least one decade below the intersection with the open loop gain A in order to take advantage of the full 90° of phase lead brought by 1/F's pole which is F's zero. This ensures that the effect of the zero is fully neutralized when the 1/F and A plots intersect each other.

Calculating Lead-Lag Compensation for LMP7717

Figure 50 is the same plot as Figure 46, but the A_{VOL} and phase curves have been redrawn as smooth lines to more readily show the concepts covered, and to clearly show the key parameters used in the calculations for lead-lag compensation.

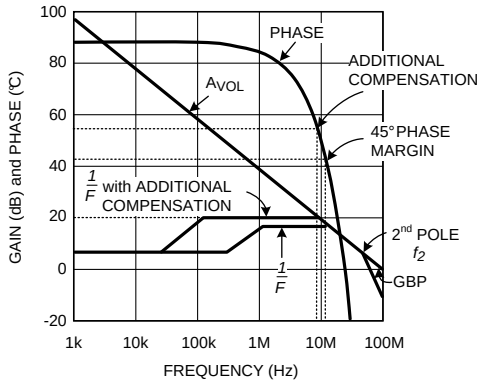


Figure 50. LMP7717/LMP7718 Simplified Bode Plot

To obtain stable operation with gains under 10 V/V the open loop gain margin must be reduced at high frequencies to where there is a 45° phase margin when the gain margin of the circuit with the external compensation is 0 dB. The pole and zero in F, the feedback factor, control the gain margin at the higher frequencies. The distance between F and A_{VOL} is the gain margin; therefore, the unity gain point (0 dB) is where F crosses the A_{VOL} curve.

For the example being used $R_{IN} = R_F$ for a gain of −1. Therefore F = 6 dB at low frequencies. At the higher frequencies the minimum value for F is 18 dB for 45° phase margin. From *Equation 5* we have the following relationship:

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$$\left(1 + \frac{R_F}{R_{IN}}\right)\left(1 + \frac{R_{IN} \parallel R_F}{R_C}\right) = 18\ dB = 7.9 \quad (9)$$

Now set $R_F = R_{IN} = R$. With these values and solving for R_C we have $R_C = R/5.9$. Note that the value of C does not affect the ratio between the resistors. Once the value of the resistors is set, then the position of the pole in F must be set. A 2 kΩ resistor is used for R_F and R_{IN} in this design. Therefore the value for R_C is set at 330Ω, the closest standard value for 2 kΩ/5.9.

Rewriting *Equation 2* to solve for the minimum capacitor value gives the following equation:

$$C = 1/(2\pi f_p R_C) \quad (10)$$

The feedback factor curve, F, intersects the A_{VOL} curve at about 12 MHz. Therefore the pole of F should not be any larger than 1.2 MHz. Using this value and R_C = 330Ω the minimum value for C is 390 pF. Figure 51 shows that there is too much overshoot, but the part is stable. Increasing C to 2.2 nF did not improve the ringing, as shown in Figure 52.

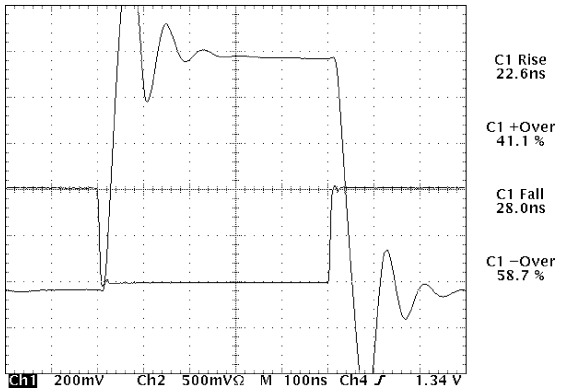


Figure 51. First Try at Compensation, Gain = −1

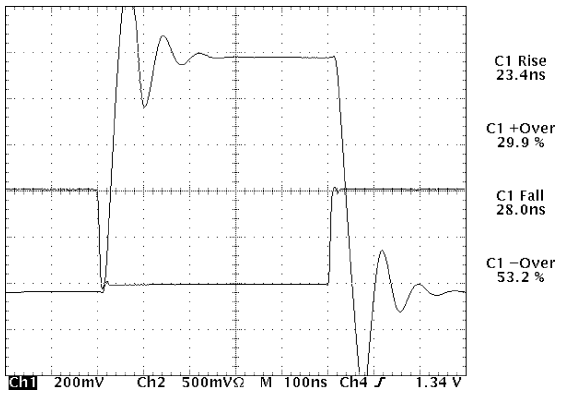


Figure 52. C Increased to 2.2 nF, Gain = −1

Some over-compensation appears to be needed for the desired overshoot characteristics. Instead of intersecting the A_{VOL} curve at 18 dB, 2 dB of over-compensation will be used, and the A_{VOL} curve will be intersected at 20 dB. Using *Equation 5* for 20 dB, or 10 V/V, the closest standard value of R_C is 240Ω. The following two waveforms show the new resistor value with C = 390 pF and 2.2 nF. Figure 54 shows the final compensation and a very good response for the 1 MHz square wave.

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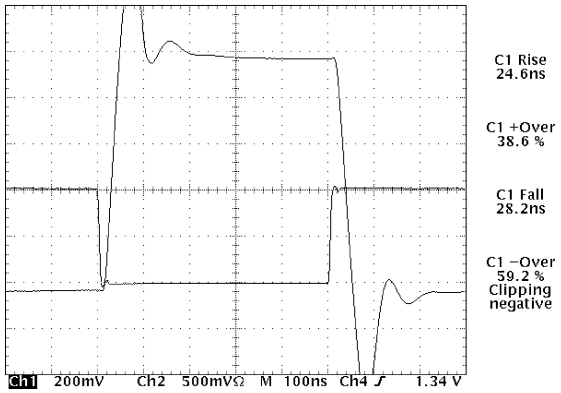


Figure 53. R_C = 240Ω and C = 390 pF, Gain = −1

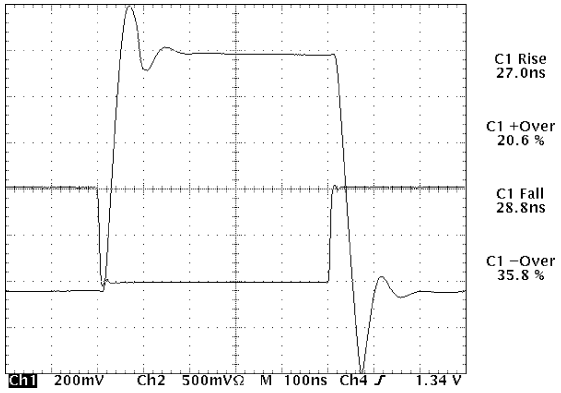


Figure 54. R_C = 240Ω and C = 2.2 nF, Gain = −1

To summarize, the following steps were taken to compensate the LMP7717 for a gain of −1:

1. Values for R_c and C were calculated from the Bode plot to give an expected phase margin of 45°. The values were based on $R_{IN} = R_F$ = 2 kΩ. These calculations gave R_c = 330Ω and C = 390 pF.
2. To reduce the ringing C was increased to 2.2 nF which moved the pole of F, the feedback factor, farther away from the A_{VOL} curve.
3. There was still too much ringing so 2 dB of over-compensation was added to F. This was done by decreasing R_C to 240Ω.

The LMP7715 is the fully compensated part which is comparable to the LMP7717. Using the LMP7715 in the same setup, but removing the compensation network, provided the response shown in Figure 55 .

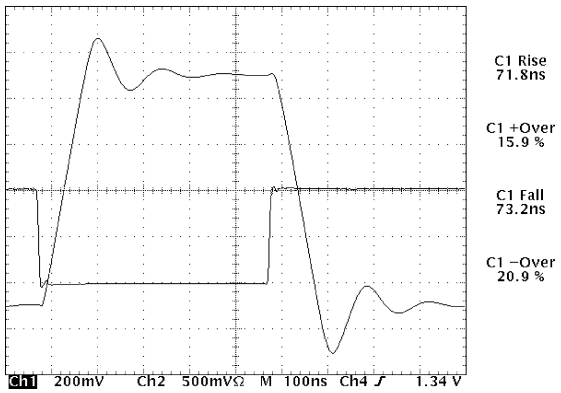


Figure 55. LMP7715 Response

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For large signal response the rise and fall times are dominated by the slew rate of the op amps. Even though both parts are quite similar the LMP7717 will give rise and fall times about 2.5 times faster than the LMP7715. This is possible because the LMP7717 is a decompensated op amp and even though it is being used at a gain of −1, the speed is preserved by using a good technique for external compensation.

Non-Inverting Compensation

For the non-inverting amp the same theory applies for establishing the needed compensation. When setting the inverting configuration for a gain of −1, F has a value of 2. For the non-inverting configuration both F and the actual gain are the same, making the non-inverting configuration more difficult to compensate. Using the same circuit as shown in Figure 49, but setting up the circuit for non-inverting operation (gain of +2) results in similar performance as the inverting configuration with the inputs set to half the amplitude to compensate for the additional gain. Figure 56 below shows the results.

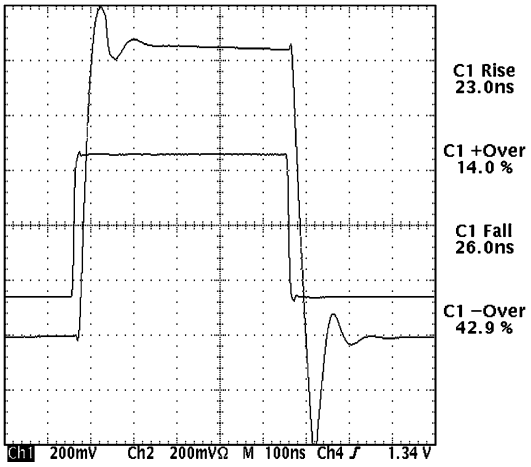


Figure 56. R_C = 240Ω and C = 2.2 nF, Gain = +2

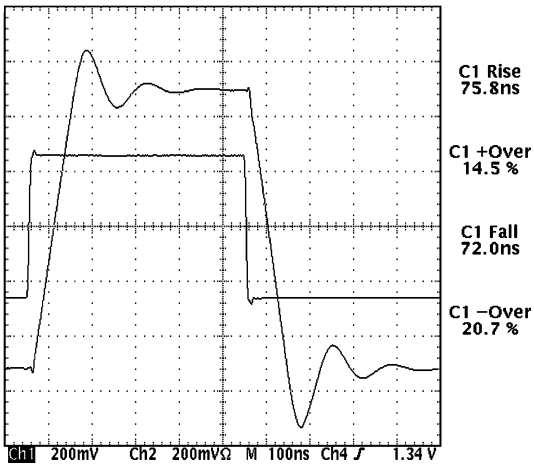


Figure 57. LMP7715 Response Gain = +2

The response shown in Figure 56 is close to the response shown in Figure 54. The part is actually slightly faster in the non-inverting configuration. Decreasing the value of R_C to around 200Ω can decrease the negative overshoot but will have slightly longer rise and fall times. The other option is to add a small resistor in series with the input signal. Figure 57 shows the performance of the LMP7715 with no compensation. Again the decompensated parts are almost 2.5 times faster than the fully compensated op amp.

The most difficult op amp configuration to stabilize is the gain of +1. With proper compensation the LMP7717/LMP7718 can be used in this configuration and still maintain higher speeds than the fully compensated parts. Figure 58 shows the gain = 1, or the buffer configuration, for these parts.

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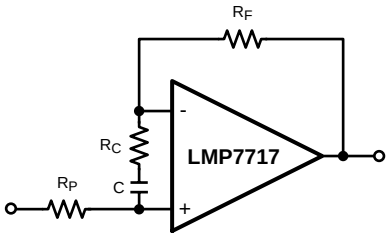


Figure 58. LMP7717 with Lead-Lag Compensation for Non-Inverting Configuration

Figure 58 is the result of using *Equation 5* and additional experimentation in the lab. R_P is not part of *Equation 5*, but it is necessary to introduce another pole at the input stage for good performance at gain = +1. *Equation 5* is shown below with $R_{IN} = \infty$.

$$\left(1 + \frac{R_F}{R_C}\right) = 18\ \text{dB} = 7.9 \tag{11}$$

Using 2 kΩ for R_F and solving for R_C gives R_C = 2000/6.9 = 290Ω. The closest standard value for R_C is 300Ω. After some fine tuning in the lab R_C = 330Ω and R_P = 1.5 kΩ were chosen as the optimum values. R_P together with the input capacitance at the non-inverting pin inserts another pole into the compensation for the LMP7717. Adding this pole and slightly reducing the compensation for 1/F (using a slightly higher resistor value for R_C) gives the optimum response for a gain of +1. Figure 59 is the response of the circuit shown in Figure 58. Figure 60 shows the response of the LMP7715 in the buffer configuration with no compensation and $R_P = R_F = 0$.

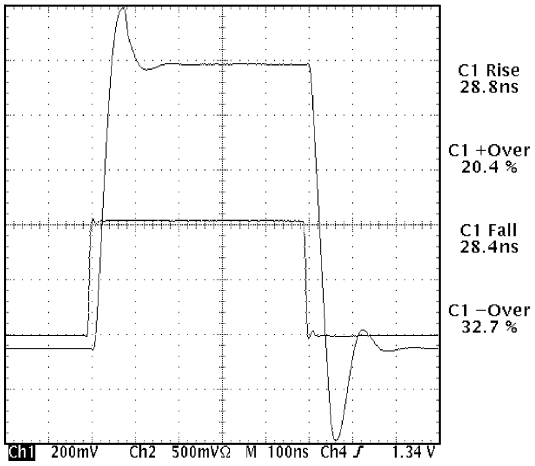


Figure 59. R_C = 330Ω and C = 10 nF, Gain = +1

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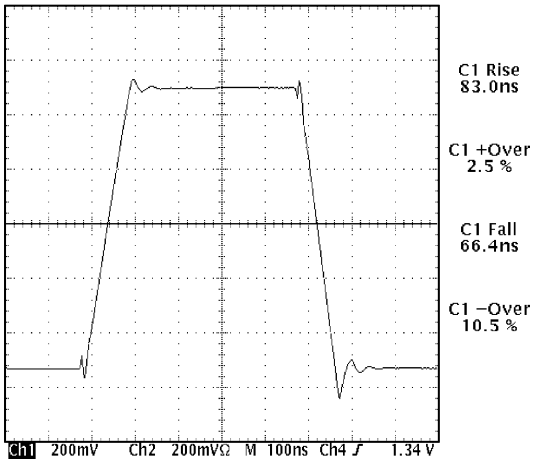


Figure 60. LMP7715 Response Gain = +1

With no increase in power consumption the decompensated op amp offers faster speed than the compensated equivalent part . These examples used R_F = 2 kΩ. This value is high enough to be easily driven by the LMP7717/LMP7718, yet small enough to minimize the effects from the parasitic capacitance of both the PCB and the op amp.

NOTE

When using the LMP7717/LMP7718, proper high frequency PCB layout must be followed. The GBW of these parts is 88 MHz, making the PCB layout significantly more critical than when using the compensated counterparts which have a GBW of 17 MHz.

TRANSIMPEDANCE AMPLIFIER

An excellent application for either the LMP7717 or the LMP7718 is as a transimpedance amplifier. With a GBW product of 88 MHz these parts are ideal for high speed data transmission by light. The circuit shown on the front page of the datasheet is the circuit used to test the LMP7717/LMP7718 as transimpedance amplifiers. The only change is that V_B is tied to the V_{CC} of the part, thus the direction of the diode is reversed from the circuit shown on the front page.

Very high speed components were used in testing to check the limits of the LMP7717/LMP7718 in a transimpedance configuration. The photodiode part number is PIN-HR040 from OSI Optoelectronics. The diode capacitance for this part is only about 7 pF for the 2.5V bias used (V_{CC} to virtual ground). The rise time for this diode is 1 nsec. A laser diode was used for the light source. Laser diodes have on and off times under 5 nsec. The speed of the selected optical components allowed an accurate evaluation of the LMP7717 as a transimpedance amplifier. TIs evaluation board for decompensated op amps, PN 551013271-001 A, was used and only minor modifications were necessary and no traces had to be cut.

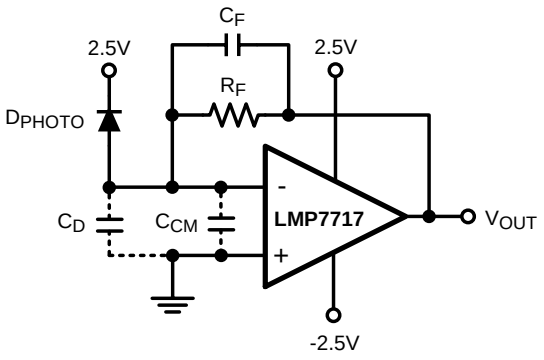


Figure 61. Transimpedance Amplifier

Figure 61 is the complete schematic for a transimpedance amplifier. Only the supply bypass capacitors are not shown. C_D represents the photodiode capacitance which is given on its datasheet. C_{CM} is the input common mode capacitance of the op amp and, for the LMP7717 it is shown in the last graph of the TYPICAL PERFORMANCE CHARACTERISTICS section of this datasheet. In Figure 61 the inverting input pin of the LMP7717 is kept at virtual ground. Even though the diode is connected to the 2.5V line, a power supply line is AC ground, thus C_D is connected to ground.

Figure 62 shows the schematic needed to derive F, the feedback factor, for a transimpedance amplifier. In Figure 62, $C_D + C_{CM} = C_{IN}$. Therefore it is critical that the designer knows the diode capacitance and the op amp input capacitance. The photodiode is close to an ideal current source once its capacitance is included in the model. What kind of circuit is this? Without C_F there is only an input capacitor and a feedback resistor. This circuit is a differentiator! Remember, differentiator circuits are inherently unstable and must be compensated. In this case C_F compensates the circuit.

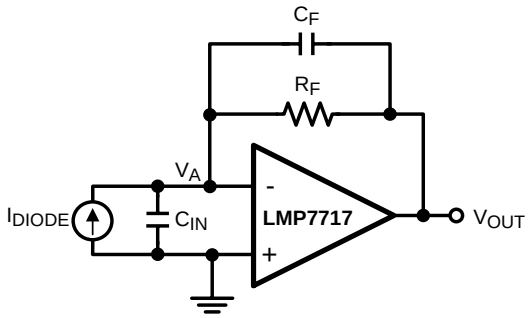


Figure 62. Transimpedance Feedback Model

Using feedback theory, $F = V_A/V_{OUT}$, this becomes a voltage divider giving the following equation:

$$F = \frac{1 + sC_FR_F}{1 + sR_F(C_F + C_{IN})} \tag{12}$$

The noise gain is 1/F. Because this is a differentiator circuit, a zero must be inserted. The location of the zero is given by:

$$f_z = \frac{1}{1 + sR_F(C_F + C_{IN})} \tag{13}$$

C_F has been added for stability. The addition of this part adds a pole to the circuit. The pole is located at:

$$f_p = \frac{1}{1 + sC_FR_F} \tag{14}$$

To attain maximum bandwidth and still have good stability the pole is to be located on the open loop gain curve which is A. If additional compensation is required one can always increase the value of C_F, but this will also reduce the bandwidth of the circuit. Therefore A = 1/F, or AF = 1. For A the equation is:

$$A = \frac{\omega_{GBW}}{\omega} = \frac{f_{GBW}}{f} \tag{15}$$

The expression f_{GBW} is the gain bandwidth product of the part. For a unity gain stable part this is the frequency where A = 1. For the LMP7717 f_{GBW} = 88 MHz. Multiplying A and F results in the following equation:

$$AF\Big|_{f_P} = \frac{f_{GBW}}{f} \times \frac{1 + sC_FR_F}{1 + sR_F(C_F + C_{IN})} =$$

$$\frac{f_{GBW}}{f} \times \frac{\sqrt{1 + \left(\frac{C_FR_F}{C_FR_F}\right)^2}}{\sqrt{1 + \left(\frac{R_F(C_F + C_{IN})}{C_FR_F}\right)^2}} = 1 \tag{16}$$

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For the above equation s = jω. To find the actual amplitude of the equation the square root of the square of the real and imaginary parts are calculated. At the intersection of F and A, we have:

$$\omega = \frac{1}{C_F R_F} \tag{17}$$

After a bit of algebraic manipulation the above equation reduces to:

$$1 + \left(\frac{C_F + C_{IN}}{C_F}\right)^2 = 8\pi^2 f_{GBW}^2 R_F^2 C_F^2 \tag{18}$$

In the above equation the only unknown is C_F. In trying to solve this equation the fourth power of C_F must be dealt with. An excel spread sheet with this equation can be used and all the known values entered. Then through iteration, the value of C_F when both sides are equal will be found. That is the correct value for C_F and of course the closest standard value is used for C_F.

Before moving to the lab, the transfer function of the transimpedance amplifier must be found and the units must be in Ohms.

$$V_{OUT} = \frac{-R_F}{1 + sC_F R_F} \times I_{DIODE} \tag{19}$$

The LMP7717 was evaluated for R_F = 10 kΩ and 100 kΩ, representing a somewhat lower gain configuration and with the 100 kΩ feedback resistor a fairly high gain configuration. The R_F = 10 kΩ is covered first. Looking at the *Input Common Mode Capacitance vs. V_{CM}* chart for C_{CM} for the operating point selected C_{CM} = 15 pF. Note that for split supplies V_{CM} = 2.5V, C_{IN} = 22 pF and f_{GBW} = 88 MHz. Solving for C_F the calculated value is 1.75 pF, so 1.8 pF is selected for use. Checking the frequency of the pole finds that it is at 8.8 MHz, which is right at the minimum gain recommended for this part. Some over compensation was necessary for stability and the final selected value for C_F is 2.7 pF. This moves the pole to 5.9 MHz. Figure 63 and Figure 64 show the rise and fall times obtained in the lab with a 1V output swing. The laser diode was difficult to drive due to thermal effects making the starting and ending point of the pulse quite different, therefore the two separate scope pictures.

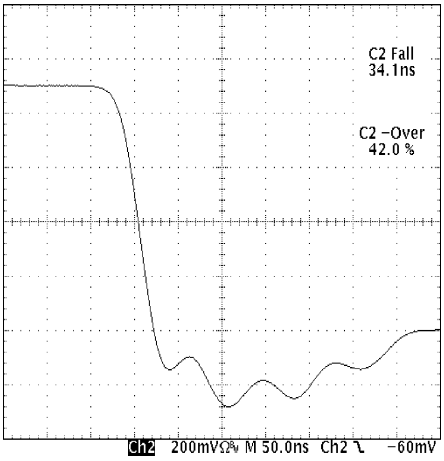


Figure 63. Fall Time

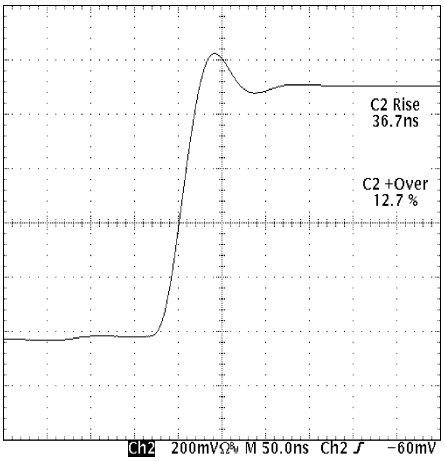


Figure 64. Rise Time

In Figure 63 the ringing and the hump during the on time is from the laser. The higher drive levels for the laser gave ringing in the light source as well as light changing from the thermal characteristics. The hump is due to the thermal characteristics.

Solving for C_F using a 100 kΩ feedback resistor, the calculated value is 0.54 pF. One of the problems with more gain is the very small value for C_F. A 0.5 pF capacitor was used, its measured value being 0.64 pF. For the 0.64 pF location the pole is at 2.5 MHz. Figure 65 shows the response for a 1V output.

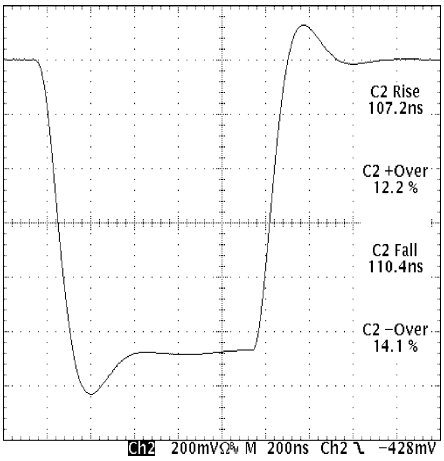


Figure 65. High Gain Response

A transimpedance amplifier is an excellent application for the LMP7717. Even with the high gain using a 100 kΩ feedback resistor, the bandwidth is still well over 1 MHz. Other than a little over compensation for the 10 kΩ feedback resistor configuration using the LMP7717 was quite easy. Of course a very good board layout was also used for this test.

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REVISION HISTORY

Changes from Revision G (March 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	26

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMP7717MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 17MA
LMP7717MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 17MA
LMP7717MAE/NOPB	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 17MA
LMP7717MAE/NOPB.A	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 17MA
LMP7717MF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AT4A
LMP7717MF/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AT4A
LMP7717MFE/NOPB	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AT4A
LMP7717MFE/NOPB.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AT4A
LMP7717MFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AT4A
LMP7717MFX/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AT4A
LMP7718MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 18MA
LMP7718MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 18MA
LMP7718MAE/NOPB	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 18MA
LMP7718MAE/NOPB.A	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 18MA
LMP7718MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 18MA
LMP7718MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP77 18MA
LMP7718MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AP4A
LMP7718MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AP4A
LMP7718MME/NOPB	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AP4A
LMP7718MME/NOPB.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AP4A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

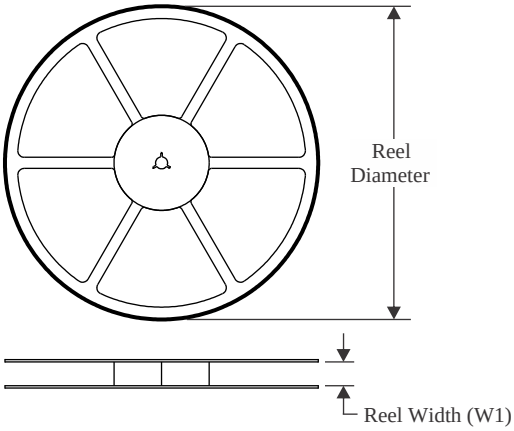
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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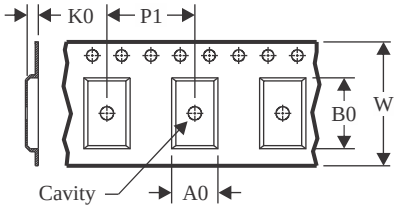
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

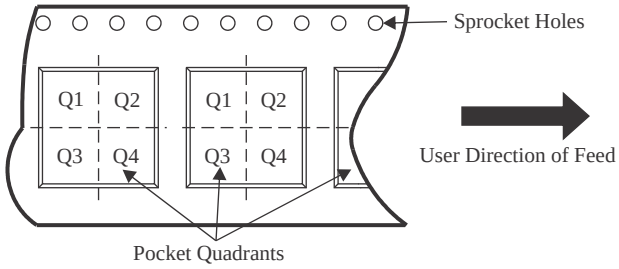


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

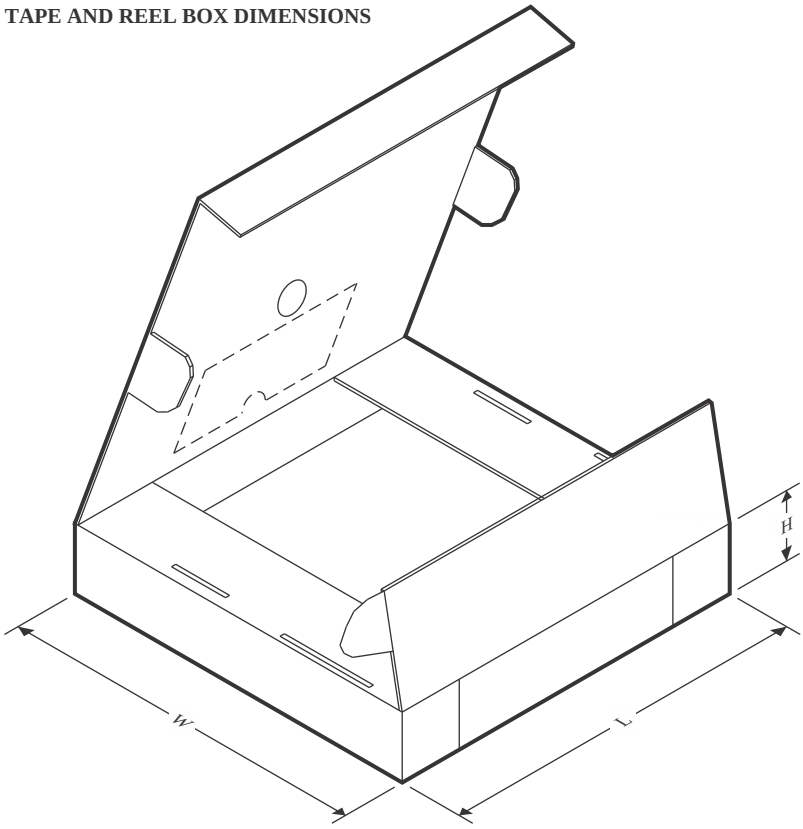
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP7717MAE/NOPB	SOIC	D	8	250	177.8	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMP7717MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7717MFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7717MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP7718MAE/NOPB	SOIC	D	8	250	177.8	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMP7718MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMP7718MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMP7718MME/NOPB	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

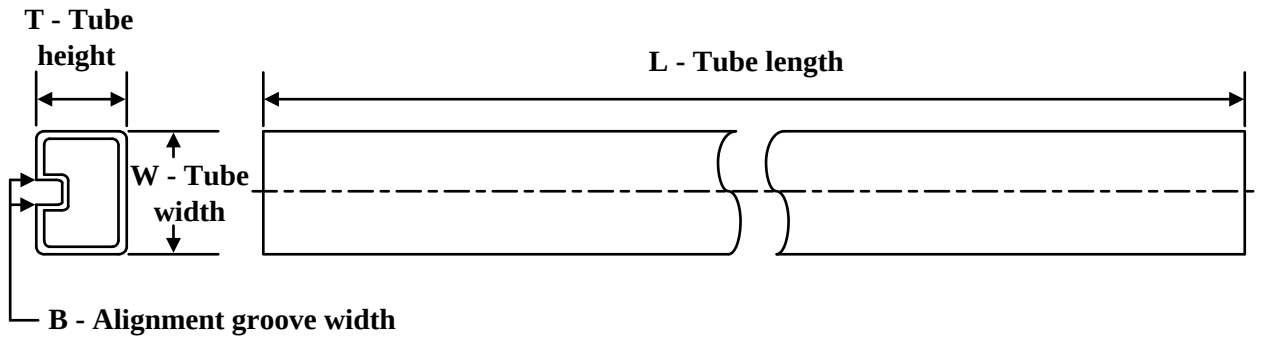
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

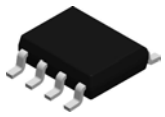
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP7717MAE/NOPB	SOIC	D	8	250	208.0	191.0	35.0
LMP7717MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMP7717MFE/NOPB	SOT-23	DBV	5	250	208.0	191.0	35.0
LMP7717MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMP7718MAE/NOPB	SOIC	D	8	250	208.0	191.0	35.0
LMP7718MAX/NOPB	SOIC	D	8	2500	356.0	356.0	35.0
LMP7718MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMP7718MME/NOPB	VSSOP	DGK	8	250	208.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMP7717MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMP7717MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMP7718MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMP7718MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

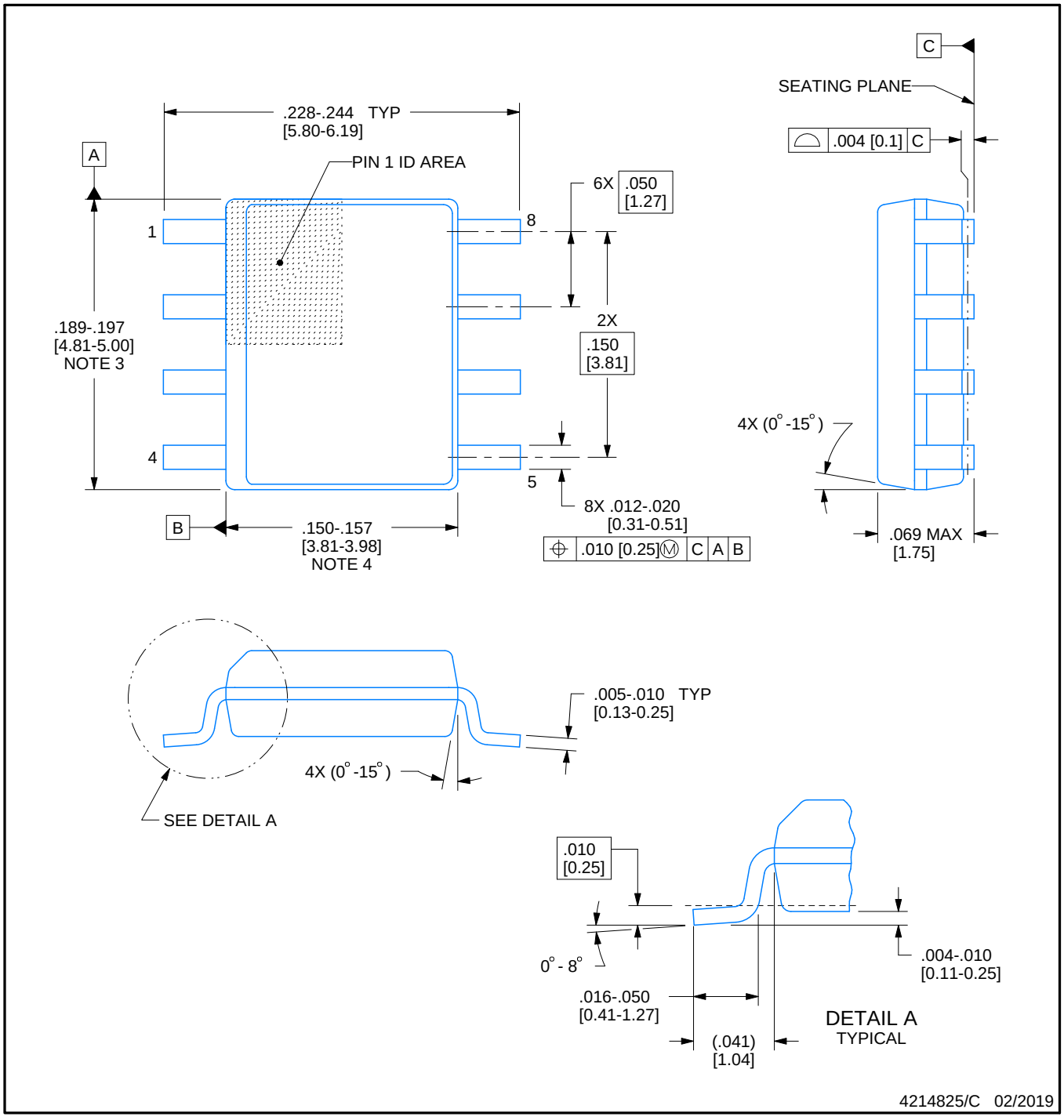


PACKAGE OUTLINE

D0008A

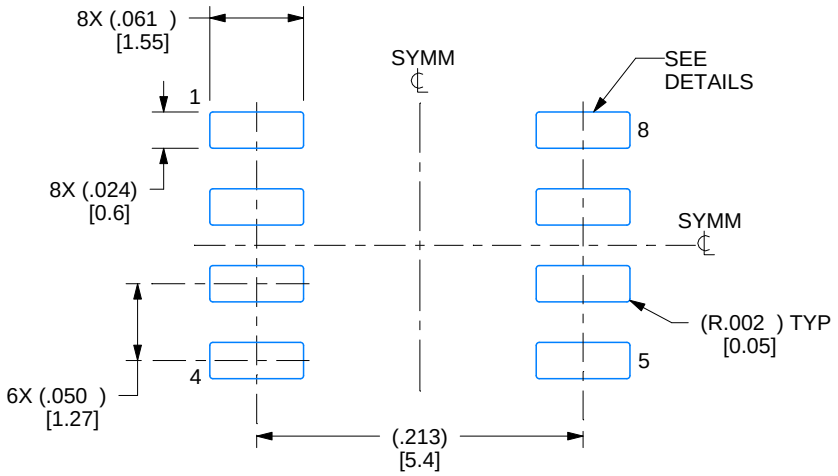
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

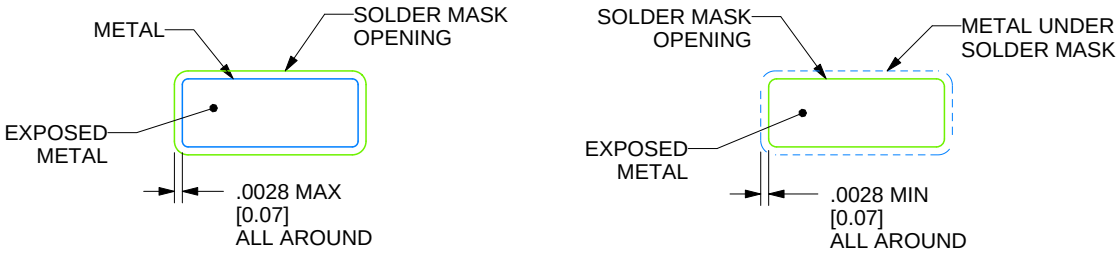


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

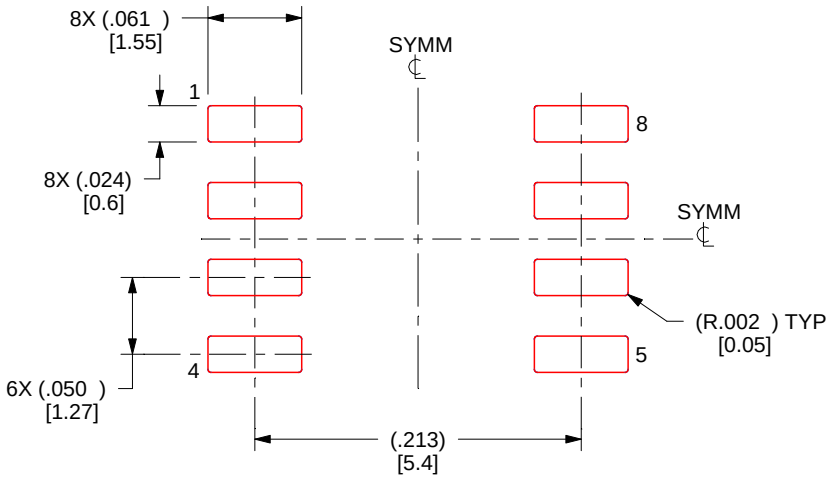
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

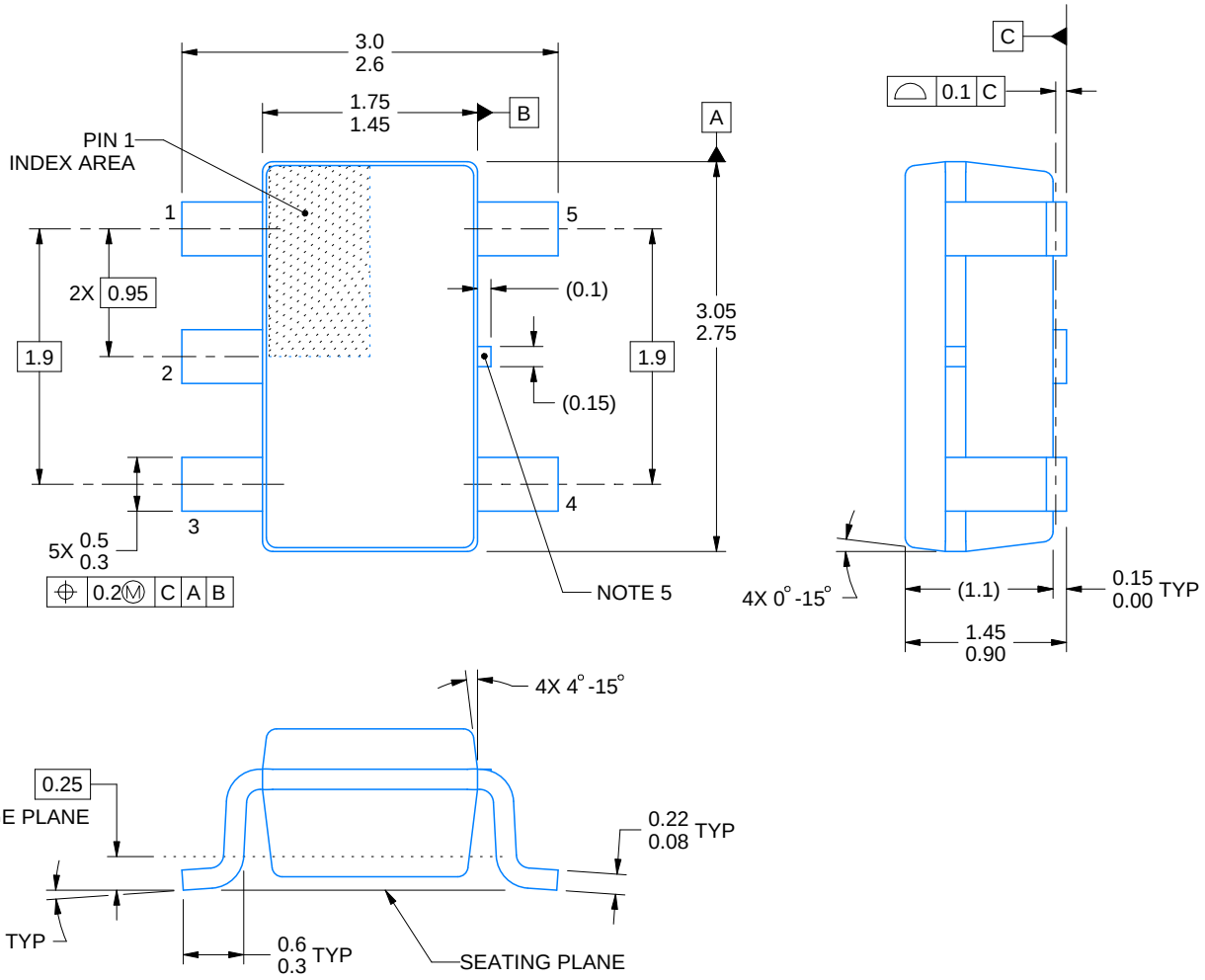
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

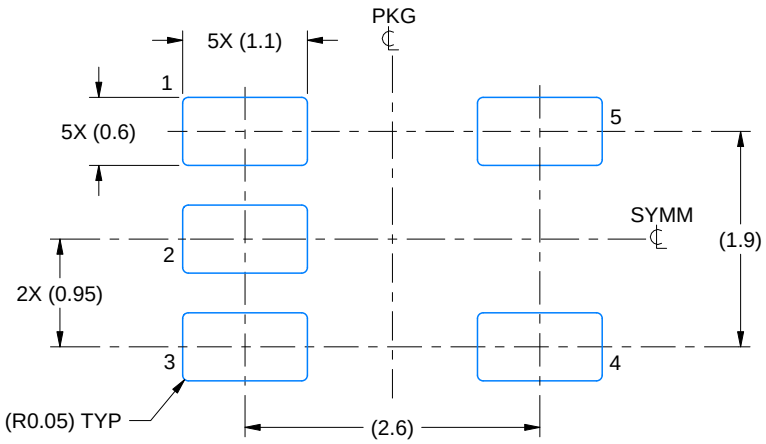
SMALL OUTLINE TRANSISTOR



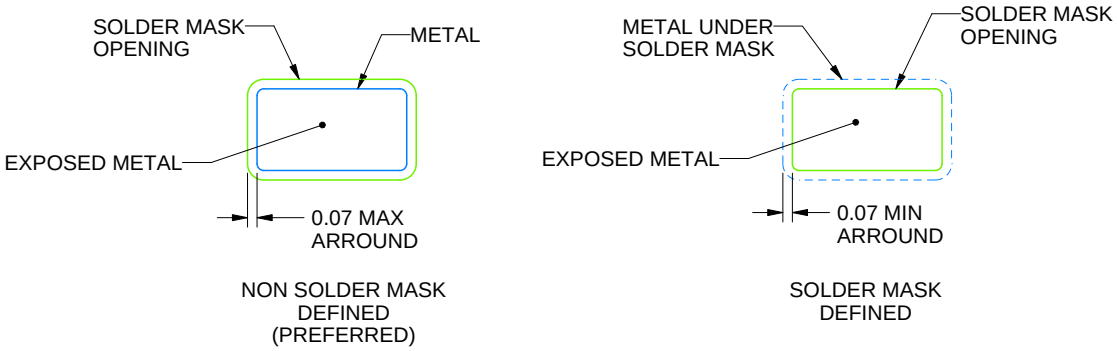
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

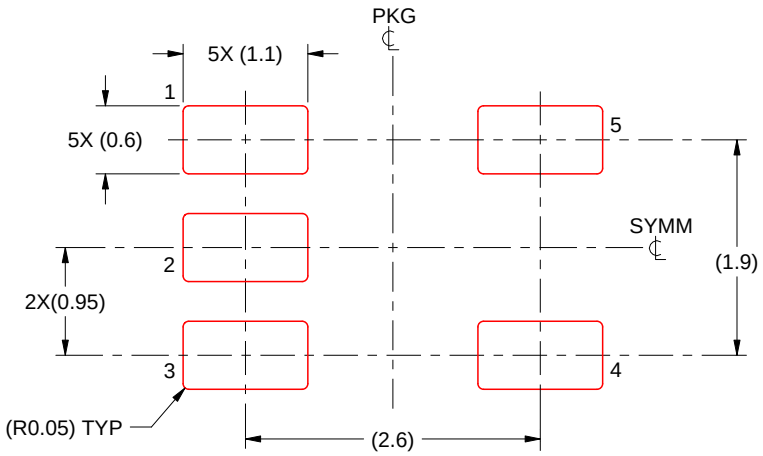


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

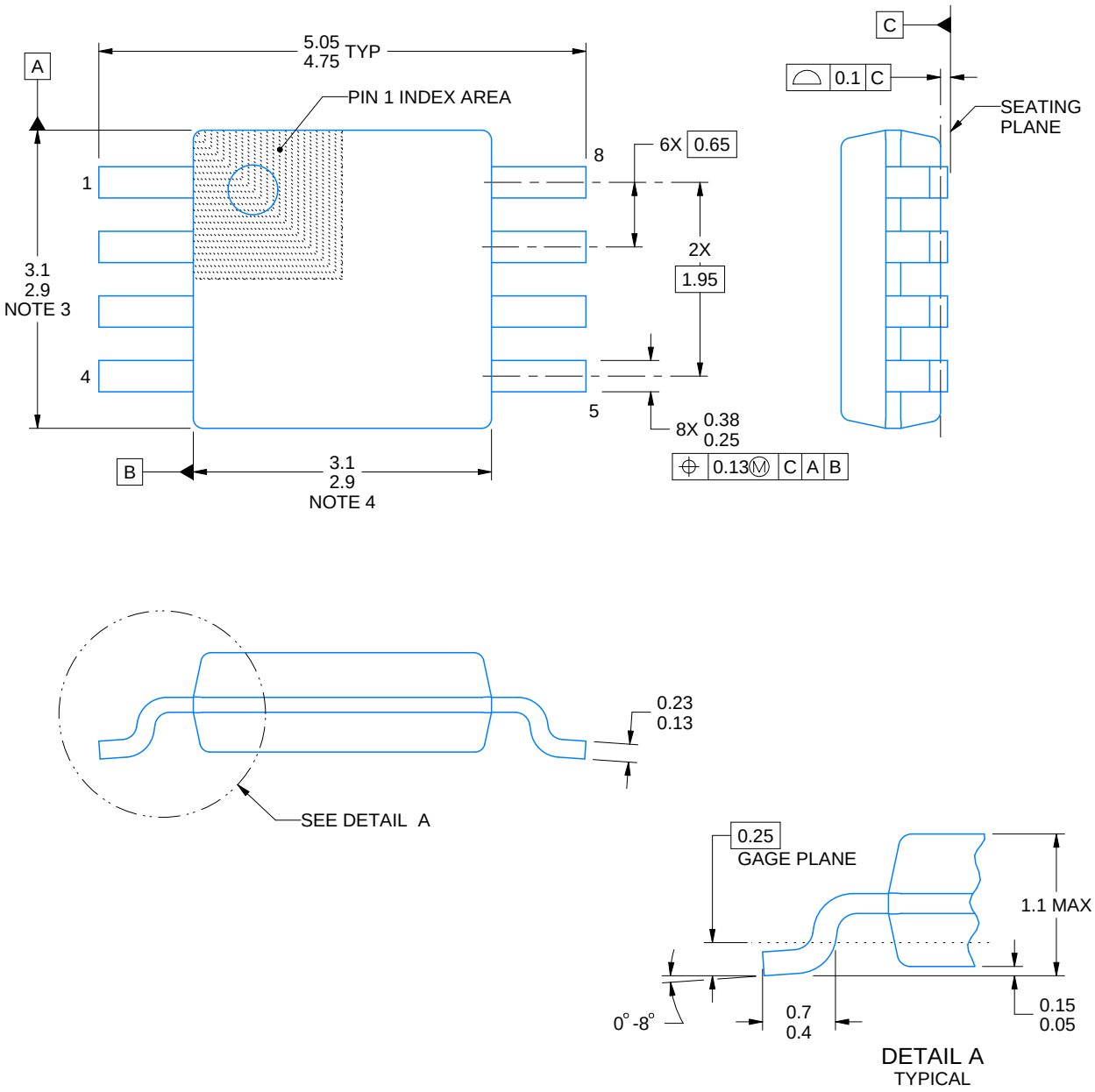
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

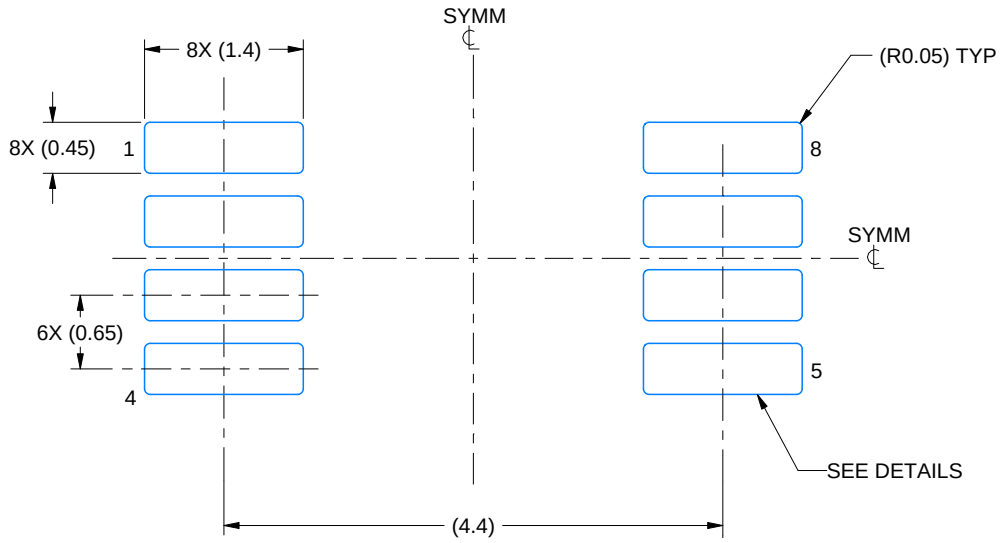
SMALL OUTLINE PACKAGE



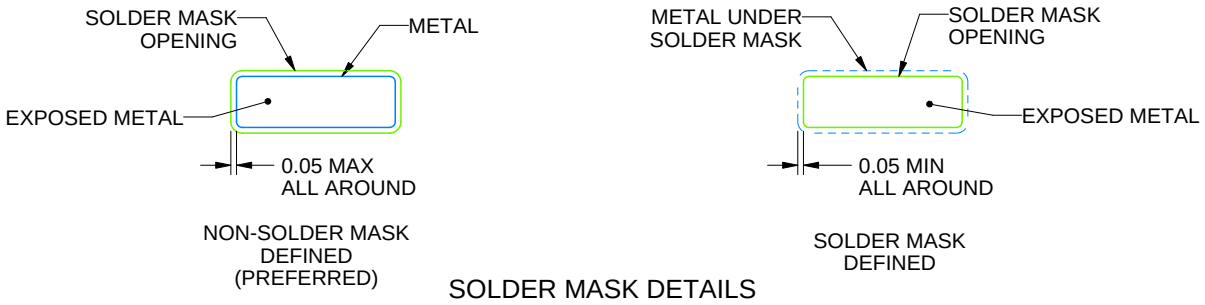
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

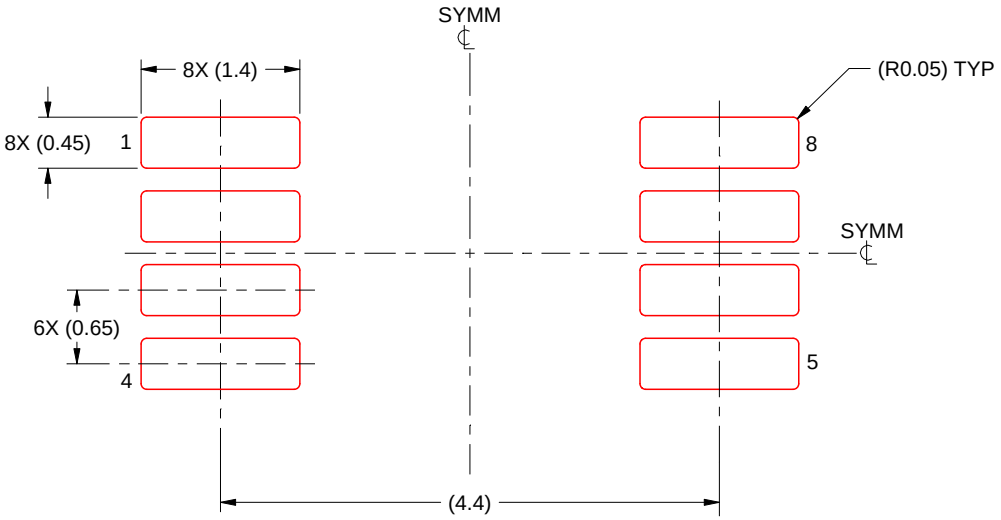


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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