LMP2012QML Dual High Precision, Rail-to-Rail Output Operational Amplifier

FEATURES

- **Total Ionizing Dose 50 krad(Si)**
- **ELDRS Free 50 krad(Si)**
- **TCV_{IO} Temperature Sensitivity (Typical) 0.015 µV/°C**
  (For V_S = 5V, Typical Unless Otherwise Noted)
- **Low Ensured V_{IO} over Temperature 60 µV**
- **Low Noise with no 1/f 35nV/$\sqrt{Hz}$**
- **High CMRR 90 dB**
- **High PSRR 90 dB**
- **High A_{VOL} 85 dB**
- **Wide Gain-Bandwidth Product 3MHz**
- **High Slew Rate 4V/µs**
- **Rail-to-Rail Output 30mV**
- **No External Capacitors Required**

APPLICATIONS

- **Attitude and Orbital Controls**
- **Static Earth Sensing**
- **Sun Sensors**
- **Inertial Sensors**
- **Pressure Sensors**
- **Gyroscopes**
- **Earth Observation Systems**

DESCRIPTION

The LMP2012 offers unprecedented accuracy and stability. This device utilizes patented techniques to measure and continually correct the input offset error voltage. The result is an amplifier which is ultra stable over time and temperature. It has excellent CMRR and PSRR ratings, and does not exhibit the familiar 1/f voltage and current noise increase that plagues traditional amplifiers. The combination of the LMP2012 characteristics makes it a good choice for transducer amplifiers, high gain configurations, ADC buffer amplifiers, DAC I-V conversion, and any other 2.7V-5V application requiring precision and long term stability.

Other useful benefits of the LMP2012 are rail-rail output, low supply current of 930 µA, and wide gain-bandwidth product of 3 MHz. These extremely versatile features found in the LMP2012 provide high performance and ease of use.

The QMLV version of the LMP2012 has been rated to tolerate a total dose level of 50krad/(Si) radiation by test method 1019 of MIL-STD-883.

Connection Diagram

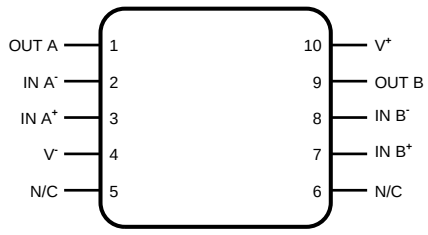


Figure 1. 10-Lead CLGA (Top View)
See NAC Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)

Supply Voltage			5.8V
Differential Input Voltage			±Supply Voltage
Power Dissipation(2)			714mW
Maximum Junction Temperature (T_{Jmax})			150°C
Common-Mode Input Voltage			$-0.3 \le V_{CM} \le V_{CC}$ +0.3V
Current at Input Pin			30 mA
Current at Output Pin			30 mA
Current at Power Supply Pin			50 mA
Operating Temperature Range			-55°C to +125°C
Storage Temperature Range			-55°C to +150°C
CLGA Lead Temperature (soldering 10 sec.)			+260°C
Thermal Resistance	θ_{JA}	CLGA (Still Air)	175°C/W
		CLGA (500LF/Min Air Flow)	115°C/W
	θ_{JC}	CLGA	12.3°C/W
Package Weight		CLGA	220mg
ESD Tolerance(3)			4000V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(3) Human body model, 1.5 kΩ in series with 100 pF.

Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Setting time at	+25
13	Setting time at	+125
14	Setting time at	-55

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LMP2012 Electrical Characteristics 2.7V DC Parameters

The following conditions apply, unless otherwise specified.
V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, V_O = 1.35V and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Notes	Typ(1)	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			0.8		36	µV	1
						60		2, 3
	Offset Calibration Time			0.5		10	ms	1
						12		2, 3
TCV_{IO}	Input Offset Voltage (Temperature Sensitivity)			0.015			µV/°C	
I_{IB}	Input Bias Current			−3			pA	
I_{IO}	Input Offset Current			6			pA	
CMRR	Common Mode Rejection Ratio	$-0.3 \le V_{CM} \le 0.9V$		130	95		dB	1
		$0 \le V_{CM} \le 0.9V$			90			2, 3
PSRR	Power Supply Rejection Ratio			120	95		dB	1
					90			2, 3
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ		130	95		dB	1
					90			2, 3
		R_L = 2 kΩ		124	90			1
					85			2, 3
V_O	Output Swing	R_L = 10 kΩ to 1.35V V_{IN}(diff) = ±0.5V		2.68	2.64		V	1
					2.63			2, 3
				0.033		0.060		1
						0.075		2,3
		R_L = 2 kΩ to 1.35V V_{IN}(diff) = ±0.5V		2.65	2.615		V	1
					2.6			2, 3
				0.061		0.085		1
						0.105		2, 3
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V		12	5		mA	1
					3			2, 3
		Sinking, V_O = 5V V_{IN}(diff) = ±0.5V		18	5			1
					3			2, 3
I_S	Supply Current per Channel			0.919		1.20	mA	1
						1.50		2, 3

(1) Typical values represent the most likely parametric norm.

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LMP2012 Electrical Characteristics 2.7V AC Parameters

The following conditions apply, unless otherwise specified.
V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, V_O = 1.35V, and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Notes	Typ(1)	Min	Max	Units	Sub-groups
GBW	Gain-Bandwidth Product			3	1	5	MHz	4
SR	Slew Rate			4			V/µs	
θ_m	Phase Margin			60			Deg	
G_m	Gain Margin			−14			dB	
e_n	Input-Referred Voltage Noise			35			nV/√Hz	
e_nP-P	Input-Referred Voltage Noise	R_S = 100Ω, DC to 10 Hz		850			nV_{PP}	
t_{rec}	Input Overload Recovery Time			50			ms	

(1) Typical values represent the most likely parametric norm.

LMP2012 Electrical Characteristics 2.7V DC Parameters – 50 krad(Si) Post Radiation Limits @ +25°C(1)

The following conditions apply, unless otherwise specified.
V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, V_O = 1.35V, and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
I_S	Supply Current per Channel					1.75	mA	1

(1) Pre and post irradiation limits are identical to those listed under DC Parameters, except those listed in the Post Radiation Limit tables.

LMP2012 Electrical Characteristics 2.7V Operating Life Test Delta Parameters T_A = +25°C

This is worst case drift, deltas are performed at room temperature post operation life. All other parameters, no deltas required.

Symbol	Parameter	Conditions	Limit	Units
V_{IO}	Input offset voltage	2.7 V	±2	µV

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LMP2012 Electrical Characteristics 5V DC Parameters

The following conditions apply, unless otherwise specified.
V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V and R_L > 1MΩ.

Symbol	Parameter	Conditions	Notes	Typ (1)	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage			0.12		36	µV	1
						60		2, 3
	Offset Calibration Time			0.5		10	ms	1
						12		2, 3
TCV_{IO}	Input Offset Voltage (Temperature Sensitivity)			0.015			µV/°C	
I_{IB}	Input Bias Current			−3			pA	
I_{IO}	Input Offset Current			6			pA	
CMRR	Common Mode Rejection Ratio	$-0.3 \le V_{CM} \le 3.2$		130	100		dB	1
		$0 \le V_{CM} \le 3.2$			90			2, 3
PSRR	Power Supply Rejection Ratio			120	95		dB	1
					90			2, 3
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ		130	105		dB	1
					100			2, 3
		R_L = 2 kΩ		132	95			1
					90			2, 3
V_O	Output Swing	R_L = 10 kΩ to 2.5V V_{IN}(diff) = ±0.5V		4.978	4.92		V	1
					4.91			2, 3
				0.040		0.080		1
						0.095		2, 3
		R_L = 2 kΩ to 2.5V V_{IN}(diff) = ±0.5V		4.919	4.875		V	1
					4.855			2, 3
				0.091		0.125		1
						0.150		2, 3
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V		15	8		mA	1
					6			2, 3
		Sourcing, V_O = 5V V_{IN}(diff) = ±0.5V		17	8			1
					6			2, 3
I_S	Supply Current per Channel			0.930		1.20	mA	1
						1.50		2, 3

(1) Typical values represent the most likely parametric norm.

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LMP2012 Electrical Characteristics 5V AC Parameters

The following conditions apply, unless otherwise specified.
V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V, and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Notes	Typ(1)	Min	Max	Units	Sub-groups
GBW	Gain-Bandwidth Product			3	1	5	MHz	4
SR	Slew Rate			4			V/µs	
θ_m	Phase Margin			60			Deg	
G_m	Gain Margin			−15			dB	
e_n	Input-Referred Voltage Noise			35			nV/√Hz	
e_nP-P	Input-Referred Voltage Noise	R_S = 100Ω, DC to 10 Hz		850			nV_{PP}	
t_{rec}	Input Overload Recovery Time			50			ms	

(1) Typical values represent the most likely parametric norm.

LMP2012 Electrical Characteristics 5V DC Parameters – 50 krad(Si) Post Radiation Limits @ +25°C(1)

The following conditions apply, unless otherwise specified.
V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V, and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Notes	Typ	Min	Max	Units	Sub-groups
I_S	Supply Current per Channel					1.75	mA	1

(1) Pre and post irradiation limits are identical to those listed under DC Parameters, except those listed in the Post Radiation Limit tables.

LMP2012 Electrical Characteristics 5V Operating Life Test Delta Parameters T_A = +25°C

This is worst case drift, deltas are performed at room temperature post operation life. All other parameters, no deltas required.

Symbol	Parameter	Conditions	Limit	Units
V_{IO}	Input offset voltage	5.0 V	±2	µV

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APPLICATION INFORMATION

THE BENEFITS OF LMP2012 NO 1/f NOISE

Using patented methods, the LMP2012 eliminates the 1/f noise present in other amplifiers. That noise, which increases as frequency decreases, is a major source of measurement error in all DC-coupled measurements. Low-frequency noise appears as a constantly-changing signal in series with any measurement being made. As a result, even when the measurement is made rapidly, this constantly-changing noise signal will corrupt the result. The value of this noise signal can be surprisingly large. For example: If a conventional amplifier has a flat-band noise level of 10nV/√Hz and a noise corner of 10 Hz, the RMS noise at 0.001 Hz is 1µV/√Hz. This is equivalent to a 0.50 µV peak-to-peak error, in the frequency range 0.001 Hz to 1.0 Hz. In a circuit with a gain of 1000, this produces a 0.50 mV peak-to-peak output error. This number of 0.001 Hz might appear unreasonably low, but when a data acquisition system is operating for 17 minutes, it has been on long enough to include this error. In this same time, the LMP2012 will only have a 0.21 mV output error. This is smaller by 2.4 x. Keep in mind that this 1/f error gets even larger at lower frequencies. At the extreme, many people try to reduce this error by integrating or taking several samples of the same signal. This is also doomed to failure because the 1/f nature of this noise means that taking longer samples just moves the measurement into lower frequencies where the noise level is even higher.

The LMP2012 eliminates this source of error. The noise level is constant with frequency so that reducing the bandwidth reduces the errors caused by noise.

OVERLOAD RECOVERY

The LMP2012 recovers from input overload much faster than most chopper-stabilized op amps. Recovery from driving the amplifier to 2X the full scale output, only requires about 40 ms. Many chopper-stabilized amplifiers will take from 250 ms to several seconds to recover from this same overload. This is because large capacitors are used to store the unadjusted offset voltage.

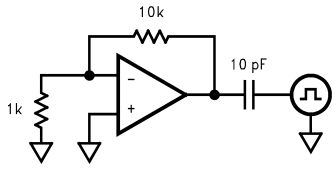


Figure 2.

The wide bandwidth of the LMP2012 enhances performance when it is used as an amplifier to drive loads that inject transients back into the output. ADCs (Analog-to-Digital Converters) and multiplexers are examples of this type of load. To simulate this type of load, a pulse generator producing a 1V peak square wave was connected to the output through a 10 pF capacitor. See Figure 2. The typical time for the output to recover to 1% of the applied pulse is 80 ns. To recover to 0.1% requires 860ns. This rapid recovery is due to the wide bandwidth of the output stage and large total GBW.

NO EXTERNAL CAPACITORS REQUIRED

The LMP2012 does not need external capacitors. This eliminates the problems caused by capacitor leakage and dielectric absorption, which can cause delays of several seconds from turn-on until the amplifier's error has settled.

MORE BENEFITS

The LMP2012 offers the benefits mentioned above and more. It has a rail-to-rail output and consumes only 950 µA of supply current while providing excellent DC and AC electrical performance. In DC performance, the LMP2012 achieves 130 dB of CMRR, 120 dB of PSRR and 130 dB of open loop gain. In AC performance, the LMP2012 provides 3 MHz of gain-bandwidth product and 4 V/µs of slew rate.

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HOW THE LMP2012 WORKS

The LMP2012 uses new, patented techniques to achieve the high DC accuracy traditionally associated with chopper-stabilized amplifiers without the major drawbacks produced by chopping. The LMP2012 continuously monitors the input offset and corrects this error. The conventional chopping process produces many mixing products, both sums and differences, between the chopping frequency and the incoming signal frequency. This mixing causes large amounts of distortion, particularly when the signal frequency approaches the chopping frequency. Even without an incoming signal, the chopper harmonics mix with each other to produce even more trash. If this sounds unlikely or difficult to understand, look at the plot in Figure 3, of the output of a typical (MAX432) chopper-stabilized op amp. This is the output when there is no incoming signal, just the amplifier in a gain of -10 with the input grounded. The chopper is operating at about 150 Hz; the rest is mixing products. Add an input signal and the noise gets much worse. Compare this plot with Figure 4 of the LMP2012. This data was taken under the exact same conditions. The auto-zero action is visible at about 30 kHz but note the absence of mixing products at other frequencies. As a result, the LMP2012 has very low distortion of 0.02% and very low mixing products.

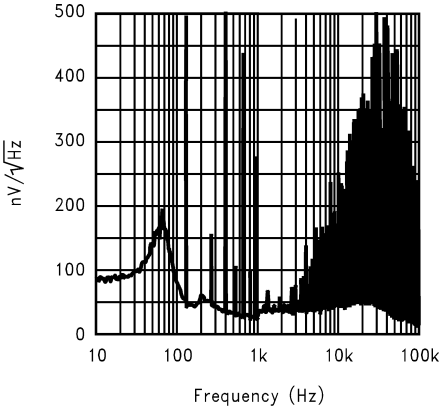


Figure 3.

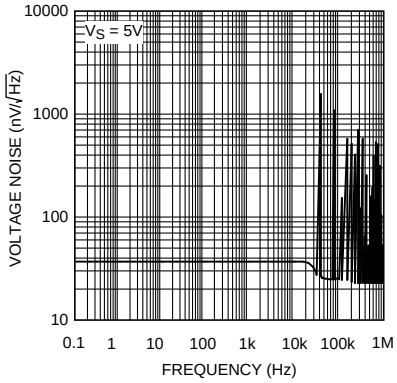


Figure 4.

INPUT CURRENTS

The LMP2012's input currents are different than standard bipolar or CMOS input currents in that it appears as a current flowing in one input and out the other. Under most operating conditions, these currents are in the picoamp level and will have little or no effect in most circuits. These currents tend to increase slightly when the common-mode voltage is near the minus supply. At high temperatures, the input currents become larger, 0.5 nA typical, and are both positive except when the V_{CM} is near V^-. If operation is expected at low common-mode voltages and high temperature, do not add resistance in series with the inputs to balance the impedances. Doing this can cause an increase in offset voltage. A small resistance such as 1 kΩ can provide some protection against very large transients or overloads, and will not increase the offset significantly.

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PRECISION STRAIN-GAUGE AMPLIFIER

This Strain-Gauge amplifier (Figure 5) provides high gain (1006 or ~60 dB) with very low offset and drift. Using the resistors' tolerances as shown, the worst case CMRR will be greater than 108 dB. The CMRR is directly related to the resistor mismatch. The rejection of common-mode error, at the output, is independent of the differential gain, which is set by R3. The CMRR is further improved, if the resistor ratio matching is improved, by specifying tighter-tolerance resistors, or by trimming.

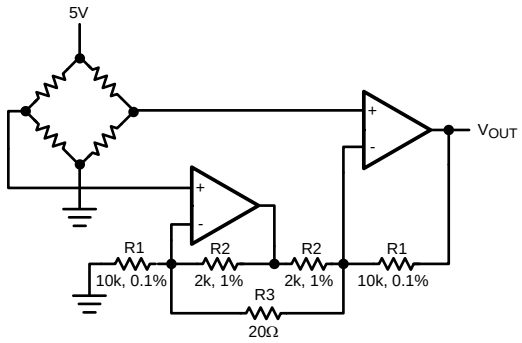


Figure 5.

Extending Supply Voltages and Output Swing by Using a Composite Amplifier Configuration:

In cases where substantially higher output swing is required with higher supply voltages, arrangements like the ones shown in Figure 6 and Figure 7 could be used. These configurations utilize the excellent DC performance of the LMP2012 while at the same time allow the superior voltage and frequency capabilities of the LM6171 to set the dynamic performance of the overall amplifier. For example, it is possible to achieve ±12V output swing with 300 MHz of overall GBW (A_V = 100) while keeping the worst case output shift due to V_{OS} less than 4 mV. The LMP2012 output voltage is kept at about mid-point of its overall supply voltage, and its input common mode voltage range allows the V- terminal to be grounded in one case (Figure 6, inverting operation) and tied to a small non-critical negative bias in another (Figure 7, non-inverting operation). Higher closed-loop gains are also possible with a corresponding reduction in realizable bandwidth. Table 2 shows some other closed loop gain possibilities along with the measured performance in each case.

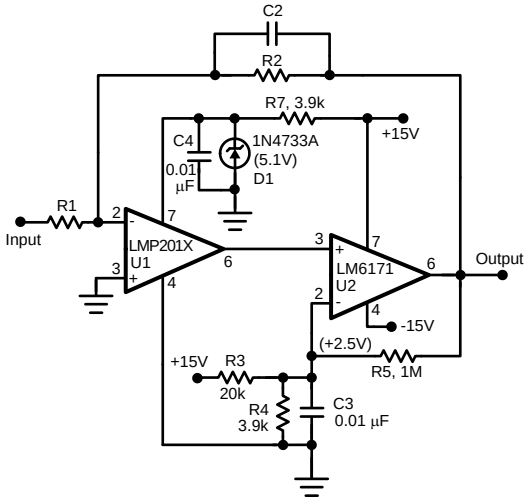


Figure 6.

Table 2. Composite Amplifier Measured Performance

AV	R1 Ω	R2 Ω	C2 pF	BW MHz	SR (V/µs)	en p-p (mV_{PP})
50	200	10k	8	3.3	178	37
100	100	10k	10	2.5	174	70
100	1k	100k	0.67	3.1	170	70
500	200	100k	1.75	1.4	96	250
1000	100	100k	2.2	0.98	64	400

In terms of the measured output peak-to-peak noise, the following relationship holds between output noise voltage, e_n p-p, for different closed-loop gain, A_V, settings, where −3 dB Bandwidth is BW:

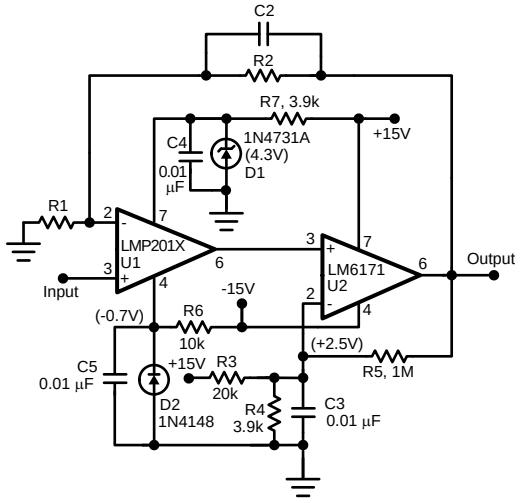


Figure 7.

It should be kept in mind that in order to minimize the output noise voltage for a given closed-loop gain setting, one could minimize the overall bandwidth. As can be seen from Equation 1 above, the output noise has a square-root relationship to the Bandwidth.

In the case of the inverting configuration, it is also possible to increase the input impedance of the overall amplifier, by raising the value of R1, without having to increase the feed-back resistor, R2, to impractical values, by utilizing a "Tee" network as feedback. See the LMC6442 data sheet (Application Notes section) for more details on this.

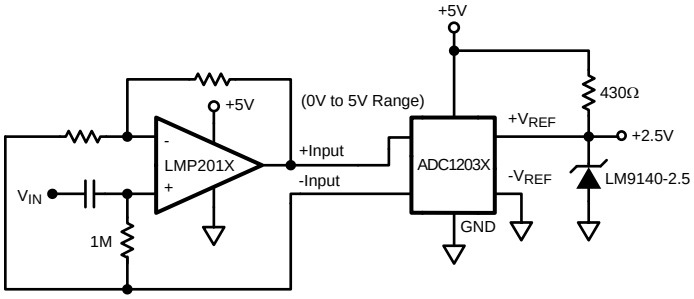


Figure 8.

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LMP2012 AS ADC INPUT AMPLIFIER

The LMP2012 is a great choice for an amplifier stage immediately before the input of an ADC (Analog-to-Digital Converter), whether AC or DC coupled. See Figure 8 and Figure 9. This is because of the following important characteristics:

A) Very low offset voltage and offset voltage drift over time and temperature allow a high closed-loop gain setting without introducing any short-term or long-term errors. For example, when set to a closed-loop gain of 100 as the analog input amplifier for a 12-bit A/D converter, the overall conversion error over full operation temperature and 30 years life of the part (operating at 50°C) would be less than 5 LSBs.

B) Fast large-signal settling time to 0.01% of final value (1.4 µs) allows 12 bit accuracy at 100 KH_Z or more sampling rate.

C) No flicker (1/f) noise means unsurpassed data accuracy over any measurement period of time, no matter how long. Consider the following op amp performance, based on a typical low-noise, high-performance commercially-available device, for comparison:
Op amp flatband noise = 8nV/√Hz
1/f corner frequency = 100 Hz
A_V = 2000
Measurement time = 100 sec
Bandwidth = 2 Hz
This example will result in about 2.2 mV_{PP} (1.9 LSB) of output noise contribution due to the op amp alone, compared to about 594 μV_{PP} (less than 0.5 LSB) when that op amp is replaced with the LMP2012 which has no 1/f contribution. If the measurement time is increased from 100 seconds to 1 hour, the improvement realized by using the LMP2012 would be a factor of about 4.8 times (2.86 mV_{PP} compared to 596 µV when LMP2012 is used) mainly because the LMP2012 accuracy is not compromised by increasing the observation time.

D) Rail-to-Rail output swing maximizes the ADC dynamic range in 5-Volt single-supply converter applications. Below are some typical block diagrams showing the LMP2012 used as an ADC amplifier (Figure 8 and Figure 9).

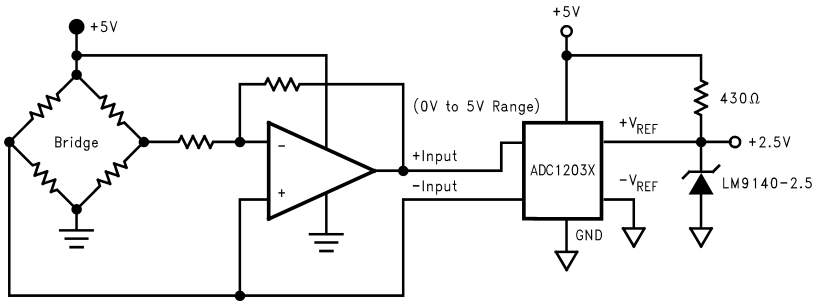


Figure 9.

RADIATION ENVIRONMENTS

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

TOTAL IONIZING DOSE

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the Ordering Information table on the front page. Testing and qualification of these products is done on a wafer level according to MIL-STD-883G, Test Method 1019.7, Condition A and the “Extended room temperature anneal test” described in section 3.11 for application environment dose rates less than 0.082 rad(Si)/s. Wafer level TID data are available with lot shipments.

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ELDRS-FREE PRODUCTS

ELDRS-Free products are tested and qualified on a wafer level basis at a dose rate of 10 mrad(Si)/s per MIL-STD-883G, Test Method 1019.7, Condition D. Wafer level low dose rate test data are available with lot shipments.

SINGLE EVENT UPSET

A report on single event upset (SEU) is available upon request.

Revision History

Date Released	Revision	Section	Changes
03/19/07	A	Initial Release	Initial Release
10/17/08	B	Electrical Section	Added typical parameters to 2.7V and 5V AC Electrical Sections. Revision A will be Archived.
07/13/09	C	2.7V DC and 5V DC Electrical Section	Added typical parameter TCV_{OS} to 2.7V DC and 5V DC Electrical Section. Revision B will be Archived.
12/08/09	D	Features, Ordering Information and Notes	Reference to ELDRS, New ELDRS part number and added ELDRS Note 6. Revision C will be Archived.
06/08/2010	E	General Description, 2.7V DC and 5V DC Electrical Section added New Radiation Section.	Removed first line. Added Delta Table to Electrical's to match what is in the SMD and New Radiation Section. Revision D will be Archived.
11/30/2010	F	AC Electrical 5V parameter table conditions	Correct typo to unless otherwise specified parameters From: V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, V_O = 1.35V, and R_L > 1 MΩ. To: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V, and R_L > 1 MΩ. Revision E will be Archived.
04/02/2013	H	All	Changed layout of National Data Sheet to TI format

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-0620601VZA	Active	Production	CFP (NAC) | 10	1 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMP2012 WG-QMLV Q 5962-06206 01VZA ACO 01VZA >T
5962L0620601VZA	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMP2012 (WGLQMLV Q, WGQMLV Q) 5962L06206 01VZA ACO 01VZA >T
5962L0620602V9A	Active	Production	DIESALE (Y) | 0	32 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
5962L0620602VZA	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMP2012 WGLLQV Q 5962L06206 02VZA ACO 02VZA >T
LMP2012 MDE	Active	Production	DIESALE (Y) | 0	32 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LMP2012 MDR	Active	Production	DIESALE (Y) | 0	32 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LMP2012-MDE.A	Active	Production	DIESALE (Y) | 0	32 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LMP2012-MDR.A	Active	Production	DIESALE (Y) | 0	32 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LMP2012WG-QMLV	Active	Production	CFP (NAC) | 10	1 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMP2012 WG-QMLV Q 5962-06206 01VZA ACO 01VZA >T
LMP2012WG-QMLV.A	Active	Production	CFP (NAC) | 10	1 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMP2012 WG-QMLV Q 5962-06206 01VZA ACO 01VZA >T
LMP2012WGLLQMLV	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMP2012 WGLLQV Q 5962L06206 02VZA ACO 02VZA >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMP2012WGLLQMLV.A	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMP2012 WGLLQV Q 5962L06206 02VZA ACO 02VZA >T
LMP2012WGLQMLV	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMP2012 (WGLQMLV Q, WGQMLV Q) 5962L06206 01VZA ACO 01VZA >T
LMP2012WGLQMLV.A	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LMP2012 (WGLQMLV Q, WGQMLV Q) 5962L06206 01VZA ACO 01VZA >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

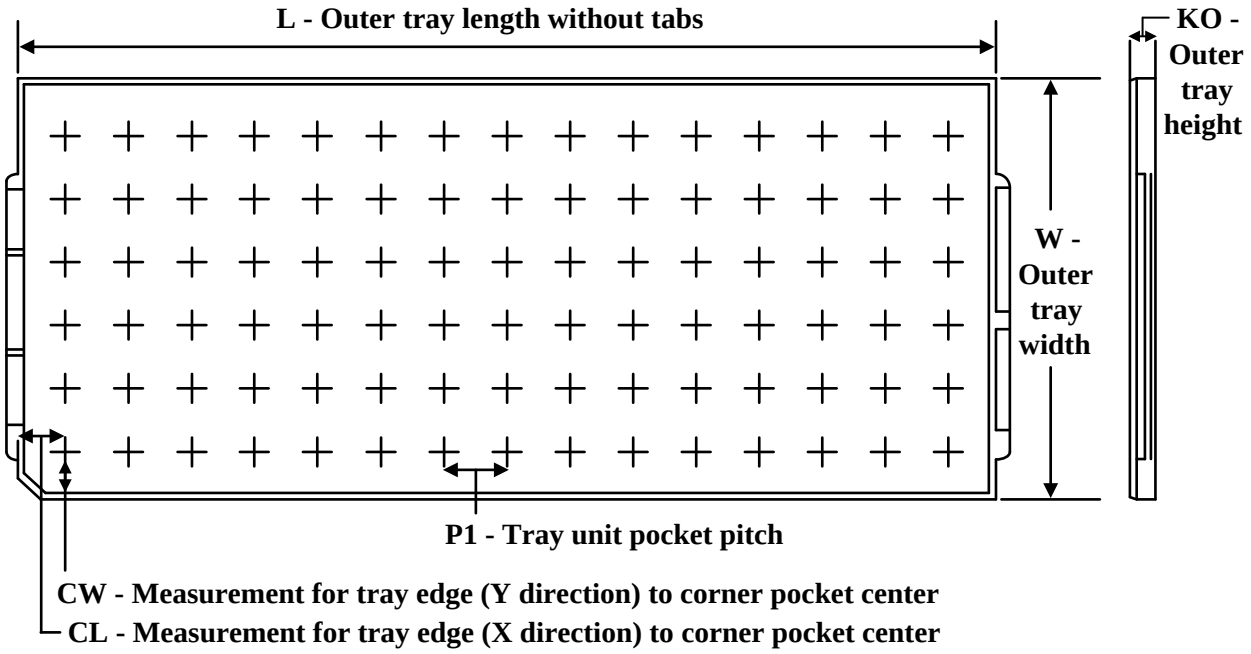
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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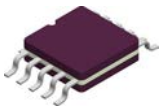
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-0620601VZA	NAC	CFP	10	1	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LMP2012WG-QMLV	NAC	CFP	10	1	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LMP2012WG-QMLV.A	NAC	CFP	10	1	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08

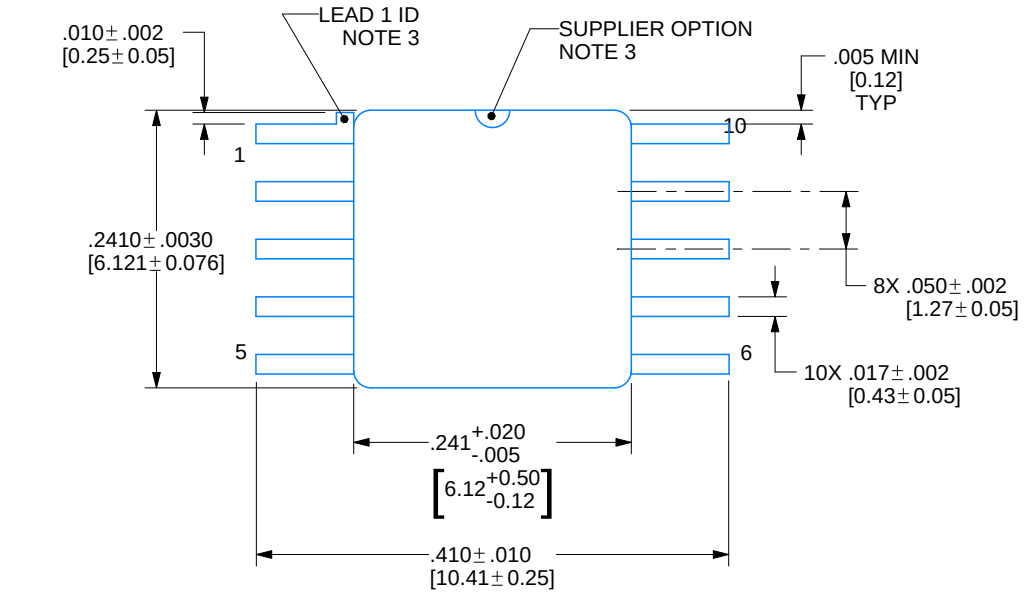


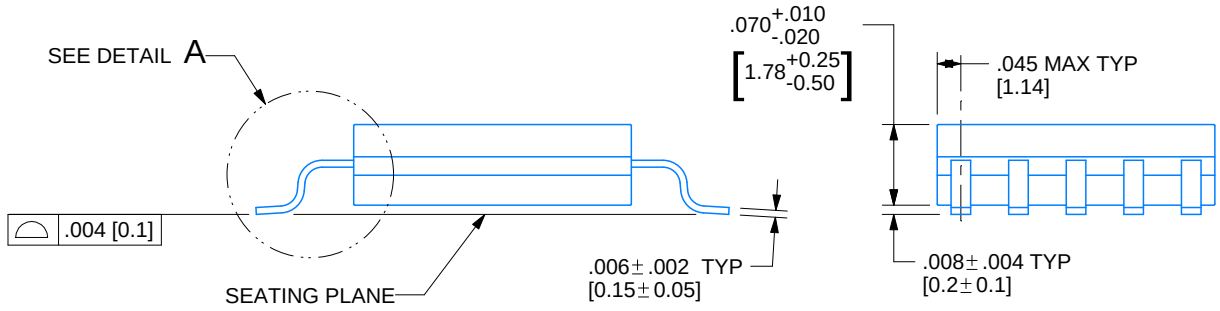
PACKAGE OUTLINE

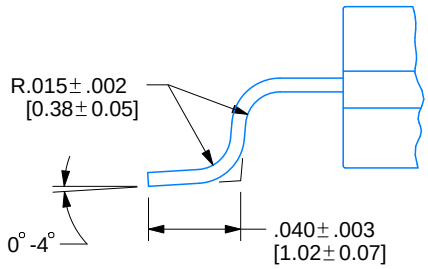
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK







DETAIL A
TYPICAL

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NOTES:

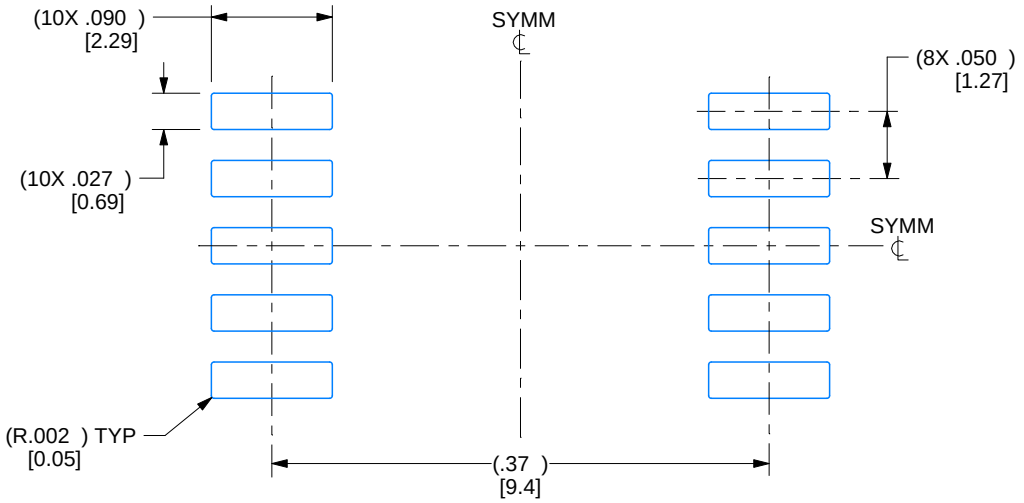
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

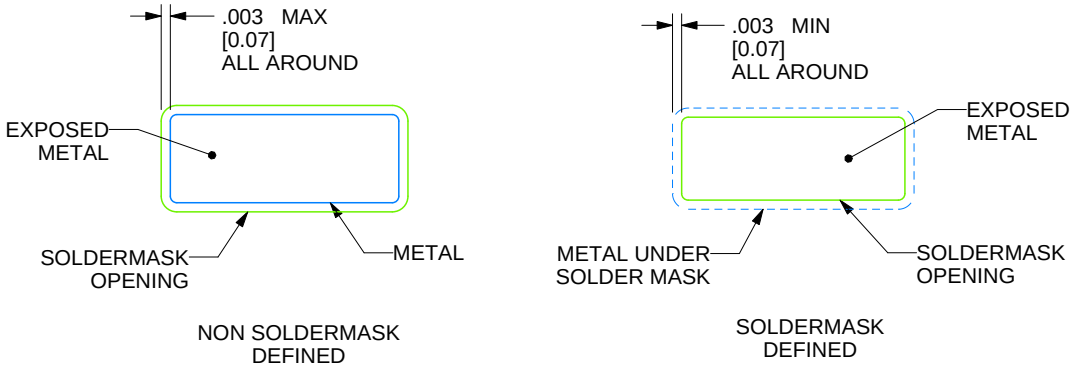
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



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REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197877	12/30/2021	DAVID CHIN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198820	02/14/2022	K. SINCERBOX
C	CHANGE PIN 1 ID LOCATION ON PIN	2198845	02/18/2022	D. CHIN / K. SINCERBOX
D	.2410± .0030 WAS .2700 +.0012/-.0002;	2200915	08/08/2022	D. CHIN / K. SINCERBOX

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