LMP2011 Single/LMP2012 Dual High Precision, Rail-to-Rail Output Operational Amplifier

1 Features

(For V_S = 5 V, Typical Unless Otherwise Noted)

- Low Ensured V_{OS} Over Temperature 60 µV
- Low Noise with No 1/f 35nV/√Hz
- High CMRR 130 dB
- High PSRR 120 dB
- High A_{VOL} 130 dB
- Wide Gain-Bandwidth Product 3 MHz
- High Slew Rate 4 V/µs
- Low Supply Current 930 µA
- Rail-to-Rail Output 30 mV
- No External Capacitors Required

2 Applications

- Precision Instrumentation Amplifiers
- Thermocouple Amplifiers
- Strain Gauge Bridge Amplifier

3 Description

The LMP201x series are the first members of TI's new LMP™ precision amplifier family. The LMP201x series offers unprecedented accuracy and stability in space-saving miniature packaging, offered at an affordable price. This device utilizes patented auto-zero techniques to measure and continually correct the input offset error voltage. The result is an amplifier which is ultra-stable over time and temperature. It has excellent CMRR and PSRR ratings, and does not exhibit the familiar 1/f voltage and current noise increase that plagues traditional amplifiers. The combination of the LMP201x characteristics makes it a good choice for transducer amplifiers, high gain configurations, ADC buffer amplifiers, DAC I-V conversion, and any other 2.7-V to 5-V application requiring precision and long term stability.

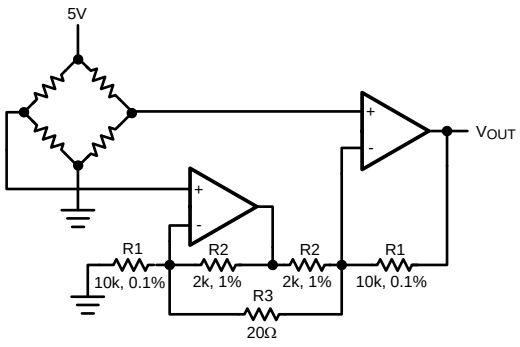
Other useful benefits of the LMP201x are rail-to-rail output, a low supply current of 930 µA, and wide gain-bandwidth product of 3 MHz. These versatile features found in the LMP201x provide high performance and ease of use.

Device Information(1)

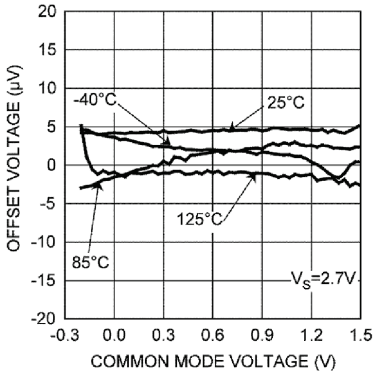
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP2011	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
LMP2012	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Bridge Amplifier



Offset Voltage vs Common Mode Voltage



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (March 2013) to Revision L **Page**

- Added *Pin Configuration and Functions* section, *Storage Conditions* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

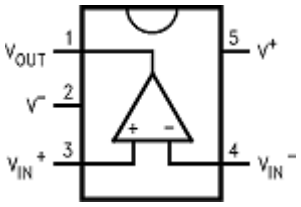
Changes from Revision J (March 2013) to Revision K **Page**

- Changed layout of National Data Sheet to TI format ... 19

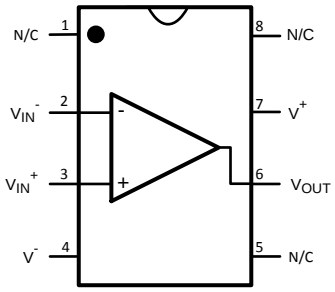
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5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23 Single
Top View



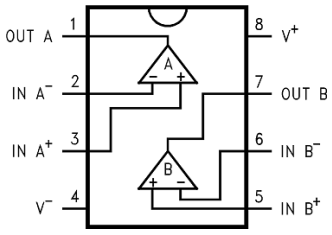
D Package
8-Pin Single SOIC
Top View



Pin Functions: LMP2011

PIN			I/O	DESCRIPTION
NAME	NO.			
	DBV	D		
-IN	4	3	O	Inverting input
+IN	3	2	I	Non-Inverting input
N/C	-	1	-	No Internal Connection
N/C	-	5	-	No Internal Connection
N/C	-	8	-	No Internal Connection
OUT	1	6	I	Output
V-	2	4	P	Negative (lowest) power supply
V+	5	7	P	Positive (highest) power supply

D or DGK Package
8-Pin Dual SOIC and VSSOP
Top View



Pin Functions: LMP2012

PIN		I/O	DESCRIPTION
NAME	NO.		
	D, DGK		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Non-Inverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Non-Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	P	Negative (lowest) power supply
V+	8	P	Positive (highest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

	MIN	MAX	UNIT
Supply Voltage		5.8	V
Common-Mode Input Voltage	(V^-) - 0.3	(V^+) + 0.3	V
Lead Temperature (soldering 10 sec.)		300	°C
Differential Input Voltage	±Supply Voltage		
Current at Input Pin	30	30	mA
Current at Output Pin	30	30	mA
Current at Power Supply Pin	50	30	mA
Storage Temperature	−65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage	2.7	5.25	V
Operating Temperature Range	−40	125	°C

6.4 Thermal Information: LMP2011

THERMAL METRIC (1)		LMP2011		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119	164	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66	116	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60	28	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17	13	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59	27	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Thermal Information: LMP2012

THERMAL METRIC[1]		LMP2012		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	157	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	51	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52	77	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8	5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51	75	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 2.7-V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.35 V, V_O = 1.35 V, and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN[1]	TYP[2]	MAX[1]	UNIT
V_{OS}	Input Offset Voltage (LMP2011 only)	T_J = 25°C			0.8	25	µV
		The temperature extremes				60	
	Input Offset Voltage (LMP2012 only)	T_J = 25°C			0.8	36	
		The temperature extremes				60	
	Offset Calibration Time	T_J = 25°C			0.5	10	ms
		The temperature extremes				12	
TCV_{OS}	Input Offset Voltage				0.015		µV/°C
	Long-Term Offset Drift				0.006		µV/month
	Lifetime V_{OS} Drift				2.5		µV
I_{IN}	Input Current				-3		pA
I_{OS}	Input Offset Current				6		pA
R_{IND}	Input Differential Resistance				9		MΩ
CMRR	Common Mode Rejection Ratio	−0.3 ≤ V_{CM} ≤ 0.9 V, 0 ≤ V_{CM} ≤ 0.9 V	T_J = 25°C	95	130		dB
			The temperature extremes	90			
PSRR	Power Supply Rejection Ratio	T_J = 25°C		95	120		dB
		The temperature extremes		90			
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ	T_J = 25°C	95	130		dB
			The temperature extremes	90			
		R_L = 2 kΩ	T_J = 25°C	90	124		
			The temperature extremes	85			

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm.

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2.7-V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.35 V, V_O = 1.35 V, and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_O	Output Swing (LMP2011 only)	R_L = 10 kΩ to 1.35 V, V_{IN}(diff) = ±0.5 V	T_J = 25°C	2.665	2.68		V
			The temperature extremes	2.655			
			T_J = 25°C		0.033	0.060	
			The temperature extremes			0.075	
		R_L = 2 kΩ to 1.35 V, V_{IN}(diff) = ±0.5 V	T_J = 25°C	2.630	2.65		V
			The temperature extremes	2.615			
			T_J = 25°C		0.061	0.085	
			The temperature extremes			0.105	
	Output Swing (LMP2012 only)	R_L = 10 kΩ to 1.35 V, V_{IN}(diff) = ±0.5 V	T_J = 25°C	2.64	2.68		V
			The temperature extremes	2.63			
			T_J = 25°C		0.033	0.060	
			The temperature extremes			0.075	
		R_L = 2 kΩ to 1.35 V, V_{IN}(diff) = ±0.5 V	T_J = 25°C	2.615	2.65		V
			The temperature extremes	2.6			
			T_J = 25°C		0.061	0.085	
			The temperature extremes			0.105	
I_O	Output Current	Sourcing, V_O = 0 V, V_{IN}(diff) = ±0.5 V	T_J = 25°C	5	12		mA
			The temperature extremes	3			
		V_{IN}(diff) = ±0.5 V, Sinking, V_O = 5 V	T_J = 25°C	5	18		
			The temperature extremes	3			
I_S	Supply Current per Channel	T_J = 25°C			0.919	1.20	mA
		The temperature extremes				1.50	

6.7 2.7-V AC Electrical Characteristics

T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.35 V, V_O = 1.35 V, and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
GBW	Gain-Bandwidth Product			3		MHz
SR	Slew Rate			4		V/µs
θ_m	Phase Margin			60		Deg
G_m	Gain Margin			−14		dB
e_n	Input-Referred Voltage Noise			35		nV/√Hz
e_np-p	Input-Referred Voltage Noise	R_S = 100 Ω, DC to 10 Hz		850		nV_{pp}
t_{rec}	Input Overload Recovery Time			50		ms

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm.

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6.8 5-V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2.5 V, V_O = 2.5 V, and R_L > 1MΩ.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage (LMP2011 only)	T_J = 25°C			0.12	25	µV
		The temperature extremes				60	
	Input Offset Voltage (LMP2012 only)	T_J = 25°C			0.12	36	
		The temperature extremes				60	
	Offset Calibration Time	T_J = 25°C			0.5	10	ms
		The temperature extremes				12	
TCV_{OS}	Input Offset Voltage				0.015		µV/°C
	Long-Term Offset Drift				0.006		µV/month
	Lifetime V_{OS} Drift				2.5		µV
I_{IN}	Input Current				-3		pA
I_{OS}	Input Offset Current				6		pA
R_{IND}	Input Differential Resistance				9		MΩ
CMRR	Common Mode Rejection Ratio	−0.3 ≤ V_{CM} ≤ 3.2, 0 ≤ V_{CM} ≤ 3.2	T_J = 25°C	100	130		dB
			The temperature extremes	90			
PSRR	Power Supply Rejection Ratio	T_J = 25°C		95	120		dB
		The temperature extremes		90			
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ	T_J = 25°C	105	130		dB
			The temperature extremes	100			
		R_L = 2 kΩ	T_J = 25°C	95	132		
			The temperature extremes	90			
V_O	Output Swing (LMP2011 only)	R_L = 10 kΩ to 2.5 V, V_{IN}(diff) = ±0.5 V	T_J = 25°C	4.96	4.978		V
			The temperature extremes	4.95			
			T_J = 25°C		0.040	0.070	
			The temperature extremes			0.085	
		R_L = 2 kΩ to 2.5 V, V_{IN}(diff) = ±0.5 V	T_J = 25°C	4.895	4.919		V
			The temperature extremes	4.875			
			T_J = 25°C		0.091	0.115	
			The temperature extremes			0.140	
	Output Swing (LMP2012 only)	R_L = 10 kΩ to 2.5 V, V_{IN}(diff) = ±0.5 V	T_J = 25°C	4.92	4.978		V
			The temperature extremes	4.91			
			T_J = 25°C		0.040	0.080	
			The temperature extremes			0.095	
		R_L = 2 kΩ to 2.5 V, V_{IN}(diff) = ±0.5 V	T_J = 25°C	4.875	4.919		V
			The temperature extremes	4.855			
			T_J = 25°C		0.0.91	0.125	
			The temperature extremes			0.150	
I_O	Output Current	Sourcing, V_O = 0 V, V_{IN}(diff) = ±0.5 V	T_J = 25°C	8	15		mA
			The temperature extremes	6			
		Sinking, V_O = 5 V, V_{IN}(diff) = ±0.5 V	T_J = 25°C	8	17		
			The temperature extremes	6			
I_S	Supply Current per Channel	T_J = 25°C			0.930	1.20	mA
		The temperature extremes				1.50	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm.

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6.9 5-V AC Electrical Characteristics

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2.5 V, V_O = 2.5 V, and R_L > 1MΩ.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
GBW	Gain-Bandwidth Product			3		MHz
SR	Slew Rate			4		V/μs
θ_m	Phase Margin			60		deg
G_m	Gain Margin			−15		dB
e_n	Input-Referred Voltage Noise			35		nV/√Hz
e_np-p	Input-Referred Voltage Noise	R_S = 100 Ω, DC to 10 Hz		850		nV_{pp}
t_{rec}	Input Overload Recovery Time			50		ms

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm.

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6.10 Typical Characteristics

T_A=25C, V_S= 5 V unless otherwise specified.

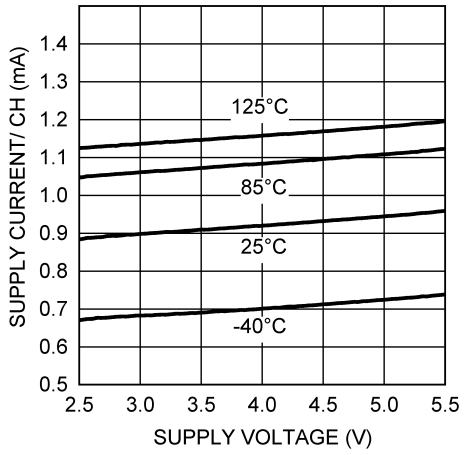


Figure 1. Supply Current vs Supply Voltage

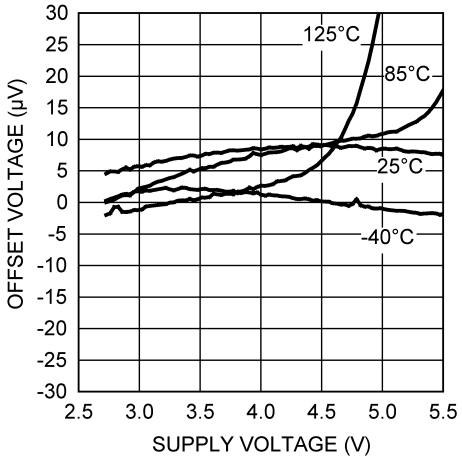


Figure 2. Offset Voltage vs Supply Voltage

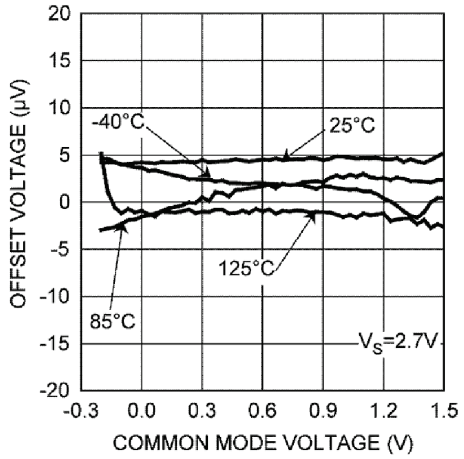


Figure 3. Offset Voltage vs Common Mode

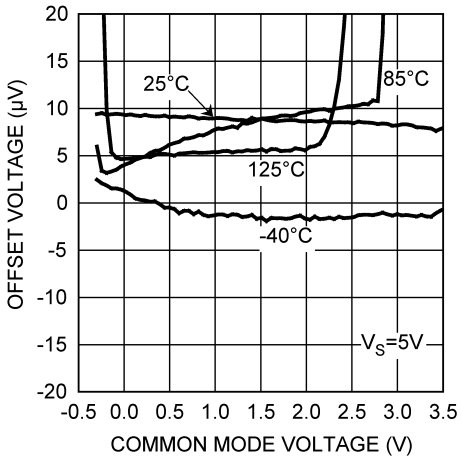


Figure 4. Offset Voltage vs Common Mode

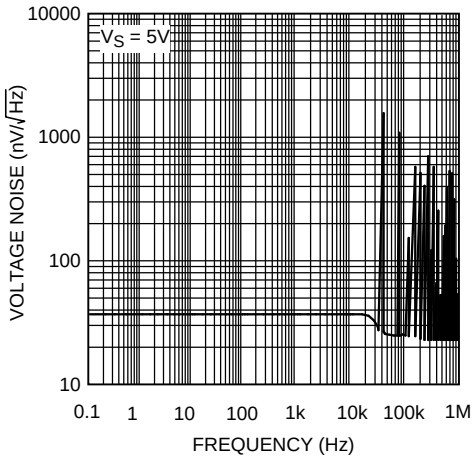


Figure 5. Voltage Noise vs Frequency

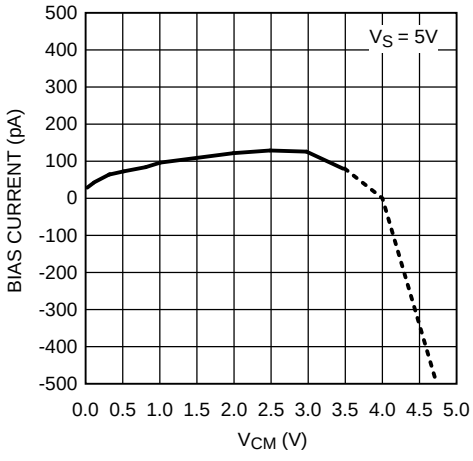


Figure 6. Input Bias Current vs Common Mode

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Typical Characteristics (continued)

T_A=25C, V_S= 5 V unless otherwise specified.

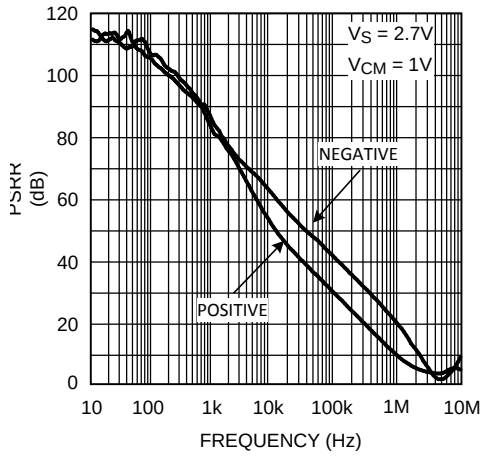


Figure 7. PSRR vs Frequency

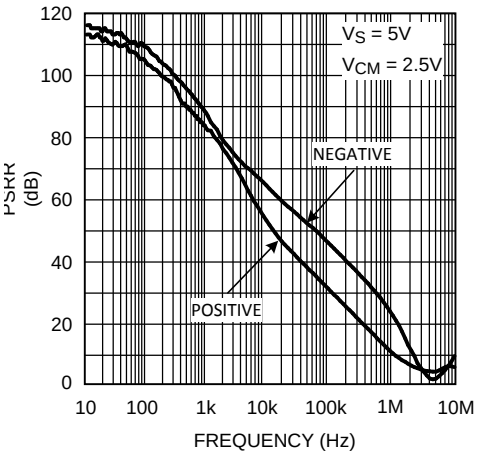


Figure 8. PSRR vs Frequency

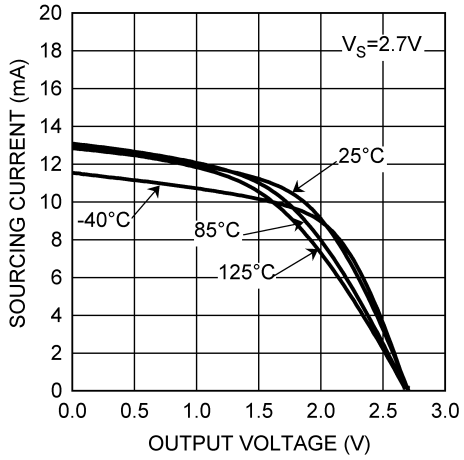


Figure 9. Output Sourcing at 2.7 V

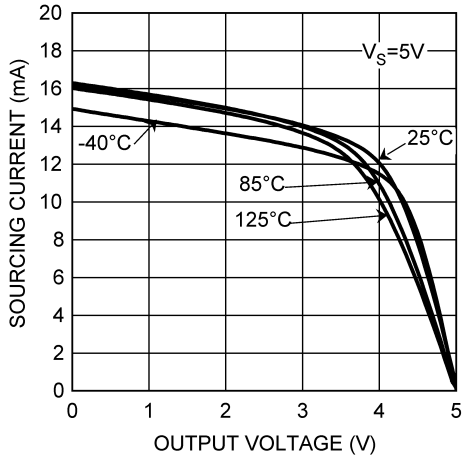


Figure 10. Output Sourcing at 5 V

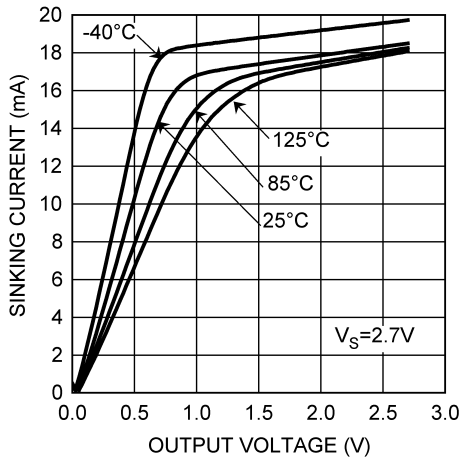


Figure 11. Output Sinking at 2.7 V

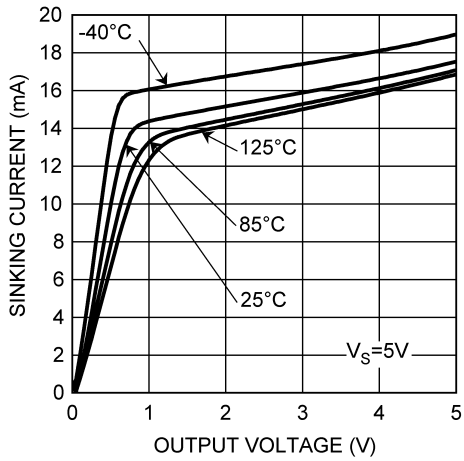


Figure 12. Output Sinking at 5 V

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Typical Characteristics (continued)

T_A=25C, V_S= 5 V unless otherwise specified.

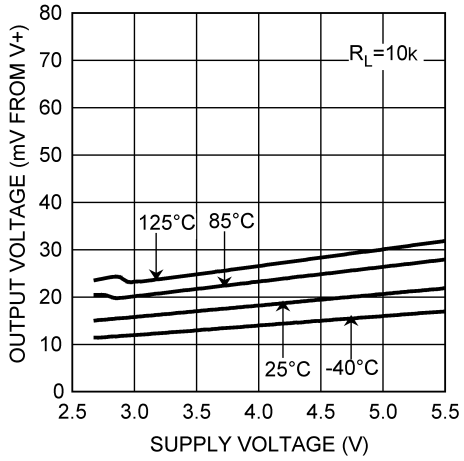


Figure 13. Maximum Output Swing vs Supply Voltage

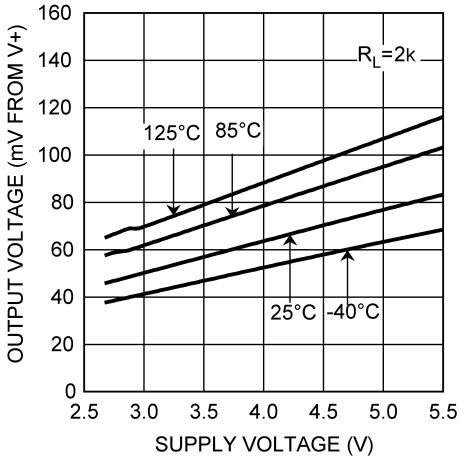


Figure 14. Maximum Output Swing vs Supply Voltage

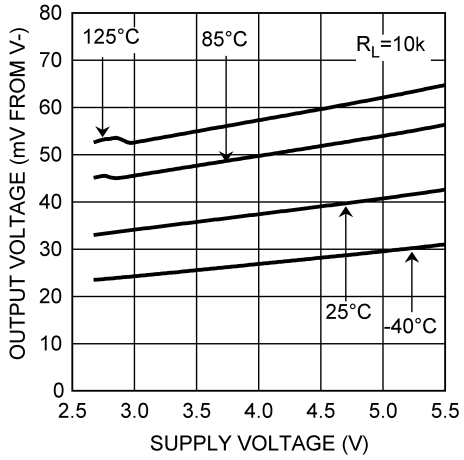


Figure 15. Minimum Output Swing vs Supply Voltage

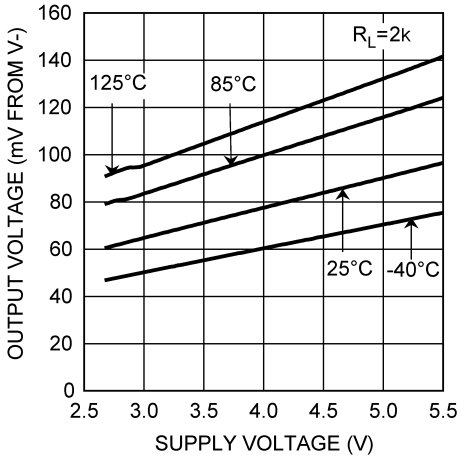


Figure 16. Minimum Output Swing vs Supply Voltage

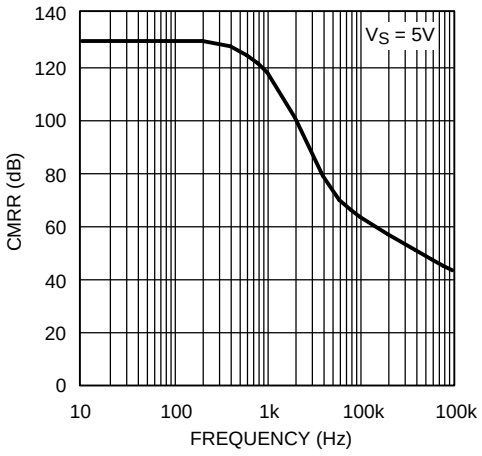


Figure 17. CMRR vs Frequency

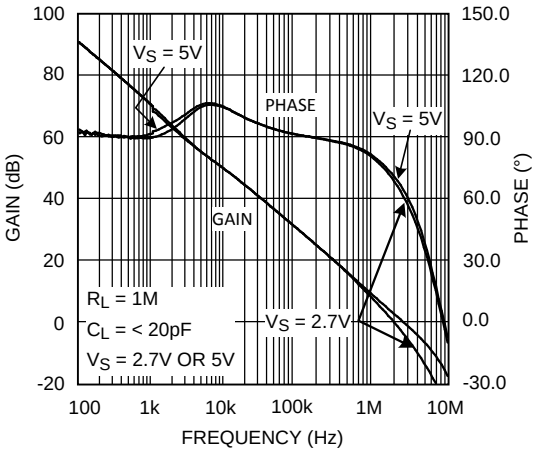


Figure 18. Open Loop Gain and Phase vs Supply Voltage

Typical Characteristics (continued)

T_A=25C, V_S= 5 V unless otherwise specified.

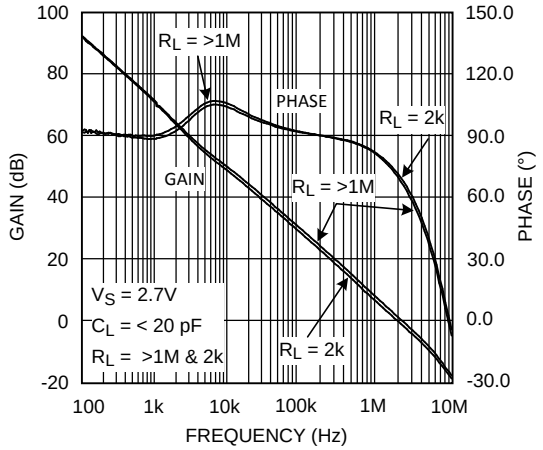


Figure 19. Open Loop Gain and Phase vs R_L at 2.7 V

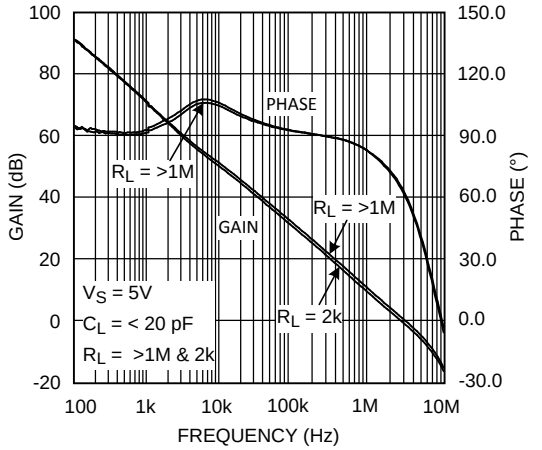


Figure 20. Open Loop Gain and Phase vs R_L at 5 V

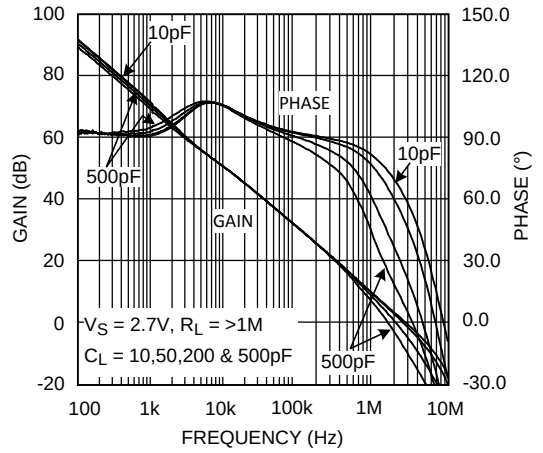


Figure 21. Open Loop Gain and Phase vs C_L at 2.7 V

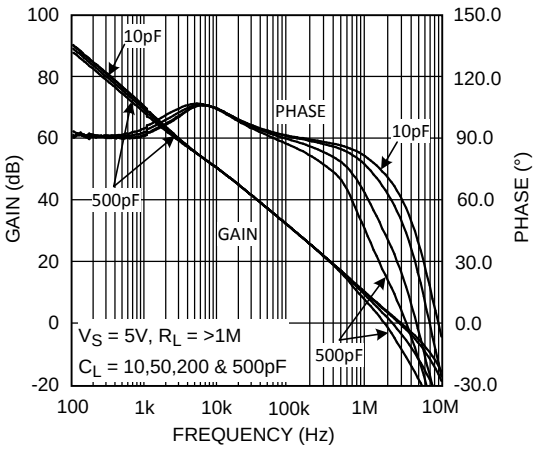


Figure 22. Open Loop Gain and Phase vs C_L at 5 V

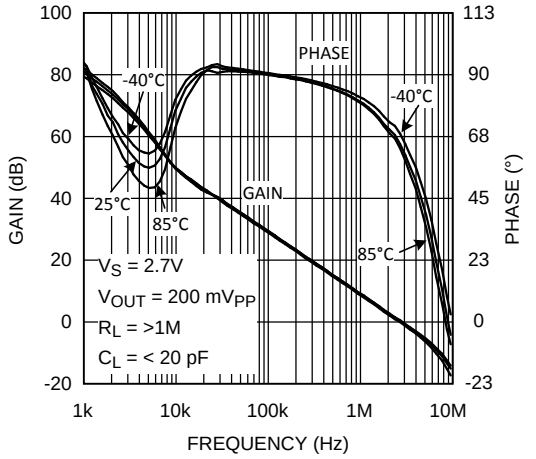


Figure 23. Open Loop Gain and Phase vs Temperature at 2.7 V

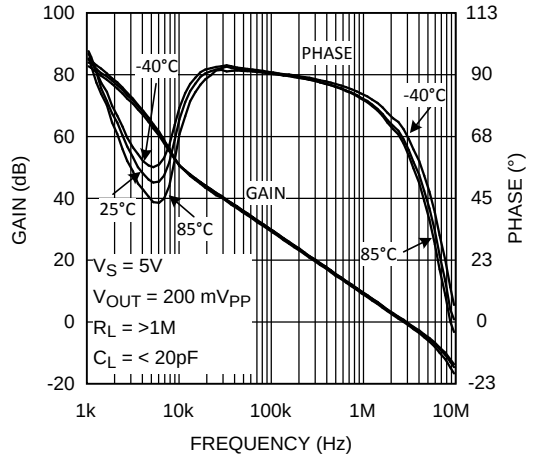


Figure 24. Open Loop Gain and Phase vs Temperature at 5 V

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Typical Characteristics (continued)

T_A=25C, V_S= 5 V unless otherwise specified.

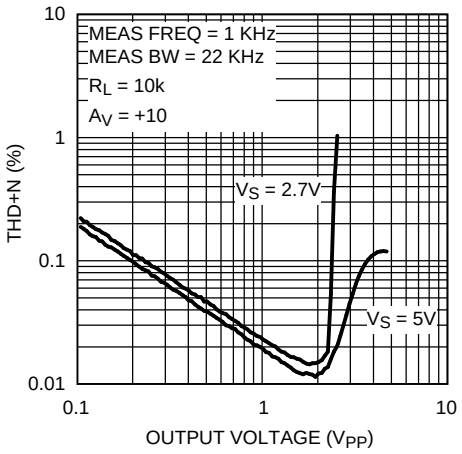


Figure 25. THD+N vs AMPL

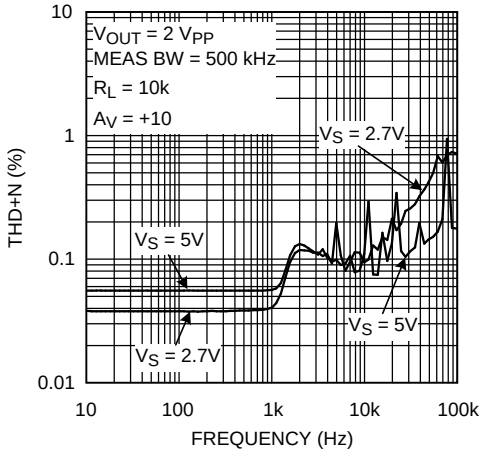


Figure 26. THD+N vs Frequency

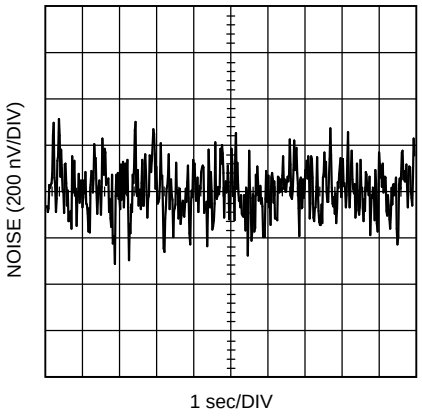


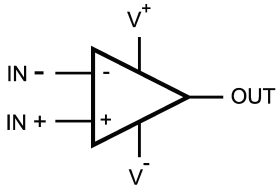
Figure 27. 0.1 Hz − 10 Hz Noise vs Time

7 Detailed Description

7.1 Overview

The LMP201x series offers unprecedented accuracy and stability in space-saving miniature packaging while also being offered at an affordable price. This device utilizes patented techniques to measure and continually correct the input offset error voltage. The result is an amplifier which is ultra stable over time and temperature.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 How the LMP201x Works

The LMP201x uses new, patented auto-zero techniques to achieve the high DC accuracy traditionally associated with chopper-stabilized amplifiers without the major drawbacks produced by chopping. The LMP201x continuously monitors the input offset and corrects this error.

The conventional low-frequency chopping process produces many mixing products, both sums and differences, between the chopping frequency and the incoming signal frequency. This mixing causes large amounts of distortion, particularly when the signal frequency approaches the chopping frequency. Even without an incoming signal, the chopper harmonics mix with each other to produce even more trash. If this sounds unlikely or difficult to understand, look at the plot (Figure 28), of the output of a typical (MAX432) chopper-stabilized op amp. This is the output when there is no incoming signal, just the amplifier in a gain of -10 with the input grounded. The chopper is operating at about 150 Hz; the rest is mixing products. Add an input signal and the noise gets much worse.

Compare this plot with Figure 29 of the LMP201x. This data was taken under the exact same conditions. The auto-zero action is visible at about 30 kHz but note the absence of mixing products at other frequencies. As a result, the LMP201x has very low distortion of 0.02% and very low mixing products.

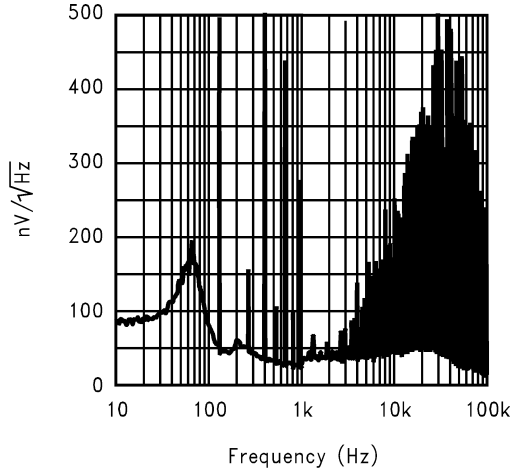


Figure 28. The Output of a Chopper Stabilized Op Amp (MAX432)

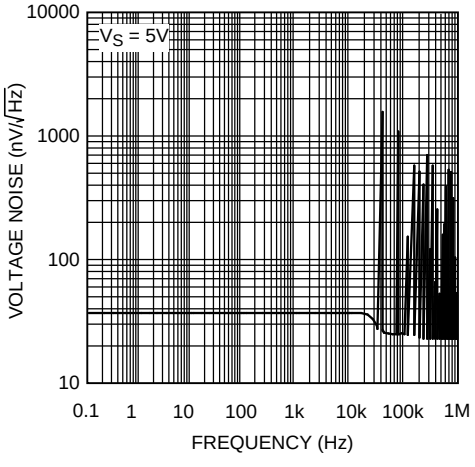


Figure 29. The Output of the LMP2011/LMP2012

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Feature Description (continued)

7.3.2 The Benefits of LMP201x: No 1/F Noise

Using patented methods, the LMP201x eliminates the 1/f noise present in other amplifiers. This noise, which increases as frequency decreases, is a major source of measurement error in all DC-coupled measurements. Low-frequency noise appears as a constantly-changing signal in series with any measurement being made. As a result, even when the measurement is made rapidly, this constantly-changing noise signal will corrupt the result.

The value of this noise signal can be surprisingly large. For example: If a conventional amplifier has a flat-band noise level of 10 nV/√Hz and a noise corner of 10 Hz, the RMS noise at 0.001 Hz is 1 µV/√Hz. This is equivalent to a 0.50-µV peak-to-peak error, in the frequency range 0.001 Hz to 1.0 Hz. In a circuit with a gain of 1000, this produces a 0.50-mV peak-to-peak output error. This number of 0.001 Hz might appear unreasonably low, but when a data acquisition system is operating for 17 minutes, it has been on long enough to include this error. In this same time, the LMP201x will only have a 0.21-mV output error. This is smaller by 2.4×. This 1/f error gets even larger at lower frequencies. At the extreme, many people try to reduce this error by integrating or taking several samples of the same signal. This is also doomed to failure because the 1/f nature of this noise means that taking longer samples just moves the measurement into lower frequencies where the noise level is even higher.

The LMP201x eliminates this source of error. The noise level is constant with frequency so that reducing the bandwidth reduces the errors caused by noise.

7.3.3 No External Capacitors Required

The LMP201x does not need external capacitors. This eliminates the problems caused by capacitor leakage and dielectric absorption, which can cause delays of several seconds from turn-on until the amplifier's error has settled.

7.3.4 Copper Leadframe

Another source of error that is rarely mentioned is the error voltage caused by the inadvertent thermocouples created when the common *Kovar type* IC package lead materials are soldered to a copper printed circuit board. These steel-based leadframe materials can produce over 35 µV/°C when soldered onto a copper trace. This can result in thermocouple noise that is equal to the LMP201x noise when there is a temperature difference of only 0.0014°C between the lead and the board!

For this reason, the lead-frame of the LMP201x is made of copper. This results in equal and opposite junctions which cancel this effect. The extremely small size of the SOT-23 package results in the leads being very close together. This further reduces the probability of temperature differences and hence decreases thermal noise.

7.3.5 More Benefits

The LMP201x offers the benefits mentioned above and more. It has a rail-to-rail output and consumes only 950 µA of supply current while providing excellent DC and AC electrical performance. In DC performance, the LMP201x achieves 130 dB of CMRR, 120 dB of PSRR, and 130 dB of open loop gain. In AC performance, the LMP201x provides 3 MHz of gain-bandwidth product and 4 V/µs of slew rate.

7.4 Device Functional Modes

7.4.1 Input Currents

The LMP201x input currents are different than standard bipolar or CMOS input currents. Due to the auto-zero action of the input stage, the input current appears as a pulsating current at the chopping frequency (35 kHz) flowing in one input and out the other. Under most operating conditions, these currents are in the picoamp level and will have little or no effect in most circuits.

These currents tend to increase slightly when the common-mode voltage is near the minus supply. (See the *Typical Characteristics*.) At high temperatures such as 85°C, the input currents become larger, 0.5 nA typical, and are both positive except when the V_{CM} is near V^-. If operation is expected at low common-mode voltages and high temperature, do not add resistance in series with the inputs to balance the impedances. Doing this can cause an increase in offset voltage. A small resistance such as 1 kΩ can provide some protection against very large transients or overloads, and will not increase the offset significantly.

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Device Functional Modes (continued)

Because of these issues, the LMV201x is not recommended for source impedances over 1MΩ.

7.4.2 Overload Recovery

The LMP201x recovers from input overload much faster than most chopper-stabilized op amps. Recovery from driving the amplifier to 2X the full scale output, only requires about 40 ms. Many chopper-stabilized amplifiers will take from 250 ms to several seconds to recover from this same overload. This is because large capacitors are used to store the unadjusted offset voltage.

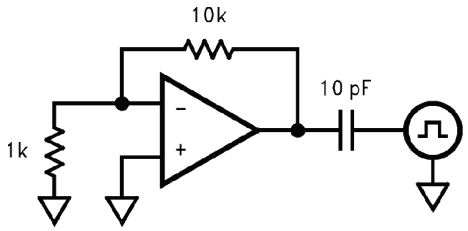


Figure 30. Overload Recovery Test Circuit

The wide bandwidth of the LMP201x enhances performance when it is used as an amplifier to drive loads that inject transients back into the output. ADCs (Analog-to-Digital Converters) and multiplexers are examples of this type of load. To simulate this type of load, a pulse generator producing a 1-V peak square wave was connected to the output through a 10-pF capacitor. (Figure 30) The typical time for the output to recover to 1% of the applied pulse is 80 ns. To recover to 0.1% requires 860 ns. This rapid recovery is due to the wide bandwidth of the output stage and large total GBW.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV201x family offers excellent dc precision and ac performance. These devices offer true rail-to-rail output, ultralow offset voltage and offset voltage drift over the entire –40 to 125°C temperature range, as well as 3-MHz bandwidth and no 1/f noise. These features make the LMV201x a robust, high performance operational amplifier ideal for industrial applications.

8.2 Typical Applications

8.2.1 Extending Supply Voltages and Output Swing with a Composite Amplifier

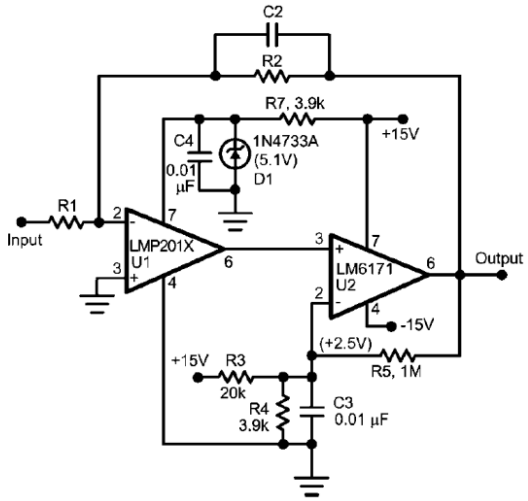


Figure 31. Inverting Composite Amplifier

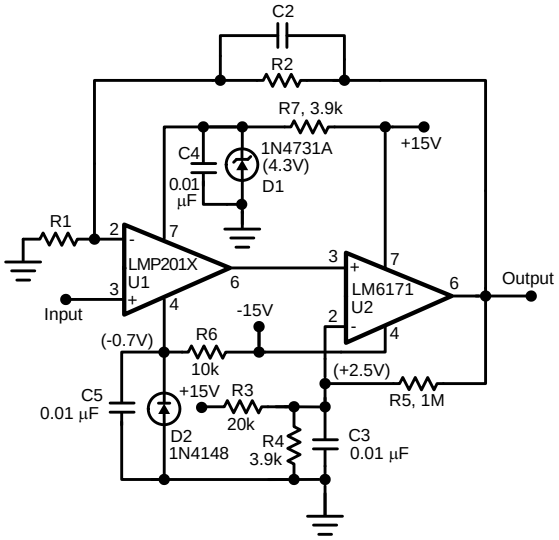


Figure 32. Non-Inverting Composite Amplifier

8.2.1.1 Design Requirements

In cases where substantially higher output swing is required with higher supply voltages, arrangements like the ones shown in Figure 31 and Figure 32 could be used. These configurations utilize the excellent DC performance of the LMP201x while at the same time allow the superior voltage and frequency capabilities of the LM6171 to set the dynamic performance of the overall amplifier.

For example, it is possible to achieve ±12-V output swing with 300 MHz of overall GBW (A_V = 100) while keeping the worst case output shift due to V_{OS} less than 4 mV.

8.2.1.2 Detailed Design Procedure

The LMP201x output voltage is kept at about mid-point of its overall supply voltage, and its input common mode voltage range allows the V- terminal to be grounded in one case (Figure 31, inverting operation) and tied to a small non-critical negative bias in another (Figure 32, non-inverting operation). Higher closed-loop gains are also possible with a corresponding reduction in realizable bandwidth. Table 1 shows some other closed loop gain possibilities along with the measured performance in each case.

In terms of the measured output peak-to-peak noise, the following relationship holds between output noise voltage, e_n p-p, for different closed-loop gain, A_V, settings, where −3 dB Bandwidth is BW:

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Typical Applications (continued)

$$\frac{e_{npp1}}{e_{npp2}} = \sqrt{\frac{BW1}{BW2}} \bullet \frac{A_V 1}{A_V 2} \quad (1)$$

It should be kept in mind that in order to minimize the output noise voltage for a given closed-loop gain setting, one could minimize the overall bandwidth. As can be seen from Equation 1 above, the output noise has a square-root relationship to the Bandwidth.

In the case of the inverting configuration, it is also possible to increase the input impedance of the overall amplifier, by raising the value of R1, without having to increase the feed-back resistor, R2, to impractical values, by utilizing a "Tee" network as feedback. See the LMC6442 data sheet (Application Notes section) for more details on this.

8.2.1.3 Application Results

Table 1 shows the results using various gains and compensation values.

Table 1. Composite Amplifier Measured Performance

A_V	R1 (Ω)	R2 (Ω)	C2 (pF)	BW (MHz)	SR (V/µs)	en p-p (mV_{PP})
50	200	10k	8	3.3	178	37
100	100	10k	10	2.5	174	70
100	1k	100k	0.67	3.1	170	70
500	200	100k	1.75	1.4	96	250
1000	100	100k	2.2	0.98	64	400

8.2.2 Precision Strain-gauge Amplifier

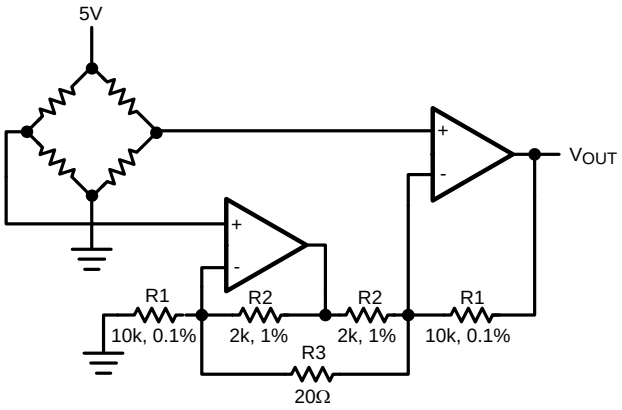


Figure 33. Precision Strain Gauge Amplifier

This Strain-Gauge amplifier (Figure 33) provides high gain (1006 or ~60 dB) with very low offset and drift. Using the resistors' tolerances as shown, the worst case CMRR will be greater than 108 dB. The CMRR is directly related to the resistor mismatch. The rejection of common-mode error, at the output, is independent of the differential gain, which is set by R3. The CMRR is further improved, if the resistor ratio matching is improved, by specifying tighter-tolerance resistors, or by trimming.

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8.2.3 ADC Input Amplifier

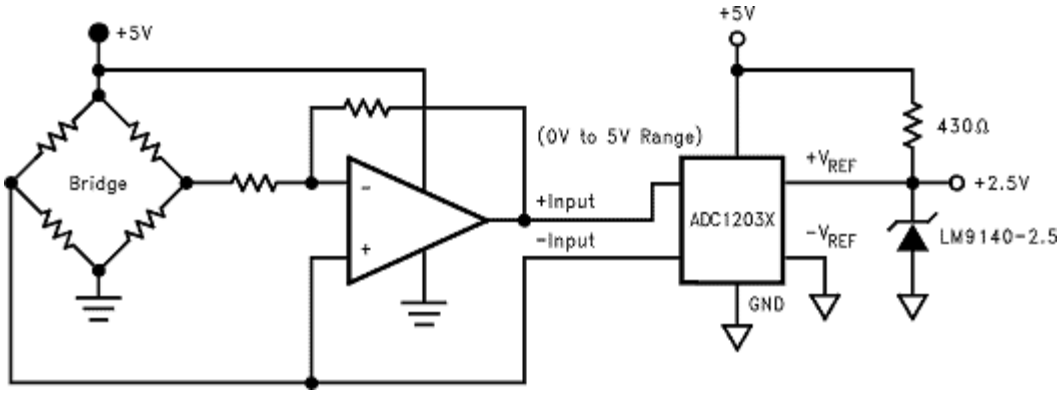


Figure 34. DC Coupled ADC Driver

The LMP201x is a great choice for an amplifier stage immediately before the input of an ADC (Analog-to-Digital Converter). See Figure 34.

This is because of the following important characteristics:

- Very low offset voltage and offset voltage drift over time and temperature allow a high closed-loop gain setting without introducing any short-term or long-term errors. For example, when set to a closed-loop gain of 100 as the analog input amplifier for a 12-bit A/D converter, the overall conversion error over full operation temperature and 30 years life of the part (operating at 50°C) would be less than 5 LSBs.
- Fast large-signal settling time to 0.01% of final value (1.4 µs) allows 12 bit accuracy at 100 KH_Z or more sampling rate
- No flicker (1/f) noise means unsurpassed data accuracy over any measurement period of time, no matter how long. Consider the following op amp performance, based on a typical low-noise, high-performance commercially-available device, for comparison:
  - Op amp flatband noise = 8 nV/$\sqrt{Hz}$
  - 1/f corner frequency = 100 Hz
  - A_V = 2000
  - Measurement time = 100 sec
  - Bandwidth = 2 Hz
- This example will result in about 2.2 mV_{PP} (1.9 LSB) of output noise contribution due to the op amp alone, compared to about 594 μV_{PP} (less than 0.5 LSB) when that op amp is replaced with the LMP201x which has no 1/f contribution. If the measurement time is increased from 100 seconds to 1 hour, the improvement realized by using the LMP201x would be a factor of about 4.8 times (2.86 mV_{PP} compared to 596 µV when LMP201x is used) mainly because the LMP201x accuracy is not compromised by increasing the observation time.
- Copper leadframe construction minimizes any thermocouple effects which would degrade low level/high gain data conversion application accuracy (see discussion under The Benefits of the LMP201X section above).
- Rail-to-Rail output swing maximizes the ADC dynamic range in 5-Volt single-supply converter applications. Below is a typical block diagram showing the LMP201x used as an ADC amplifier (Figure 34).

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9 Power Supply Recommendations

The LMP201x is specified for operation from 2.7 V to 5.25 V (±1.35 V to ±2.625 V) over a –40°C to +125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the op amp power supply pins. For single supply, place a capacitor between V+ and V− supply leads. For dual supplies, place one capacitor between V+ and ground, and one capacitor between V- and ground.

CAUTION

Supply voltages larger than 6 V can permanently damage the device.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to SLOA089, *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in *Layout Example*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

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10.2 Layout Example

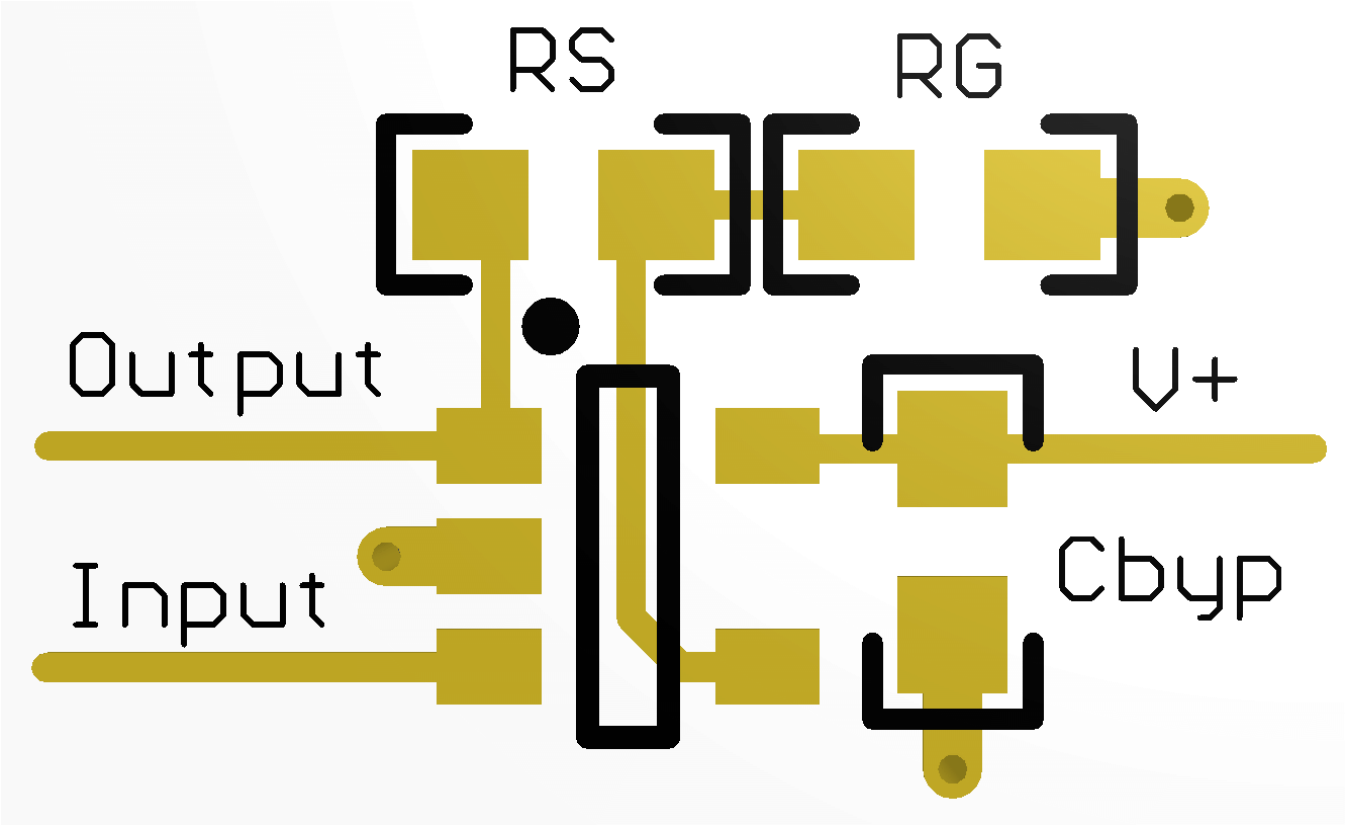


Figure 35. Single Non-Inverting Amplifier Example Layout

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LMP2011/12 PSPICE Model, SNOM113

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

TI Filterpro Software, http://www.ti.com/tool/filterpro

DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm

TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

Manual for LMH730268 Evaluation board 551012922-001

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- SBOA015 (AB-028), *Feedback Plots Define Op Amp AC Performance*
- SLOA089, *Circuit Board Layout Techniques*
- SLOD006, *Op Amps for Everyone*
- TIPD128, *Capacitive Load Drive Solution using an Isolation Resistor*
- SBOA092, *Handbook of Operational Amplifier Applications*

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMP2011	Click here	Click here	Click here	Click here	Click here
LMP2012	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

LMP, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMP2011MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP20 11MA
LMP2011MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP20 11MA
LMP2011MF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AN1A
LMP2011MF/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AN1A
LMP2011MFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AN1A
LMP2011MFX/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AN1A
LMP2012MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP20 12MA
LMP2012MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP20 12MA
LMP2012MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP20 12MA
LMP2012MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMP20 12MA
LMP2012MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AP1A
LMP2012MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AP1A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

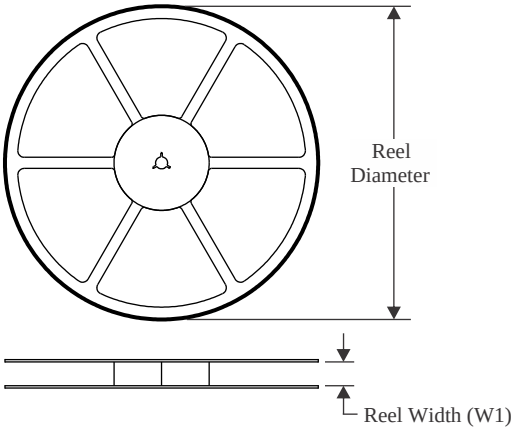
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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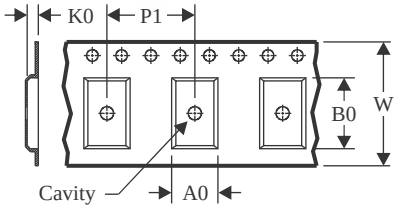
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

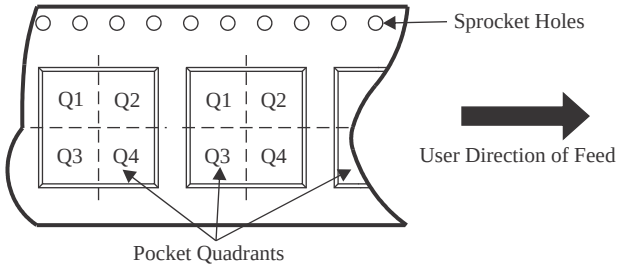


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

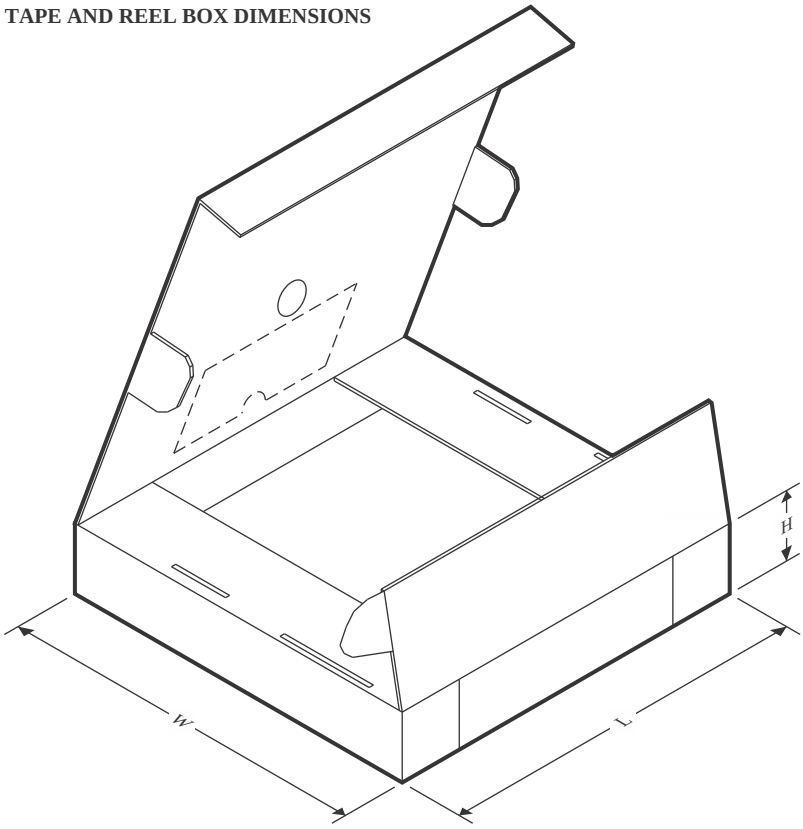
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP2011MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2011MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP2012MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMP2012MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

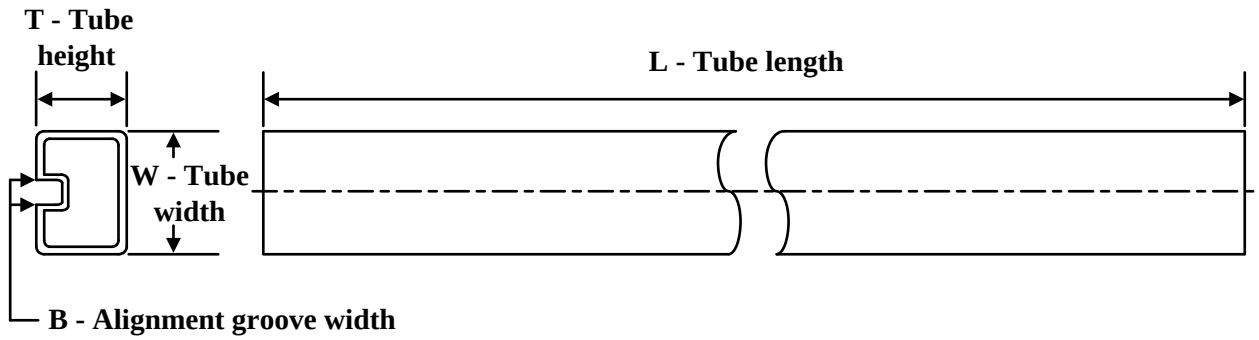
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

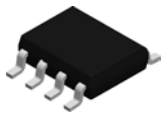
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP2011MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMP2011MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMP2012MAX/NOPB	SOIC	D	8	2500	356.0	356.0	35.0
LMP2012MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMP2011MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMP2011MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMP2012MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMP2012MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

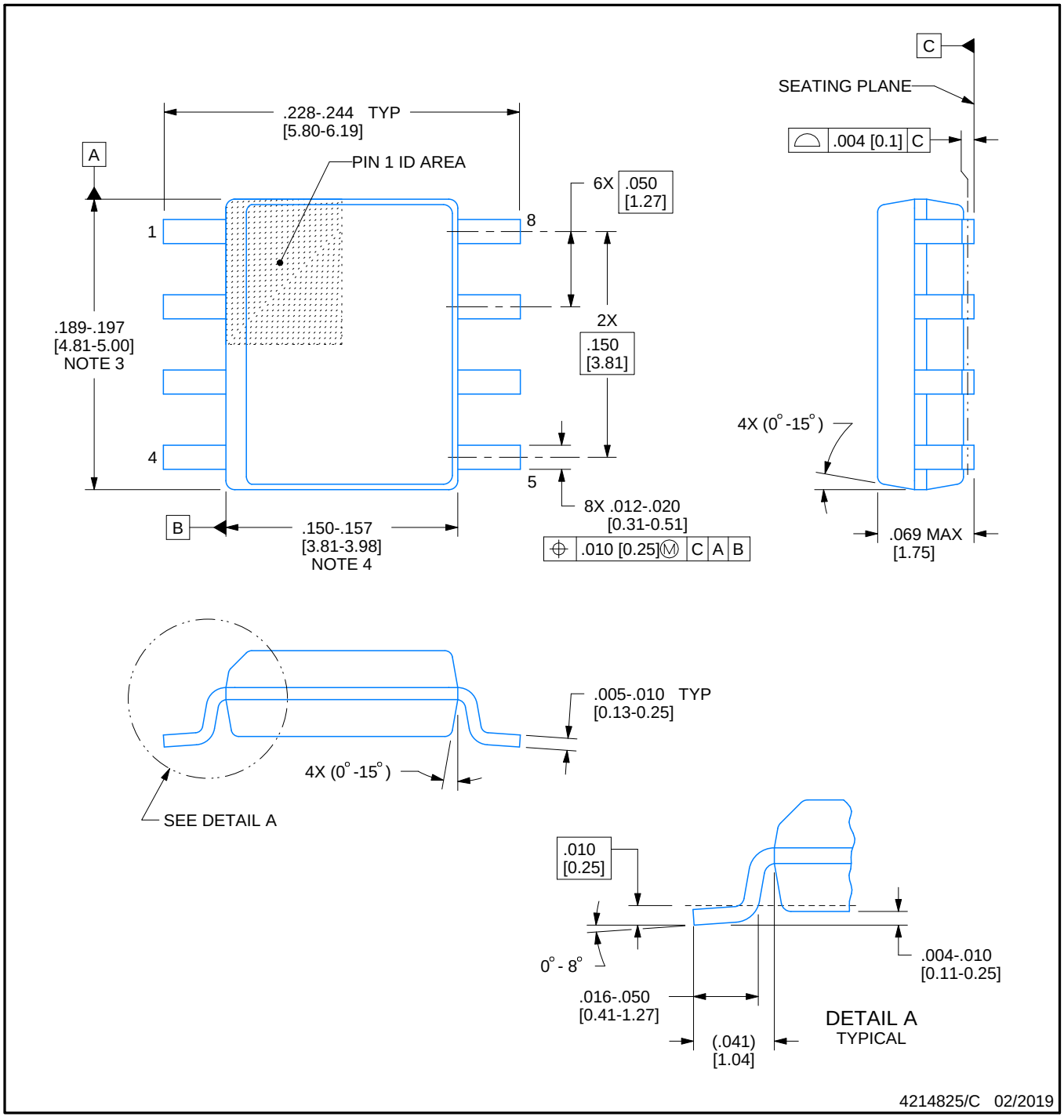


PACKAGE OUTLINE

D0008A

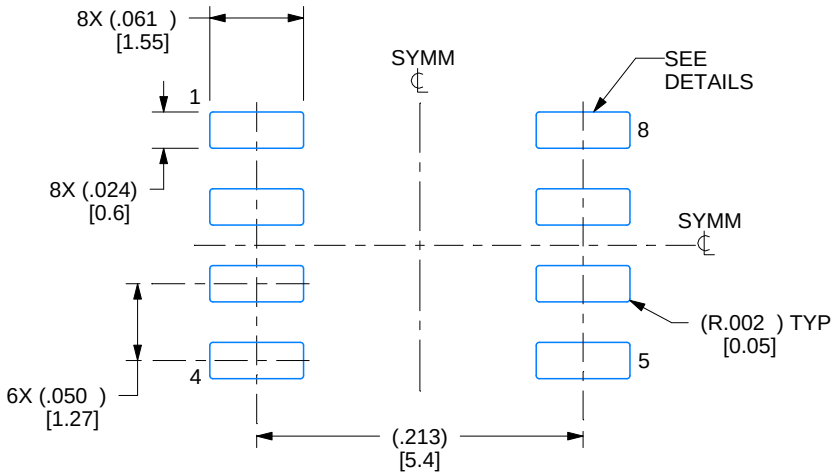
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

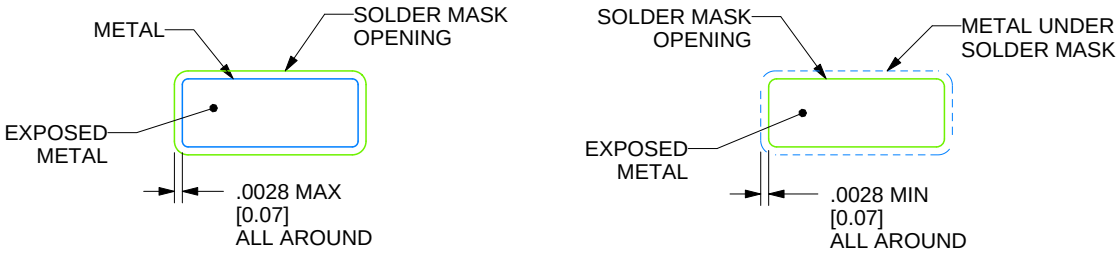


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

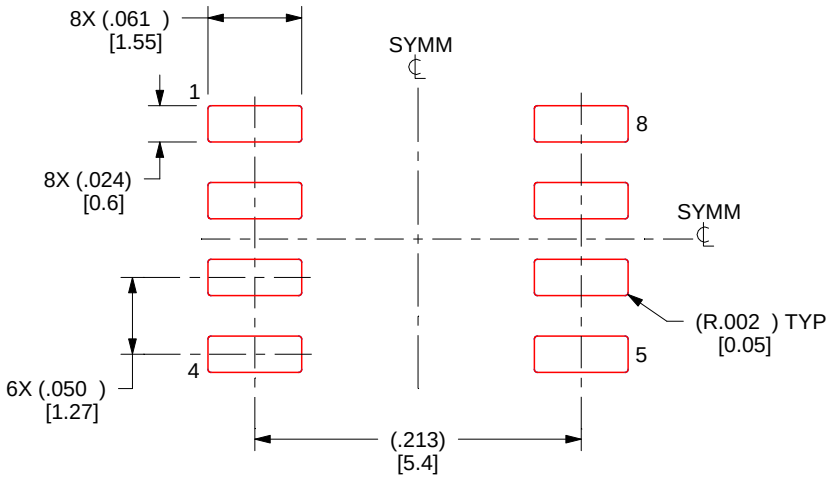
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

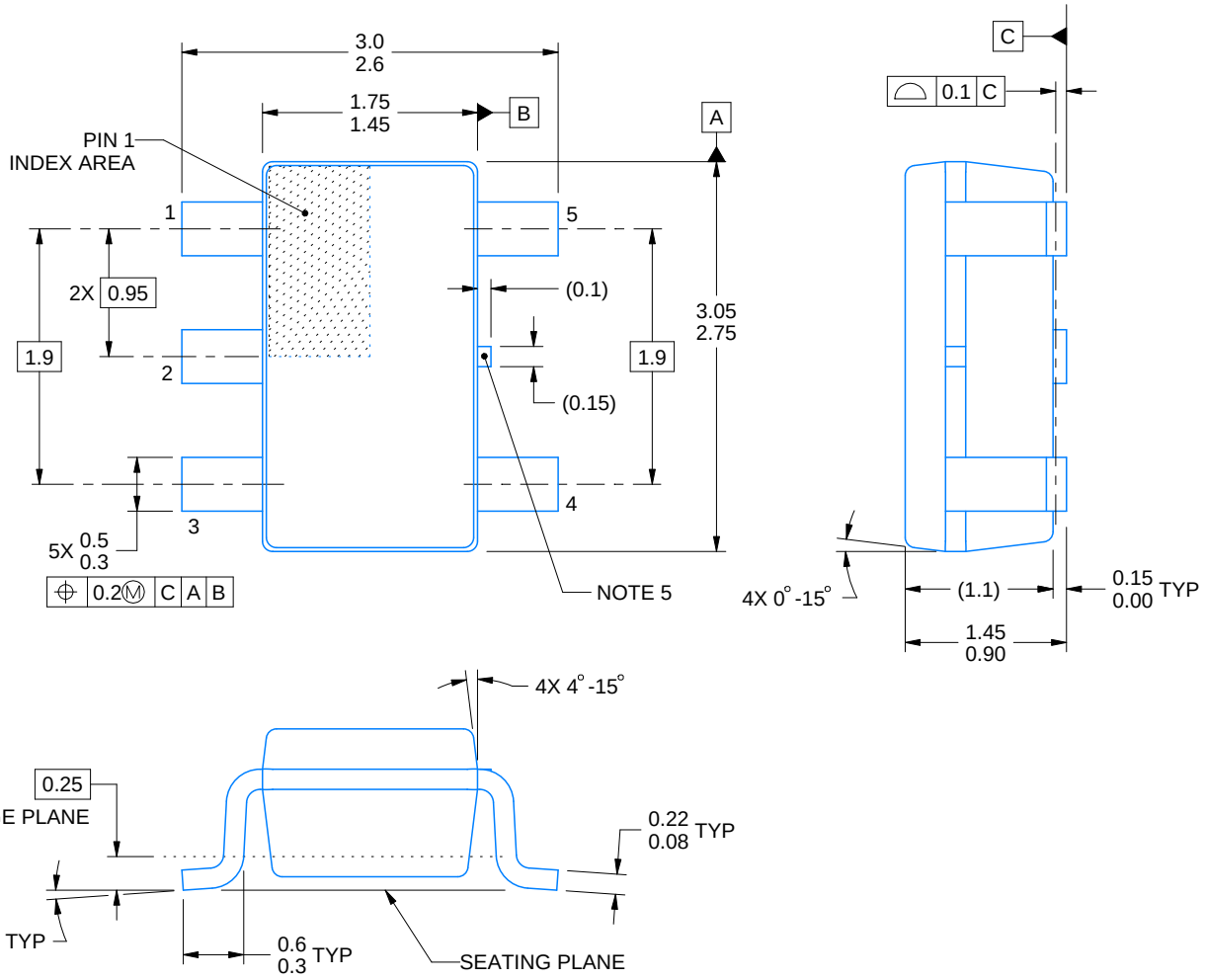
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

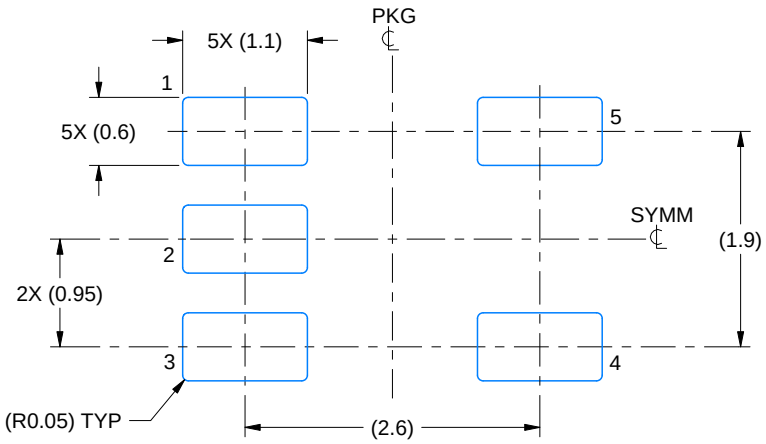
SMALL OUTLINE TRANSISTOR



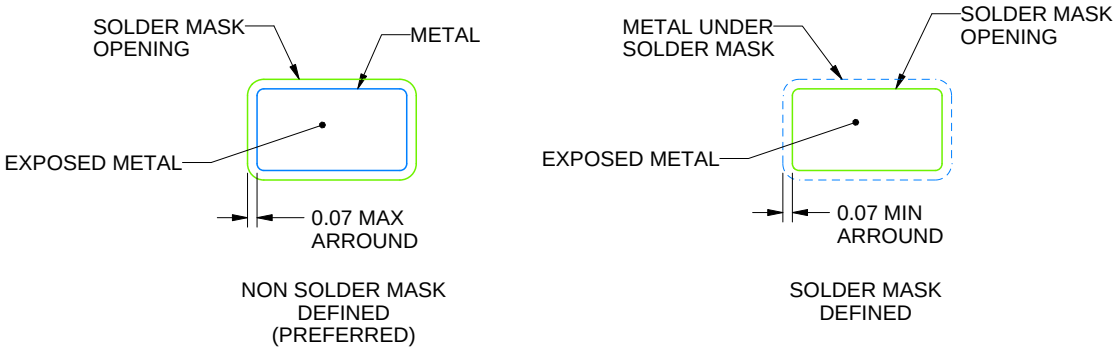
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

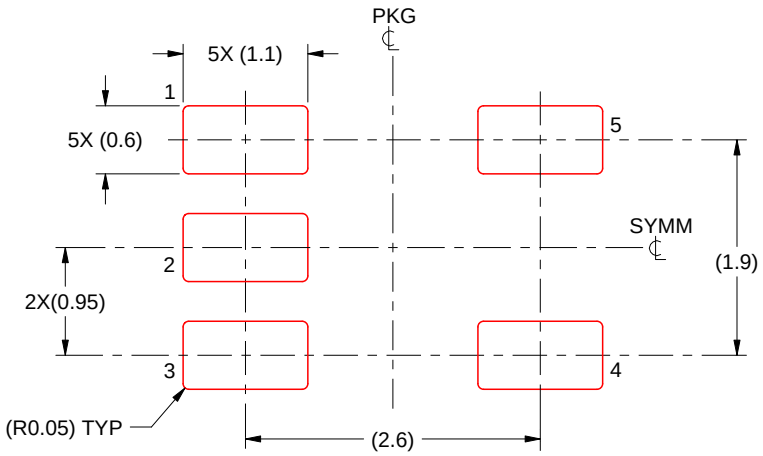


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

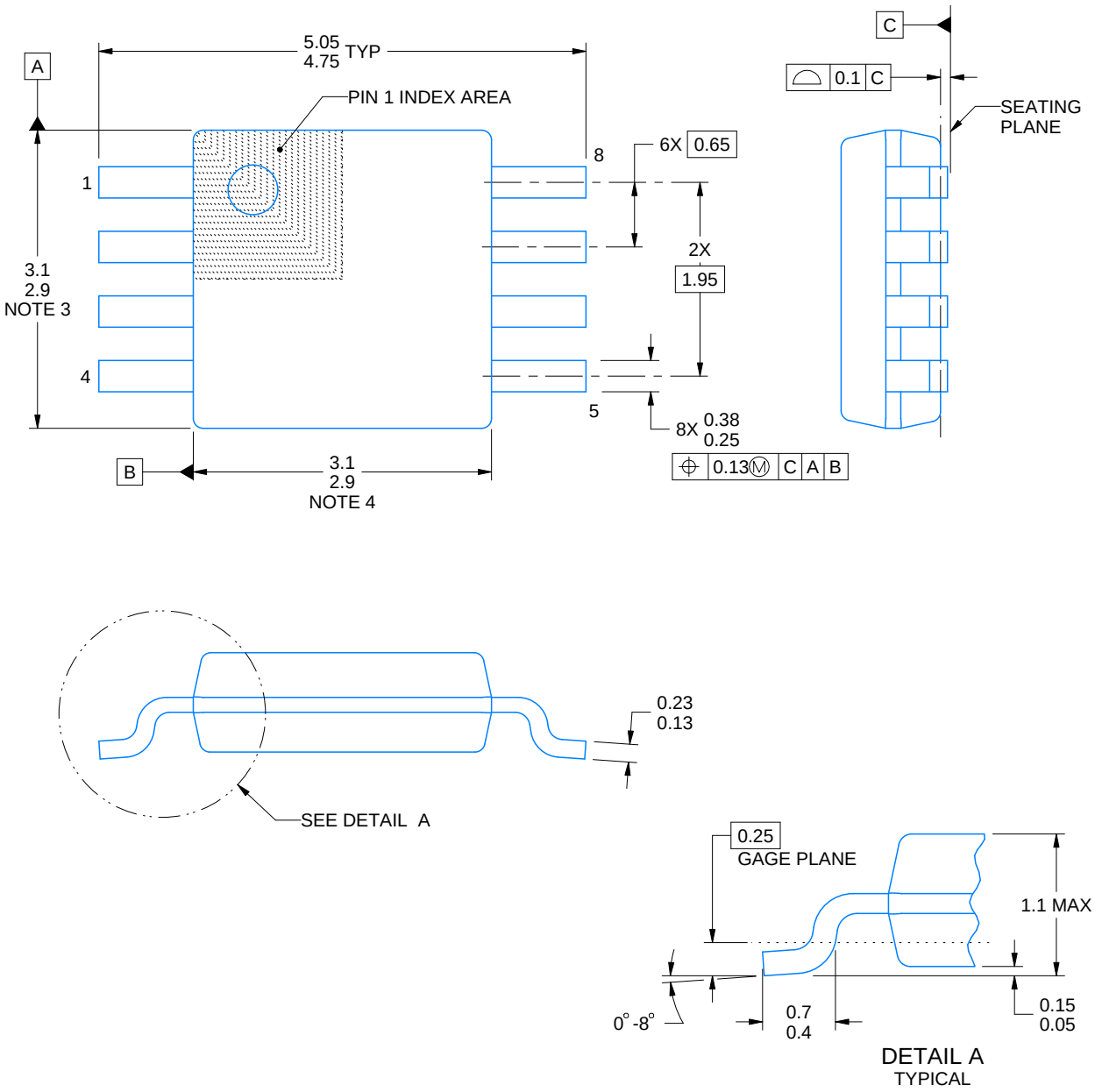
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

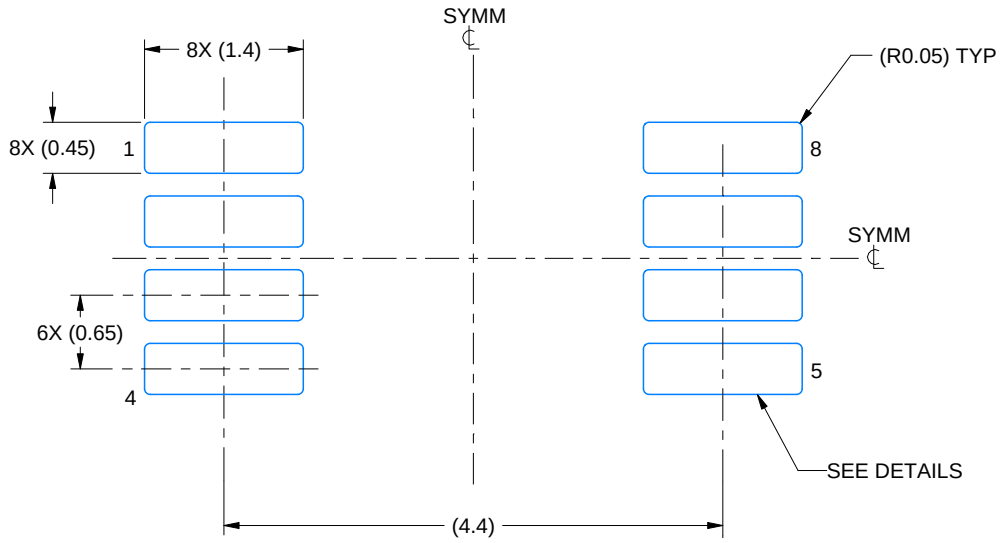
SMALL OUTLINE PACKAGE



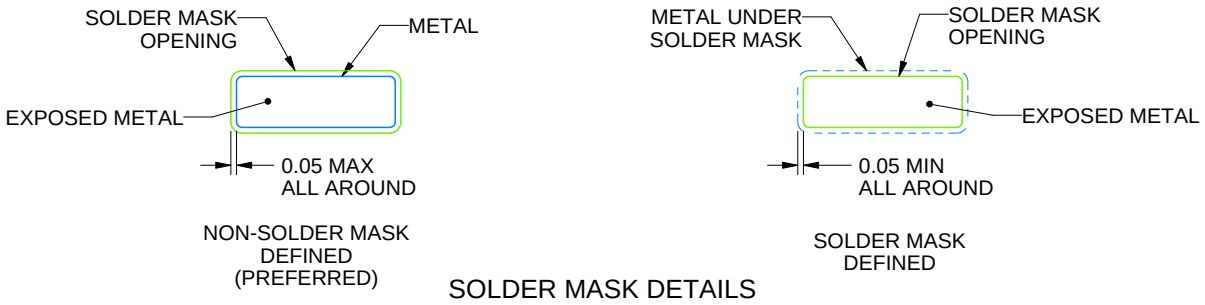
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

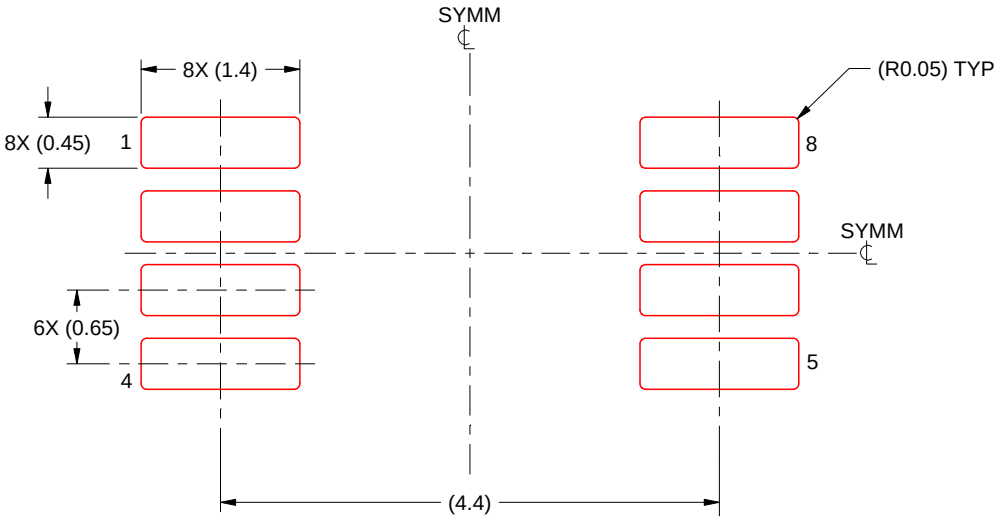


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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