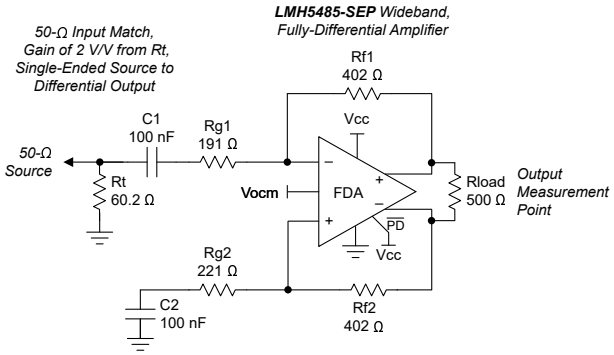
LMH5485-SEP Radiation Tolerant, Negative Rail Input, Rail-to-Rail Output, Precision, 850 MHz Fully Differential Amplifier

1 Features

- Radiation tolerant
  - TID assured for every wafer lot up to 30 krad (Si)
  - Single event latch-up (SEL) immune to LET = 43 MeV-cm2 /mg
  - Qualified over the military temperature range: –55°C to 125°C
- Gain bandwidth product (GBWP): 850 MHz
- Slew rate: 1300 V/µs
- HD2, HD3: –118 dBc, –147 dBc (100 kHz, 2 V_{PP})
- Input voltage noise: 2.4 nV/√Hz
- Low offset drift: ±0.5 µV/°C (typical)
- Negative rail input (NRI), rail-to-rail output (RRO)
- Power supply:
  - Supply voltage range: 2.7 V to 5.4 V
  - Quiescent current: 10.1 mA
  - Power-down capability: 2 µA (typical)

2 Applications

- Low-power, high-performance ADC driver:
  - SAR, ΔΣ, and pipeline
- Differential DAC output driver
- Command and data handling
- Launch vehicle systems
- Space imaging systems:
  - Optical imaging payload
  - Radar imaging payload
  - Thermal imaging cameras



Simplified Schematic

3 Description

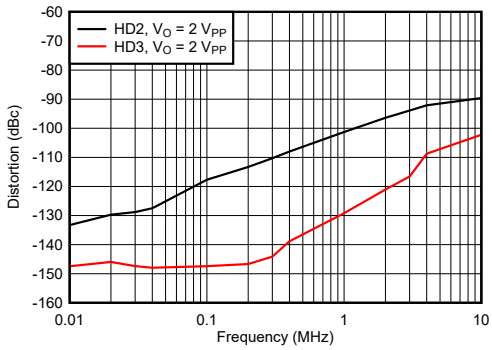
The LMH5485-SEP is a radiation tolerant, low-power, voltage-feedback, fully differential amplifier (FDA). This part is able to achieve a high gain bandwidth product (GBWP) of 850-MHz, allowing it to maintain excellent distortion performance over a wide range of frequencies as shown in the following figure. This wide bandwidth range is also achieved with a relatively low power consumption of 10.1-mA and broadband voltage noise of 2.4nV/√Hz. This combination of power consumption, bandwidth and noise allows the LMH5485-SEP to be well suited for power sensitive data acquisition systems with frequencies >10 MHz that require both the best signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR).

The LMH5485-SEP features the negative-rail input required when interfacing with a DC-coupled, ground-centered, source signal. This negative-rail input, with a rail-to-rail output, allows for easy interface between single-ended, ground-referenced, bipolar signal sources and a wide variety of successive approximation register (SAR), delta-sigma (ΔΣ), or pipeline ADCs using only a single 2.7 V to 5.4 V power supply. This device also features a low offset voltage drift of ±0.5 µV/°C, allowing it to maintain excellent DC performance over it's wide temperature range of –55°C to +125°C.

Package Information(1)(2)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH5485-SEP	DGK (VSSOP, 8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) See the *Device Information Table*



Harmonic Distortion vs Frequency

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2021) to Revision A (September 2022)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

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5 Device Comparison Table

DEVICE	RAD TOLERANCE	GBWP (MHz)	I_Q (mA)	HD2 / HD3 (dBc) 2 V_{PP} at 10 MHz	INPUT NOISE (nV/√Hz)	RAIL-TO-RAIL
LMH5485-SP	100 kRad TID	850	10.1	–79 / –97	2.4	NRI/Out
LMH5485-SEP	30 kRad TID	850	10.1	–90 / –102	2.4	NRI/Out
THS4513-SP	150 kRad TID	3000	37.7	–106 / –108	2.2	No
LMH5401-SP	100 kRad TID	6500	60	–99 / –100	1.25	No

6 Pin Configuration and Functions

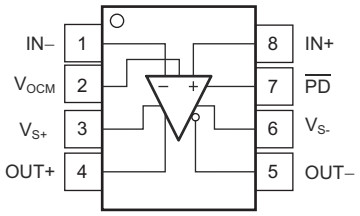


Figure 6-1. DGK Package, 8-Pin VSSOP (Top View)

Table 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN+	8	I	Noninverting (positive) amplifier input
IN–	1	I	Inverting (negative) amplifier input
OUT+	4	O	Noninverted (positive) amplifier output
OUT–	5	O	Inverted (negative) amplifier output
$\overline{PD}$	7	I	Power down. $\overline{PD}$ = logic low = power-down mode; $\overline{PD}$ = logic high = normal operation.
V_{OCM}	2	I	Common-mode voltage input
Vs+	3	P	Positive power-supply input
Vs–	6	P	Negative power-supply input

(1) I = input, O = output, P = power

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	Supply voltage (normal operation), (Vs+) – (Vs–), $\overline{PD}$ = logic high		5.5	V
	Supply voltage (power-down), (Vs+) – (Vs–), $\overline{PD}$ = logic low		5.25	
	Input-output voltage range	(Vs–) – 0.5	(Vs+) + 0.5	
	Differential input voltage		±1	
Current	Continuous input current		±20	mA
	Continuous output current		±80	
	Continuous power dissipation	See *Thermal Information* table and *Thermal Analysis* section		
Temperature	Maximum junction temperature		150	°C
	Operating free-air temperature range	–55	125	
	Storage temperature, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If the device is under continous operation with $\overline{PD}$ permanantly tied to VS+, absolute maximum supply voltage is 5.5V. If $\overline{PD}$ functionality is toggled during operation, abs max supply voltage should be limited to 5.25V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Vs+	Single-supply voltage (normal operation), $\overline{PD}$ = logic high	2.7	5	5.4	V
	Single-supply voltage (power-down), $\overline{PD}$ = logic low	2.7	5	5.1	
T_A	Ambient temperature	–55	25	125	°C

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7.4 Thermal Information

THERMAL METRIC(1)		LMH5485-SEP DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	93.4	
ψ_{JT}	Junction-to-top characterization parameter	9.2	
ψ_{JB}	Junction-to-board characterization parameter	91.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics: Vs+ – Vs- = 5 V

at T_A = -55°C to 125°C, V_{OCM} = open (defaults midsupply), Vout = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = Vs+, unless otherwise noted. See Figure 8-1 for an AC-coupled gain of a 2-V/V test circuit, and Figure 8-2 for a DC-coupled gain of a 2-V/V test circuit.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	Vout = 100 mV_{PP}, G = 1			590		MHz
		Vout = 100 mV_{PP}, G = 2			495		
		Vout = 100 mV_{PP}, G = 5			185		
		Vout = 100 mV_{PP}, G = 10			110		
GBWP	Gain-bandwidth product	Vout = 100 mV_{PP}, G = 20			850		
LSBW	Large-signal bandwidth	Vout = 2 V_{PP}			295		
	Bandwidth for 0.1-dB flatness	Vout = 2 V_{PP}			125		
	Slew rate(1)	Vout = 2-V_{PP}, FPBW			1300		V/µs
	Rise/fall time	Vout = 2-V step, input ≤ 0.5 ns t_r			1.3		ns
	Settling time	Vout = 2-V step, t_r = 2 ns	To 1%		4		
			To 0.1%		8		
	Overshoot and undershoot	Vout = 2-V step, input ≤ 0.3 ns t_r			10%		
HD	100-kHz harmonic distortion	Vout = 2 V_{PP}	HD2		–118		dBc
			HD3		–147		
	10-MHz harmonic distortion	Vout = 2 V_{PP}	HD2		–90		
			HD3		–102		
	2nd-order intermodulation distortion	f = 10 MHz, 100-kHz tone spacing, Vout envelope = 2 V_{PP} (1 V_{PP} per tone)			–90		
	3rd-order intermodulation distortion				–85		
e_n	Input voltage noise	f > 100 kHz			2.4		nV/√Hz
i_n	Input current noise	f > 1 MHz			1.9		pA/√Hz
	Overdrive recovery time	2x output overdrive, either polarity			20		ns
Z_{OUT}	Closed-loop output impedance	f = 10 MHz (differential)			0.1		Ω
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain			97	119		dB
V_{OS}	Input-referred offset voltage			–900	±100	900	µV
	Input offset voltage drift(2)			–2.5	±0.5	2.5	µV/°C
I_{B+}, $I_{B–}$	Input bias current	Positive out of node		1.7	10	15	µA
	Input bias current drift(2)				6	15	nA/°C
I_{OS}	Input offset current			–650	±150	650	nA
	Input offset current drift(2)			–1.5	±0.3	1.5	nA/°C
INPUT							
V_{ICML}	Common-mode input low	< 3-dB degradation in CMRR from midsupply			(Vs–) – 0.2	Vs–	V
V_{ICMH}	Common-mode input high			(Vs+) – 1.3	(Vs+) –1.2		
CMRR	Common-mode rejection ratio	Input pins at midsupply		82	100		dB
	Input impedance differential mode	Input pins at midsupply			110 || 0.9		kΩ || pF

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7.5 Electrical Characteristics: Vs+ – Vs- = 5 V (continued)

at T_A = -55°C to 125°C, V_{OCM} = open (defaults midsupply), Vout = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = Vs+, unless otherwise noted. See Figure 8-1 for an AC-coupled gain of a 2-V/V test circuit, and Figure 8-2 for a DC-coupled gain of a 2-V/V test circuit.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Output voltage low			(Vs–) + 0.2	(Vs–) + 0.25	V
	Output voltage high		(Vs+) – 0.25	(Vs+) – 0.2		
	Output current drive		±75	±100		mA
POWER SUPPLY						
I_Q	Quiescent operating current		9.2	10.1	11	mA
PSRR	Power-supply rejection ratio	Either supply pin to differential Vout	82	100		dB
POWER DOWN						
V_{EN}	Enable voltage threshold		(Vs–) + 1.7			V
V_{DIS}	Disable voltage threshold				(Vs–) + 0.7	
	Disable pin bias current	$\overline{PD}$ = Vs– → Vs+		20	50	nA
	Power-down quiescent current	$\overline{PD}$ = (Vs–) + 0.7 V		6	30	µA
		$\overline{PD}$ = Vs–		2	8	
	Turnon-time delay	Time from $\overline{PD}$ = low to Vout = 90% of final value		100		ns
	Turnoff time delay	Time from $\overline{PD}$ = low to Vout = 10% of final value		60		
OUTPUT COMMON-MODE VOLTAGE CONTROL(3)						
	Small-signal bandwidth	V_{OCM} = 100 mV_{PP}		150		MHz
	Slew rate(1)	V_{OCM} = 2-V step		400		V/µs
	Gain		0.975	0.982	0.995	V/V
	Input bias current	Considered positive out of node	–0.8	0.1	0.8	µA
	Input impedance	V_{OCM} input driven to midsupply		47 || 1.2		kΩ || pF
	Default voltage offset from midsupply	V_{OCM} pin open	–45	±8	45	mV
	Common-mode offset voltage	V_{OCM} input driven to midsupply	–8	±2	8	
	CM V_{OS} drift(2)	V_{OCM} input driven to midsupply	–20	±4	+20	µV/°C
	Common-mode loop supply headroom to negative supply	< ±15-mV shift from midsupply CM V_{OS}	0.94			V
	Common-mode loop supply headroom to positive supply	< ±15-mV shift from midsupply CM V_{OS}	1.2			

(1) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: (V_P / $\sqrt{2}$) × 2π × f_{-3dB}.
(2) Input offset voltage drift, input bias current drift, input offset current drift, and V_{OCM} drift are average values calculated by taking data at the at the maximum-range ambient-temperature end-points, computing the difference, and dividing by the temperature range.
(3) Specifications are from the input V_{OCM} pin to the differential output average voltage.

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7.6 Electrical Characteristics: Vs+ – Vs- = 3 V

at T_A = -55°C to 125°C, V_{OCM} = open (defaults midsupply), Vout = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = Vs+, unless otherwise noted. See Figure 8-1 for an AC-coupled gain of a 2-V/V test circuit, and Figure 8-2 for a DC-coupled gain of a 2-V/V test circuit.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
	Small-signal bandwidth	Vout = 100 mV_{PP}, G = 1			585		MHz
		Vout = 100 mV_{PP}, G = 2			490		MHz
		Vout = 100 mV_{PP}, G = 5			180		MHz
GBWP	Gain-bandwidth product	Vout = 100 mV_{PP}, G = 20			850		MHz
	Large-signal bandwidth	Vout = 2 V_{PP}			275		MHz
	Bandwidth for 0.1-dB flatness	Vout = 2 V_{PP}			120		MHz
	Slew rate(1)	Vout = 2-V step, FPBW			1200		V/µs
	Rise/fall time	Vout = 2-V step, input ≤ 0.5 ns t_r			1.6		ns
	Settling time	Vout = 2-V step, t_r = 2 ns	To 1%		5		ns
			To 0.1%		8		ns
	Overshoot and undershoot	Vout = 2-V step, input ≤ 0.3 ns t_r			11%		
	100-kHz harmonic distortion	Vout = 2 V_{PP}	HD2		–118		dBc
			HD3		–148		dBc
	10-MHz harmonic distortion	Vout = 2 V_{PP}	HD2		–90		dBc
			HD3		–100		dBc
	2nd-order intermodulation distortion	f = 10 MHz, 100-kHz tone spacing, Vout envelope = 2 V_{PP} (1 V_{PP} per tone)			–89		dBc
	3rd-order intermodulation distortion				–87		dBc
e_n	Input voltage noise	f > 100 kHz			2.4		nV/√Hz
i_n	Input current noise	f > 1 MHz			1.9		pA/√Hz
	Overdrive recovery time	2X output overdrive, either polarity			20		ns
	Closed-loop output impedance	f = 10 MHz (differential)			0.1		Ω
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain			97	119		dB
	Input-referred offset voltage			–900	±100	900	µV
	Input offset voltage drift(2)			–2.5	±0.5	2.5	µV/°C
	Input bias current	Positive out of node		1.7	9	15	µA
	Input bias current drift(2)				5	15	nA/°C
	Input offset current			–650	±150	650	nA
	Input offset current drift(2)			–1.5	±0.3	1.5	nA/°C
INPUT							
	Common-mode input low	< 3-dB degradation in CMRR from midsupply			(Vs–) – 0.2	Vs–	V
	Common-mode input high	< 3-dB degradation in CMRR from midsupply		(Vs+) – 1.3	(Vs+) –1.2		V
	Common-mode rejection ratio	Input pins at midsupply		82	100		dB
	Input impedance differential mode	Input pins at midsupply			110 || 0.9		kΩ || pF

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7.6 Electrical Characteristics: Vs+ – Vs- = 3 V (continued)

at T_A = -55°C to 125°C, V_{OCM} = open (defaults midsupply), Vout = 2 V_{PP}, Rf = 402 Ω, Rload = 499 Ω, 50-Ω input match, G = 2 V/V, single-ended input, differential output, and $\overline{PD}$ = Vs+, unless otherwise noted. See Figure 8-1 for an AC-coupled gain of a 2-V/V test circuit, and Figure 8-2 for a DC-coupled gain of a 2-V/V test circuit.

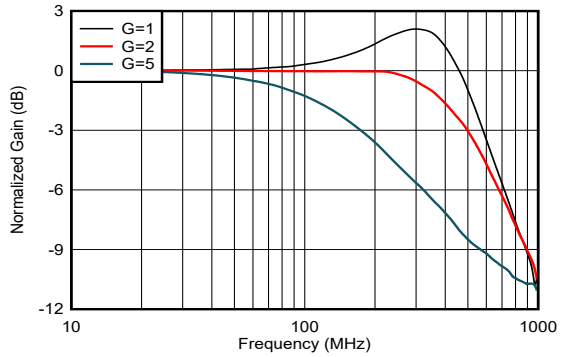
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Output voltage low			(Vs–) + 0.2	(Vs–) + 0.25	V
	Output voltage high		(Vs+) – 0.25	(Vs+) – 0.2		V
	Output current drive		±55	±60		mA
POWER SUPPLY						
	Specified operating voltage		2.7	3	5.1	V
	Quiescent operating current		9	9.7	10.6	mA
±PSRR	Power-supply rejection ratio	Either supply pin to differential Vout	82	100		dB
POWER DOWN						
	Enable voltage threshold		(Vs–) + 1.7			V
	Disable voltage threshold				(Vs–) + 0.7	V
	Disable pin bias current	$\overline{PD}$ = Vs– → Vs+		20	50	nA
	Power-down quiescent current	$\overline{PD}$ = (Vs–) + 0.7 V		2	30	µA
		$\overline{PD}$ = Vs–		1	8	µA
	Turnon-time delay	Time from $\overline{PD}$ = low to Vout = 90% of final value		100		ns
	Turnoff time delay	Time from $\overline{PD}$ = low to Vout = 10% of final value		60		ns
OUTPUT COMMON-MODE VOLTAGE CONTROL(3)						
	Small-signal bandwidth	V_{OCM} = 100 mV_{PP}		140		MHz
	Slew rate(1)	V_{OCM} = 1-V step		350		V/µs
	Gain		0.975	0.987	0.990	V/V
	Input bias current	Considered positive out of node	–0.7	0.1	0.7	µA
	Input impedance	V_{OCM} input driven to midsupply		47 || 1.2		kΩ || pF
	Default voltage offset from midsupply	V_{OCM} pin open	–45	±10	45	mV
CM V_{OS}	Common-mode offset voltage	V_{OCM} input driven to midsupply	–8	±2	8	mV
	CM V_{OS} drift(2)	V_{OCM} input driven to midsupply	–20	±4	20	µV/°C
	Common-mode loop supply headroom to negative supply	< ±15-mV shift from midsupply CM V_{OS}	0.94			V
	Common-mode loop supply headroom to positive supply	< ±15-mV shift from midsupply CM V_{OS}	1.2			V

(1) This slew rate is the average of the rising and falling time estimated from the large-signal bandwidth as: (V_P / √2) × 2π × f_{-3dB}.
(2) Input offset voltage drift, input bias current drift, input offset current drift, and V_{OCM} drift are average values calculated by taking data at the at the maximum-range ambient-temperature end-points, computing the difference, and dividing by the temperature range. Maximum drift set by distribution of a large sampling of devices. Drift is not specified by test or QA sample test.
(3) Specifications are from input V_{OCM} pin to differential output average voltage.

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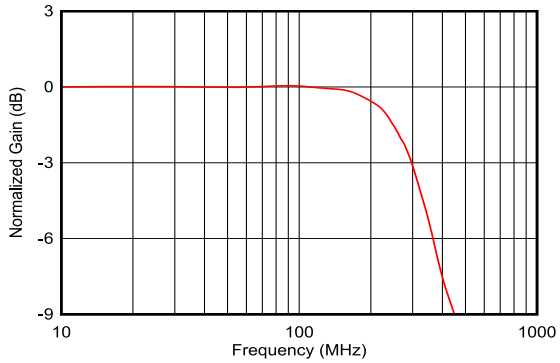
7.7 Typical Characteristics: 5 V Single Supply

at Vs+ = 5 V, Vs– = GND, R_F= 402 Ω, V_{OCM} is open, 50 Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≅ 25°C (unless otherwise noted)



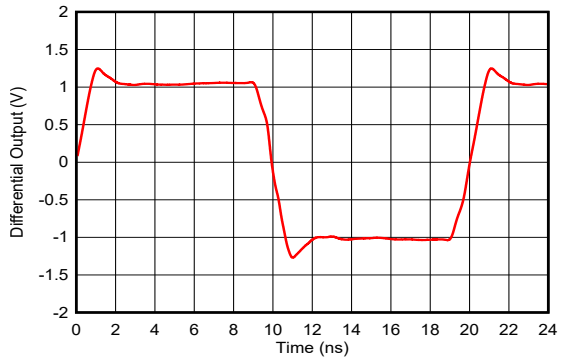
Vo = 100 mV_{PP}

Figure 7-1. Small-Signal Frequency Response vs Gain



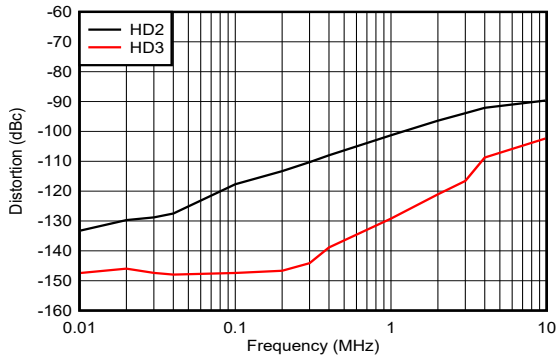
V_O = 2 V_{PP}

Figure 7-2. Large-Signal Frequency Response



50 MHz input, 0.5-ns input edge rate, single-ended to differential output, split supply, DC-coupled, see Figure 8-2

Figure 7-3. Large-Signal Step Response



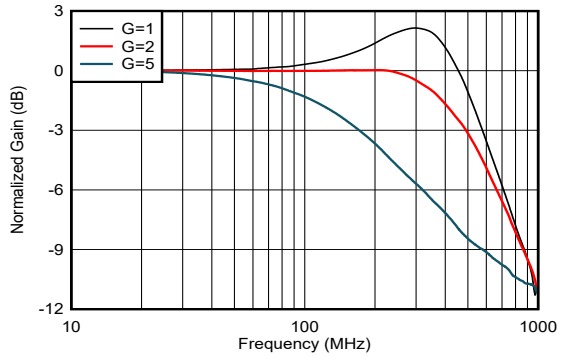
2 V_{PP} output, see Figure 8-1

Figure 7-4. Harmonic Distortion Over Frequency

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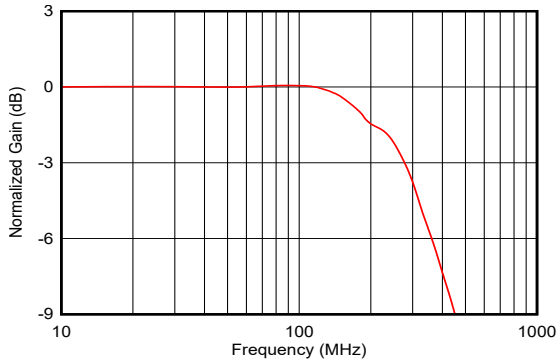
7.8 Typical Characteristics: 3 V Single Supply

at Vs+ = 3 V, Vs– = GND, V_{OCM} is open, 50 Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≅ 25°C (unless otherwise noted)



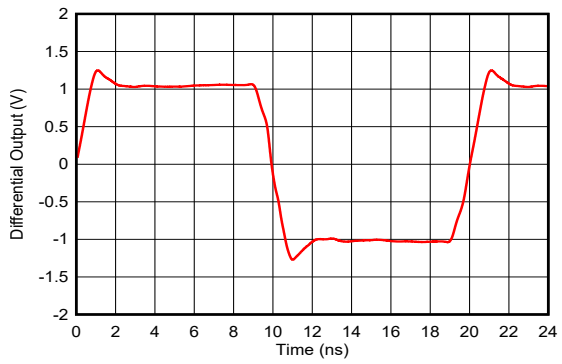
Rf = 402 Ω, Vout = 100 mV_{PP}

Figure 7-5. Small-Signal Frequency Response vs Gain



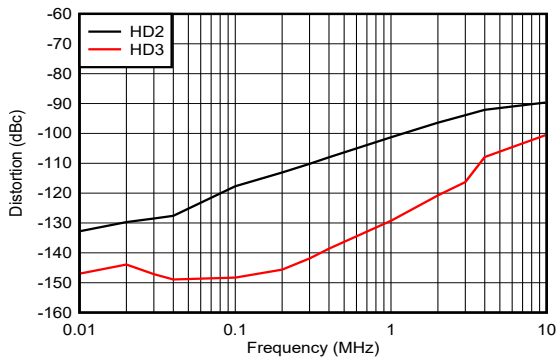
Rf = 402 Ω, Vout = 2 V_{PP}

Figure 7-6. Large-Signal Frequency Response



50 MHz input, 0.5-ns input edge rate, single-ended input to differential output, split supply, DC coupled, see Figure 8-2

Figure 7-7. Large-Signal Step Response



2 V_{PP} output, see Figure 8-1 with Vs+ = 3 V, V_{OCM} = 1.5 V

Figure 7-8. Harmonic Distortion Over Frequency

7.9 Typical Characteristics: 3 V to 5 V Supply Range

at Vs+ = 3 V and 5 V, Vs– = GND, V_{OCM} is open, 50 Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≅ 25°C (unless otherwise noted)

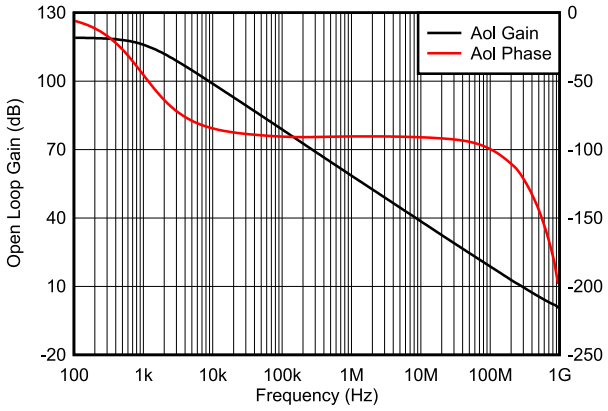
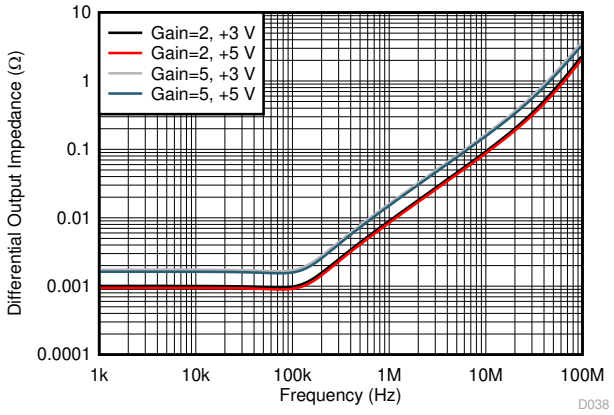


Figure 7-9. Main Amplifier Differential Open-Loop Gain and Phase vs Frequency



Single-ended input to differential output, simulated differential output impedance, see Figure 8-1

Figure 7-10. Closed-Loop Output Impedance

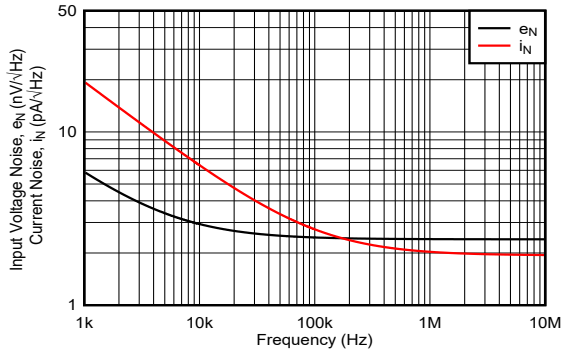
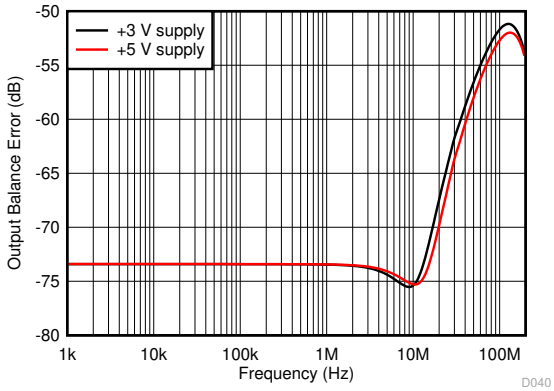
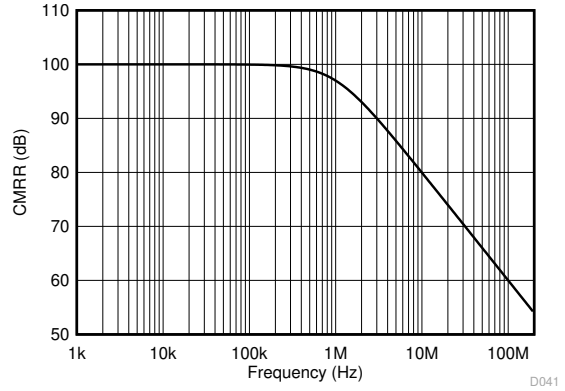


Figure 7-11. Input Spot Noise Over Frequency



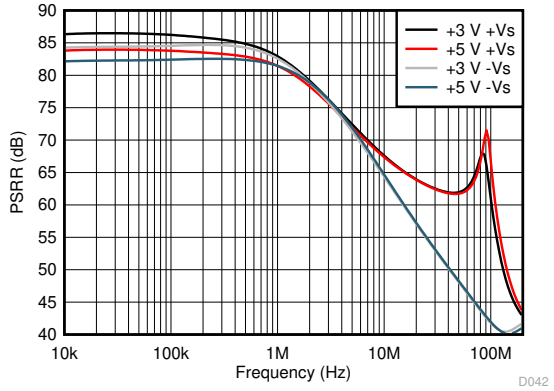
Single-ended input to differential output, gain of 2 (see Figure 8-1), simulated with 1% resistor, worst-case mismatch

Figure 7-12. Output Balance Error Over Frequency



Common-mode in to differential out, gain of 2 simulation

Figure 7-13. CMRR Over Frequency



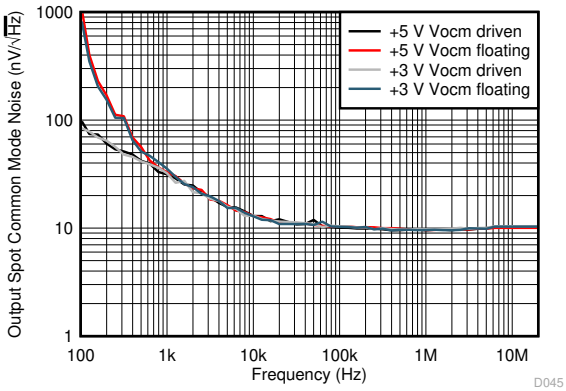
Single-ended to differential, gain of 2 (see Figure 8-1) PSRR simulated to differential output

Figure 7-14. PSRR Over Frequency

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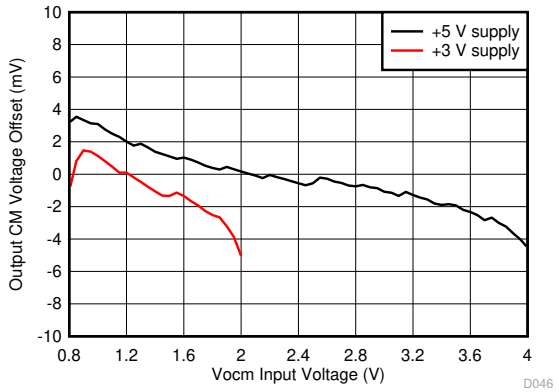
7.9 Typical Characteristics: 3 V to 5 V Supply Range (continued)

at Vs+ = 3 V and 5 V, Vs– = GND, V_{OCM} is open, 50 Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≅ 25°C (unless otherwise noted)



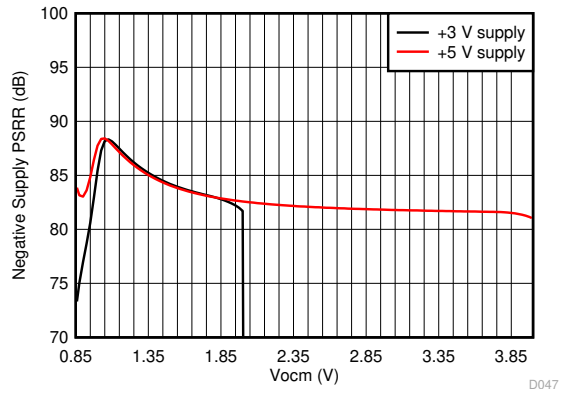
V_{OCM} input either driven to mid-supply by low impedance source, or allowed to float and default to mid-supply

Figure 7-15. Output Common-Mode Noise



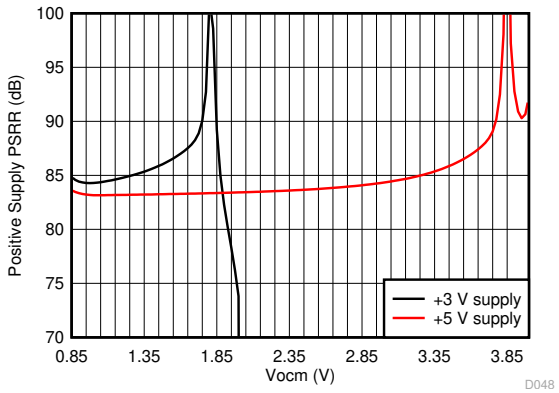
Average V_{OCM} output offset of 37 units, Standard deviation < 2.5 mV, see Figure 8-2

Figure 7-16. V_{OCM} Offset vs V_{OCM} Setting



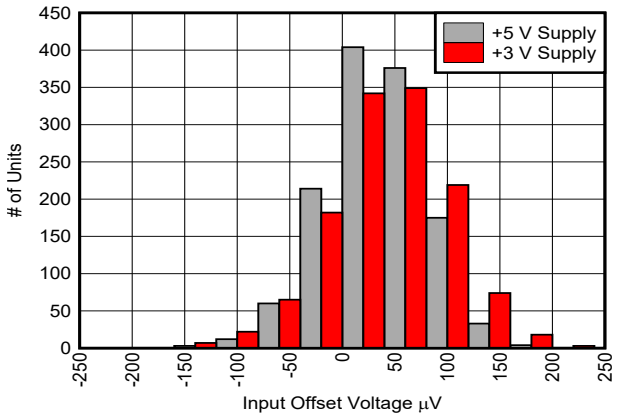
Single-ended to differential gain of 2 (see Figure 8-1), PSRR for negative supply to differential output (1-kHz simulation)

Figure 7-17. –PSRR vs V_{OCM} Approaching Vs–



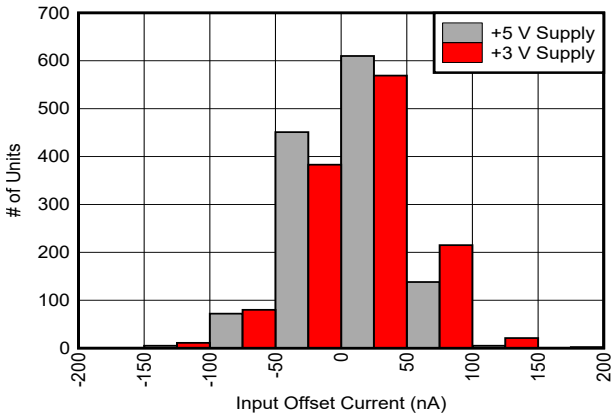
Single-ended to differential gain of 2 (see Figure 8-1), PSRR for positive supply to differential output (1-kHz simulation)

Figure 7-18. +PSRR vs V_{OCM} Approaching Vs+



Total of 1281 units for each supply. For Vs = 5 V: µ = 34.1 µV, σ = 47.1 µV

Figure 7-19. Input Offset Voltage



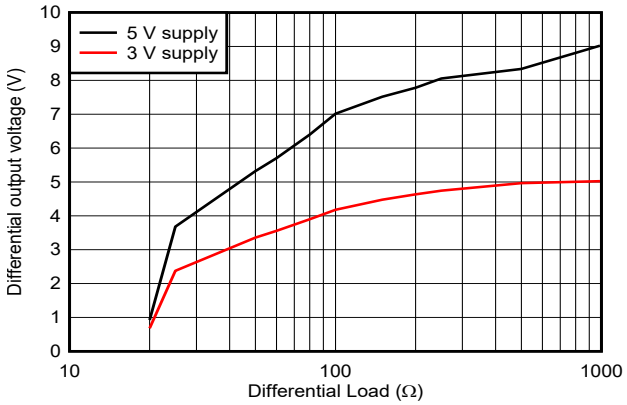
Total of 1281 units for each supply. For Vs = 5 V: µ = 7.0 nA, σ = 35.9 nA

Figure 7-20. Input Offset Current

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7.9 Typical Characteristics: 3 V to 5 V Supply Range (continued)

at Vs+ = 3 V and 5 V, Vs– = GND, V_{OCM} is open, 50 Ω single-ended input to differential output, gain = 2 V/V, Rload = 500 Ω, and T_A ≅ 25°C (unless otherwise noted)



Maximum differential output swing, V_{OCM} at mid-supply

Figure 7-21. Differenital Output Voltage vs Rload

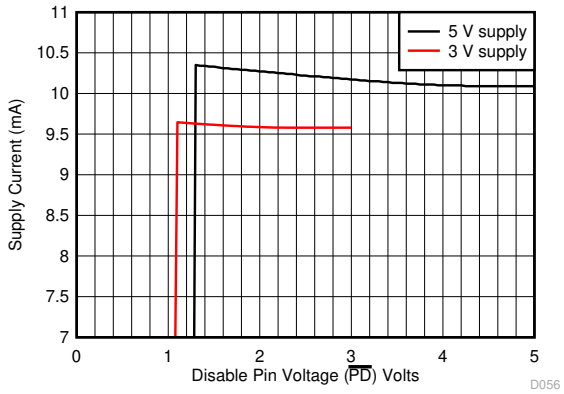
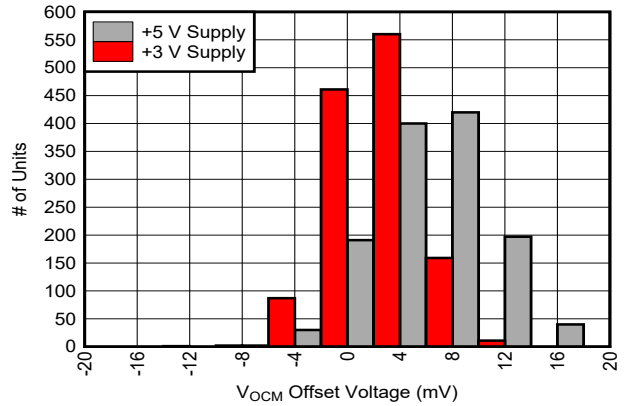
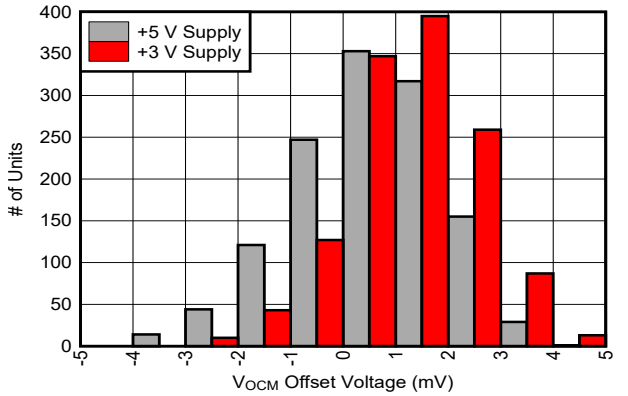


Figure 7-22. Supply Current vs $\overline{PD}$ Voltage



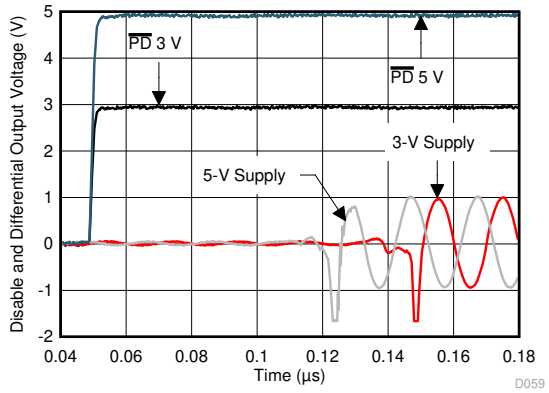
V_{OCM} input floating. Total of 1281 units for each supply. For Vs = 5 V: μ = 8.1 mV, σ = 4.3 mV

Figure 7-23. Common-Mode Output Offset from Vs+ / 2 Default Value



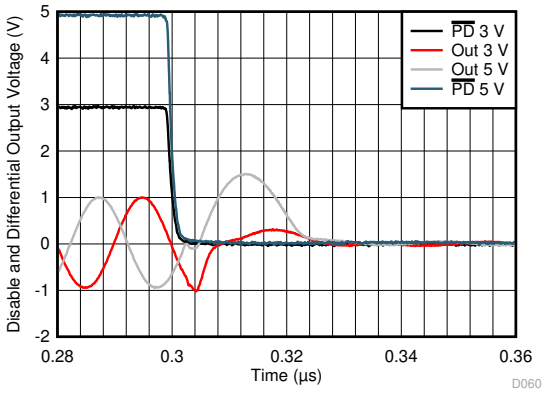
Total of 1281 units for each supply. For Vs = 5 V: μ = 0.52 mV, σ = 1.4 mV

Figure 7-24. Common-Mode Output Offset from Driven V_{OCM}



10 MHz, 1 V_{PP} input single to differential gain of 2, see Figure 8-2

Figure 7-25. $\overline{PD}$ Turn On Waveform



10 MHz, 1 V_{PP} input single to differential gain of 2, see Figure 8-2

Figure 7-26. $\overline{PD}$ Turn Off Waveform

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8 Parameter Measurement Information

8.1 Example Characterization Circuits

The LMH5485-SEP offers the advantages of a fully differential amplifier (FDA) design, with the trimmed input offset voltage of a precision op amp. The FDA is an extremely flexible device that provides a purely differential output signal centered on a settable output common-mode level. The primary options revolve around the choices of single-ended or differential inputs, AC-coupled or DC-coupled signal paths, gain targets, and resistor Value selections. Differential sources can certainly be supported and are often simpler to both implement and analyze. Examples of both AC and DC coupled single-ended to differential circuits is shown in Figure 8-1 and Figure 8-2.

Because most lab equipment is single-ended, the characterization circuits typically operate with a single-ended, matched, 50 Ω input termination to a differential output at the FDA output pins. That output is then translated back to single-ended through a variety of baluns (or transformers) depending on the test and frequency range. DC-coupled, step-response testing uses two 50 Ω scope inputs with trace math.

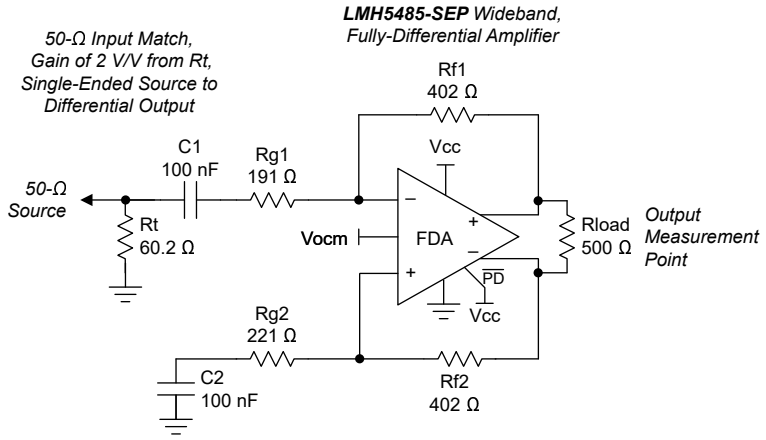


Figure 8-1. AC-Coupled, Single-Ended Source to a Differential Gain of a 2 V/V Test Circuit

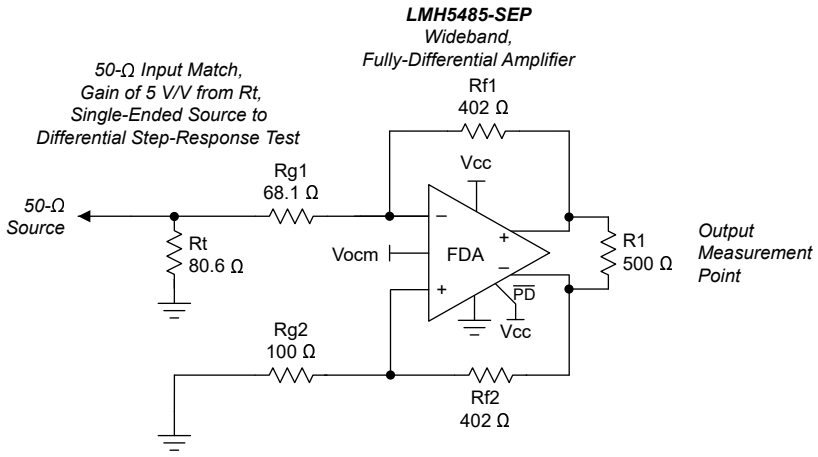


Figure 8-2. DC-Coupled, Single-Ended-to-Differential, Basic Test Circuit Set for a Gain of 5 V/V

Figure 8-1 shows how most characterization plots fix the R_f value at 402 Ω. This value is completely flexible in application, but the 402 Ω provides a good compromise for the issues linked to this value, specifically:

- Added output loading. The FDA appears like an inverting op amp design with both feedback resistors as an added load across the outputs (approximate total differential load in Figure 8-1 is 500 Ω || 804 Ω = 308 Ω).
- Noise contributions because of the resistor values. The resistors contribute both a 4kTR term and provide gain for the input current noise.

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- Parasitic feedback pole at the input summing nodes. This pole created by the feedback R value and the differential input capacitance (as well as any board layout parasitic) introduces a zero in the noise gain, decreasing the phase margin in most situations. This effect must be managed for best frequency response flatness or step response overshoot. The 402 Ω value selected does degrade the phase margin slightly over a lower value, but does not decrease the loading significantly from the nominal 500 Ω value across the output pins.

9 Detailed Description

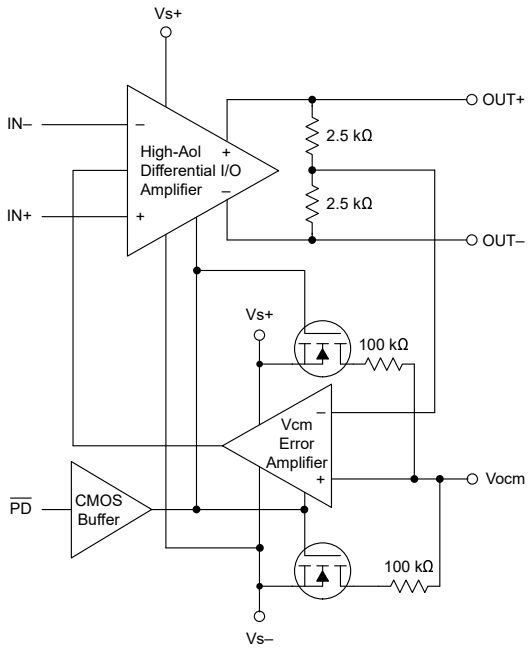
9.1 Overview

The LMH5485-SEP is a voltage-feedback (VFA) based, fully-differential amplifier (FDA) with a trimmed supply current and input offset voltage. The core differential amplifier is a slightly decompensated voltage-feedback design with a high slew-rate, precision input stage. This design gives a MHz gain of 2 V/V small-signal bandwidth shown in the characterization curves, with a V/µs slew rate, yielding approximately a MHz, 2 V_{PP}, large-signal bandwidth in the same circuit configuration.

The outputs offer near rail-to-rail output swing (0.2 V headroom to either supply), while the device inputs are negative rail inputs with approximately 1.2 V of headroom required to the positive supply. Figure 8-2 shows how this negative rail input directly supports a bipolar input around ground in a DC-coupled, single-supply design. Similar to all FDA devices, the output average voltage (common-mode) is controlled by a separate common-mode loop. The target for this output average is set by the V_{OCM} input pin that can be either floated to default near mid-supply or driven to a desired output common-mode voltage. The V_{OCM} range extends from a very low 0.91 V above the negative supply to 1.1 V below the positive supply, supporting a wide range of modern analog-to-digital converter (ADC) input common-mode requirements using a single 2.7 V to 5.4 V supply range for the LMH5485-SEP.

A power-down pin ($\overline{PD}$) is included. Pull the $\overline{PD}$ pin voltage to the negative supply to turn the device off, putting the LMH5485-SEP into a very-low quiescent current state. To be able to use the full supply range of the device, the device must be kept in normal operation by keeping the $\overline{PD}$ pin asserted high. When the device is disabled, remember that the signal path is still present through the passive external resistors. Input signals applied to a disabled LMH5485-SEP still appear at the outputs at some level through this passive resistor path as they would for any disabled FDA device.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Differential I/O

The LMH5485-SEP combines a core differential I/O, high-gain block with an output common-mode sense that is compared to a reference voltage and then fed back into the main amplifier block to control the average output to that reference. The differential I/O block is a classic, high open-loop gain stage with a dominant pole at approximately 900 Hz. This voltage feedback structure projects a single-pole, unity-gain Aol at 850 MHz (gain bandwidth product). The high-speed differential outputs include an internal averaging resistor network to sense the output common-mode voltage. This voltage is compared by a separate Vcm error amplifier to the voltage on the V_{OCM} pin. If floated, this reference is at half the total supply voltage across the device using two 100-kΩ resistors. This Vcm error amplifier transmits a correction signal into the main amplifier to force the output average voltage to meet the target voltage on the V_{OCM} pin. The bandwidth of this error amplifier is approximately the same bandwidth as the main differential I/O amplifier.

The differential outputs are collector outputs to obtain the rail-to-rail output swing. These outputs are relatively high-impedance, open-loop sources; however, closing the loop provides a very low output impedance for load driving. No output current limit or thermal shutdown features are provided in this lower-power device. The differential inputs are PNP inputs to provide a negative-rail input range.

To operate the LMH5485-SEP connect the OUT– pin to the IN+ pin through an Rf, and the OUT+ pin to the IN– pin through the same value of Rf. Bring in the inputs through additional resistors to the IN+ and IN– pins. The differential I/O op amp operates similarly to an inverting op amp structure where the source must drive the input resistor and the gain is the ratio of the feedback to the input resistor.

9.3.2 Power-Down Control Pin ($\overline{PD}$)

The LMH5485-SEP includes a power-down control pin, $\overline{PD}$. This pin must be asserted high for correct amplifier operation. The $\overline{PD}$ pin cannot be floated because there is no internal pullup or pulldown resistor on this pin to reduce disabled power consumption. Asserting this pin low (within 0.7 V of the negative supply) puts the LMH5485-SEP into a very low quiescent state (approximately 2 µA). Switches in the default V_{OCM} resistor string open to eliminate the fixed bias current (25 µA) across the supply in this 200-kΩ voltage divider to mid-supply.

9.3.2.1 Operating the Power Shutdown Feature

When the $\overline{PD}$ pin is asserted high, close to the positive supply, the device will be in normal active mode of operation. To disable the device for reduced power consumption, $\overline{PD}$ pin must be asserted low, close to the negative supply. Figure 7-22 shows the $\overline{PD}$ pin voltage and the corresponding quiescent current drawn. For applications that require the device to only be powered on when the supplies are present, tie the $\overline{PD}$ pin to the positive supply voltage.

The disable operation is referenced from the negative supply (normally, ground). For split-supply operation, with the negative supply below ground, a disable control voltage below ground is required to turn the LMH5485-SEP off when the negative supply exceeds –0.7 V.

For single-supply operation, a minimum of 1.7 V above the negative supply (ground, in this case) is required to assure operation. This minimum logic-high level allows for direct operation from 1.8 V supply logic.

9.3.3 Input Overdrive Operation

The LMH5485-SEP input stage architecture is intrinsically robust to input overdrives with the series input resistor required by all applications. High input overdrives cause the outputs to limit into their maximum swings with the remaining input current through the Rg resistors absorbed by internal, back-to-back protection diodes across the two inputs. These diodes are normally off in application, and only turn on to absorb the currents that a large input overdrive might produce through the source impedance and or the series Rg elements required by all designs.

The internal input diodes can safely absorb up to ±15 mA in an overdrive condition. For designs that require more current to be absorbed, consider adding an external protection diode such as BAV99.

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9.4 Device Functional Modes

This wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either *on* with the $\overline{PD}$ pin asserted to a voltage greater than (Vs–) + 1.7 V or turned *off* by asserting $\overline{PD}$ low. Disabling the amplifier shuts off the quiescent current and stops the correct amplifier operation. The signal path is still present for the source signal through the external resistors.

The V_{OCM} control pin sets the output average voltage. Left open, V_{OCM} defaults to an internal mid-supply value. Driving this high-impedance input with a voltage reference within its valid range sets a target for the internal Vcm error amplifier.

9.4.1 Operation from Single-Ended Sources to Differential Outputs

One of the most useful features supported by the FDA device is an easy conversion from a single-ended input to a differential output centered on a user-controlled, common-mode level. While the output side is relatively straightforward, the device input pins move in a common-mode sense with the input signal. This common-mode voltage at the input pins moving with the input signal acts to increase the apparent input impedance to be greater than the Rg value. This input active impedance issue applies to both AC- and DC-coupled designs, and requires somewhat more complex solutions for the resistors to account for this active impedance, as shown in the following subsections.

9.4.1.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversion

When the signal path can be AC-coupled, the DC biasing for the LMH5485-SEP becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The AC-coupling issue can be separated for the input and output sides of an FDA design. In any case, the design starts by setting the desired V_{OCM}. When an AC-coupled path follows the output pins, the best linearity is achieved by operating V_{OCM} at mid-supply. The V_{OCM} voltage must be within the linear range for the common-mode loop, as specified in the headroom specifications (approximately 0.91 V greater than the negative supply and 1.1 V less than the positive supply). If the output path is also AC coupled, simply letting the V_{OCM} control pin float is usually preferred in order to get a mid-supply default V_{OCM} bias with minimal elements. To limit noise, place a 0.1 µF decoupling capacitor on the V_{OCM} pin to ground.

After V_{OCM} is defined, check the target output voltage swing to ensure that the V_{OCM} plus the positive or negative output swing on each side does not clip into the supplies. Check that V_{OCM} ±Vp does not exceed the absolute supply rails for this rail-to-rail output (RRO) device.

Going to the device input pins side, because both the source and balancing resistor on the nonsignal input side are DC blocked (see Figure 8-1), no common-mode current flows from the output common-mode voltage, thus setting the input common-mode equal to the output common-mode voltage.

This input headroom also sets a limit for higher V_{OCM} voltages. Because the input Vicm is the output V_{OCM} for AC-coupled sources, the 1.2 V minimum headroom for the input pins to the positive supply overrides the 1.1 V headroom limit for the output V_{OCM}. The input signal also moves this input Vicm around the DC bias point.

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9.4.1.2 DC-Coupled Input Signal Path Considerations for Single-Ended to Differential Conversion

The output considerations remain the same as for the AC-coupled design. Again, the input can be DC-coupled while the output is AC-coupled. A DC-coupled input with an AC-coupled output might have some advantages to move the input Vicm down if the source is ground referenced. Figure 8-2 shows how when the source is DC-coupled into the LMH5485-SEP, both sides of the input circuit must be DC coupled to retain differential balance. Normally, the nonsignal input side has an Rg element biased to whatever the source midrange is expected to be. Providing this midscale reference gives a balanced differential swing around V_{OCM} at the outputs.

One significant consideration for a DC-coupled input is that V_{OCM} sets up a common-mode bias current from the output back through Rf and Rg to the source on both sides of the feedback. Without input balancing networks, the source must sink or source this DC current. After the input signal range and biasing on the other Rg element is set, check that the voltage divider from V_{OCM} to Vin through Rf and Rg (and possibly Rs) establishes an input Vicm at the device input pins that is in range. If the average source is at ground, the negative rail input stage for the LMH5485-SEP is in range for applications using a single positive supply and a positive output V_{OCM} setting because this DC current lifts the average FDA input summing junctions up off of ground to a positive voltage (the average of the V+ and V– input pin voltages on the FDA).

9.4.2 Differential-Input to Differential-Output Operation

In many ways, this method is a much simpler way to operate the FDA from a design equations perspective. Assuming the two sides of the circuit are balanced with equal Rf and Rg elements, the differential input impedance is the sum of the two Rg elements to a differential inverting summing junction. In these designs, the input common-mode voltage at the summing junctions does not move with the signal, but must be DC biased in the allowable range for the input pins with consideration given to the voltage headroom required from each supply. Slightly different considerations apply to AC- or DC-coupled, differential-in to differential-out designs, as described in the following sections.

9.4.2.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

There are two typical ways to use the LMH5485-SEP with an AC-coupled differential source. In the first method, the source is differential and can be coupled in through two blocking capacitors. The second method uses either a single-ended or a differential source and couples in through a transformer (or balun). Figure 9-1 shows a typical blocking capacitor approach to a differential input. An optional input differential termination resistor (Rm) is included in this design. This Rm element allows the input Rg resistors to be scaled up while still delivering lower differential input impedance to the source. In this example, the Rg elements sum to show a 200 Ω differential impedance, while the Rm element combines in parallel to give a net 100 Ω, AC-coupled, differential impedance to the source. Again, the design proceeds ideally by selecting the Rf element values, then the Rg to set the differential gain, then an Rm element (if needed) to achieve a target input impedance. Alternatively, the Rm element can be eliminated, the Rg elements set to the desired input impedance, and Rf set to the get the differential gain (= Rf / Rg).

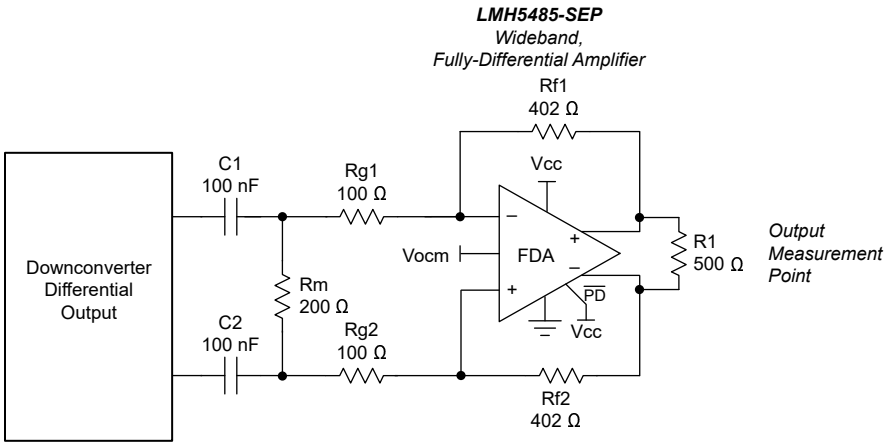


Figure 9-1. Down-Converting Mixer Delivering an AC-Coupled Differential Signal to the LMH5485-SEP

The DC biasing here is very simple. The output V_{OCM} is set by the input control voltage. Because there is no DC current path for the output common-mode voltage, that DC bias also sets the input pins common-mode operating points.

Transformer input coupling allows either a single-ended or differential source to be coupled into the LMH5485-SEP, which also improves the input-referred noise figure. These designs assume a source impedance that must be matched in the balun interface. Figure 9-2 shows the simplest approach where an example 1:2 turns ratio step-up transformer is used from a 50 Ω source.

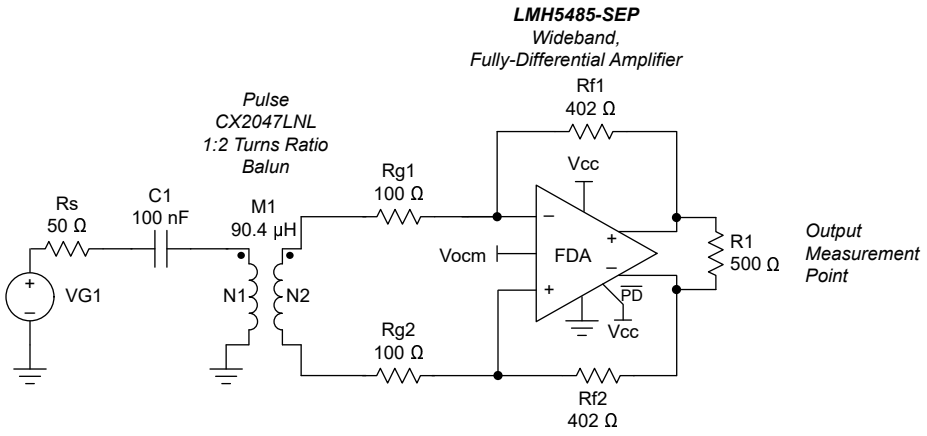


Figure 9-2. Input Balun Interface Delivers a Differential Input to the LMH5485-SEP

In this example, this 1:2 turns ratio step-up transformer provides a source and load match from the 50 Ω source if the secondary is terminated in 200 Ω (turns-ratio squared is the impedance ratio across a balun). The two Rg elements provide that termination as they sum to the differential virtual ground at the FDA summing junctions. The input blocking cap (C1) is optional and included only to eliminate DC shorts to ground from the source. This solution often improves the total noise figure compared to using just the FDA, as it allows for the noise gain of the amplifier to be reduced.

9.4.2.2 DC-Coupled, Differential-Input to Differential-Output Design Issues

Operating the LMH5485-SEP with a DC-coupled differential input source is very simple and only requires that the input pins stay in range of the DC common-mode operating voltage. One example is a DC-to-50 MHz quadrature down-converter output. These outputs typically sit on a DC level with some internal source impedance to the external loads. The example of Figure 9-3 shows a design using the LMH5485-SEP with a simple, passive RLC filter to the inputs (the Rg elements act as the differential termination for the filter design). From the original source behind the internal 250 Ω outputs, this circuit is a gain of 1 to the LMH5485-SEP output pins. The DC common-mode operating voltage level shifts from the 1.2 V internal, to the mixer, to an output at the ADC Vcm voltage of 0.95 V. In this case, a simple average of the two DC voltages in the gain of 1 stage gives a 1.08 V input pin common-mode result that is well within range.

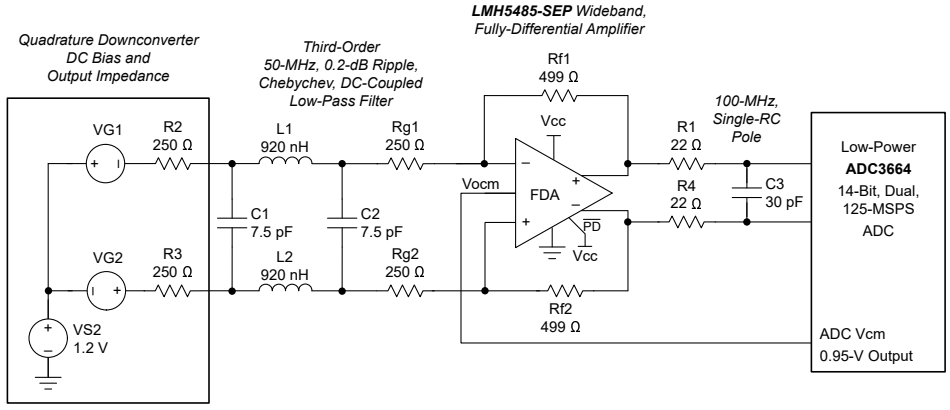


Figure 9-3. Example DC-Coupled, Differential I/O Design from a Quadrature Mixer to an ADC

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LMH5485-SEP offers an effective solution over a broad range of applications. Two examples are developed here. First, an attenuator stage that directly receives a higher input signal voltage and translates it to a lower differential swing on a fixed common-mode is shown. This design requires some attention to frequency-response flatness issues, and one approach to managing these issues is shown. The second example is a gain of 2 V/V, matched input of 50 Ω to an output set to 0.95 V common-mode followed by a third-order Bessel filter with approximately 20 MHz of bandwidth, designed for interfacing with a high-speed ADC.

10.2 Typical Applications

10.2.1 Designing Attenuators

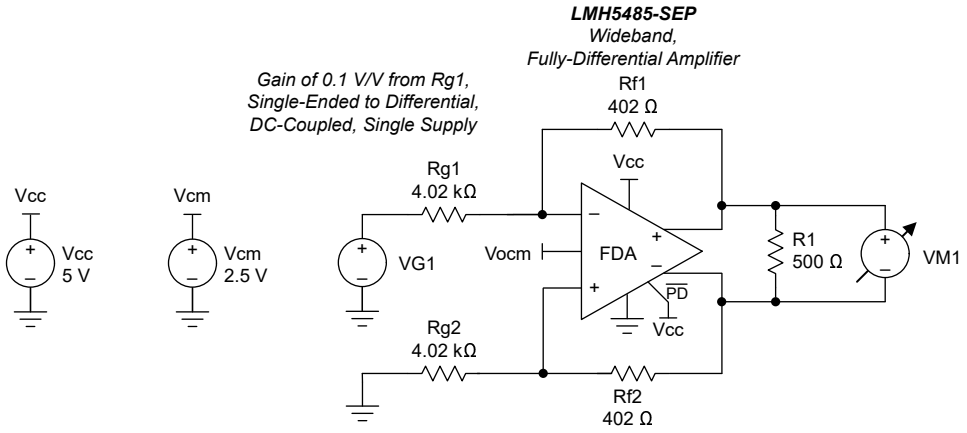


Figure 10-1. Divide-by-10 Attenuator Application for the LMH5485-SEP

10.2.1.1 Design Requirements

In this design, the aim is to do the following:

1. Present a 4 kΩ input impedance to a ±40 V input signal (maximum ±10 mA from the prior stage).
2. Attenuate that swing by a factor 1/10 (–20 dB) to a differential output swing.
3. Place that swing on a 2.5 V common-mode voltage at the LMH5485-SEP outputs.
4. Operate on a single + 5 V supply and ground.
5. Tune the frequency response to a flat Butterworth response with external capacitors.

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10.2.1.2 Detailed Design Procedure

Operating the LMH5485-SEP at a low DC noise gain, or with higher feedback resistors, can cause a lower phase margin to exist, giving the response peaking shown in Figure 10-3 for the gain of 0.1 (a 1/10 attenuator) condition. Although it is often useful operating the LMH5485-SEP as an attenuator (taking a large input range to a purely differential signal around a controlled-output, common-mode voltage), the response peaking illustrated in Figure 10-3 is usually undesirable. Several methods can be used to reduce or eliminate this peaking; usually, at the cost of higher output noise. Using DC techniques always increases the output noise broadband, while using an ac noise-gain-shaping technique peaks the noise, but only at higher frequencies that can then be filtered off with the typical passive filters often used after this stage. Figure 10-1 shows a simplified schematic for the gain of 0.1 V/V test from Figure 8-1.

This configuration simulates to a nominal 18° phase margin; therefore, a very highly-peaked response is shown in Figure 10-3. This peaking can be eliminated by placing two feedback capacitors across the Rf elements and a differential input capacitor. Adding these capacitors provides a transition from a resistively set noise gain to a capacitive divider at high-frequency flattening out to a higher noise gain (NG2 here). The key for this approach is to target a Zo, where the noise gain begins to peak up. Using only the following terms, and targeting a closed-loop flat (Butterworth) response, gives this solution sequence for Zo and then the capacitor values.

1. Gain bandwidth product in Hz (850 MHz for the LMH5485-SEP)
2. Low frequency noise gain, NG1 (= 1.1 in the attenuator gain of 0.1 V/V design)
3. Target high-frequency noise gain selected to be higher than NG1 (NG2 = 3.1 V/V is selected for this design)
4. Feedback resistor value, Rf (assumed balanced for this differential design = 402 Ω for this design example)

From these elements, for any decompensated voltage-feedback op amp or FDA, solve for Zo (in Hz) using Equation 1:

$$Zo = \frac{GBP}{NG1^2}\left(1 - \frac{NG1}{NG2} - \sqrt{1 - 2\frac{NG1}{NG2}}\right) \tag{1}$$

From this target zero frequency in the noise gain, solve for the feedback capacitors using Equation 2:

$$Cf = \frac{1}{2\pi \bullet Rf \bullet Zo \bullet NG2} \tag{2}$$

The next step is to resolve the input capacitance on the summing junction. Equation 3 is for a single-ended op amp where that capacitor goes to ground. To use Equation 3 for a voltage-feedback FDA, cut the target value in half, and place the result across the two inputs (reducing the external value by the specified internal differential capacitance).

$$Cs = (NG2 - 1)Cf \tag{3}$$

Setting the external compensation elements using Equation 1 to Equation 3 allows an estimate of the resulting flat bandwidth f_{-3dB} frequency, as shown in Equation 4:

$$f_{-3dB} \approx \sqrt{GBP \bullet Zo} \tag{4}$$

Running through these steps for the LMH5485-SEP in the attenuator circuit of Figure 10-1 gives the proposed compensation of Figure 10-2 where Equation 4 estimates a bandwidth of 252 MHz (Zo target is 74.7 MHz).

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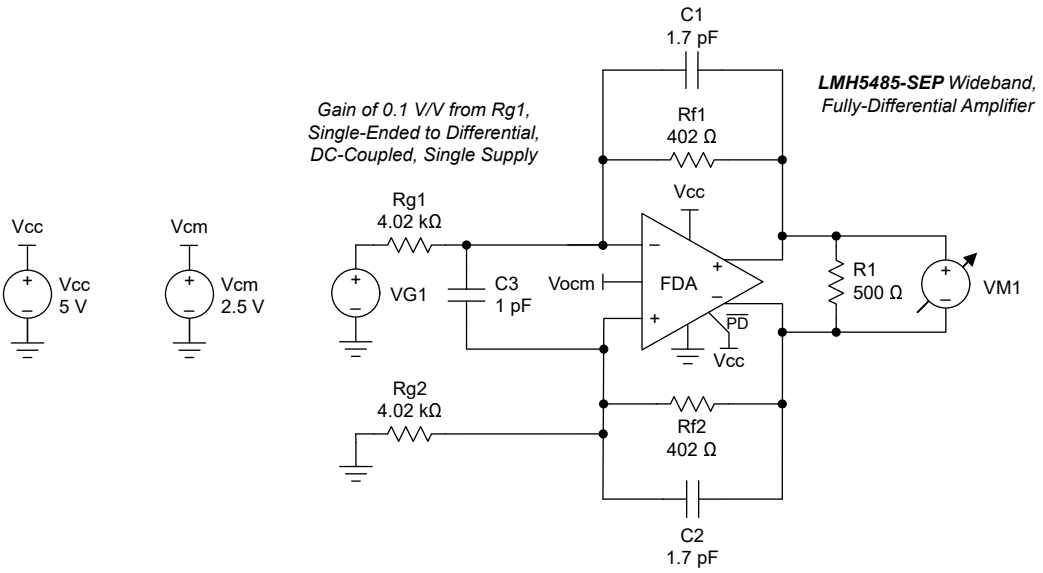


Figure 10-2. Compensated Attenuator Circuit Using the LMH5485-SEP

The 1 pF across the inputs is really a total 1.9 pF, including the internal differential capacitance. These two designs (with and without the capacitors) were both bench tested and simulated using the LMH5485-SEP TINA model giving the results of Figure 10-3.

This method does a good job of flattening the response for what starts out as a low phase-margin attenuator application. The simulation model does a very good job of predicting the peaking and showing the same improvement with the external capacitors; both giving a flat, approximately 250 MHz, closed-loop bandwidth for this gain of a 0.1 V/V design. In this example, the output noise begins to peak up (as a result of the noise-gain shaping of the capacitors) above 70 MHz. Use postfiltering to minimize any increase in the integrated noise using this technique. Using this solution to deliver an 8 V_{PP} differential output to a successive approximation register (SAR) ADC (using the 2.5 V V_{OCM} shown), the circuit accepts up to ±40 V inputs, where the 4 kΩ input Rg1 draws ±10 mA from the source.

10.2.1.3 Application Curve

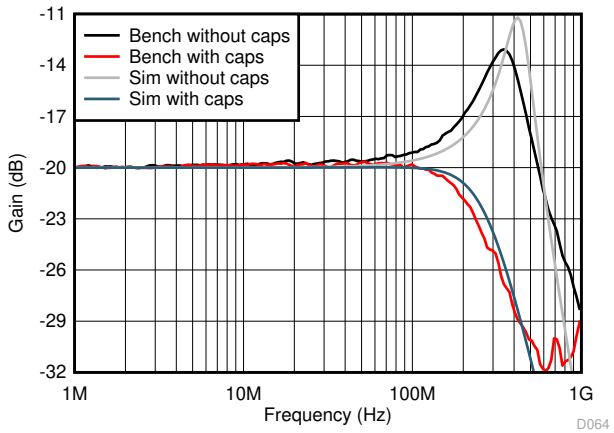


Figure 10-3. Attenuator Response Shapes with and without External Compensation

10.2.2 Interfacing to High-Performance ADCs

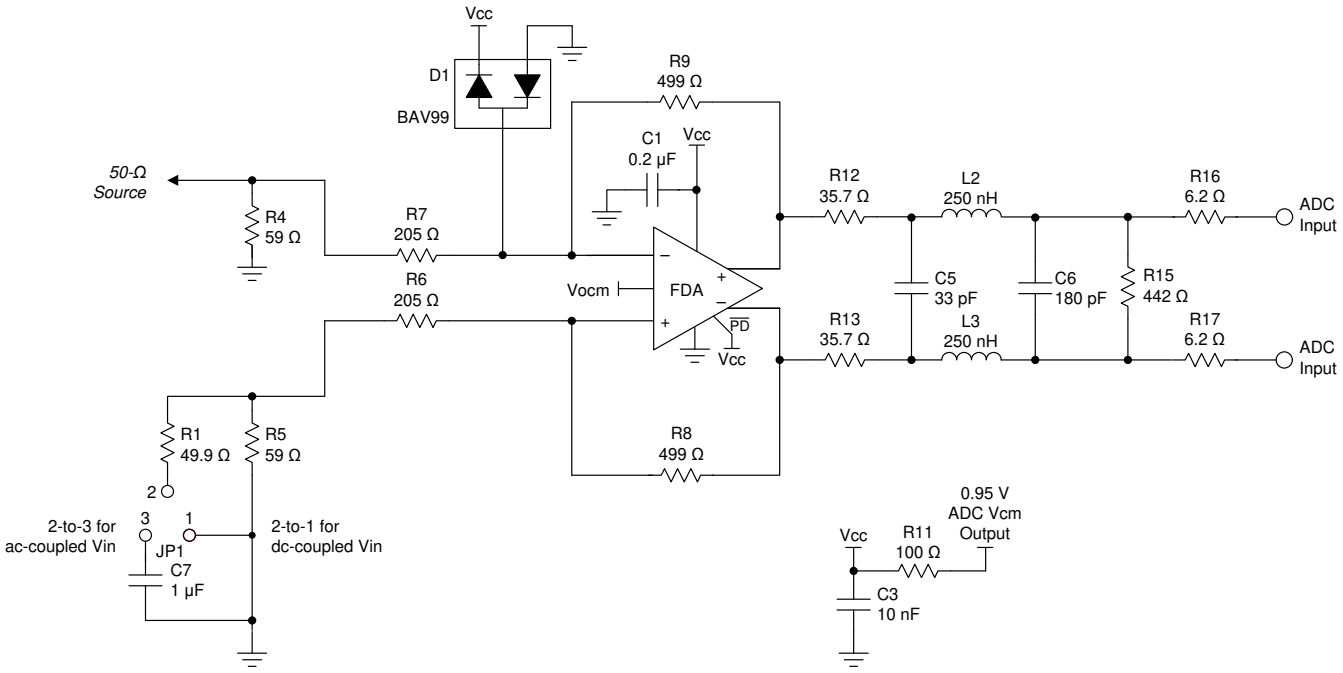


Figure 10-4. DC-Coupled, Bipolar Input Gain of 2 V/V Single-Ended to Differential Interface to ADC

10.2.2.1 Design Requirements

In this example design, an impedance matched input assuming a 50 Ω source is implemented with a DC-coupled gain of 2 V/V to the ADC. This configuration effectively reduces the required full-scale input to ±0.5 V for a 2 V_{PP} full-scale input ADC. Add a low insertion-loss interstage filter to the ADC to control the broadband noise where the goal is to show minimal SNR reduction in the FFT, as well as minimal degradation in SFDR performance.

10.2.2.2 Detailed Design Procedure

The LMH5485-SEP provides a simple interface to a wide variety of precision SAR, ΔΣ, or higher-speed pipeline ADCs. To deliver the exceptional distortion at the output pins, considerably wider bandwidth than typically required in the signal path to the ADC inputs is provided by the LMH5485-SEP. For instance, the gain of 2 single-ended to differential design example provides approximately a 500 MHz, small-signal bandwidth. Even if the source signal is Nyquist bandlimited, this broad bandwidth can possibly integrate enough LMH5485-SEP noise to degrade the SNR through the ADC if the broadband noise is not bandlimited between the amplifier and ADC. Figure 10-4 shows an example DC-coupled, gain of 2 interface with a controlled, interstage-bandwidth filter.

Designed for a DC-coupled 50 Ω input match, this design starts with a 499 Ω feedback resistor, and provides a gain of 2.35 V/V to the LMH5485-SEP output pins. The third-order interstage, low-pass filter provides a 20 MHz Bessel response with a 0.85 V/V insertion loss to the ADC, providing a net gain of 2 V/V from board edge to the ADC inputs. Although the LMH5485-SEP can absorb overdrives, an external protection element is added using the BAV99 low-capacitance device, shown in Figure 10-4. For DC-coupled testing, pins 1 and 2 of JP1 are jumpered together. When the source is an AC-coupled, 50 Ω source, pins 2 and 3 of JP1 are jumpered to maintain differential balance.

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11 Power Supply Recommendations

The LMH5485-SEP is principally intended to operate with a nominal single-supply voltage of +3 V to +5 V. Supply decoupling is required, as described in the *Layout Guidelines*. The amplifier signal path is flexible for single or split-supply operation. Most applications are intended to be single supply, but any split-supply design can be used, as long as the total supply across the LMH5485-SEP is less than 5.25 V and the required input, output, and common-mode pin headrooms to each supply are observed. Left open, the V_{OCM} pin defaults to near mid-supply for any combination of split or single supplies used. The disable pin is negative-rail referenced. Using a negative supply requires the disable pin to be pulled down to within 0.7 V of the negative supply to disable the amplifier.

12 Layout

12.1 Layout Guidelines

Similar to all high-speed devices, best system performance is achieved with a close attention to board layout. The LMH5485-SEP evaluation module (EVM) shows a good example of high frequency layout techniques as a reference. This EVM includes numerous extra elements and features for characterization purposes that may not apply to some applications. General high-speed, signal-path layout suggestions include the following:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs; however, ground and power planes around the capacitive sensitive input and output device pins should be open. After the signal is sent into a resistor, the parasitic capacitance becomes more of a band limiting issue and less of a stability issue.
- Use good, high-frequency decoupling capacitors (0.1 µF) on the ground plane at the device power pins. Higher value capacitors (2.2 µF) are required, but may be placed further from the device power pins and shared among devices. A supply decoupling capacitor across the two power supplies (for bipolar operation) should also be added. For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- For each LMH5485-SEP, attach a separate 0.1 µF capacitor to a nearby ground plane. With cascaded or multiple parallel channels, including ferrite beads from the larger capacitor is often useful to the local high-frequency decoupling capacitor.
- When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces.
- The input summing junctions are very sensitive to parasitic capacitance. Connect any Rg elements into the summing junction with minimal trace length to the device pin side of the resistor. The other side of the Rg elements can have more trace length if needed to the source or to ground.

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Design for a Wideband, Differential Transimpedance DAC Output* application report
- Texas Instruments, *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts* reference guide
- Texas Instruments, *LMH6554 2.8-GHz Ultra Linear Fully Differential Amplifier* data sheet
- Texas Instruments, *Maximizing the dynamic range of analog front ends having a transimpedance amplifier* technical brief
- Texas Instruments, Fully Differential Amplifiers application note
- Texas Instruments, Maximizing Signal Chain Distortion Performance Using High Speed Amplifiers application note
- Texas Instruments, TI Precision Labs - Fully Differential Amplifiers video series

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

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13.5 Electrostatic Discharge Caution



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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH5485DGKSEP	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	5485

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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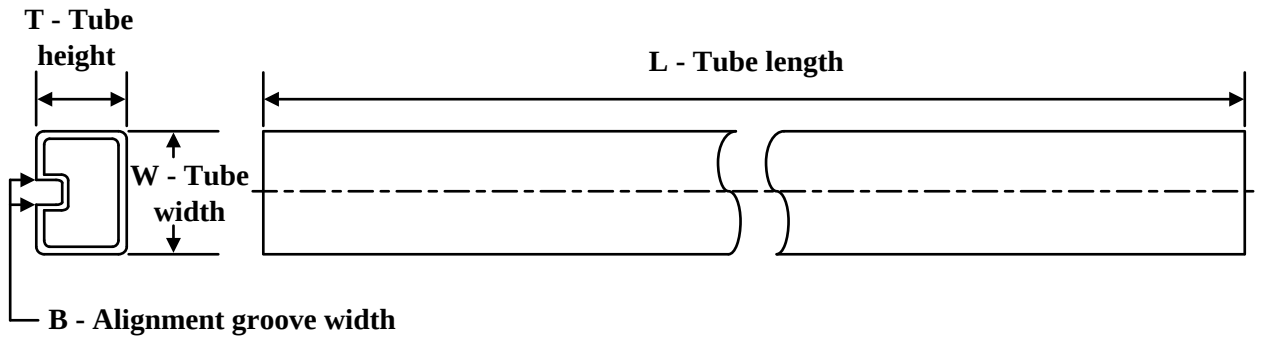
OTHER QUALIFIED VERSIONS OF LMH5485-SEP :

- Space : LMH5485-SP

NOTE: Qualified Version Definitions:

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TUBE



*All dimensions are nominal

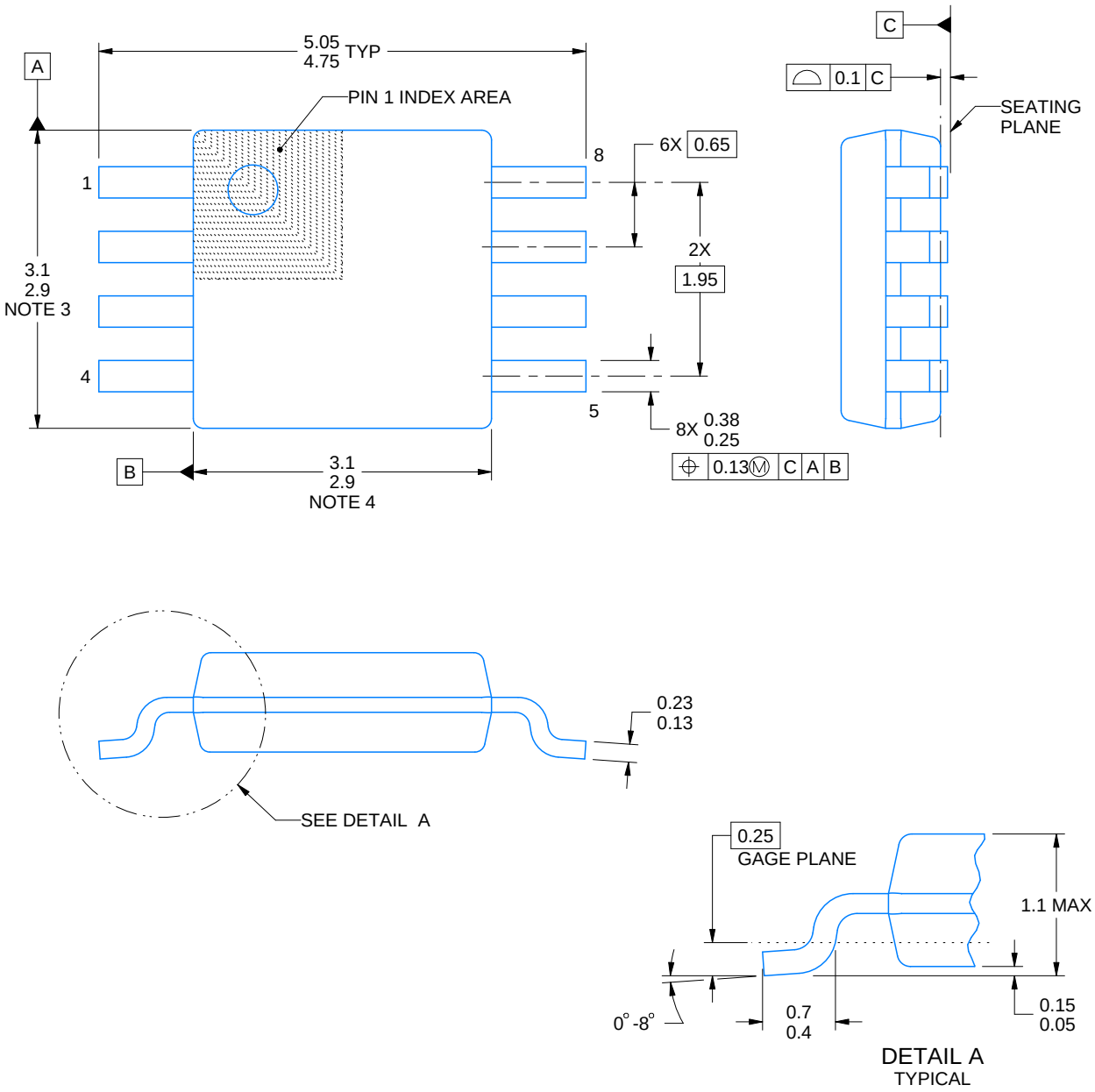
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH5485DGKSEP	DGK	VSSOP	8	80	330.2	6.6	3005	1.88

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

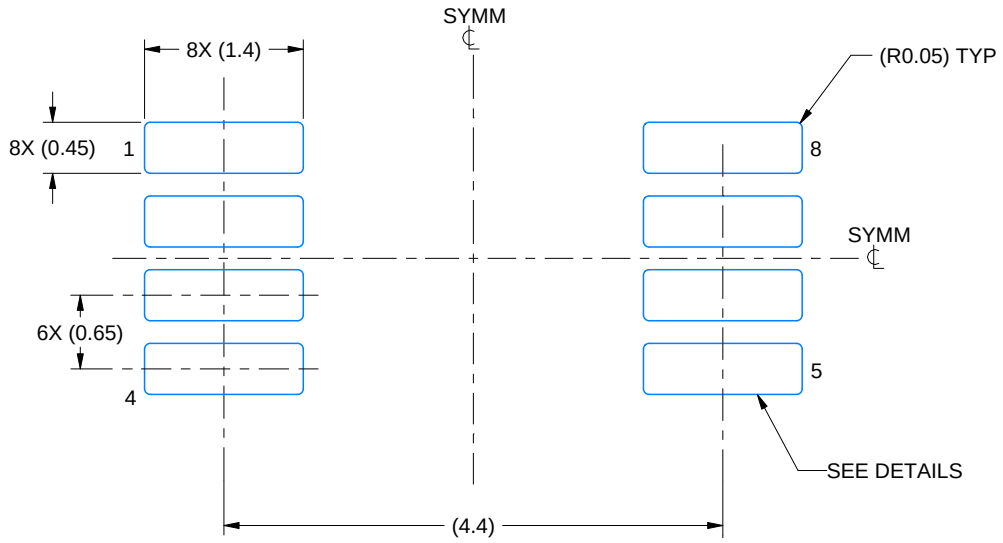
SMALL OUTLINE PACKAGE



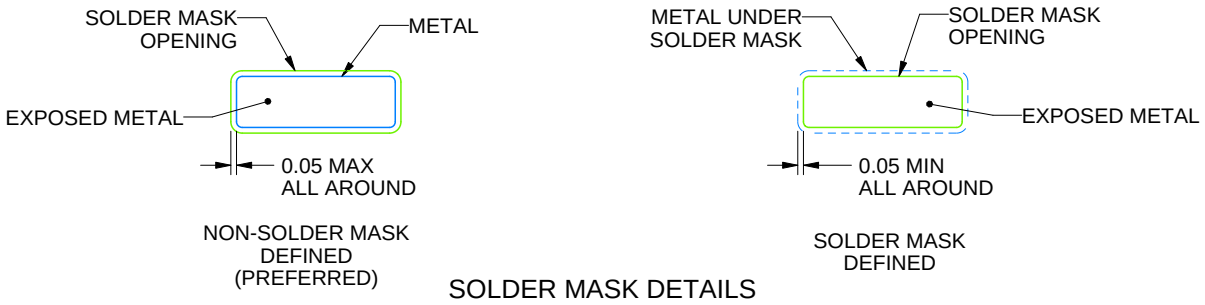
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

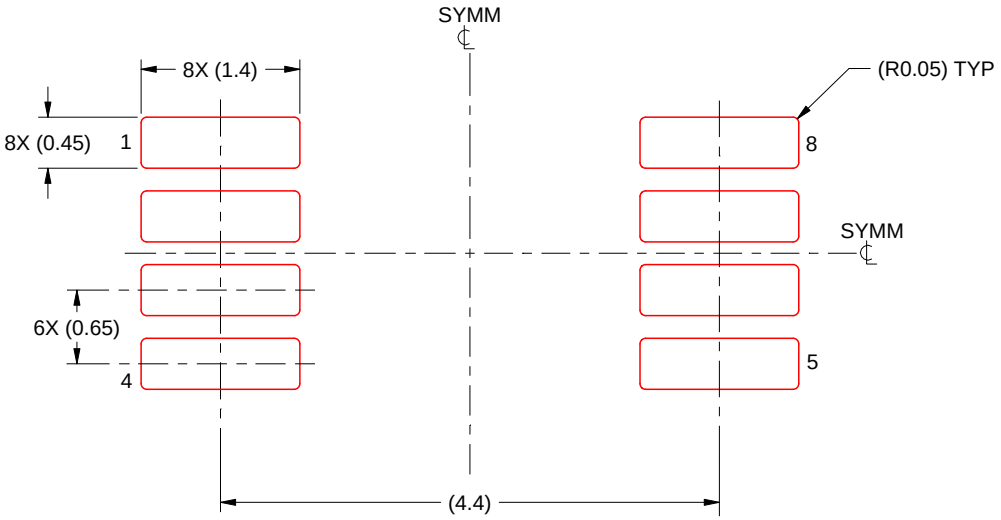


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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