LM7321x Single and LM7322x Dual Rail-to-Rail Input and Output ±15V, High-Output Current and Unlimited Capacitive Load Operational Amplifier

1 Features

- (V_S = ±15, T_A = 25°C, typical values unless specified.)
- Wide supply voltage range: 2.7V to 32V
- Output current: ±125mA
- Gain bandwidth product: 24MHz
- Slew rate: 35V/µs
- Unlimited capacitive load tolerance
- Input common-mode voltage: 0.1V beyond rails
- Input voltage noise: 12nV/$\sqrt{Hz}$
- Input current noise: 1pA/$\sqrt{Hz}$
- Supply current/channel 1.35mA
- Distortion THD+Noise: −113dB
- Temperature range: −40°C to 125°C
- LM732xx are automotive grade products that are AEC-Q100 Grade 1 Qualified

2 Applications

- Driving MOSFETs and power transistors
- Capacitive proximity sensors
- Driving analog optocouplers
- High-side sensing
- Below ground current sensing
- Photodiode biasing
- Driving varactor diodes in PLLs
- Wide voltage range power supplies
- Automotive
- International power supplies

3 Description

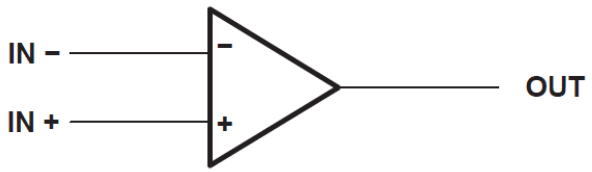
The LM732xx devices are rail-to-rail input and output amplifiers with wide operating voltages and high-output currents. The LM732xx family is efficient, achieving 35V/µs slew rate and 24MHz unity gain bandwidth while requiring only 1.35mA of supply current per op amp. The LM732xx device performance is fully specified for operation at 2.7V, ±5V, and ±15V.

The LM732xx devices are designed to drive unlimited capacitive loads without oscillations. Greater than rail-to-rail input common-mode voltage range with 90dB of common-mode rejection across this wide voltage range allows both high-side and low-side sensing. Most device parameters are insensitive to power supply voltage, and making the parts easier to use where supply voltage can vary, such as automotive electrical systems and battery powered equipment.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM7321	D (SOIC, 8)	4.90mm × 3.90mm
	DBV (SOT-23, 5)	2.90mm × 1.60mm
LM7322	DGK (VSSOP, 8)	3.00mm × 3.00mm
	D (SOIC, 8)	4.90mm × 3.90mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol (each amplifier)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

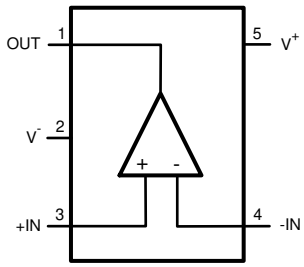


Figure 4-1. DBV Package 5-Pin SOT-23 Top View

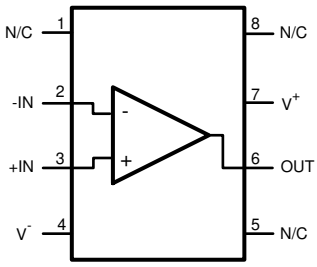


Figure 4-2. D Package 8-Pin SOIC Top View

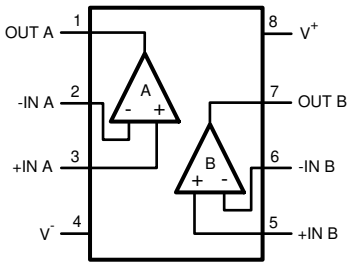


Figure 4-3. DGK Package 8-Pin VSSOP or SOIC Top View

Table 4-1. Pin Functions

PIN				TYPE[1]	DESCRIPTION
NAME	SOT-23 NO.	SOIC NO.	VSSOP, SOIC NO.		
OUT	1	6	—	O	Output
OUT A	—	—	1	O	Output for Amplifier A
OUT B	—	—	7	O	Output for Amplifier B
V+	5	7	8	P	Positive Supply
V–	2	4	4	P	Negative Supply
+IN	3	3	—	I	Non-inverting Input
–IN	4	2	—	I	Inverting Input
+IN A	—	—	3	I	Non-inverting Input for Amplifier A
–IN A	—	—	2	I	Inverting Input for Amplifier A
+IN B	—	—	5	I	Non-inverting Input for Amplifier B
–IN B	—	—	6	I	Inverting Input for Amplifier B
N/C	—	1, 5, 8	—	—	No connection

(1) I = input, O = output, P = power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	33	V
Signal input pins	Common-mode voltage(3)	(V–) –0.5	(V+) +0.5	V
	Differential voltage(4)		±10	V
	Current(3)		±10	mA
Output short-circuit(2)		Continuous		
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(4) Input pins are connected by back-to-back diodes for input protection. If the differential input voltage may exceed 0.5V, limit the input current to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(3)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model	200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

5.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage (V_S = V^+ - V^-)	2.7	32	V
Temperature Range(1)	−40	125	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}) – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

5.4 Thermal Information

THERMAL METRIC(2)		LM732x			UNIT
		D (SOIC)	DBV (SOT)	DGK (VSSOP)	
		8 PINS	5 PINS	8 PINS	
$R_{\theta JA}$ (1)	Junction-to-ambient thermal resistance	133.5	185.4	169.6	°C/W

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}) – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7V to 32V (±1.35V to ±16V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = V–		–5	±0.35	+5	mV
			T_A = –40°C to +125°C	–6		+6	
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = V–			±2.5		µV/°C
I_B	Input Bias Current			–2	0.4		µA
			T_A = –40°C to +125°C	–2.5			
					0.4	1	
			T_A = –40°C to +125°C			1.5	
I_{OS}	Input Offset Current				7	200	nA
			T_A = –40°C to +125°C			300	
CMRR	Common-Mode Rejection Ratio	V_S = 32V, V– < V_{CM} < (V+) – 2V (Main Input Pair)	T_A = –40°C to 125°C	109	125		dB
		V_S = 5V, V– < V_{CM} < (V+) – 2V (Main Input Pair)(1)	T_A = –40°C to 125°C	93	111		
		V_S = 2.7V, V– < V_{CM} < (V+) – 2V (Main Input Pair)	T_A = –40°C to 125°C		114		
		V_S = 2.7 – 32V, (V+) – 1V < V_{CM} < V+ (Aux Input Pair)	T_A = –40°C to 125°C		77		
		(V+) – 2V < V_{CM} < (V+) – 1V	T_A = –40°C to 125°C	See Offset Voltage vs Common-Mode Voltage, New Die			
PSRR	Power Supply Rejection Ratio	V_{CM} = V–, V_S = 5V to 32V	T_A = –40°C to 125°C	78	104		dB
		V_{CM} = V–, V_S = 2.7V to 32V	T_A = –40°C to 125°C	74			
V_{CM}	Common-mode input voltage range			(V–) – 0.1		(V+) + 0.1	V
A_{VOL}	Open-Loop Voltage Gain	V_S = 32V, V_{CM} = V_S / 2, (V–) + 1V < V_O < (V+) – 1V		75	87		dB
			T_A = –40°C to 125°C	70	87		
		V_S = 5V, V_{CM} = V_S / 2, (V–) + 1V < V_O < (V+) – 1V(1)		74	80		
			T_A = –40°C to 125°C	70	80		
		V_S = 2.7V, V_{CM} = V_S / 2, (V–) + 1V < V_O < (V+) – 1V(1)		65	80		
			T_A = –40°C to 125°C	62	80		
V_{OUT}	Output Voltage Swing High	V_{ID} = 100mV			50	150	mV from either rail
			T_A = –40°C to +125°C			160	
		R_L = 2kΩ V_{ID} = 100mV			50	250	
			T_A = –40°C to +125°C			280	
	Output Voltage Swing Low	V_{ID} = –100mV			50	120	
			T_A = –40°C to +125°C			150	
		R_L = 2kΩ V_{ID} = –100mV			50	120	
			T_A = –40°C to +125°C			150	
I_{OUT}	Output Current	V_S = 32V		±40	±125		mA
		V_S = 5V(1)		±35	±85		
			T_A = –40°C to +125°C	±20			
		V_S = 2.7V(1)		±30	±60		
			T_A = –40°C to +125°C	±20			

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5.5 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 2.7V to 32V (±1.35V to ±16V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
I_S	Supply Current (per channel)				1.35	1.93	mA
			T_A = –40°C to +125°C			2.23	
SR	Slew Rate	A_V = +1, V_I = 10V Step			35		V/µs
f_u	Unity Gain Frequency	R_L = 2kΩ, C_L = 20pF			11		MHz
GBW	Gain Bandwidth	f = 50kHz			24		MHz
e_n	Input Referred Voltage Noise Density	f = 2kHz			11.9		nV/√Hz
i_n	Input Referred Current Noise Density	f = 2kHz			0.5		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	V^+ = 1.9V, V^- = −0.8V f = 1kHz, R_L = 100kΩ, A_V = +2 V_{OUT} = 210mV_{PP}			−113		dB
CT Rej.	Crosstalk Rejection	f = 100kHz, Driver R_L = 10kΩ			60		dB

(1) Specified by characterization only.

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5.6 Typical Characteristics

Old Die : unless otherwise specified: T_A = 25°C. New Die : at T_A = 25°C, vs = ±16V, V_{CM} = vs / 2, R_L = 10kΩ (unless otherwise noted)

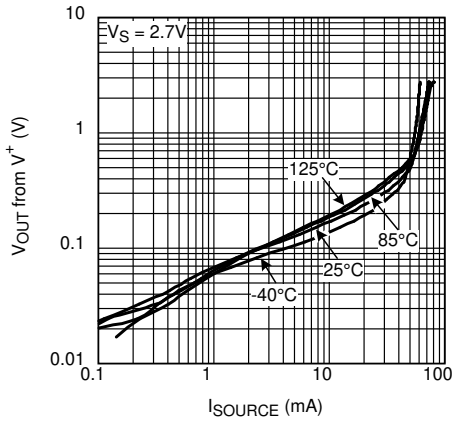


Figure 5-1. Output Swing vs Sourcing Current, Old Die

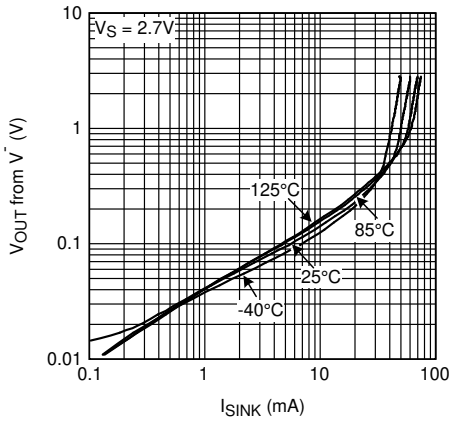


Figure 5-2. Output Swing vs Sinking Current, Old Die

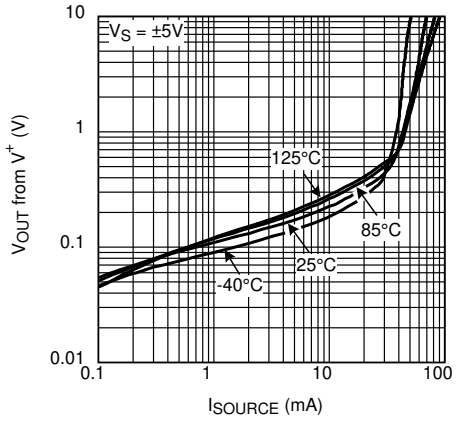


Figure 5-3. Output Swing vs Sourcing Current, Old Die

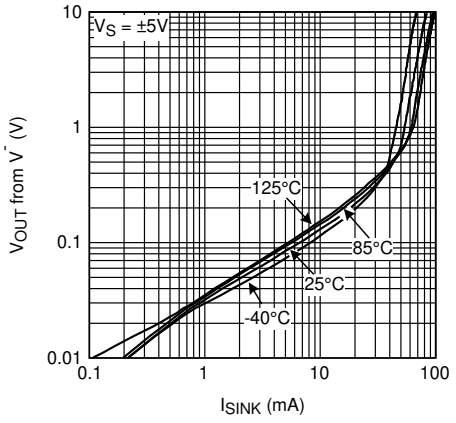


Figure 5-4. Output Swing vs Sinking Current, Old Die

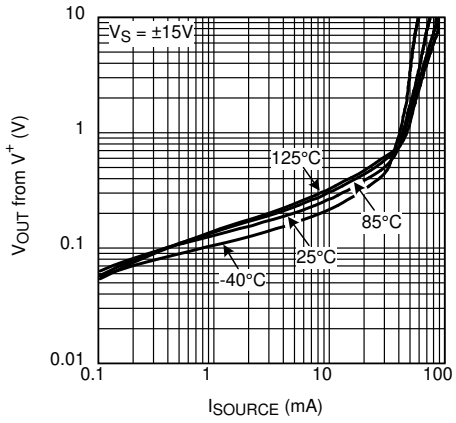


Figure 5-5. Output Swing vs Sourcing Current, Old Die

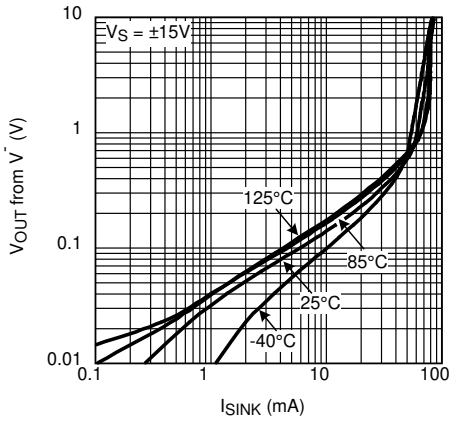


Figure 5-6. Output Swing vs Sinking Current, Old Die

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5.6 Typical Characteristics (continued)

Old Die : unless otherwise specified: T_A = 25°C. New Die : at T_A = 25°C, vs = ±16V, V_{CM} = vs / 2, R_L = 10kΩ (unless otherwise noted)

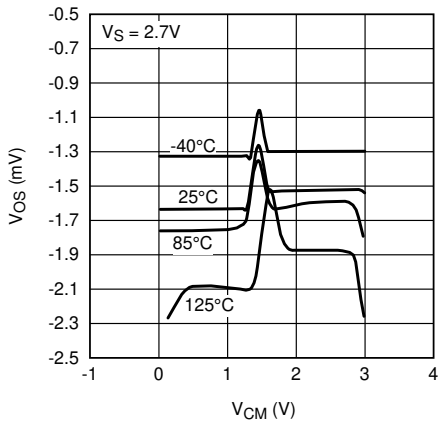


Figure 5-7. V_{OS} vs V_{CM} (Unit 1), Old Die

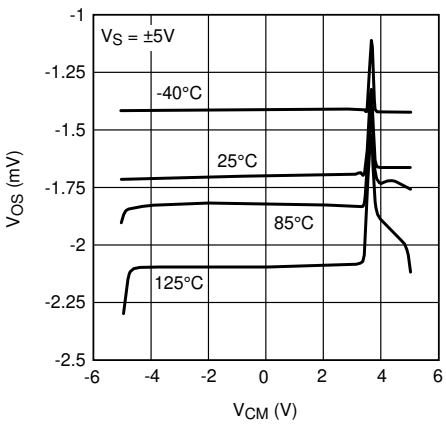


Figure 5-8. V_{OS} vs V_{CM} (Unit 1), Old Die

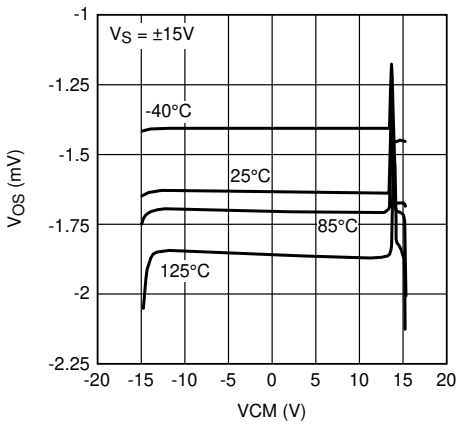


Figure 5-9. V_{OS} vs V_{CM} (Unit 1), Old Die

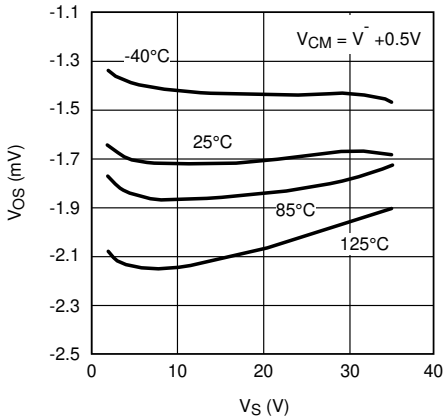


Figure 5-10. V_{OS} vs (Unit 1), Old Die

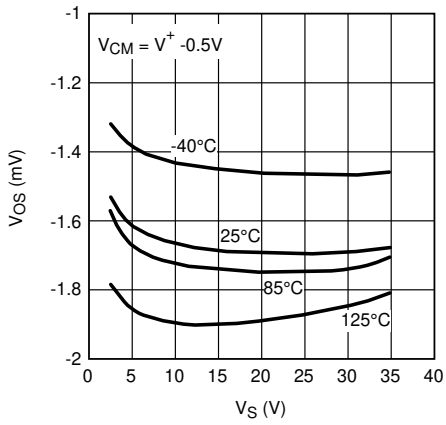


Figure 5-11. V_{OS} vs (Unit 1), Old Die

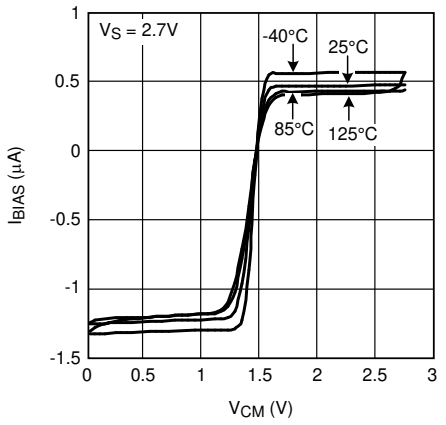


Figure 5-12. I_{BIAS} vs V_{CM}, Old Die

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5.6 Typical Characteristics (continued)

Old Die : unless otherwise specified: T_A = 25°C. New Die : at T_A = 25°C, vs = ±16V, V_{CM} = vs / 2, R_L = 10kΩ (unless otherwise noted)

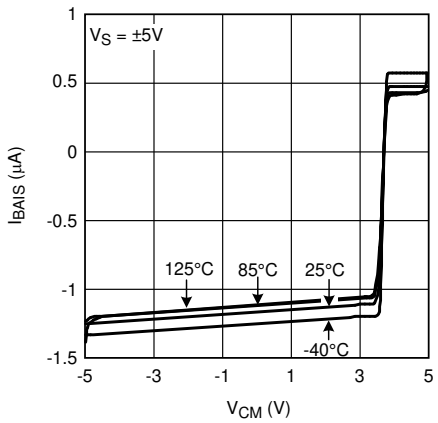


Figure 5-13. I_{BIAS} vs V_{CM}, Old Die

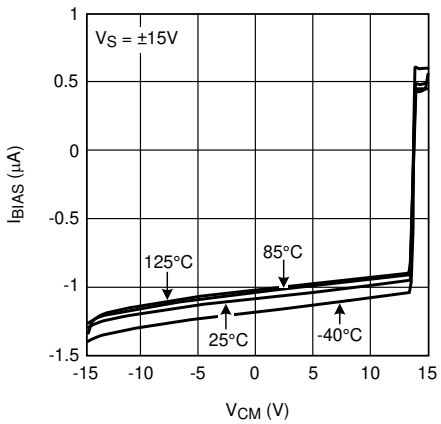


Figure 5-14. I_{BIAS} vs V_{CM}, Old Die

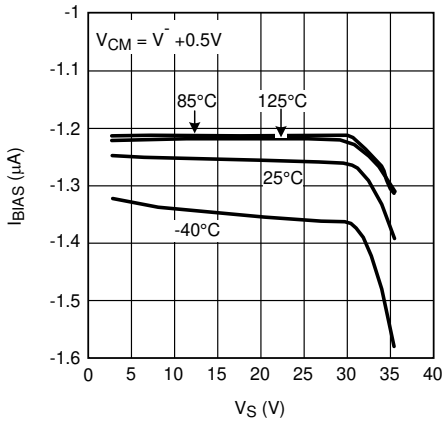


Figure 5-15. I_{BIAS} vs Old Die

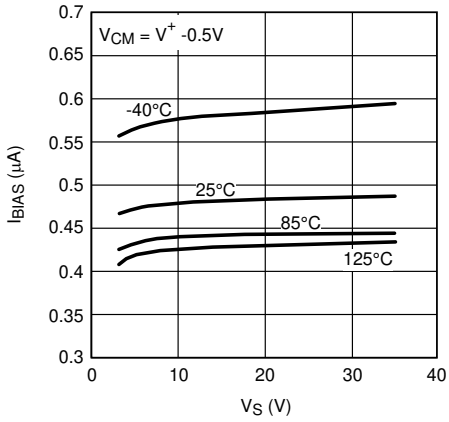


Figure 5-16. I_{BIAS} vs Old Die

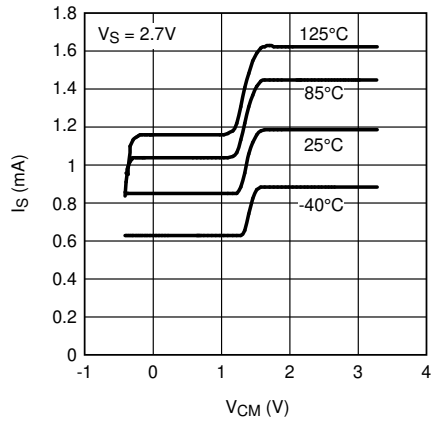


Figure 5-17. I_S vs V_{CM} (LM7321), Old Die

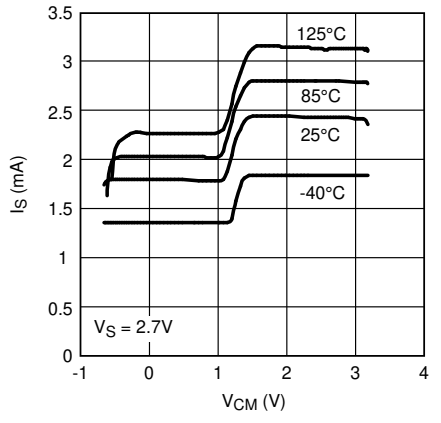


Figure 5-18. I_S vs V_{CM} (LM7322), Old Die

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5.6 Typical Characteristics (continued)

Old Die : unless otherwise specified: T_A = 25°C. New Die : at T_A = 25°C, vs = ±16V, V_{CM} = vs / 2, R_L = 10kΩ (unless otherwise noted)

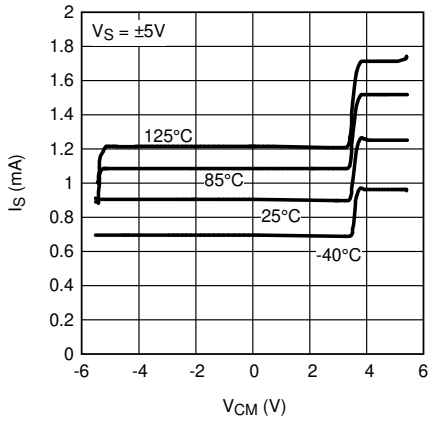


Figure 5-19. I_S vs V_{CM} (LM7321), Old Die

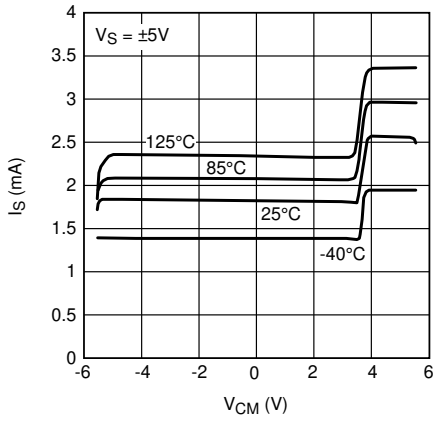


Figure 5-20. I_S vs V_{CM} (LM7322), Old Die

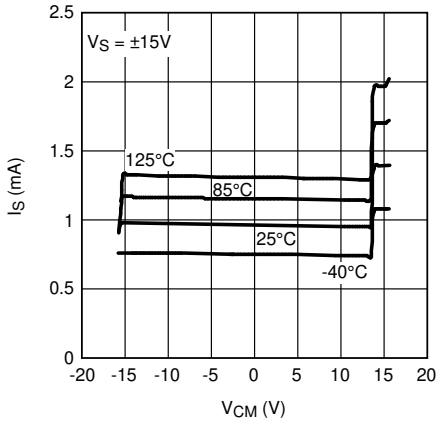


Figure 5-21. I_S vs V_{CM} (LM7321), Old Die

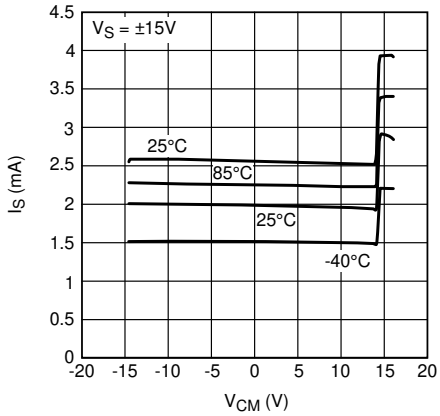


Figure 5-22. I_S vs V_{CM} (LM7322), Old Die

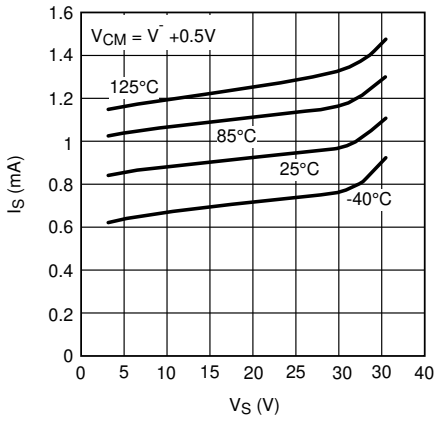


Figure 5-23. I_S vs (LM7321), Old Die

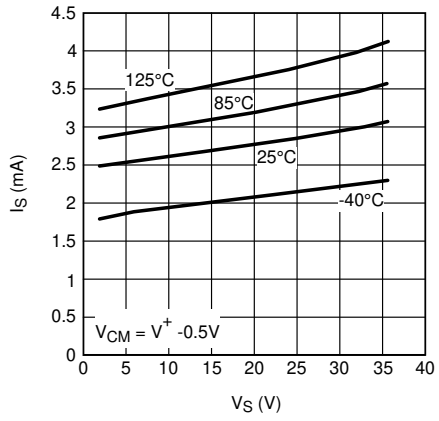


Figure 5-24. I_S vs (LM7322), Old Die

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5.6 Typical Characteristics (continued)

Old Die : unless otherwise specified: T_A = 25°C. New Die : at T_A = 25°C, vs = ±16V, V_{CM} = vs / 2, R_L = 10kΩ (unless otherwise noted)

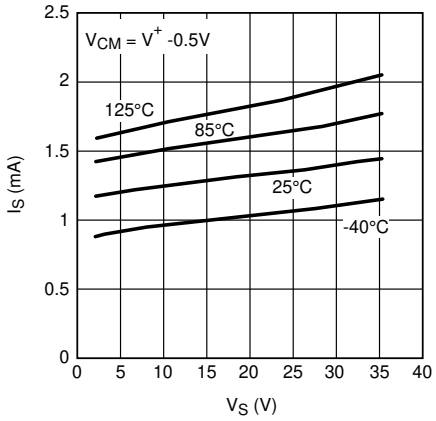


Figure 5-25. I_S vs (LM7321), Old Die

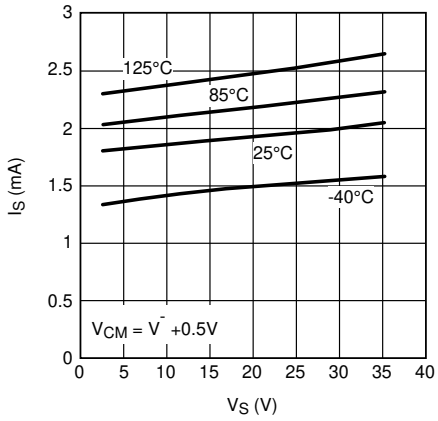


Figure 5-26. I_S vs (LM7322), Old Die

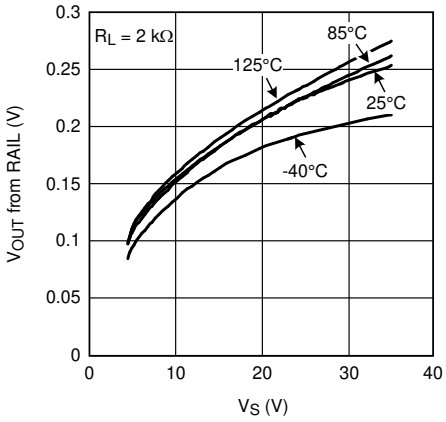


Figure 5-27. Positive Output Swing vs Supply Voltage, Old Die

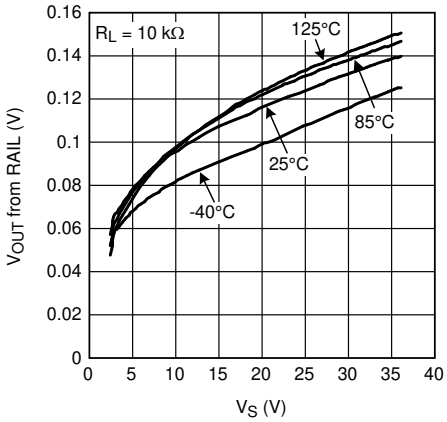


Figure 5-28. Positive Output Swing vs Supply Voltage, Old Die

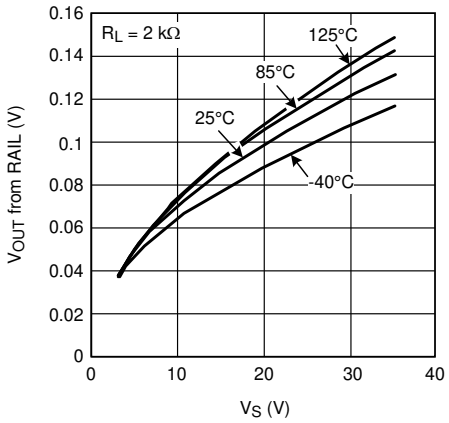


Figure 5-29. Negative Output Swing vs Supply Voltage, Old Die

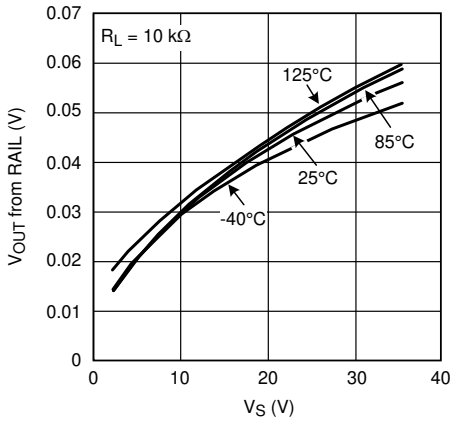


Figure 5-30. Negative Output Swing vs Supply Voltage, Old Die

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5.6 Typical Characteristics (continued)

Old Die : unless otherwise specified: T_A = 25°C. New Die : at T_A = 25°C, vs = ±16V, V_{CM} = vs / 2, R_L = 10kΩ (unless otherwise noted)

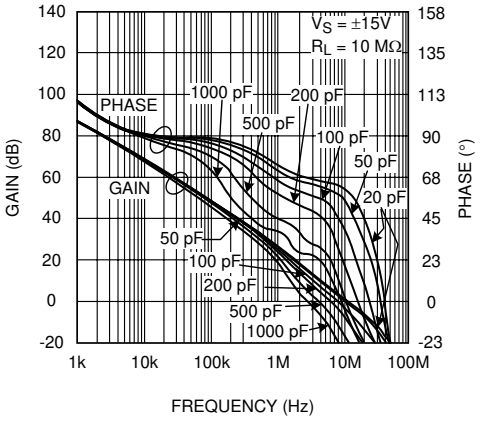


Figure 5-31. Open-Loop Frequency Response with Various Capacitive Load, Old Die

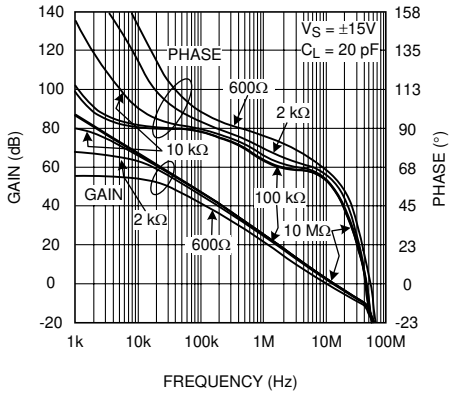


Figure 5-32. Open-Loop Frequency Response with Various Resistive Load, Old Die

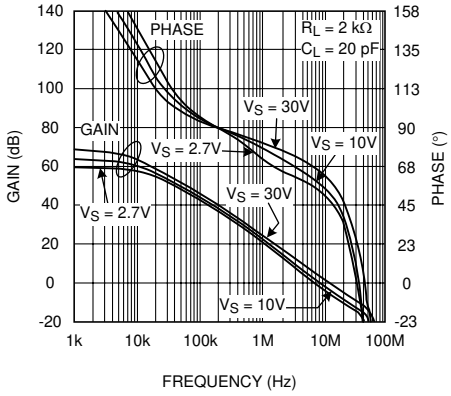


Figure 5-33. Open-Loop Frequency Response with Various Supply Voltage, Old Die

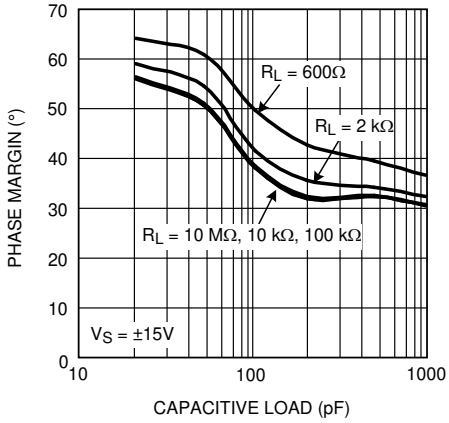


Figure 5-34. Phase Margin vs Capacitive Load, Old Die

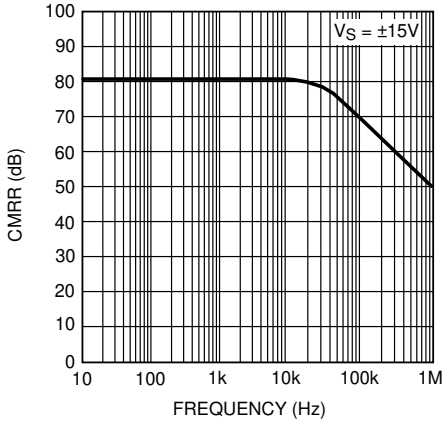


Figure 5-35. CMRR vs Frequency, Old Die

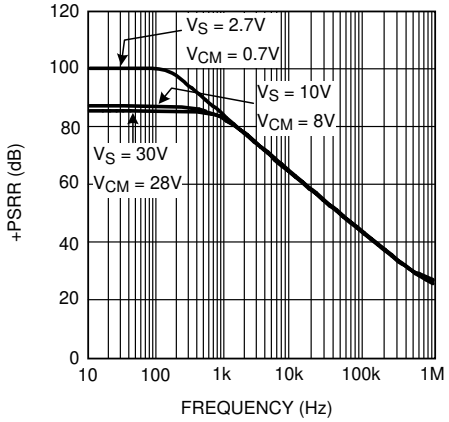


Figure 5-36. +PSRR vs Frequency, Old Die

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5.6 Typical Characteristics (continued)

Old Die : unless otherwise specified: T_A = 25°C. New Die : at T_A = 25°C, vs = ±16V, V_{CM} = vs / 2, R_L = 10kΩ (unless otherwise noted)

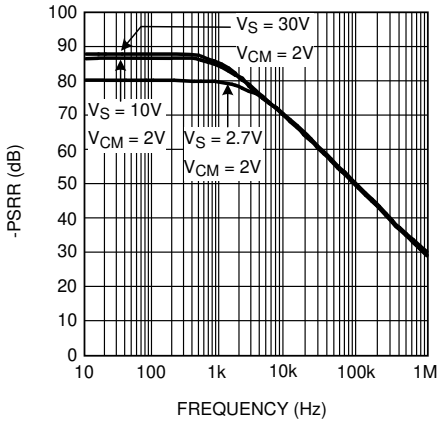


Figure 5-37. −PSRR vs Frequency, Old Die

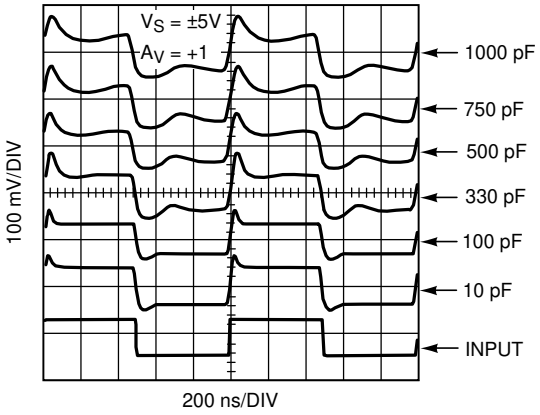


Figure 5-38. Small Signal Step Response, Old Die

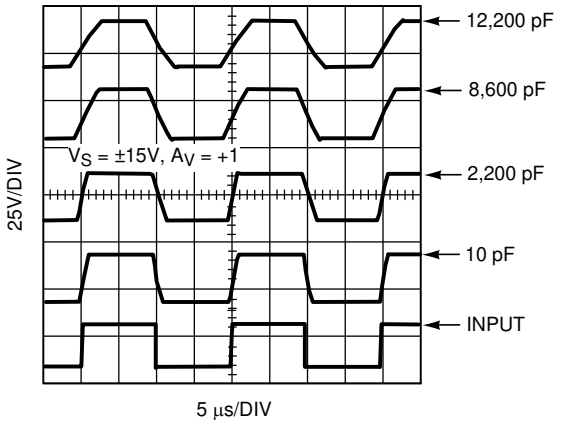


Figure 5-39. Large Signal Step Response, Old Die

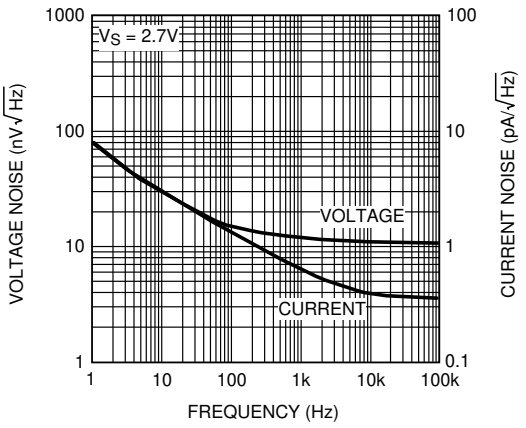


Figure 5-40. Input Referred Noise Density vs Frequency, Old Die

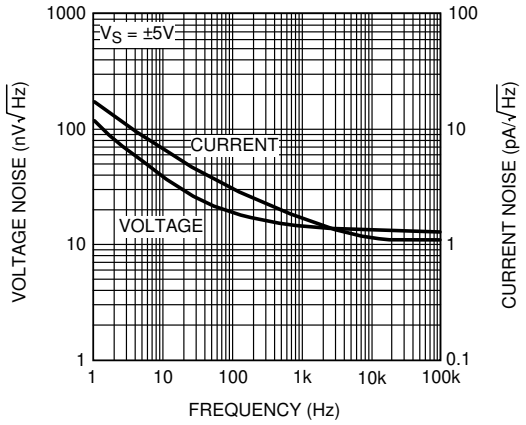


Figure 5-41. Input Referred Noise Density vs Frequency, Old Die

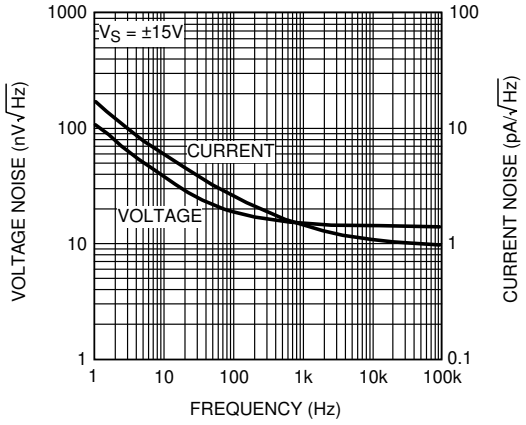


Figure 5-42. Input Referred Noise Density vs Frequency, Old Die

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5.6 Typical Characteristics (continued)

Old Die : unless otherwise specified: T_A = 25°C. New Die : at T_A = 25°C, vs = ±16V, V_{CM} = vs / 2, R_L = 10kΩ (unless otherwise noted)

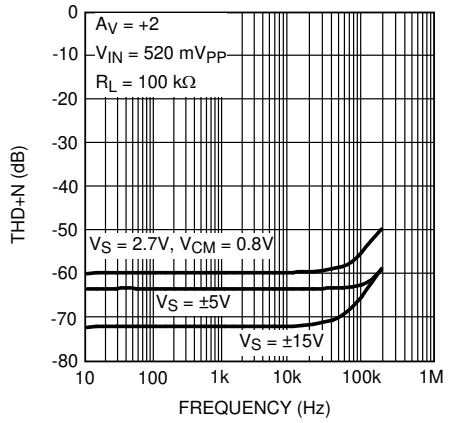


Figure 5-43. THD+N vs Frequency, Old Die

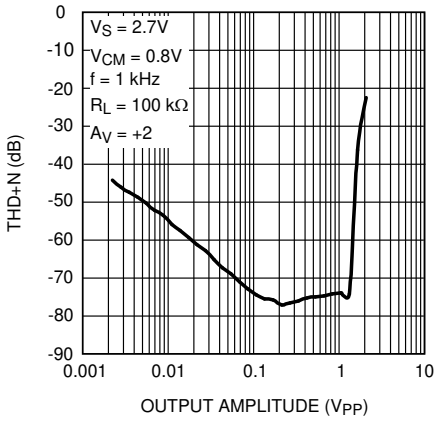


Figure 5-44. THD+N vs Output Amplitude, Old Die

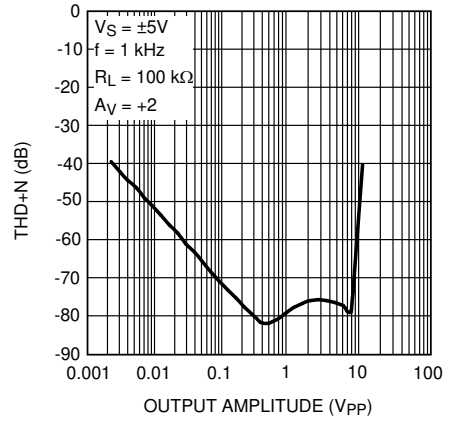


Figure 5-45. THD+N vs Output Amplitude, Old Die

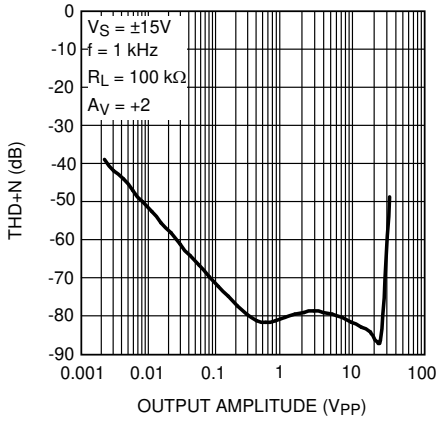


Figure 5-46. THD+N vs Output Amplitude, Old Die

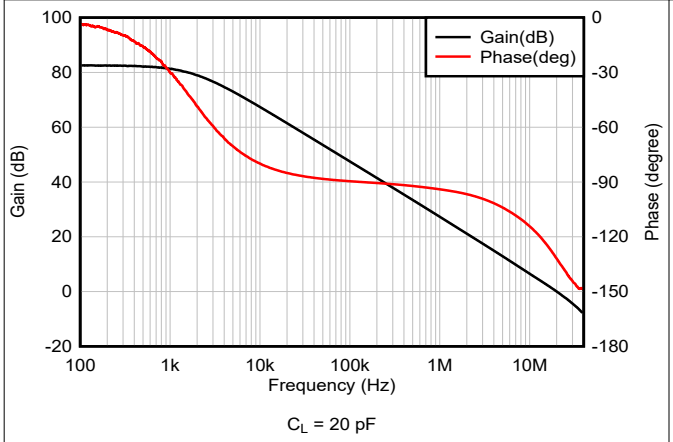


Figure 5-47. Open-Loop Gain and Phase vs Frequency, New Die

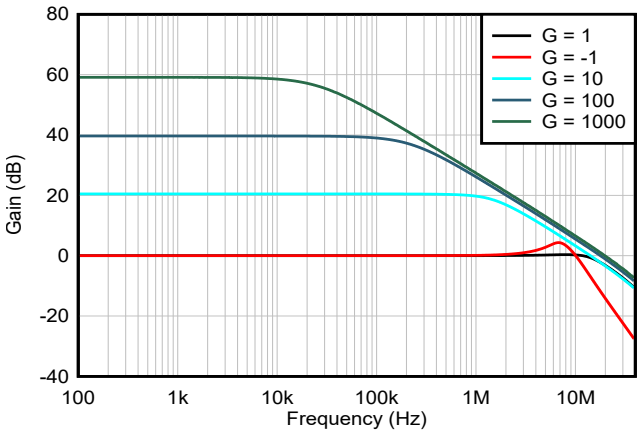


Figure 5-48. Closed-Loop Gain vs Frequency, New Die

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5.6 Typical Characteristics (continued)

Old Die : unless otherwise specified: T_A = 25°C. New Die : at T_A = 25°C, vs = ±16V, V_{CM} = vs / 2, R_L = 10kΩ (unless otherwise noted)

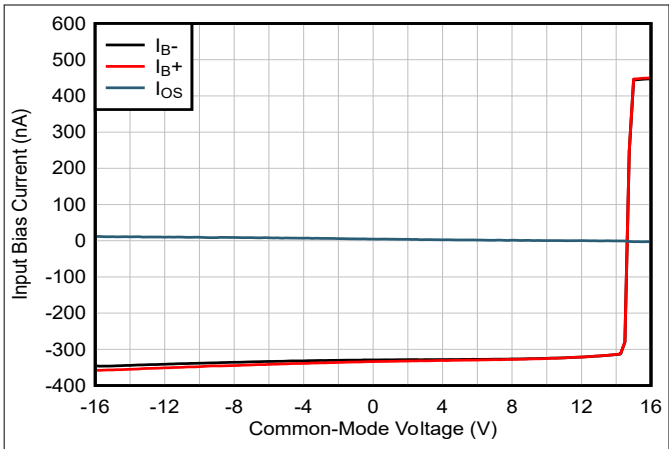
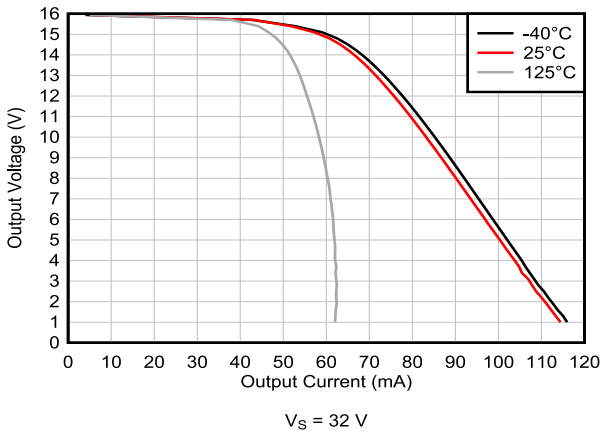
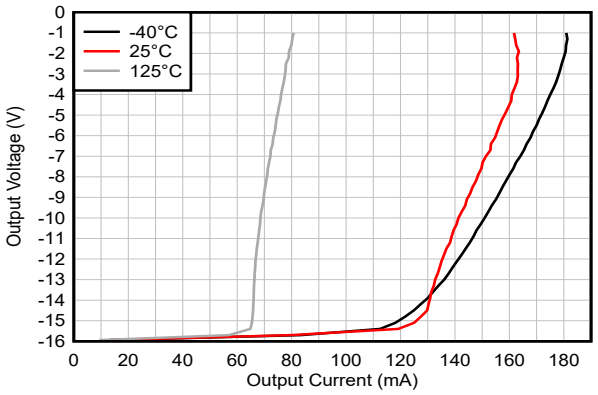


Figure 5-49. Input Bias Current and Offset Current vs Common-Mode Voltage, New Die



V_S = 32 V

Figure 5-50. Output Voltage Swing vs Output Current (Sourcing), New Die



V_S = 32 V

Figure 5-51. Output Voltage Swing vs Output Current (Sinking), New Die

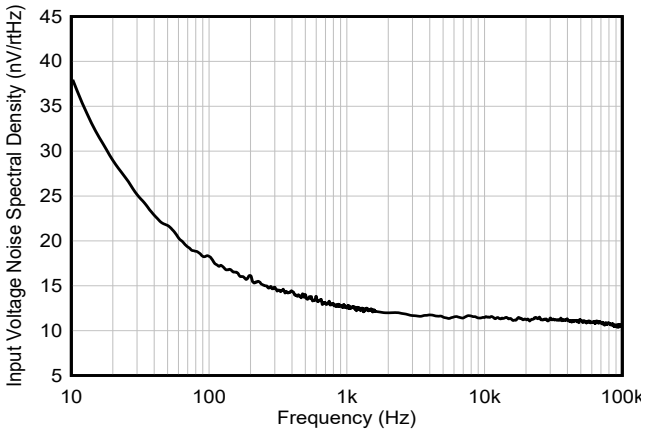
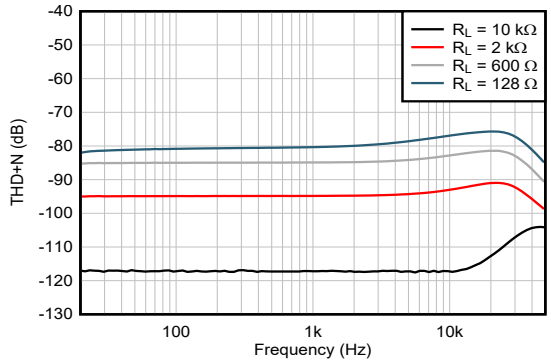
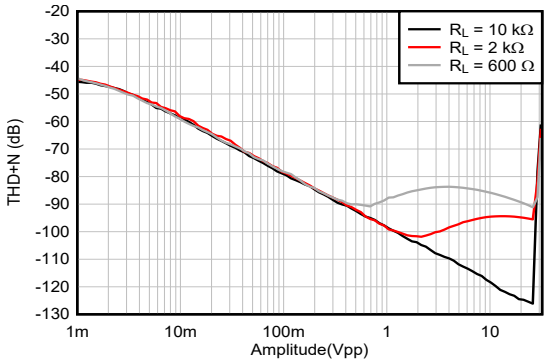


Figure 5-52. Input Voltage Noise Spectral Density vs Frequency, New Die



G = +1
V_{OUT} = 3 V_{RMS}
BW = 80 kHz

Figure 5-53. THD+N Ratio vs Frequency, New Die



f = 1 kHz
BW = 80 kHz
G = +1

Figure 5-54. THD+N vs Output Amplitude, New Die

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5.6 Typical Characteristics (continued)

Old Die : unless otherwise specified: T_A = 25°C. New Die : at T_A = 25°C, vs = ±16V, V_{CM} = vs / 2, R_L = 10kΩ (unless otherwise noted)

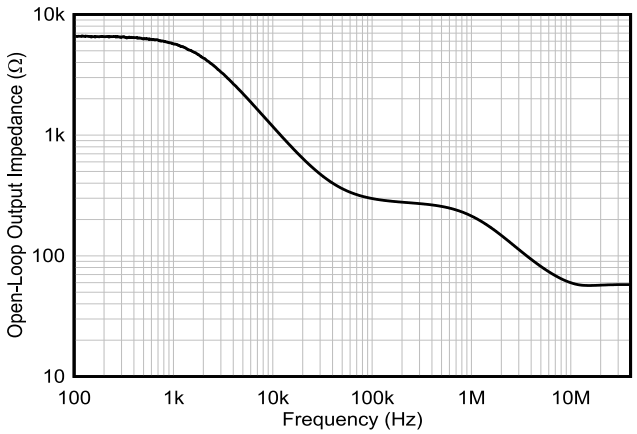


Figure 5-55. Open-Loop Output Impedance vs Frequency, New Die

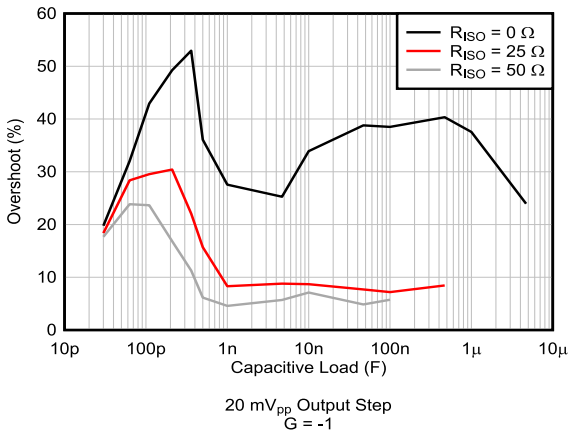


Figure 5-56. Small-Signal Overshoot vs Capacitive Load, New Die

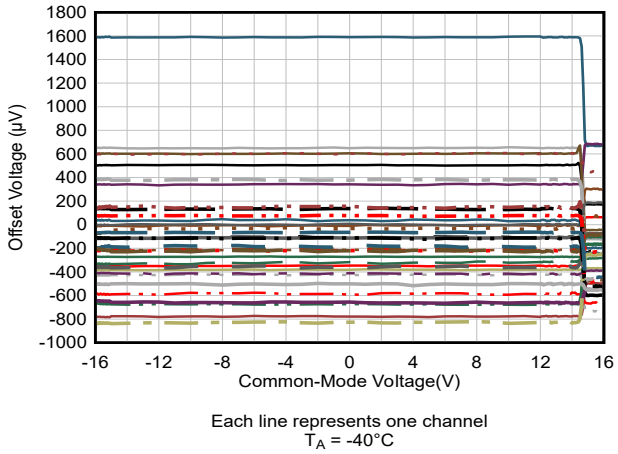


Figure 5-57. Offset Voltage vs Common-Mode Voltage, New Die

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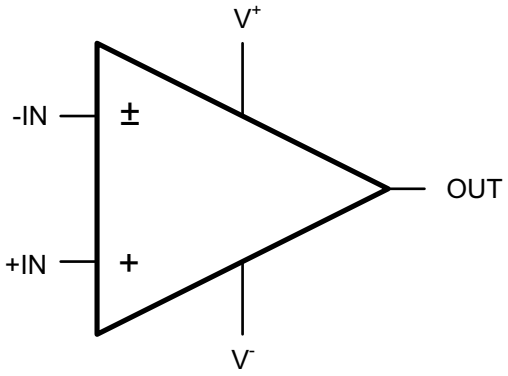
6 Detailed Description

6.1 Overview

The LM732xx devices are rail-to-rail input and output amplifiers with wide operating voltages and high-output currents. The LM732xx family is efficient, achieving 35V/µs slew rate and 24MHz gain bandwidth while requiring only 1.35mA of supply current per op amp. The LM732xx device performance is fully specified for operation at 2.7V to 32V.

The LM732xx devices are designed to drive unlimited capacitive loads without oscillations. Greater than rail-to-rail input common-mode voltage range with 90dB of common-mode rejection across this wide voltage range allows both high-side and low-side sensing. Most device parameters are insensitive to power supply voltage, and this makes the parts easier to use where supply voltage can vary, such as automotive electrical systems and battery-powered equipment.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Output Short Circuit Current and Dissipation Issues

The LM732xx output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below supply voltage of 6V, the output short circuit condition can be tolerated indefinitely.

With the op amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power can include an average value (due to a DC load current) and an AC component. DC load current flows if there is an output voltage offset, or the output AC average current is non-zero, or if the op amp operates in a single supply application where the output is maintained somewhere in the range of linear operation.

Therefore,

$$P_{TOTAL} = P_Q + P_{DC} + P_{AC} \quad (1)$$

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The Op Amp Quiescent Power Dissipation is calculated as:

$$P_Q = I_S \times V_S \quad (2)$$

where

- I_S: Supply Current
- V_S: Total Supply Voltage ($V^+ - V^-$)

The DC Load Power is calculated as:

$$P_{DC} = I_O \times (V_r - V_o) \quad (3)$$

where

- V_O: Average Output Voltage
- V_r: V^+ for sourcing and V^- for sinking current

The AC Load Power is calculated as P_{AC} = See Table 6-1.

Table 6-1 shows the maximum AC component of the load power dissipated by the op amp for standard Sinusoidal, Triangular, and Square Waveforms:

Table 6-1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} (W.Ω/V^2)		
Sinusoidal	Triangular	Square
50.7 × 10^{-3}	46.9 × 10^{-3}	62.5 × 10^{-3}

The table entries are normalized to $V_S{}^2/R_L$. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor $V_S{}^2/R_L$. For example, with ±12V supplies, a 600Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = \left(46.9 \times 10^{-3}\right) \times \left(\frac{576}{600}\right) = 45.0\text{mW} \quad (4)$$

The maximum power dissipation allowed at a certain temperature is a function of maximum die junction temperature ($T_{J(MAX)}$) allowed, ambient temperature T_A, and package thermal resistance from junction to ambient, θ_{JA}.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (5)$$

For the LM732xx, the maximum junction temperature allowed is 150°C at which no power dissipation is allowed. The power capability at 25°C is given by the following calculations:

For VSSOP package (dual channel):

$$P_{D(Max)} = \frac{150°C - 25°C}{169.6°C} = 0.737\text{W} \quad (6)$$

For SOIC package (single channel):

$$P_{D(Max)} = \frac{150°C - 25°C}{133.5°C} = 0.936\text{W} \quad (7)$$

Similarly, the power capability at 125°C is given by:

For VSSOP package (dual channel):

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$$P_{D(Max)} = \frac{150°C - 125°C}{169.6°C} = 0.147W \quad (8)$$

For SOIC package (single channel):

$$P_{D(Max)} = \frac{150°C - 125°C}{124°C} = 0.202W \quad (9)$$

When high power is required and ambient temperature can't be reduced, providing air flow is an effective approach to reduce thermal resistance therefore to improve power capability.

6.4 Device Functional Modes

6.4.1 Driving Capacitive Loads

The LM732xx are specifically designed to drive unlimited capacitive loads without oscillations as shown in Figure 6-1

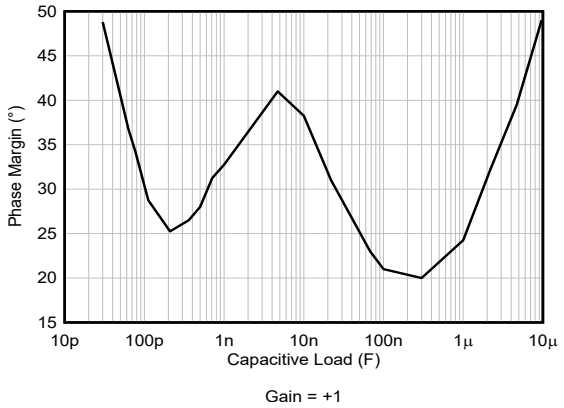


Figure 6-1. Phase Margin vs Capacitive Load

In addition, the output current handling capability of the device allows for good slewing characteristics, even with large capacitive loads. The combination of these features is practical for applications such as TFT flat panel buffers, A/D converter input amplifiers, and so forth.

However, as in most op amps, addition of a series isolation resistor between the op amp and the capacitive load improves the settling and overshoot performance. To keep an acceptable phase margin, unlimited capacitive load drive devices lower the gain bandwidth product under larger capacitive loads. The LM732x is specified to have a gain bandwidth product of 24MHz without significant capacitive load, but this value begins to decrease at the point where a traditional amplifier begins to become unstable. This tradeoff is what extends the output drive capability. LM732x is designed with a wide gain bandwidth product to make sure there is headroom for many general-purpose applications with higher capacitive loads.

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6.4.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application shows an illustration of the ESD circuits contained in the LM732x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This ESD protection also includes back to back input diodes, which are intended to protect the input transistors from large differential signals. This protection circuitry is intended to remain inactive during normal circuit operation.

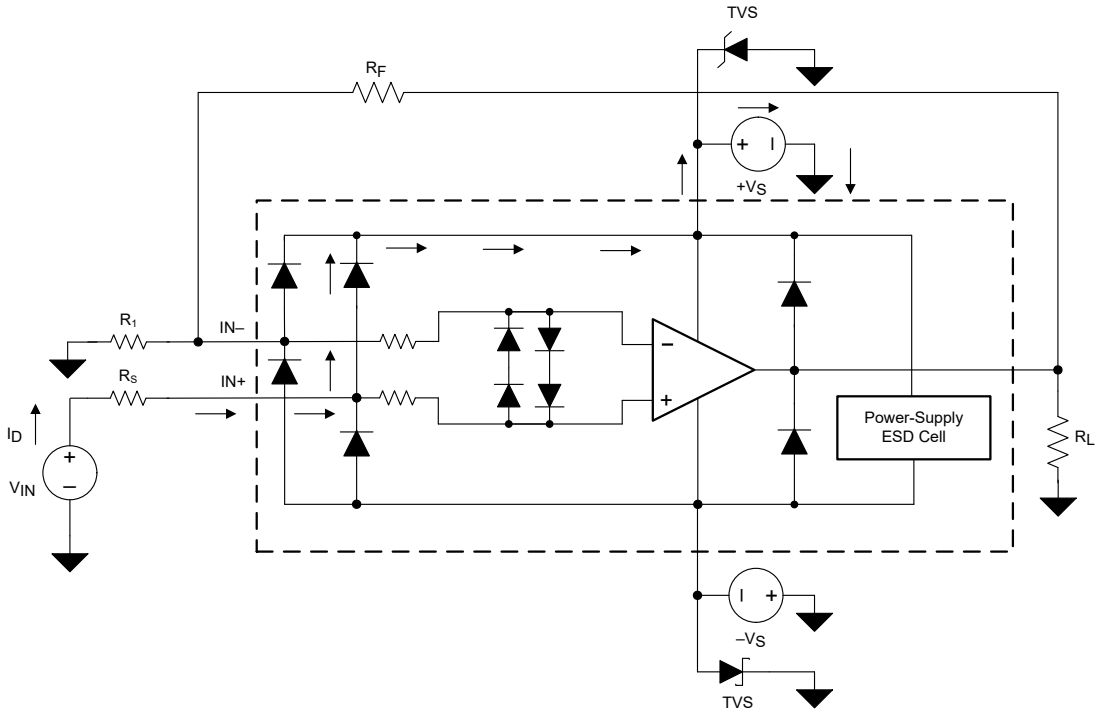


Figure 6-2. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

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An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device terminals, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the LM732x but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. Using this device in a comparator configuration can activate the back-to-back input diodes if the differential signal is large. Circumstances can arise where an applied voltage exceeds the operating voltage range of a given terminal. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0V. Again, this question depends on the supply characteristic while at 0V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply terminals; see Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply terminal begins to rise above the safe-operating, supply-voltage level.

The LM732x input terminals are protected from excessive differential voltage with back-to-back diodes; see Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the LM732x. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application shows an example configuration that implements a current-limiting feedback resistor.

6.4.3 Old Versus New Die Comparison

As of the publication of revision F of this datasheet, Texas Instruments has moved manufacturing of the die for LM732x to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die. The die origin can be separated from the “Chip Source Origin” (CSO) parameter

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in the shipping information. The old die CSO is “GF6”, for the new die CSO is “RFB”. The old die information is maintained in this datasheet for comparison purposes, but all new manufacturing has moved to the new die.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Typical Application

Figure 7-1 shows a typical application where the LM732xx is used as a buffer amplifier for the V_{COM} signal employed in a TFT LCD flat panel:

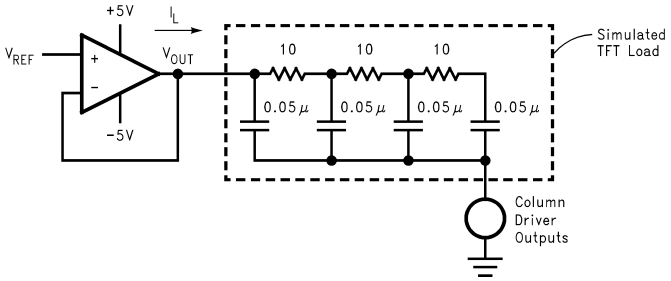


Figure 7-1. V_{COM} Driver Application Schematic

7.2 Layout

7.2.1 Layout Guidelines

Take care to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. A ground plane underneath the device is recommended; any bypass components to ground must have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins lowers the power supply inductance and provides a more stable power supply.

The feedback components must be placed as close to the device as possible to minimize stray parasitics.

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7.2.2 Layout Example

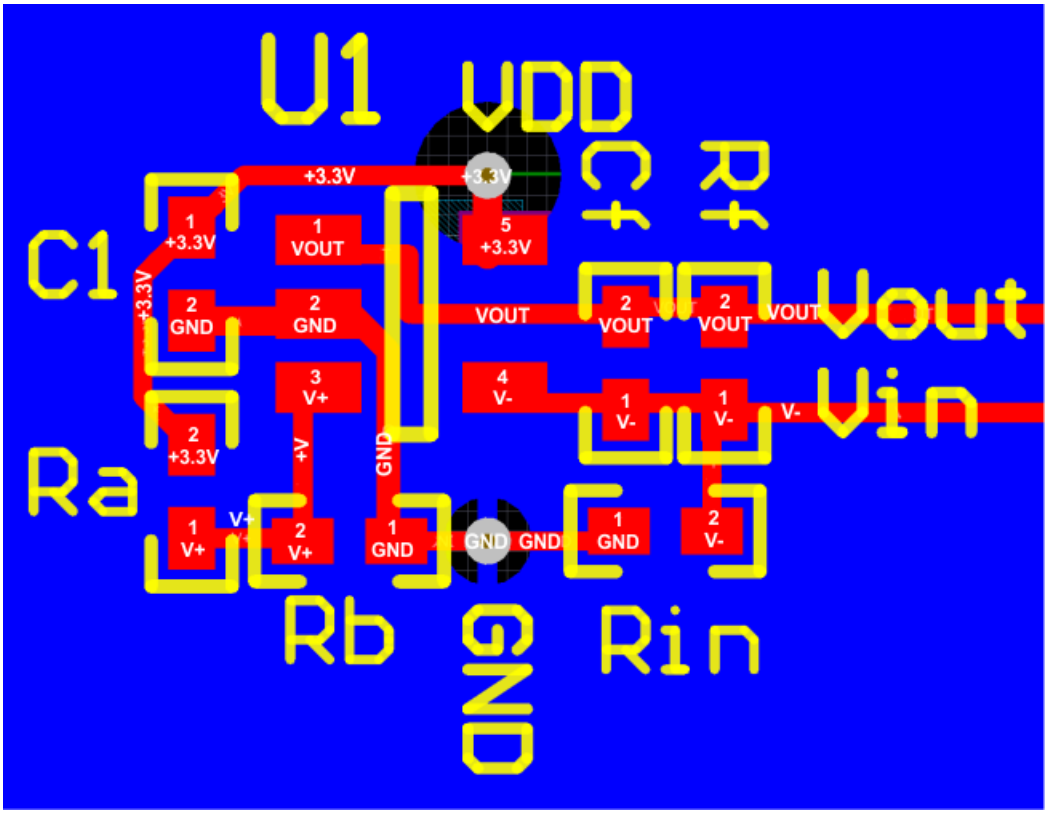


Figure 7-2. LM732xx Layout Example

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8 Power Supply Recommendations

The use of supply decoupling is mandatory in most applications. As with most relatively high-speed or high-output current op amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (about 0.01µF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum (> 4.7µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor acts as the charge *bucket* for fast load current spikes at the op amp output. The combination of these capacitors provides supply decoupling and helps keep the op amp oscillation-free under any load.

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9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2015) to Revision F (March 2022)	Page
• Updated *Features* section per New Die specifications	1
• Updated *Description* section per New Die specifications	1
• Updated *Absolute Maximum Ratings* section as per New Die specifications	4
• Updated Supply Voltage minimum from 2.5V to 2.7V	4
• Updated Junction-to-ambient thermal resistance from 165°C/W, 325°C/W, and 235°C/W to 133.5°C/W, 185.4°C/W, and 169.6°C/W respectively	4
• Updated Input Offset Voltage typical value from ±0.7mV to ±0.35mV	5
• Updated Input Offset Voltage Temperature Drift typical value from ±2µV/°C to 2.5µV/°C	5
• Updated Input Bias Current typical values from −1.2µA to 0.4µA and from 0.45µA to 0.4µA	5
• Updated Input Offset Current from 20nA to 7nA	5
• Updated Output Voltage Swing High for R_L= 2kΩ V_{ID}= 100mV typical value from 100mV to 50mV	5
• Updated Output Voltage Swing Low for V_{ID}= −100mV typical value from 20mV to 50mV	5
• Updated Output Voltage Swing Low for R_L= 2kΩ V_{ID}= −100mV typical value from 40mV to 50mV	5
• Updated Supply Current typical value from 0.95mA to 1.35mA and maximum value for T_A= –40°C to +125°C from 1.9mA to 2.23mA and maximum value from 1.3mA to 1.93mA	5
• Updated Slew Rate from 8.5V/µs to 35V/µs	5
• Updated Unity Gain Frequency 7.5MHz to 11MHz	5
• Updated Unity Gain Bandwidth 16MHz to 24MHz	5
• Updated Total Harmonic Distortion + Noise from −77dB to −113dB	5
• Updated CMRR test conditions, typical and minimum values from 70dB to 109dB	5
• Removed CMVR parameter from 20mV to 50mV	5
• Added V_{CM} parameter	5

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- Updated A_{VOL} test conditions and typical values from 65dB to 75dB....5
- Updated A_{VOL} test conditions and typical values from 62dB to 70dB....5
- Updated A_{VOL} test conditions and typical values from 59dB to 65dB....5
- Updated A_{VOL} test conditions and typical values from 55dB to 62dB....5
- Updated I_{OUT} test conditions and min values from 30mA to ±40mA....5
- Updated I_{OUT} test conditions and min values from 20mA to ±35mA....5
- Updated I_{OUT} test conditions and min values from 40mA to ±20mA....5
- Updated I_{OUT} test conditions and min values from 30mA to ±20mA....5
- Updated I_{OUT} test conditions and typical values from 48mA to ±85mA....5
- Updated I_{OUT} test conditions and typical values from 65mA to ±60mA....5
- Deleted *±5-V Electrical Characteristics* section....5
- Deleted *±15-V Electrical Characteristics* section....5
- Updated *Typical Characteristics* section per New Die specifications....7
- Removed *Estimating the Output Voltage Swing* section....17
- Updated *Output Short Circuit Current and Dissipation Issues* 17
- Added *Electrical Overstress* section....20
- Added *Old Versus New Die Comparison* section....21

Changes from Revision D (March 2013) to Revision E (September 2015) **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision C (May 2008) to Revision D (March 2013) **Page**

- Changed layout of National Semiconductor Datasheet to TI format....1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM7321MA/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	LM732 1MA
LM7321MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LM732 1MA
LM7321MAX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM732 1MA
LM7321MF/NOPB	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	AU4A
LM7321MFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AU4A
LM7321MFX/NOPB.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AU4A
LM7321QMF/NOPB	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	AR8A
LM7321QMFE/NOPB	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	AR8A
LM7321QMFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AR8A
LM7321QMFX/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AR8A
LM7321QMFX/NOPB.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AR8A
LM7322MA/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	LM732 2MA
LM7322MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LM732 2MA
LM7322MAX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM732 2MA
LM7322MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AZ4A
LM7322MM/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AZ4A
LM7322MME/NOPB	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 125	AZ4A
LM7322QMA/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	LM732 2QMA
LM7322QMAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(7322Q, LM732) 2QMA
LM7322QMAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(7322Q, LM732) 2QMA
LM7322QMAX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(7322Q, LM732) 2QMA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM7321, LM7321-Q1, LM7322, LM7322-Q1 :

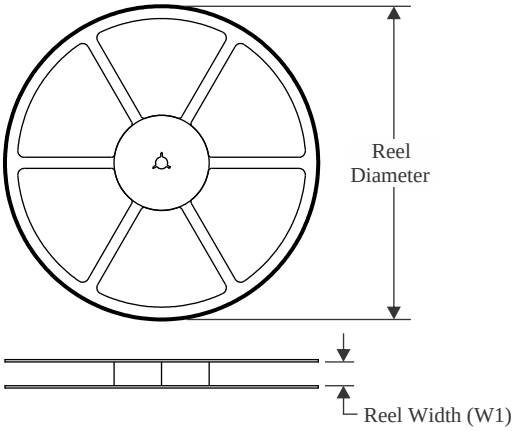
- Catalog : LM7321, LM7322
- Automotive : LM7321-Q1, LM7322-Q1

NOTE: Qualified Version Definitions:

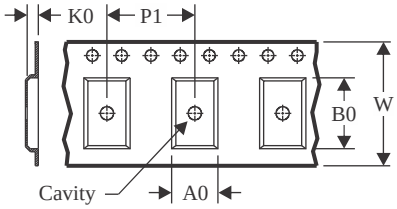
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

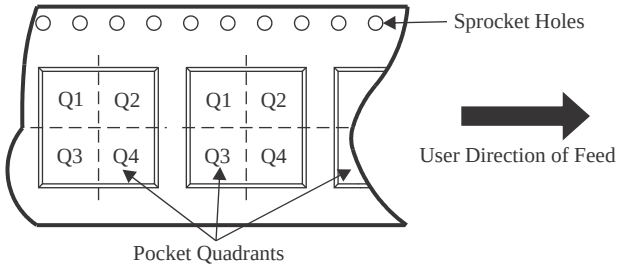


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

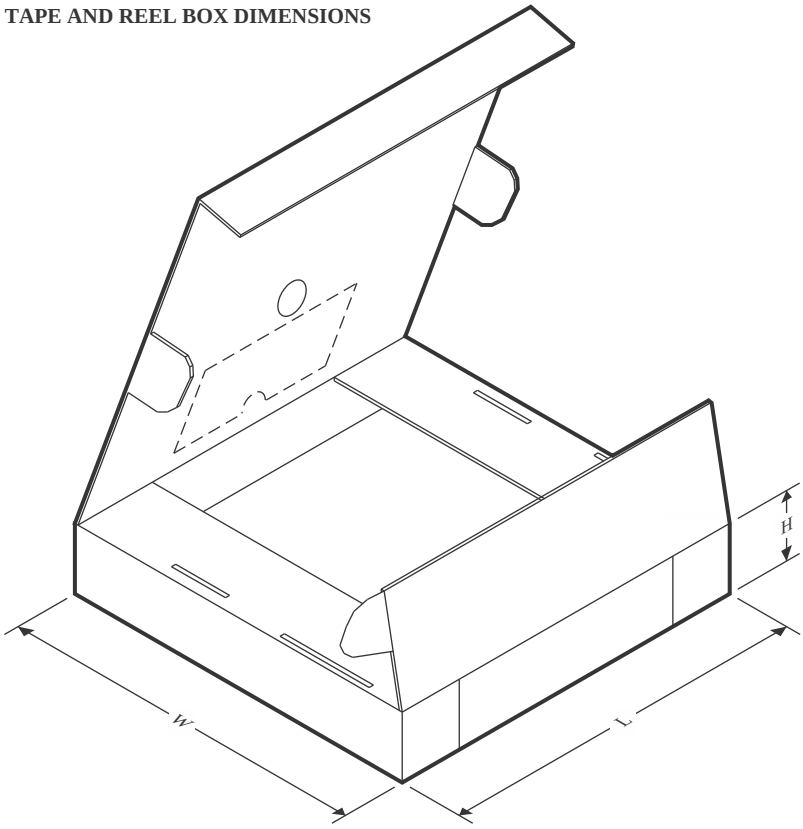
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

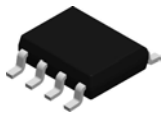
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7321MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM7321MFX/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7321QMFX/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7321QMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7322MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM7322MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM7322MM/NOPB	VSSOP	DGK	8	1000	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LM7322MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7322QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7321MAX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0
LM7321MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM7321QMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM7321QMFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM7322MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM7322MAX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0
LM7322MM/NOPB	VSSOP	DGK	8	1000	366.0	364.0	50.0
LM7322MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM7322QMAX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0

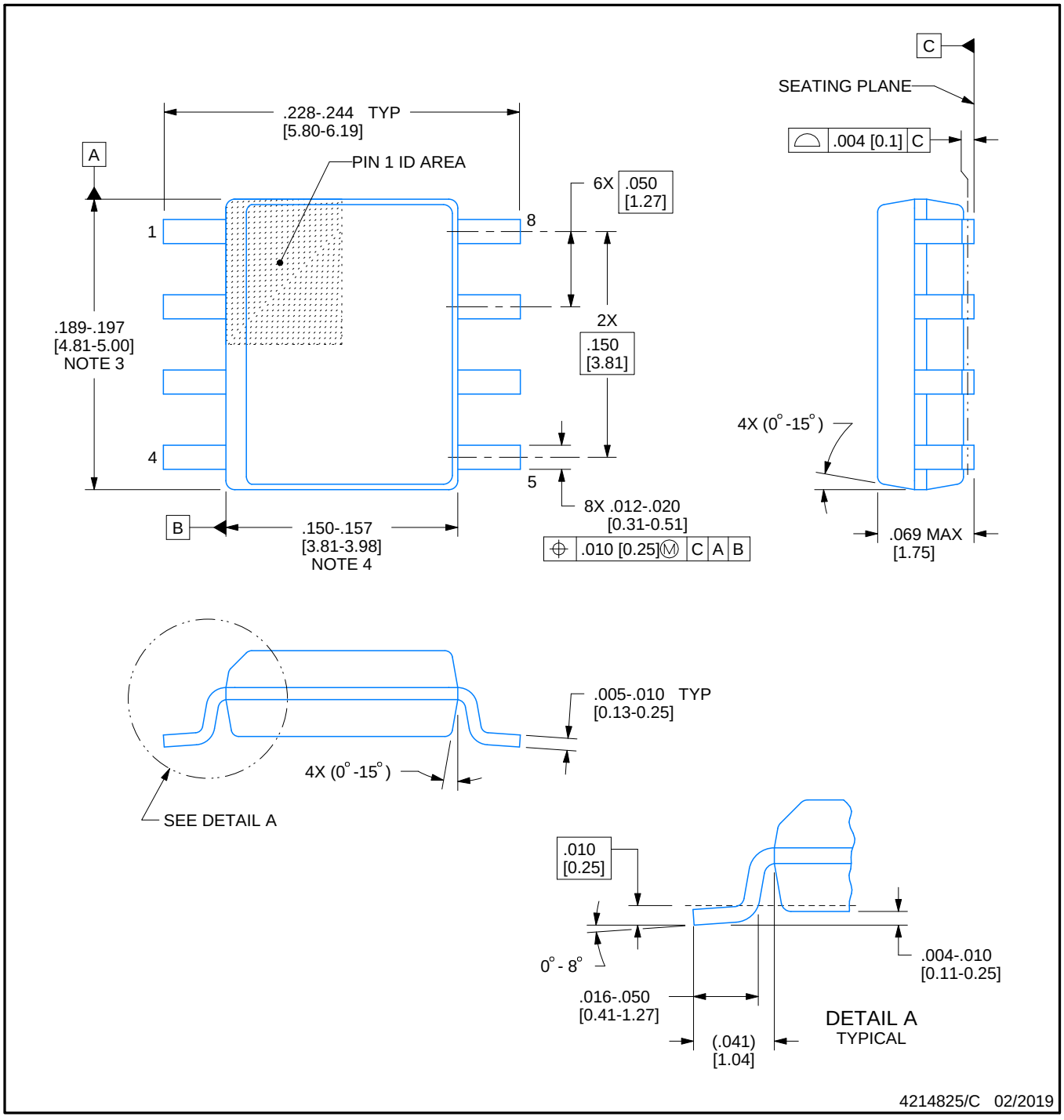


PACKAGE OUTLINE

D0008A

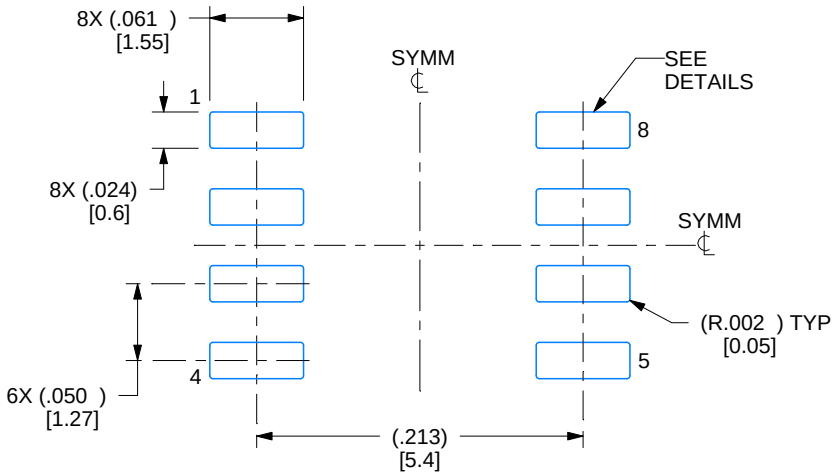
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

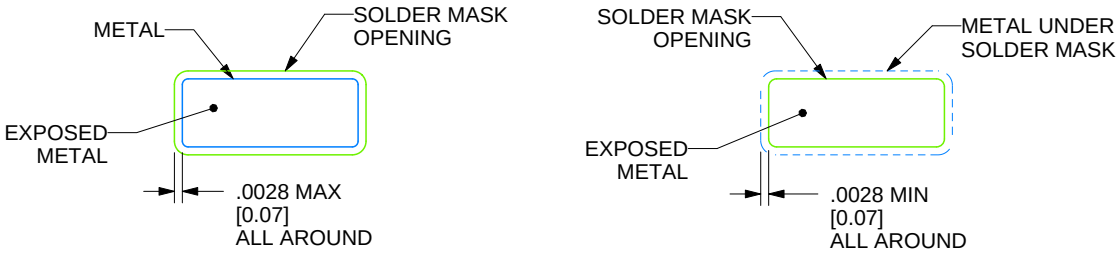


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

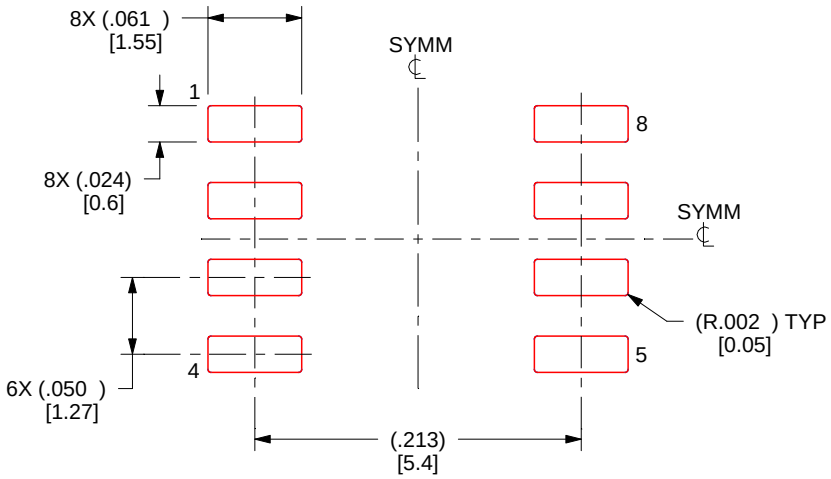
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

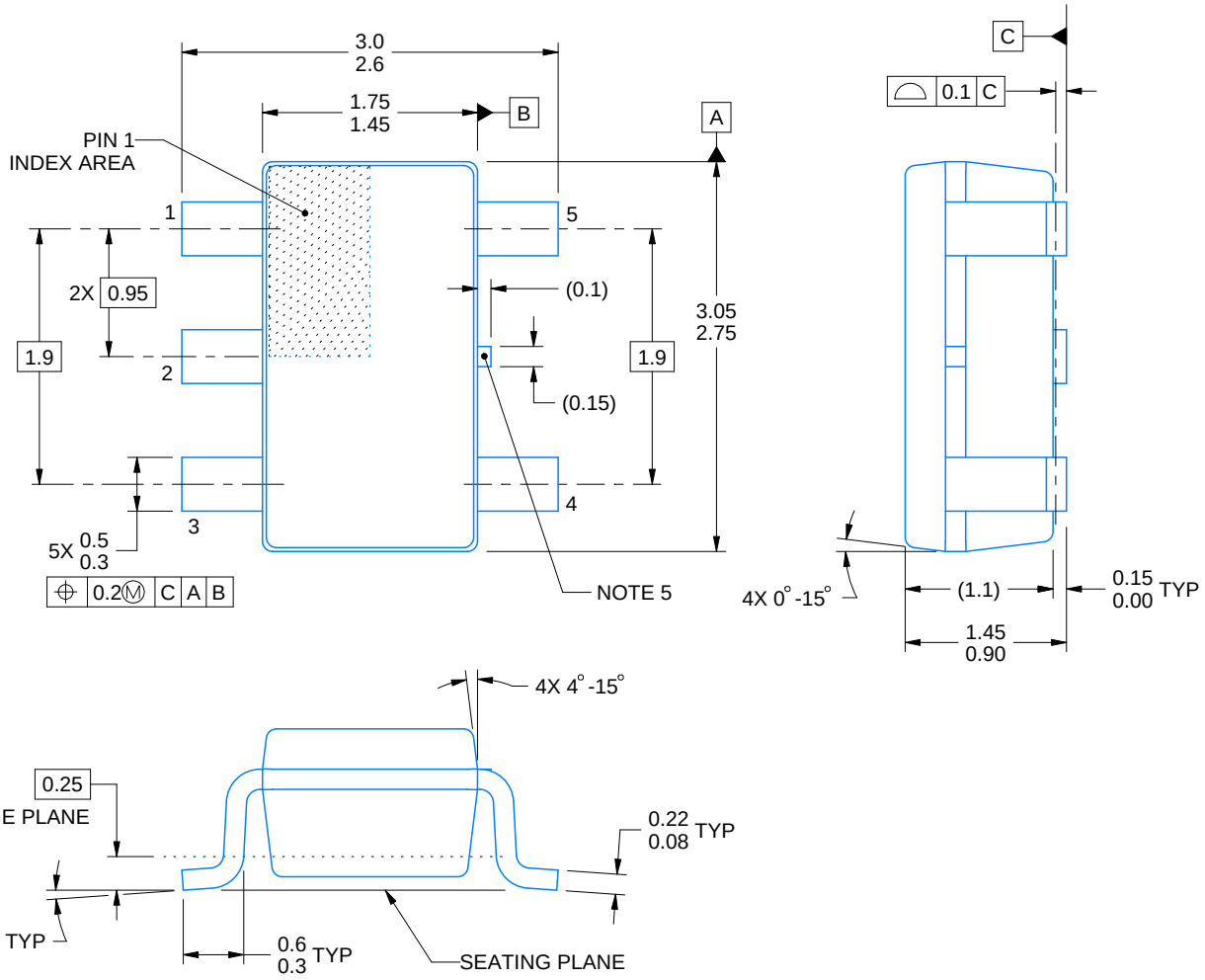
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

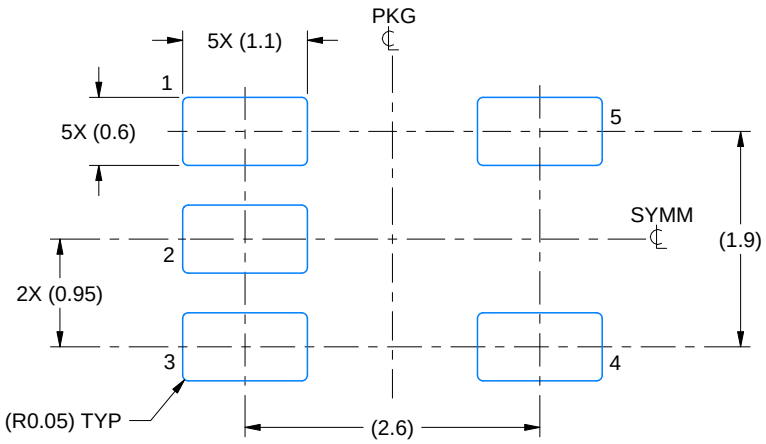
SMALL OUTLINE TRANSISTOR



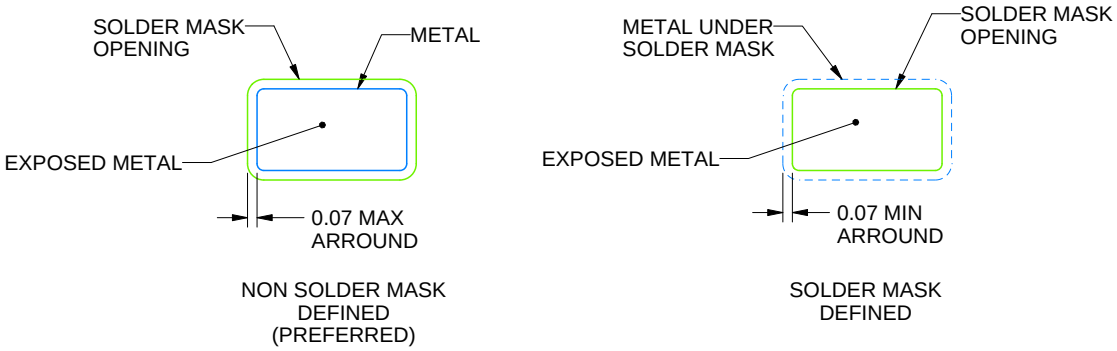
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

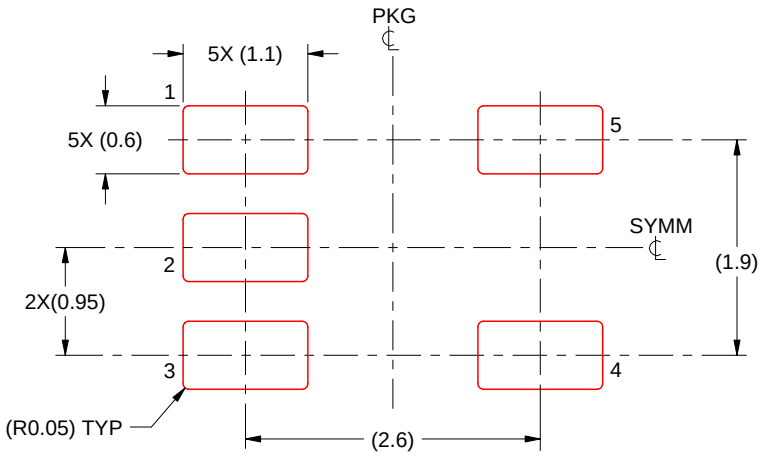


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

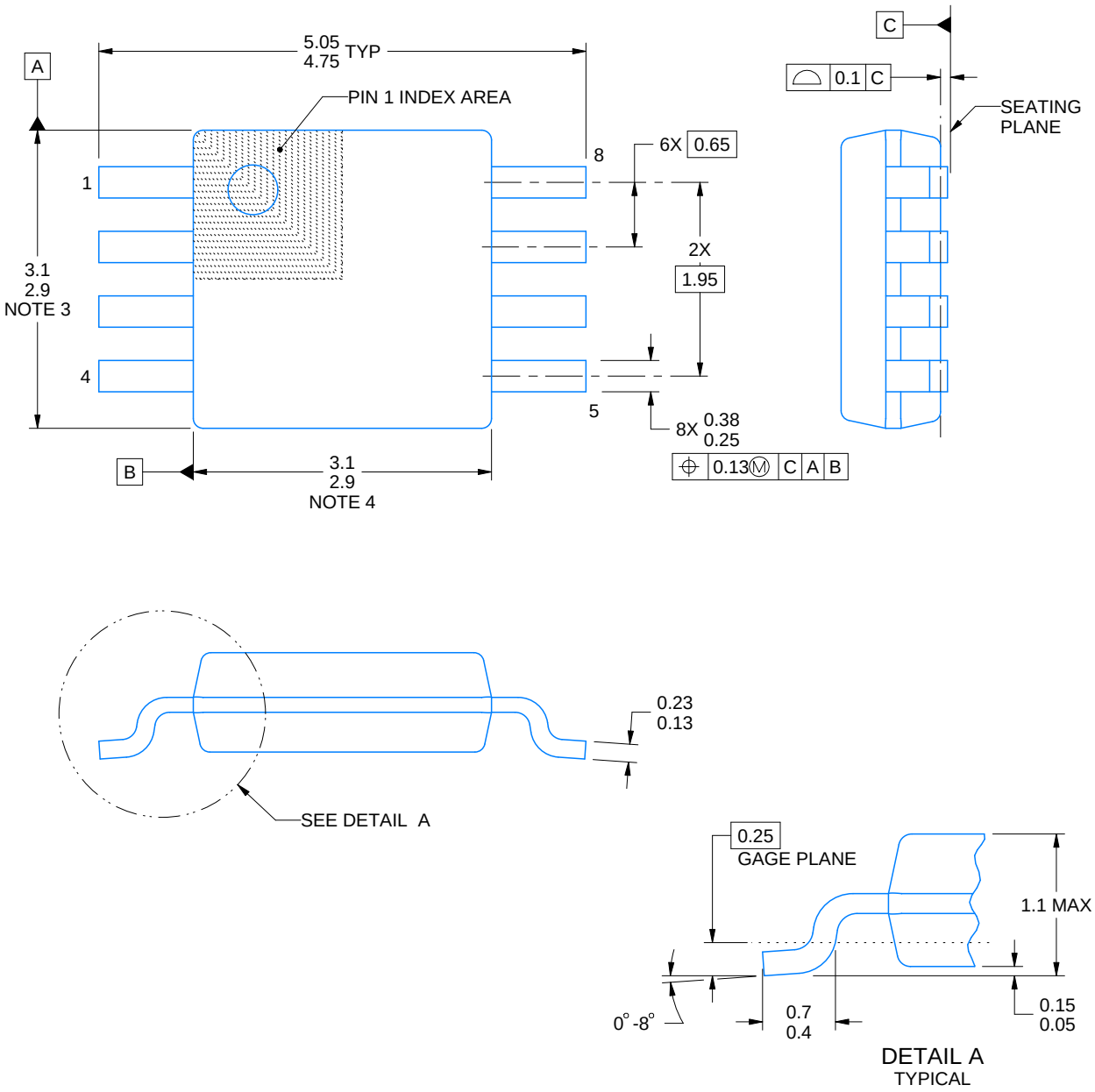
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

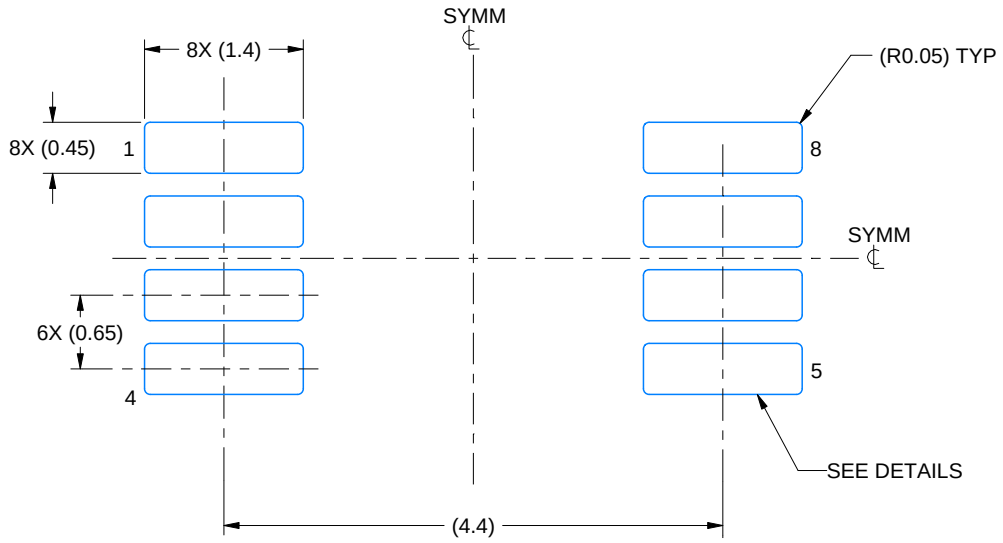
SMALL OUTLINE PACKAGE



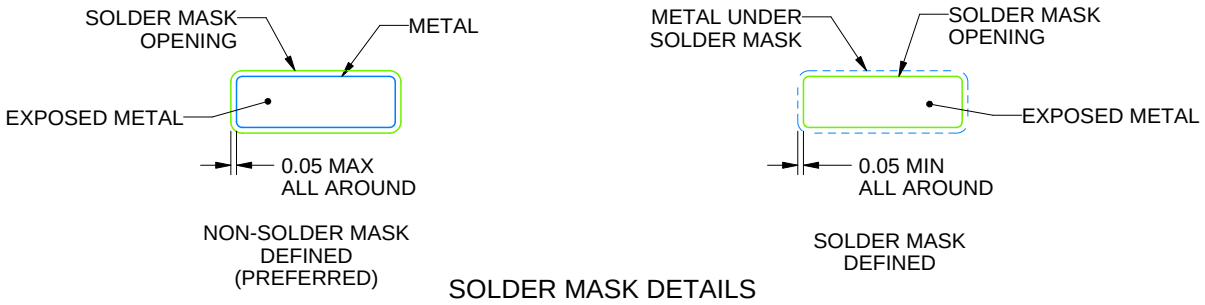
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

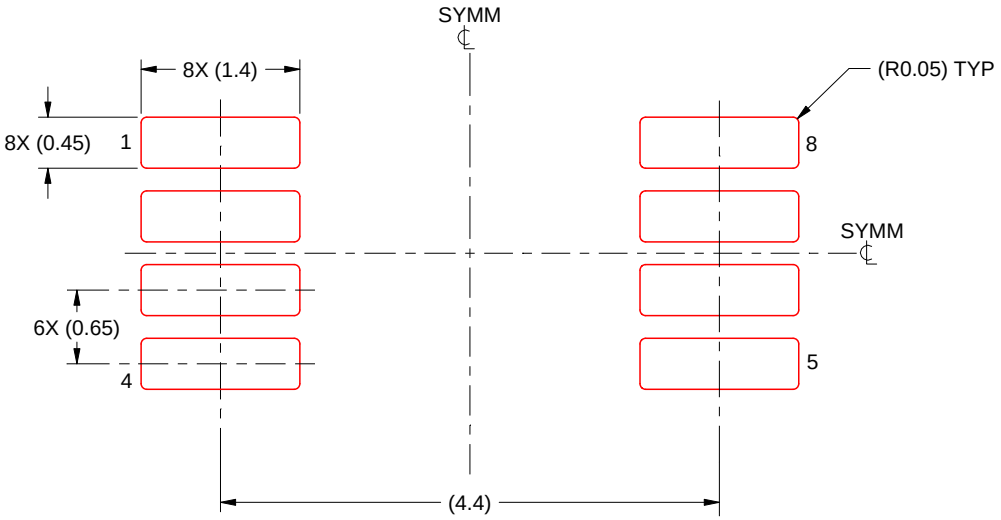


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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