# LM613x Dual and Quad, Low-Power, 10MHz, Rail-to-Rail I/O Operational Amplifiers

## 1 Features

- (For 5V supply, typical unless noted)
- Rail-to-rail input CMVR: −0.25V to 5.25V
- Rail-to-rail output
- High gain-bandwidth: 10MHz at 20kHz
- Slew rate: 12V/µs
- Low supply current: 360µA/amp
- Wide supply range: 2.7V to over 24V
- CMRR: 100dB
- Gain: 100dB with $R_L$ = 10kΩ
- PSRR: 82dB

## 2 Applications

- Battery-operated instrumentation
- Instrumentation amplifiers
- Portable scanners
- Wireless communications
- Flat-panel display driver

## 3 Description

The LM6132 and LM6134 (LM613x) provide new levels of speed versus power performance in applications where low-voltage supplies or power limitations previously made compromise necessary. With only 360µA/amp supply current, the 10MHz gain-bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

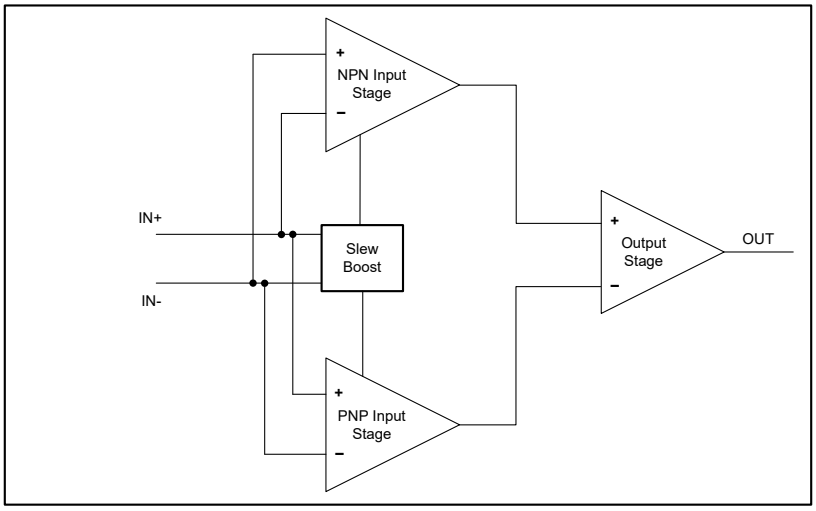
The LM613x can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This feature is particularly important when operating on low supply voltages. The LM613x also drives large capacitive loads without oscillating.

Operating on supplies from 2.7V to over 24V, the LM6132x are excellent for a very wide range of applications, from battery-operated systems with large bandwidth requirements to high-speed instrumentation.

**Device Information**

| PART NUMBER | CHANNEL COUNT | PACKAGE(1) | BODY SIZE |
|---|---|---|---|
| LM6132 | Dual | D (SOIC, 8) | 4.90mm × 3.91mm |
| | | P (PDIP, 8) | 9.81mm × 6.35mm |
| LM6134 | Quad | D (SOIC, 14) | 8.65mm × 3.91mm |
| | | NFF (PDIP, 14) | 19.177mm × 6.35mm |

(1) For more information, see Section 9.




**Functional Block Diagram**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Pin Configuration and Functions

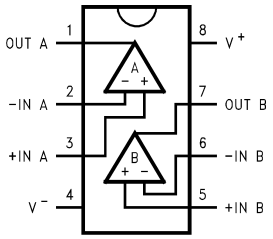



**Figure 4-1. D Package, 8-Pin SOIC,and P Package, 8-Pin PDIP (Top View)**

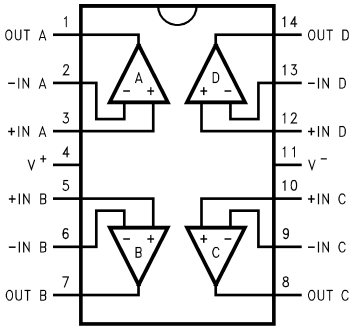



**Figure 4-2. D Package, 14-Pin SOIC, and NFF Package, 14-Pin PDIP (Top View)**

**Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | LM6132 | LM6134 | | |
| | D (SOIC), P (PDIP) | D (SOIC), NFF (PDIP) | | |
| –IN A | 2 | 2 | Input | ChA inverting input |
| +IN A | 3 | 3 | Input | ChA noninverting input |
| –IN B | 6 | 6 | Input | ChB inverting input |
| +IN B | 5 | 5 | Input | ChB noninverting input |
| –IN C | | 9 | Input | ChC inverting input |
| +IN C | | 10 | Input | ChC noninverting input |
| –IN D | | 13 | Input | ChD inverting input |
| +IN D | | 12 | Input | ChD noninverting input |
| OUT A | 1 | 1 | Output | ChA output |
| OUT B | 7 | 7 | Output | ChB output |
| OUT C | | 8 | Output | ChC output |
| OUT D | | 14 | Output | ChD output |
| $V^-$ | 4 | 11 | Input | Negative supply |
| $V^+$ | 8 | 4 | Input | Positive supply |

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_S$ = (V+) – (V–) | | 0 | 33 | V |
| Signal input pins | Common-mode voltage(3) | (V–) – 0.5 | (V+) + 0.5 | V |
| | Differential voltage(4) | | ±15 | V |
| | Current(3) | | ±10 | mA |
| Output short-circuit(2) | | Continuous | | |
| Operating ambient temperature, $T_A$ | | –55 | 150 | °C |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(4) Input pins are connected by back-to-back diodes for input protection. If the differential input voltage may exceed 0.5V, limit the input current to 10mA or less.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage, (V+) – (V–) | 2.7 | 24 | V |
| $V_I$ | Common mode voltage range | (V–) – 0.1 | (V+) + 0.1 | V |
| $T_A$ | Specified temperature | –40 | 85 | °C |


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## 5.4 Thermal Information LM6132

| THERMAL METRIC[1] | | LM6132 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | P (PDIP) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 127.10 | 84.45 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 63.27 | 58.07 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 71.20 | 50.90 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 13.91 | 30.43 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 70.54 | 50.44 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 5.5 Thermal Information LM6134

| THERMAL METRIC[1] | | LM6134 | | Unit |
|---|---|---|---|---|
| | | D (SOIC) | NFF (PDIP) | |
| | | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 82.48 | 81 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 38.77 | N/A | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 37.86 | N/A | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.66 | N/A | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 37.51 | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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## 5.6 Electrical Characteristics: $V_S$ = 5V

For $V^+$ = 5.0V, $V^-$ = 0V, $R_L$ > 1MΩ connected to $V_S$ / 2, $V_{CM}$ = $V^+$ / 2, and $V_O$ = $V^+$ / 2, at $T_A$ = 25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | LM6132AI, LM6134AI | | | 0.25 | 2 | mV |
| | | | $T_A$ = –40°C to 85°C | | | 4 | |
| | | LM6132BI, LM6134BI | | | 0.25 | 6 | |
| | | | $T_A$ = –40°C to 85°C | | | 8 | |
| $dV_{OS}/dT$ | Input offset voltage drift | $T_A$ = –40°C to 85°C | | | 5 | | µV/°C |
| PSRR | Input offset voltage versus power supply | 2.5V ≤ $\|V_S\|$ ≤ 12V, LM6132AI, LM6134AI | | 78 | 82 | | dB |
| | | | $T_A$ = –40°C to 85°C | 75 | | | |
| | | 2.5V ≤ $\|V_S\|$ ≤ 12V, LM6132BI, LM6134BI | | 78 | 82 | | |
| | | | $T_A$ = –40°C to 85°C | 75 | | | |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | 0V ≤ $V_{CM}$ ≤ 5V, LM6132AI, LM6134AI | | | 110 | 140 | nA |
| | | | $T_A$ = –40°C to 85°C | | | 300 | |
| | | 0V ≤ $V_{CM}$ ≤ 5V, LM6132BI, LM6134BI | | | 110 | 180 | |
| | | | $T_A$ = –40°C to 85°C | | | 350 | |
| $I_{OS}$ | Input offset current | LM6132AI, LM6134AI | | | 3.4 | 30 | nA |
| | | | $T_A$ = –40°C to 85°C | | | 50 | |
| | | LM6132BI, LM6134BI | | | 3.4 | 30 | |
| | | | $T_A$ = –40°C to 85°C | | | 50 | |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Common-mode input voltage range | | | – 0.25 | | 5.25 | V |
| | | $T_A$ = –40°C to 85°C | | 0 | | 5 | V |
| CMRR | Common-mode rejection ratio | 0V ≤ $V_{CM}$ ≤ 4V, LM6132AI, LM6134AI | | 75 | 100 | | dB |
| | | | $T_A$ = –40°C to 85°C | 70 | | | |
| | | 0V ≤ $V_{CM}$ ≤ 4V, LM6132BI, LM6134BI | | 75 | 100 | | |
| | | | $T_A$ = –40°C to 85°C | 70 | | | |
| | | 0V ≤ $V_{CM}$ ≤ 5V, LM6132AI, LM6134AI | | 60 | 100 | | |
| | | | $T_A$ = –40°C to 85°C | 55 | | | |
| | | 0V ≤ $V_{CM}$ ≤ 5V, LM6132BI, LM6134BI | | 60 | 100 | | |
| | | | $T_A$ = –40°C to 85°C | 55 | | | |
| **INPUT IMPEDANCE** | | | | | | | |
| $R_{IN}$ | Common-mode input resistance | | | | 104 | | MΩ |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $R_L$ = 10kΩ, LM6132AI, LM6134AI | | 25 | 100 | | V/mV |
| | | | $T_A$ = –40°C to 85°C | 8 | | | |
| | | $R_L$ = 10kΩ, LM6132BI, LM6134BI | | 15 | 100 | | |
| | | | $T_A$ = –40°C to 85°C | 6 | | | |
| **NOISE** | | | | | | | |
| $e_N$ | Input voltage noise density | f = 1kHz | | | 27 | | nV/√Hz |
| $i_N$ | Input current noise density | f = 1kHz | | | 0.18 | | pA/√Hz |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain-bandwidth product | f = 20kHz | | 7.4 | 10 | | MHz |
| | | | $T_A$ = –40°C to 85°C | 7 | | | |
| SR | Slew rate | $V_S$ = 12V, $V_{STEP}$ = 8V, $R_S$ < 1kΩ | | 8 | 14 | | V/µs |
| | | | $T_A$ = –40°C to 85°C | 7 | | | |
| PM | Phase margin | $R_L$ = 10 kΩ | | | 33 | | ° |
| GM | Gain margin | $R_L$ = 10 kΩ | | | 10 | | dB |


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For $V^+$ = 5.0V, $V^-$ = 0V, $R_L$ > 1MΩ connected to $V_S$ / 2, $V_{CM}$ = $V^+$ / 2, and $V_O$ = $V^+$ / 2, at $T_A$ = 25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing | $R_L$ = 100kΩ, From positive rail | | | 30 | 40 | mV |
| | | | $T_A$ = –40°C to 85°C | | | 70 | |
| | | $R_L$ = 100kΩ, From negative rail | | | 30 | 35 | |
| | | | $T_A$ = –40°C to 85°C | | | 50 | |
| | | $R_L$ = 10kΩ, From positive rail | | | 48 | 60 | |
| | | | $T_A$ = –40°C to 85°C | | | 150 | |
| | | $R_L$ = 10kΩ, From negative rail | | | 32 | 70 | |
| | | | $T_A$ = –40°C to 85°C | | | 90 | |
| | | $R_L$ = 5kΩ, From positive rail | | | 77 | 100 | |
| | | | $T_A$ = –40°C to 85°C | | | 150 | |
| | | $R_L$ = 5kΩ, From negative rail | | | 51 | 95 | |
| | | | $T_A$ = –40°C to 85°C | | | 120 | |
| $I_{SC}$ | Short-circuit current | Sourcing, LM6132A | | 2 | 4 | | mA |
| | | | $T_A$ = –40°C to 85°C | 2 | | | |
| | | Sourcing, LM6132B | | 2 | 4 | | |
| | | | $T_A$ = –40°C to 85°C | 1 | | | |
| | | Sinking, LM6132A | | 1.8 | 3.5 | | |
| | | | $T_A$ = –40°C to 85°C | 1.8 | | | |
| | | Sinking, LM6132B | | 1.8 | 3.5 | | |
| | | | $T_A$ = –40°C to 85°C | 1 | | | |
| | | Sourcing, LM6134A | | 2 | 3 | | |
| | | | $T_A$ = –40°C to 85°C | 1.6 | | | |
| | | Sourcing, LM6134B | | 2 | 3 | | |
| | | | $T_A$ = –40°C to 85°C | 1 | | | |
| | | Sinking, LM6134A | | 1.8 | 3.5 | | |
| | | | $T_A$ = –40°C to 85°C | 1.3 | | | |
| | | Sinking, LM6134B | | 1.8 | 3.5 | | |
| | | | $T_A$ = –40°C to 85°C | 1 | | | |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | LM6132AI, LM6134AI | | | 360 | 400 | µA |
| | | | $T_A$ = –40°C to 85°C | | | 450 | |
| | | LM6132BI, LM6134BI | | | 360 | 400 | µA |
| | | | $T_A$ = –40°C to 85°C | | | 450 | µA |

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## 5.7 Electrical Characteristics: $V_S$ = 2.7V

For $V^+$ = 2.7V, $V^-$ = 0V, $R_L$ > 1MΩ connected to $V_S$ / 2, $V_{CM}$ = $V^+$ / 2, and $V_O$ = $V^+$ / 2, at $T_A$ = 25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | LM6132AI, LM6134AI | | | 0.12 | 2 | mV |
| | | | $T_A$ = –40°C to 85°C | | | 8 | |
| | | LM6132BI, LM6134BI | | | 0.12 | 6 | |
| | | | $T_A$ = –40°C to 85°C | | | 12 | |
| PSRR | Input offset voltage versus power supply | 1.35V ≤ \|$V_S$\| ≤ 12V, | | | 80 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | 0V ≤ $V_{CM}$ ≤ 2.7V | | | 90 | | nA |
| $I_{OS}$ | Input offset current | | | | 2.8 | | nA |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Common-mode input voltage range | | | 0 | | 2.7 | V |
| CMRR | Common-mode rejection ratio | 0V ≤ $V_{CM}$ ≤ 2.7V | | | 82 | | dB |
| **INPUT IMPEDANCE** | | | | | | | |
| $R_{IN}$ | Common-mode input resistance | | | | 134 | | MΩ |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $R_L$ = 10kΩ | | | 100 | | V/mV |
| **NOISE** | | | | | | | |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain-bandwidth product | f = 20kHz, $R_L$ = 10 kΩ | | | 7 | | MHz |
| PM | Phase margin | $R_L$ = 10 kΩ | | | 23 | | ° |
| GM | Gain margin | | | | 12 | | dB |
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing | $R_L$ = 100kΩ, From positive rail | | | 40 | 50 | mV |
| | | | $T_A$ = –40°C to 85°C | | | 450 | |
| | | $R_L$ = 100kΩ, From negative rail | | | 30 | 80 | |
| | | | $T_A$ = –40°C to 85°C | | | 112 | |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | | | | 330 | | µA |


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## 5.8 Electrical Characteristics: $V_S$ = 24V

For $V^+$ = 24V, $V^-$ = 0V, $R_L$ > 1MΩ connected to $V_S$ / 2, $V_{CM}$ = $V^+$ / 2, and $V_O$ = $V^+$ / 2, at $T_A$ = 25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | LM6132AI, LM6134AI | | | 1.7 | 3 | mV |
| | | | $T_A$ = –40°C to 85°C | | | 5 | |
| | | LM6132BI, LM6134BI | | | 1.7 | 7 | |
| | | | $T_A$ = –40°C to 85°C | | | 9 | |
| PSRR | Input offset voltage versus power supply | 1.35V ≤ \|$V_S$\| ≤ 12V, | | | 82 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | 0V ≤ $V_{CM}$ ≤ 24V | | | 125 | | nA |
| $I_{OS}$ | Input offset current | | | | 4.8 | | nA |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Common-mode input voltage range | | | 0 | | 24 | V |
| CMRR | Common-mode rejection ratio | 0V ≤ $V_{CM}$ ≤ 24V | | | 82 | | dB |
| **INPUT IMPEDANCE** | | | | | | | |
| $R_{IN}$ | Common-mode input resistance | | | | 210 | | MΩ |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $R_L$ = 10kΩ | | | 102 | | V/mV |
| **NOISE** | | | | | | | |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain-bandwidth product | f = 20kHz, $R_L$ = 10 kΩ | | | 11 | | MHz |
| PM | Phase margin | $R_L$ = 10 kΩ | | | 23 | | ° |
| GM | Gain margin | $R_L$ = 10 kΩ | | | 12 | | dB |
| THD+N | Total harmonic distortion + noise | $V_O$ = 20$V_{PP}$, G = 1, f = 10kHz | | | 0.0015 | | % |
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing | $R_L$ = 10kΩ, From positive rail | | | 140 | 200 | mV |
| | | $R_L$ = 10kΩ, From negative rail | | | 75 | 150 | |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | | | | 390 | 450 | µA |
| | | $T_A$ = –40°C to 85°C | | | | 490 | |

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## 5.9 Typical Characteristics

at $T_A$ = 25°C and $R_L$ = 10 kΩ (unless otherwise specified)

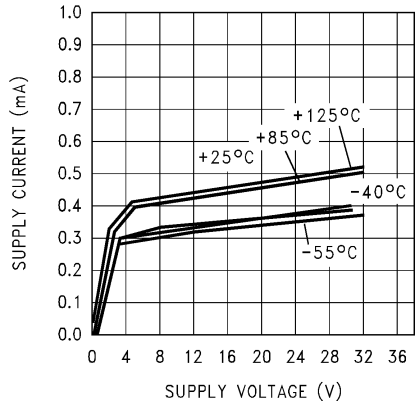



**Figure 5-1. Supply Current vs Supply Voltage**

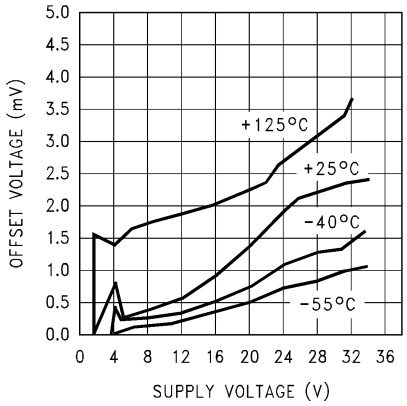



**Figure 5-2. Offset Voltage vs Supply Voltage**

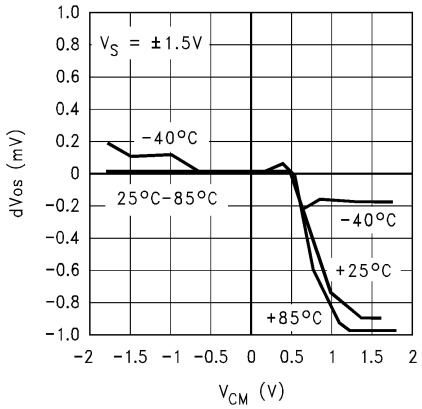



**Figure 5-3. $dV_{OS}$ vs $V_{CM}$**

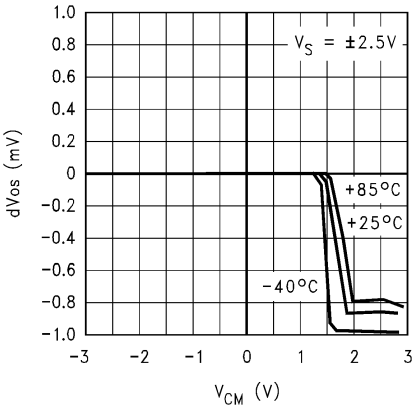



**Figure 5-4. $dV_{OS}$ vs $V_{CM}$**

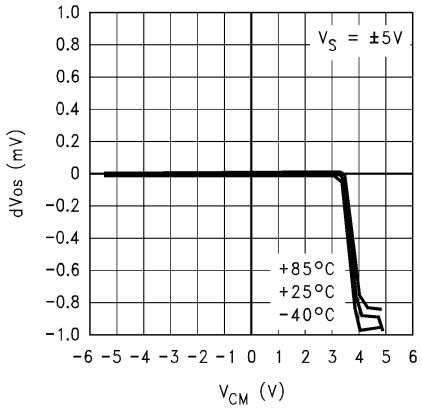



**Figure 5-5. $dV_{OS}$ vs $V_{CM}$**

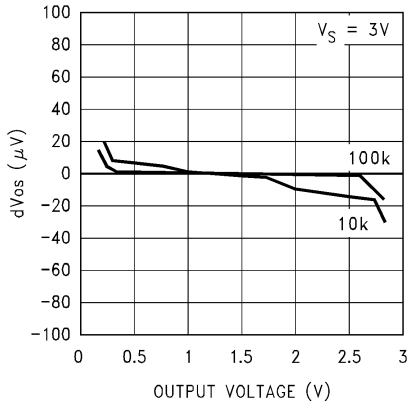



**Figure 5-6. $dV_{OS}$ vs Output Voltage**


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## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C and $R_L$ = 10 kΩ (unless otherwise specified)

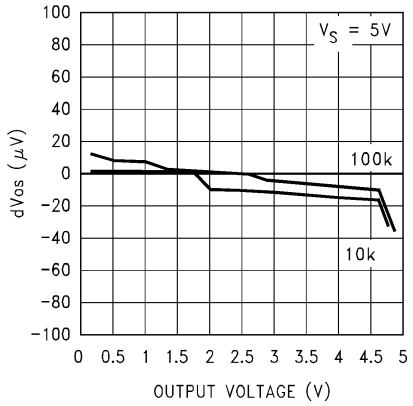



**Figure 5-7. $dV_{OS}$ vs Output Voltage**

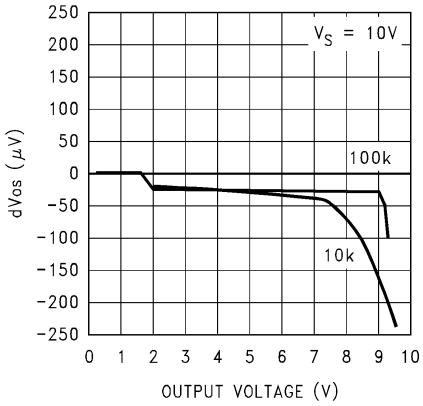



**Figure 5-8. $dV_{OS}$ vs Output Voltage**

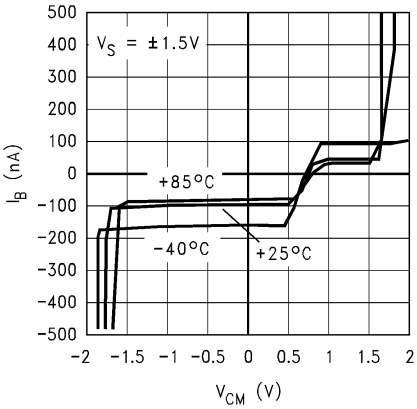



**Figure 5-9. $I_{BIAS}$ vs $V_{CM}$**

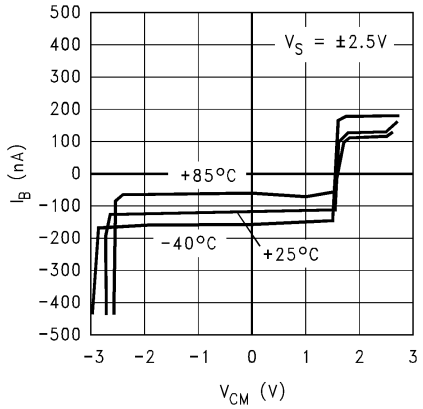



**Figure 5-10. $I_{BIAS}$ vs $V_{CM}$**

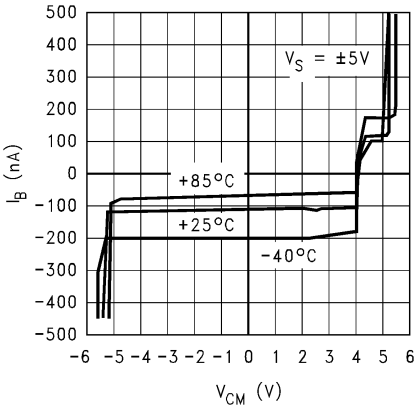



**Figure 5-11. $I_{BIAS}$ vs $V_{CM}$**

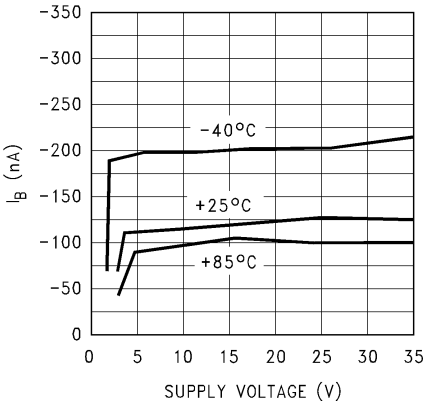



**Figure 5-12. Input Bias Current vs Supply Voltage**

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## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C and $R_L$ = 10 kΩ (unless otherwise specified)

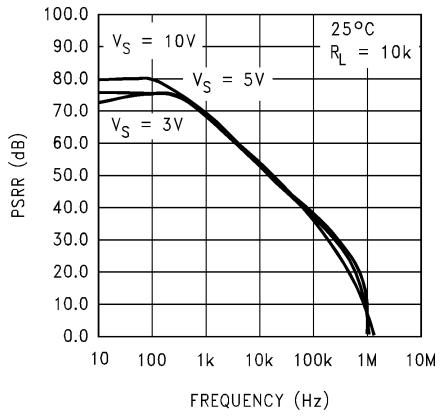



**Figure 5-13. Negative PSRR vs Frequency, Old Die**

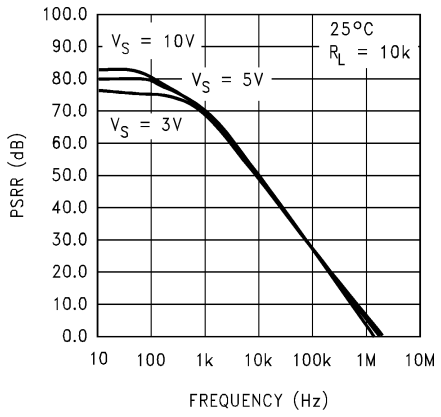



**Figure 5-14. Positive PSSR vs Frequency, Old Die**

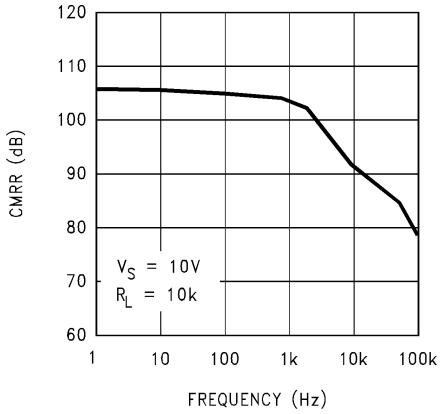



**Figure 5-15. CMRR vs Frequency, Old Die**

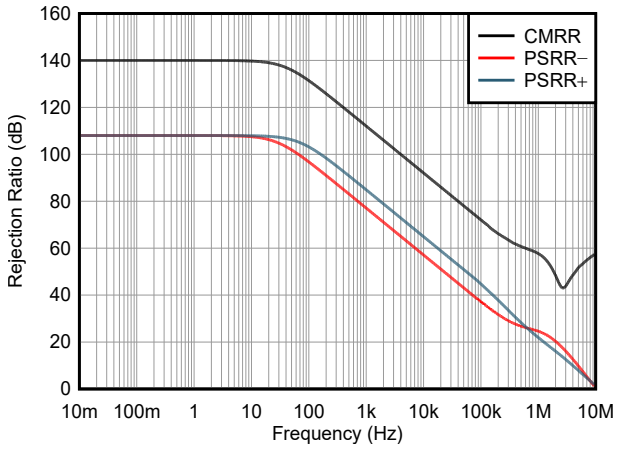



**Figure 5-16. CMRR and PSRR vs Frequency, New Die**

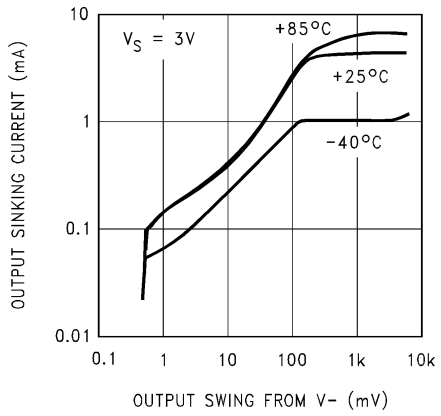



**Figure 5-17. Output Voltage vs Sinking Current**

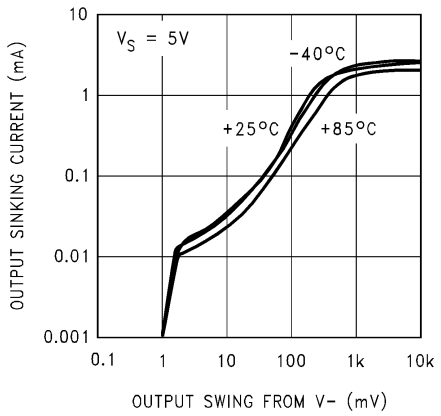



**Figure 5-18. Output Voltage vs Sinking Current**


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## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C and $R_L$ = 10 kΩ (unless otherwise specified)

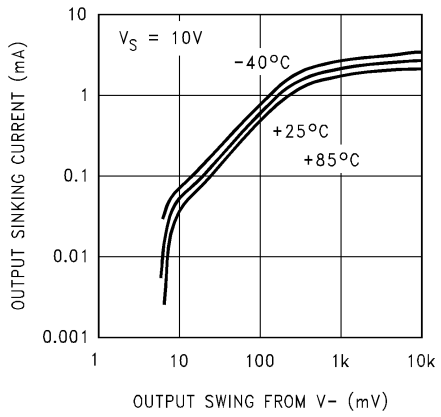



**Figure 5-19. Output Voltage vs Sinking Current**

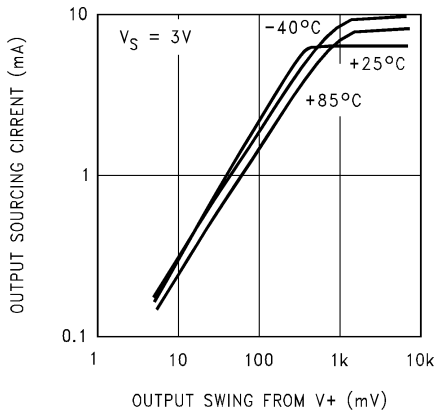



**Figure 5-20. Output Voltage vs Sourcing Current**

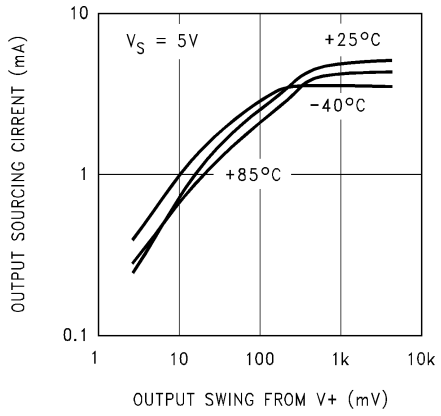



**Figure 5-21. Output Voltage vs Sourcing Current**

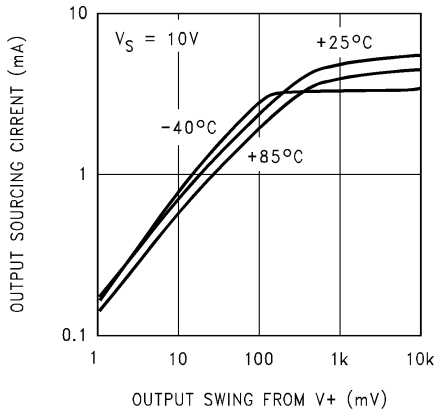



**Figure 5-22. Output Voltage vs Sourcing Current**

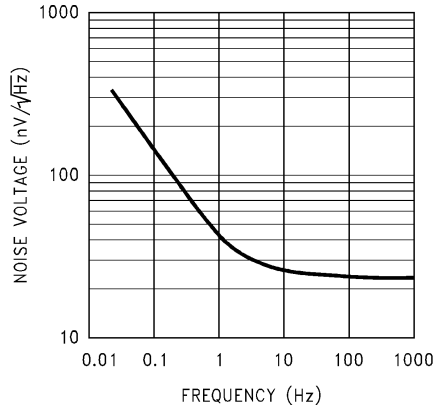



**Figure 5-23. Noise Voltage vs Frequency**

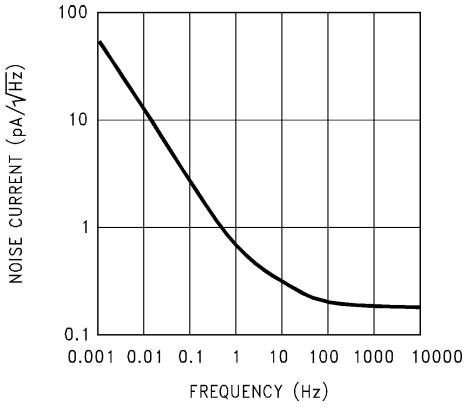



**Figure 5-24. Noise Current vs Frequency**

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## 5.9 Typical Characteristics (continued)

at $T_A$ = 25°C and $R_L$ = 10 kΩ (unless otherwise specified)

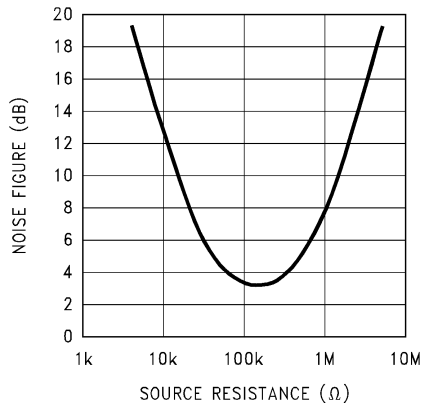



**Figure 5-25. NF vs Source Resistance**

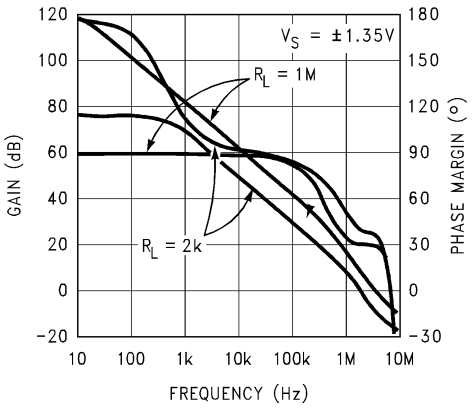



**Figure 5-26. Gain and Phase vs Frequency, Old Die**

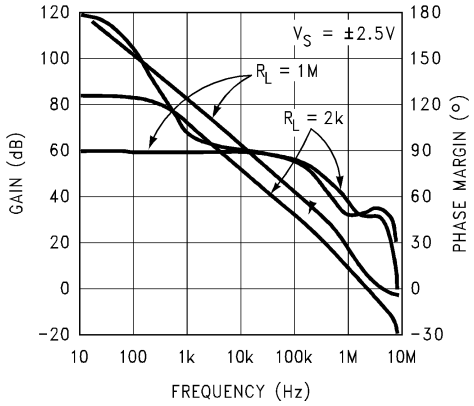



**Figure 5-27. Gain and Phase vs Frequency, Old Die**

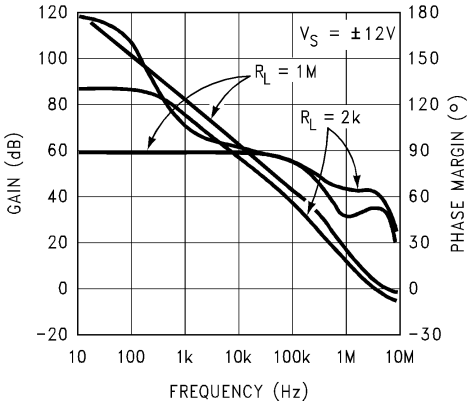



**Figure 5-28. Gain and Phase vs Frequency, Old Die**

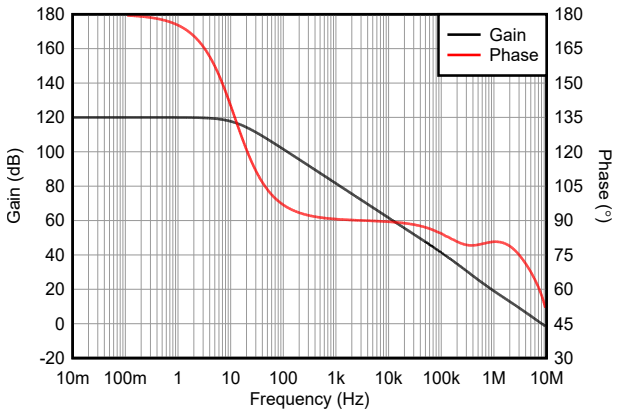



**Figure 5-29. Gain and Phase vs Frequency, New Die**

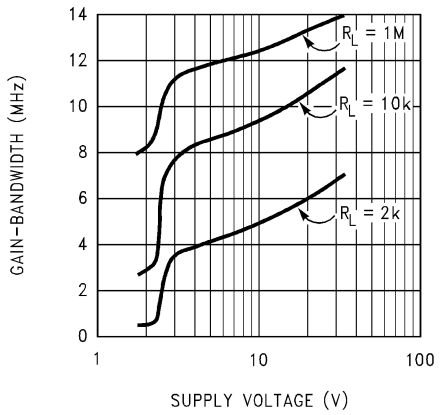



**Figure 5-30. GBW vs Supply Voltage at 20 kHz**


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## 5.10 Old Versus New Die Comparison

As of the publication of revision F of this data sheet, Texas Instruments has moved manufacturing of the die for LM6132 and LM6134 to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die. The die origin can be separated from the “Chip Source Origin” (CSO) parameter in the shipping information. The old die CSO is “GF6”, for the new die CSO is “RFB”. The old die information is maintained in this data sheet for comparison purposes, but all new manufacturing has moved to the new die.

**Table 5-1. Old Versus New Die Comparison**

| Description | Old Die | New Die |
|---|---|---|
| Minimum supply voltage | 1.8V | 2.7V |
| Typical output voltage range for 100kΩ load ($V_S$ = 5V) | 0.007V - 4.992V | 0.03V - 4.97V |
| Minimum output voltage range for 100kΩ load ($V_S$ = 5V) | 0.017V - 4.98V | 0.04V - 4.965V |
| Output voltage slew architecture | Standard slew architecture | Slew-boosted architecture |

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# 6 Application and Implementation

## 6.1 Application Information

The LM6132 brings a new level of ease of use to op amp system design. Greater than rail-to-rail input voltage eliminates concern over exceeding the common-mode voltage range.

Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications, where high power consumption previously reduced battery life to unacceptable levels.

To take advantage of these features, keep some ideas in mind, which are outlined in subsequent sections.


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## 6.2 Typical Applications

### *6.2.1 Three Op Amp Instrumentation Amp with Rail-to-Rail Input and Output*

Using the LM6134, a 3 op amp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers an excellent choice for single supply systems.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that the method also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6134, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage (Figure 6-1). These buffers assure that the input impedance is over 100MΩ and they eliminate the requirement for precision matched resistors in the input stage. The buffers also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1–R2 with R3–R4.

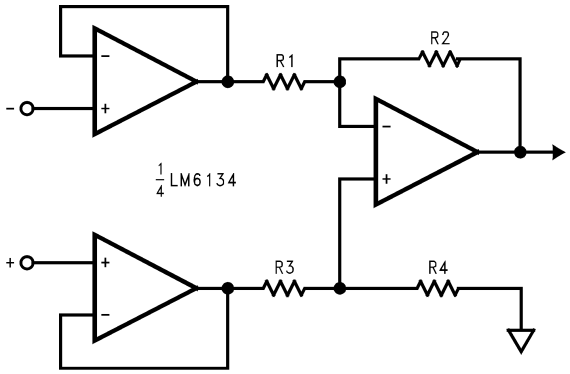



**Figure 6-1. Instrumentation Amplifier**

### *6.2.2 Flat Panel Display Buffering*

Three features of the LM6132/34 make the device a superb choice for TFT LCD applications. First, the low current draw (360µA per amplifier at 5V) makes the device an excellent choice for battery powered applications such as in laptop computers. Second, since the device operates down to 2.7V, the device is a natural choice for next generation 3V TFT panels. Last, but not least, the large capacitive drive capability of the LM6132 comes in very handy in driving highly capacitive loads that are characteristic of LCD display drivers.

The large capacitive drive capability of the LM6132/34 allows the device to be used as buffers for the gamma correction reference voltage inputs of resistor-DAC type column (Source) drivers in TFT LCD panels. This amplifier is also useful for buffering only the center reference voltage input of Capacitor-DAC type column (Source) drivers such as the LMC750X series.

Since for VGA and SVGA displays, the buffered voltages must settle within approximately 4µs, the well known technique of using a small isolation resistor in series with the amplifier's output very effectively dampens the ringing at the output.

With the wide supply voltage range of 2.7V to 24V, the LM6132/34 can be used for a diverse range of applications. The system designer is thus able to select a single device type that serves many sub-circuits in the system, eliminating the need to specify multiple devices in the bill of materials. Along with the sister parts, the LM6142 and LM6152 that have the same wide supply voltage capability, choice of the LM6132 in a design eliminates the need to search for multiple sources for new designs.

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# 7 Device and Documentation Support

## 7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (September 2014) to Revision F (June 2026) | Page |
|---|---|
| • Deleted "Swing 0.01V to 4.99V" in *Features* | 1 |
| • Deleted Supply Current vs. Supply Voltage plot | 1 |
| • Deleted Offset Voltage vs. Supply Voltage plot | 1 |
| • Added Functional Block Diagram | 1 |
| • Updated table note 3 in *Absolute Maximum Ratings* | 4 |
| • Changed from (V–) – 0.3V to (V–) – 0.5V | 4 |
| • Changed from (V+) + 0.3V to (V+) + 0.5V | 4 |
| • Updated table note 4 in *Absolute Maximum Ratings* | 4 |
| • Updated table note 2 in *Absolute Maximum Ratings* | 4 |
| • Changed from ±25mA to Continuous | 4 |
| • Changed rating from Current at Output Pin to Output short circuit | 4 |
| • Added Operating ambient temperature rating | 4 |
| • Added CDM ESD rating | 4 |
| • Updated table note in *ESD Ratings* | 4 |
| • Added table note in *ESD Ratings* | 4 |
| • Deleted table note 1 in *Recommended Operating Conditions* | 4 |
| • Changed minimum supply voltage from 1.8V to 2.7V | 4 |
| • Changed Junction-to-case thermal resistance for LM6132D from 193°C/W to 127.1°C/W | 5 |
| • Changed Junction-to-case thermal resistance for LM6132P from 115°C/W to 84.45°C/W | 5 |
| • Added Junction-to-case (top) thermal resistance for packages | 5 |
| • Added Junction-to-board thermal resistance for packages | 5 |
| • Added Junction-to-top characterization parameter for packages | 5 |


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- Added Junction-to-board characterization parameter for packages....5
- Changed Junction-to-case thermal resistance for LM6134D from 126°C/W to 82.48°C/W....5
- Updated all *Electrical Characteristics* tables to latest format....6
- Updated Output Swing format to refer to rails....6
- Changed typical voltage output swing for 100kΩ load from 4.992V to 30mV from positive rail....6
- Changed maximum voltage output swing for 100kΩ load from 4.98V to 40mV from positive rail....6
- Changed typical voltage output swing for 100kΩ load from 0.007V to 30mV from negative rail....6
- Changed maximum voltage output swing for 100kΩ load from 0.017V to 35mV from negative rail....6
- Changed maximum voltage output swing for 100kΩ load over temperature from 0.019V to 50mV from negative rail....6
- Deleted table notes for all *Electric Characteristic* tables....6
- Updated Output Swing format to refer to rails....8
- Updated Output Swing format to refer to rails....9
- Added CMRR and PSRR vs Frequency plot for new die....10
- Added Gain and Phase vs Frequency plot for new die....10
- Added a new sub-section *Old Versus New Die Comparison*....15
- Deleted sub-section *Enhanced Slew Rate*....16

**Changes from Revision D (February 2013) to Revision E (September 2014)** **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....0

**Changes from Revision C (February 2013) to Revision D (February 2013)** **Page**

- Changed layout of National Semicondutor Data Sheet to TI format....17

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM6132AIM/NOPB | Obsolete | Production | SOIC (D) \| 8 | - | - | Call TI | Call TI | -40 to 85 | LM61 32AIM |
| LM6132AIMX/NOPB | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | (LM61, M6132A) 32AIM |
| LM6132AIMX/NOPB.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (LM61, M6132A) 32AIM |
| LM6132AIMX/NOPB.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (LM61, M6132A) 32AIM |
| LM6132BIMX/NOPB | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM61 32BIM |
| LM6132BIMX/NOPB.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM61 32BIM |
| LM6132BIMX/NOPB.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM61 32BIM |
| LM6132BIN/NOPB | Active | Production | PDIP (P) \| 8 | 40 \| TUBE | Yes | NIPDAU | Level-1-NA-UNLIM | -40 to 85 | (LM6132, LM6132BIN) BIN |
| LM6132BIN/NOPB.A | Active | Production | PDIP (P) \| 8 | 40 \| TUBE | Yes | NIPDAU | Level-1-NA-UNLIM | -40 to 85 | (LM6132, LM6132BIN) BIN |
| LM6132BIN/NOPB.B | Active | Production | PDIP (P) \| 8 | 40 \| TUBE | Yes | NIPDAU | Level-1-NA-UNLIM | -40 to 85 | (LM6132, LM6132BIN) BIN |
| LM6134AIM/NOPB | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | -40 to 85 | LM6134AIM |
| LM6134AIMX/NOPB | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM6134AIM |
| LM6134AIMX/NOPB.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM6134AIM |
| LM6134BIM/NOPB | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | -40 to 85 | LM6134BIM |
| LM6134BIMX/NOPB | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM6134BIM |
| LM6134BIMX/NOPB.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | LM6134BIM |
| LM6134BIN/NOPB | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | Level-1-NA-UNLIM | -40 to 85 | LM6134BIN |
| LM6134BIN/NOPB.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | Level-1-NA-UNLIM | -40 to 85 | LM6134BIN |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

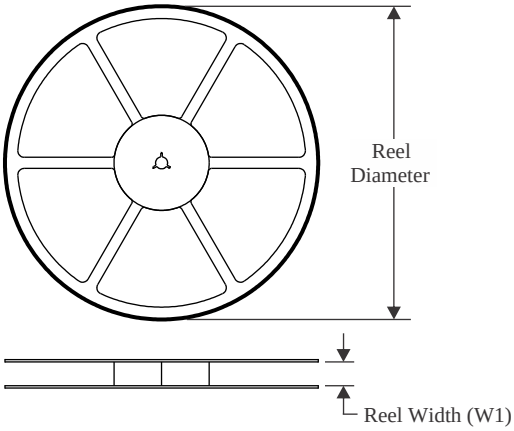
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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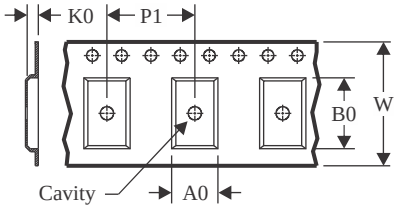
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

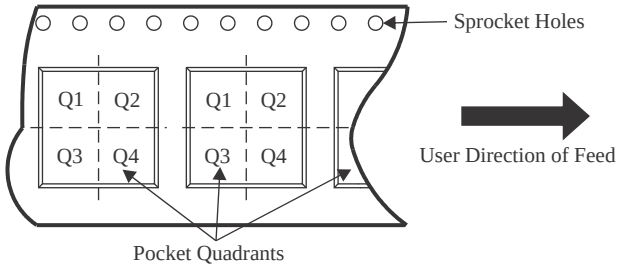



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

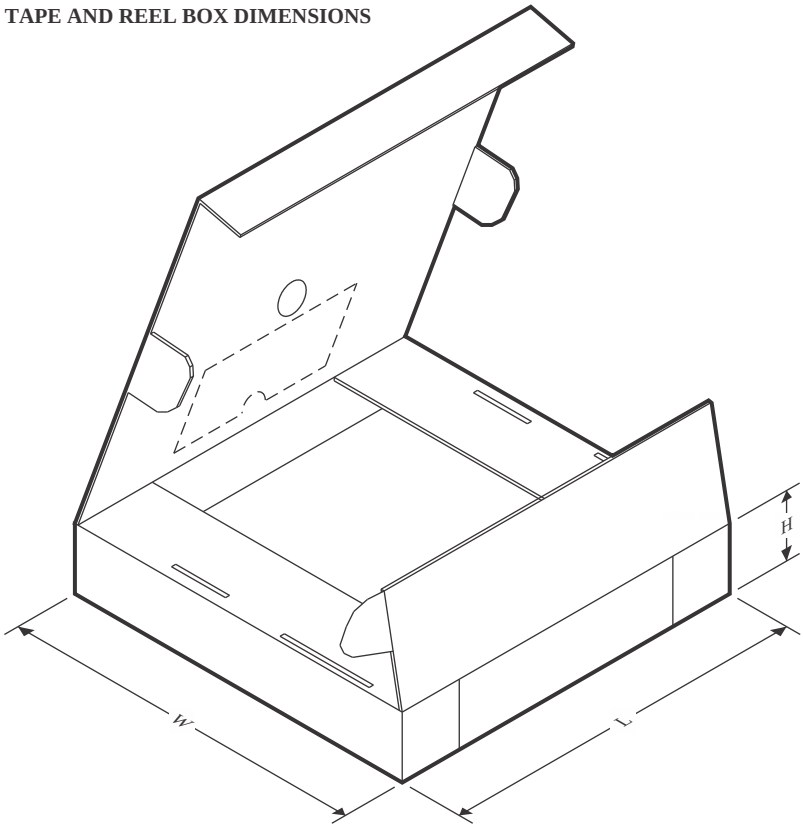
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM6132AIMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LM6132BIMX/NOPB | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| LM6134AIMX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |
| LM6134BIMX/NOPB | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.35 | 2.3 | 8.0 | 16.0 | Q1 |

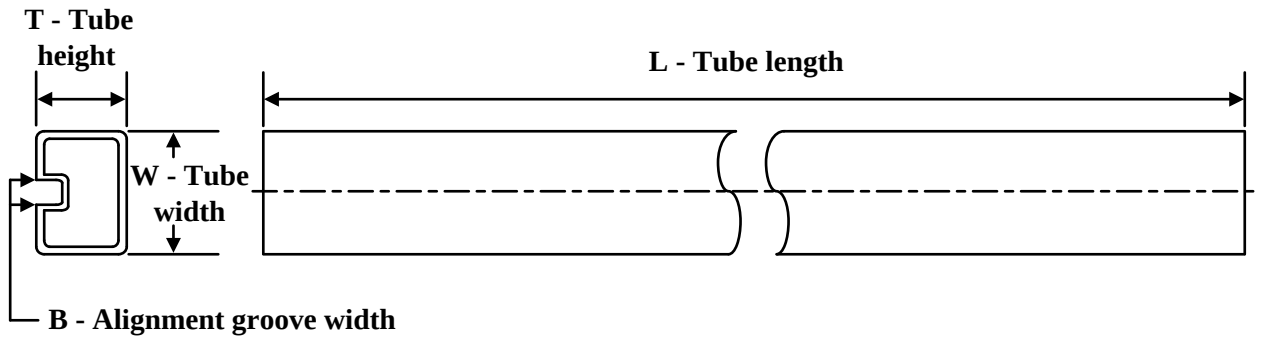
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

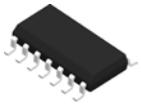
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM6132AIMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LM6132BIMX/NOPB | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LM6134AIMX/NOPB | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |
| LM6134BIMX/NOPB | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM6132BIN/NOPB | P | PDIP | 8 | 40 | 506 | 13.97 | 11230 | 4.32 |
| LM6132BIN/NOPB | P | PDIP | 8 | 40 | 502 | 14 | 11938 | 4.32 |
| LM6132BIN/NOPB.A | P | PDIP | 8 | 40 | 502 | 14 | 11938 | 4.32 |
| LM6132BIN/NOPB.A | P | PDIP | 8 | 40 | 506 | 13.97 | 11230 | 4.32 |
| LM6132BIN/NOPB.B | P | PDIP | 8 | 40 | 506 | 13.97 | 11230 | 4.32 |
| LM6132BIN/NOPB.B | P | PDIP | 8 | 40 | 502 | 14 | 11938 | 4.32 |
| LM6134BIN/NOPB | N | PDIP | 14 | 25 | 502 | 14 | 11938 | 4.32 |
| LM6134BIN/NOPB.A | N | PDIP | 14 | 25 | 502 | 14 | 11938 | 4.32 |

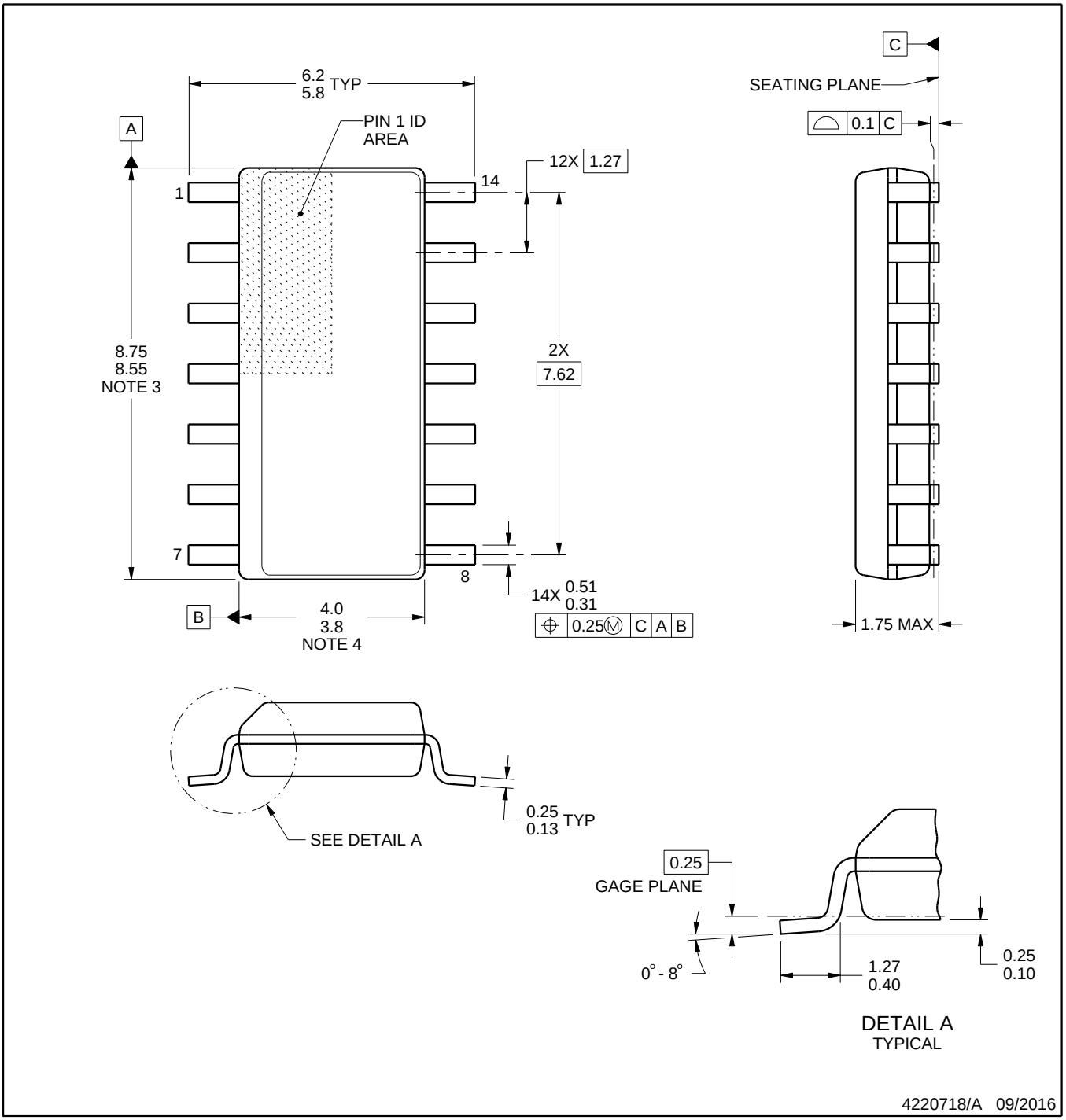


# PACKAGE OUTLINE

## D0014A

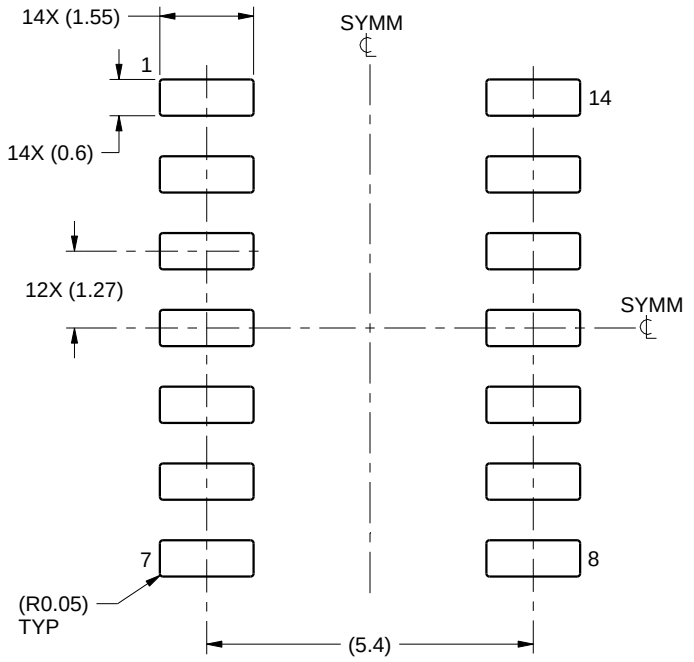
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

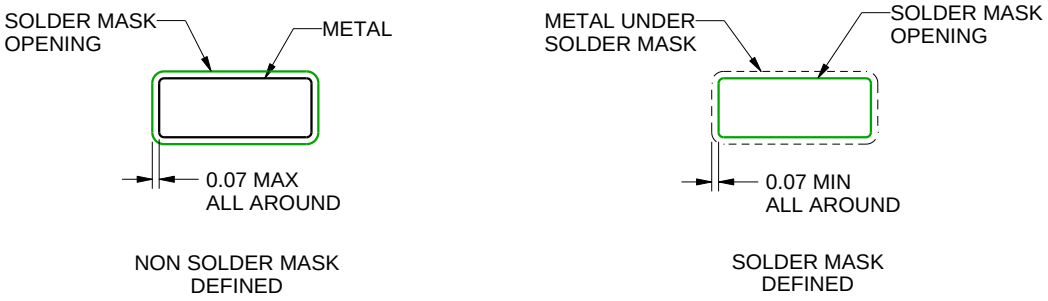



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

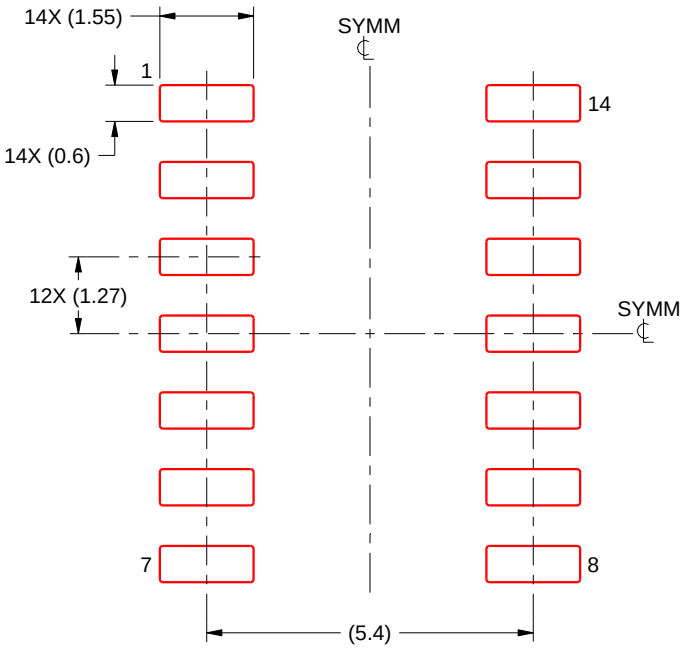
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

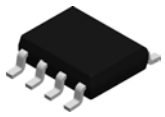



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

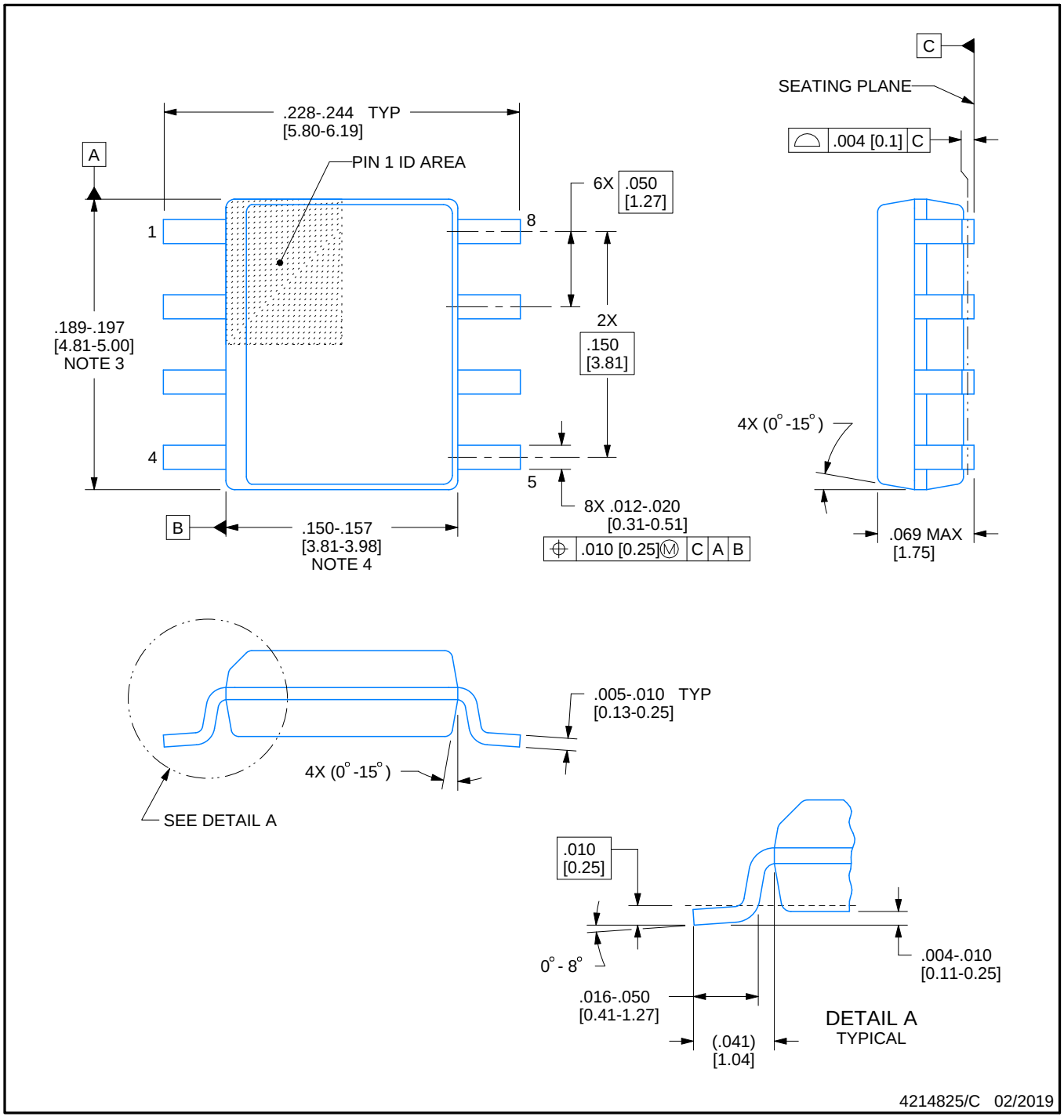


# PACKAGE OUTLINE

## D0008A

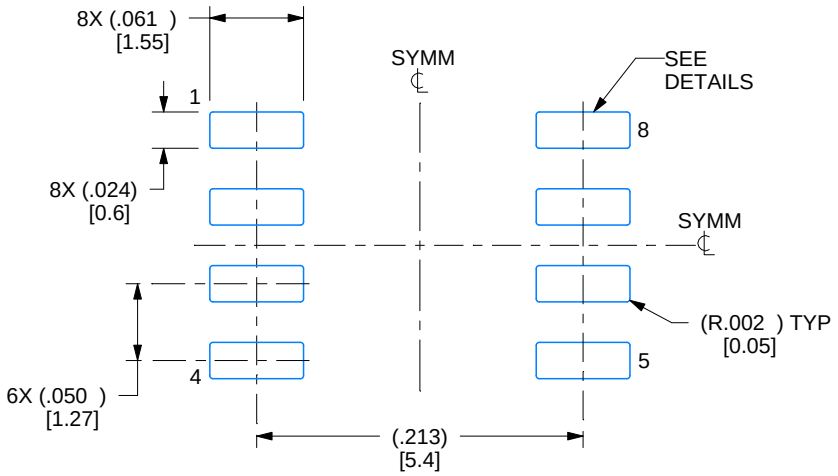
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

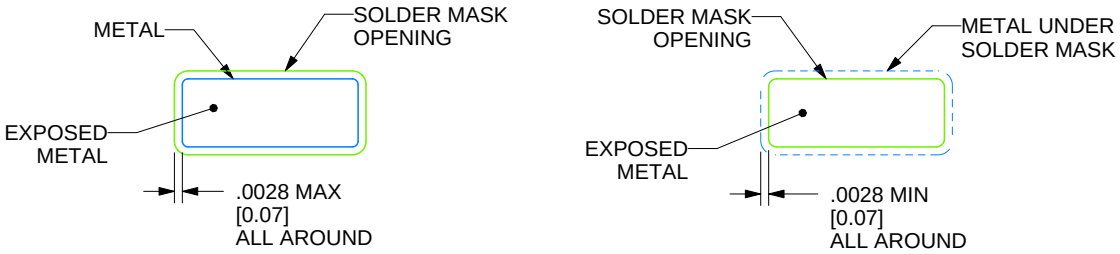



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

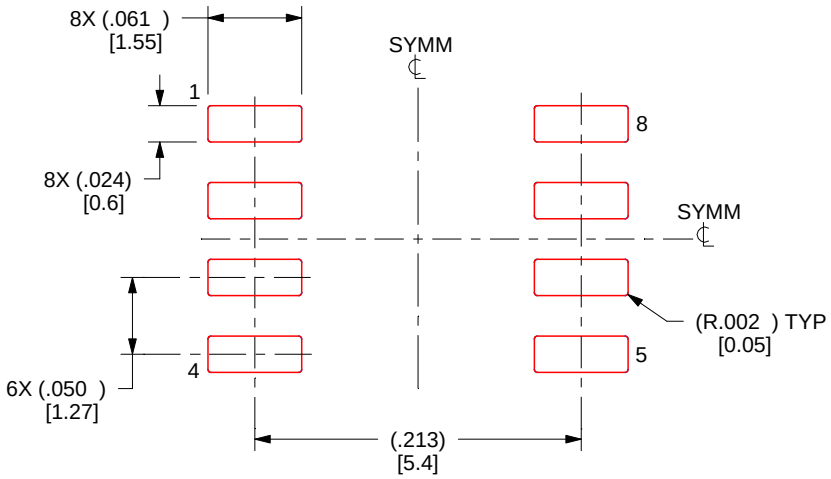
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



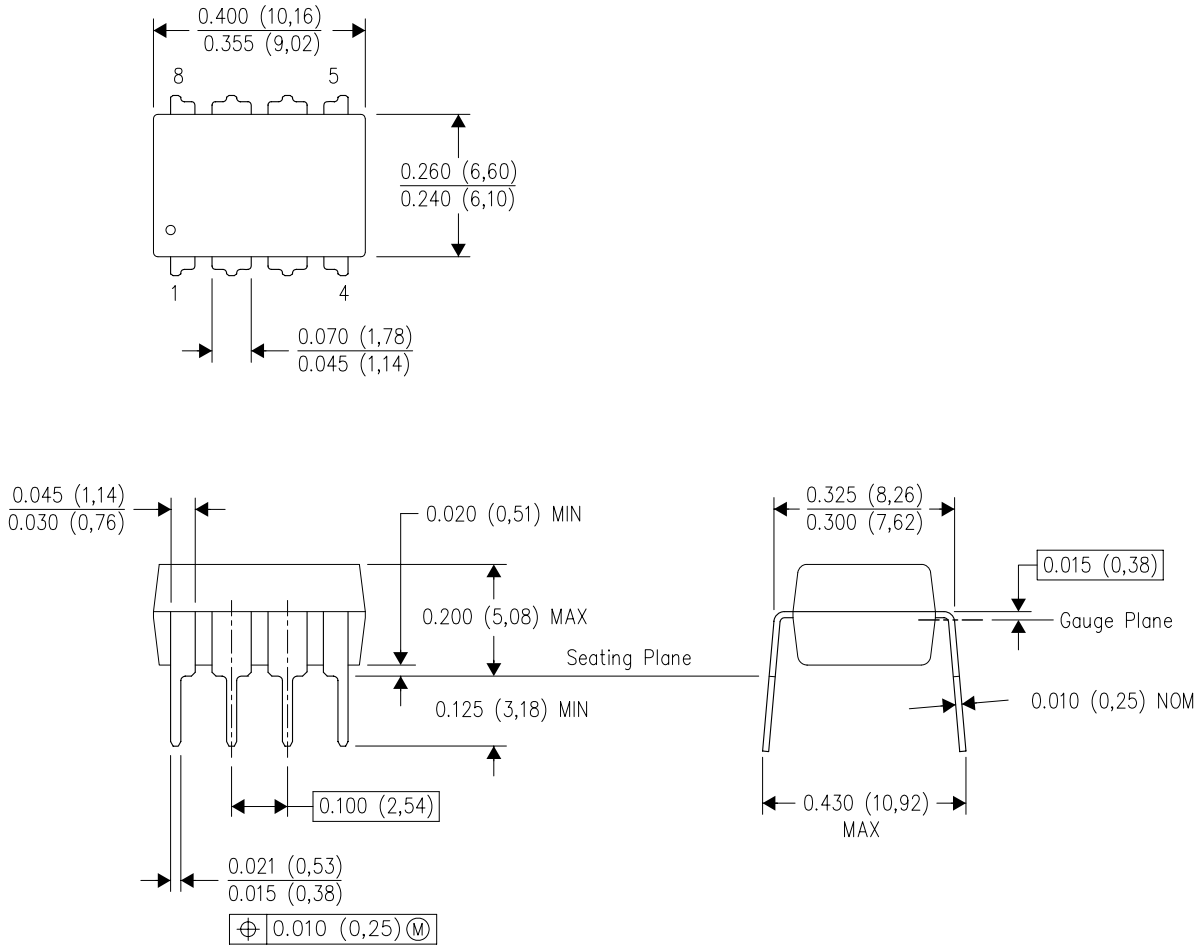

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

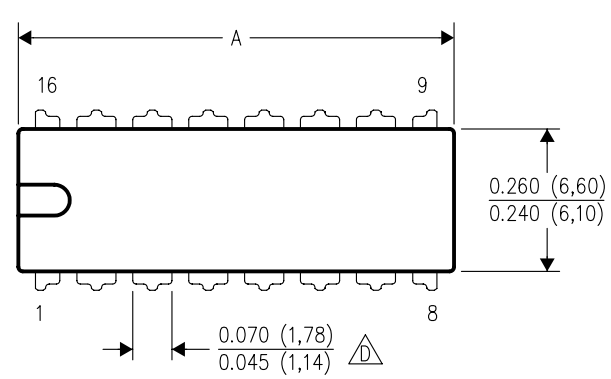



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

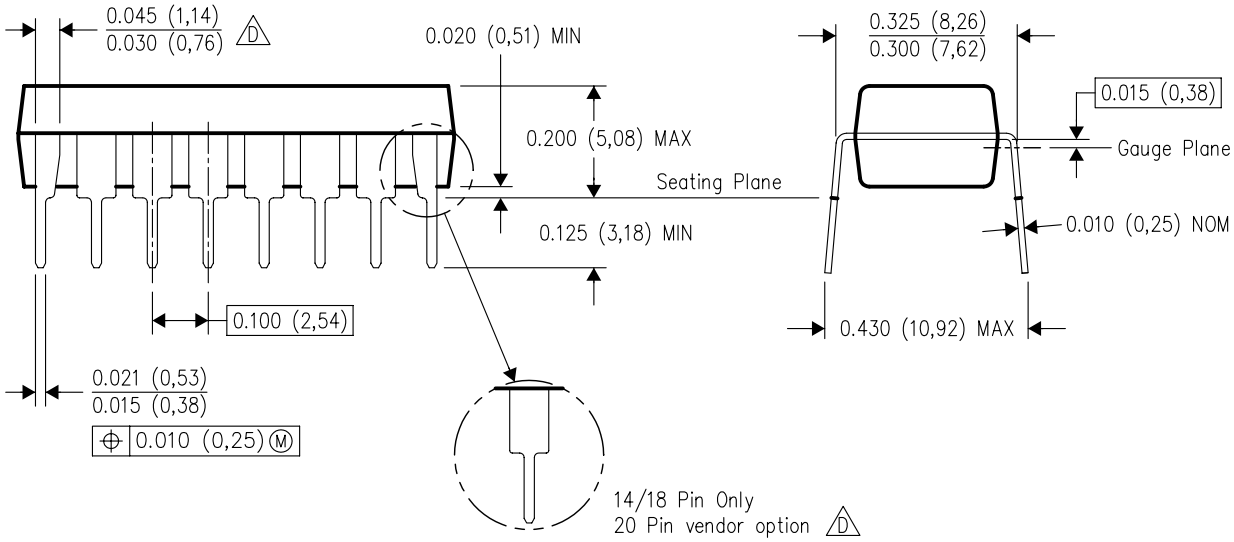
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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