LM3526 Dual Port USB Power Switch and Over-Current Protection

Check for Samples: LM3526

FEATURES

- **Compatible with USB1.1 and USB 2.0**
- **1 ms Fault Flag Delay Filters Hot-Plug Events**
- **Smooth Turn-on Eliminates In-rush Induced Voltage Drop**
- **UL Recognized Component: REF# 205202**
- **1A Nominal Short Circuit Output Current Protects PC Power Supplies**
- **Thermal Shutdown Protects Device in Direct Short Condition**
- **500mA Minimum Continuous Load Current**
- **Small SOIC-8 package minimizes board space**
- **2.7V to 5.5V Input Voltage Range**
- **140 mΩ Max. Switch Resistance**
- **1 µA Max. Standby Current**
- **200 µA Max. Operating Current**
- **Under-voltage Lockout (UVLO)**

APPLICATIONS

- **Universal Serial Bus (USB) Root Hubs including Desktop and Notebook PC**
- **USB Monitor Hubs**
- **Other Self-Powered USB Hub Devices**
- **High Power USB Devices Requiring In-rush Limiting**
- **General Purpose High Side Switch Applications**

DESCRIPTION

The LM3526 provides Universal Serial Bus standard power switch and over-current protection for all host port applications. The dual port device is ideal for Notebook and desktop PC's that supply power to more than one port.

A 1 ms delay on the fault flag output prevents erroneous overcurrent reporting caused by in-rush currents during hot-plug events.

The dual stage thermal protection circuit in the LM3526 provides individual protection to each switch and the entire device. In a short-circuit/over-current event, the switch dissipating excessive heat is turned off, allowing the second switch to continue to function uninterrupted.

The LM3526 accepts an input voltage between 2.7V and 5.5V allowing use as a device-based in-rush current limiter for 3.3V USB peripherals, as well as Root and Self-Powered Hubs at 5.5V. The Enable inputs accept both 3.3V and 5.0V logic thresholds.

The small size, low R_{ON}, and 1 ms fault flag delay make the LM3526 a good choice for root hubs as well as per-port power control in embedded and stand-alone hubs.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Typical Operating Circuit and Connection Diagram

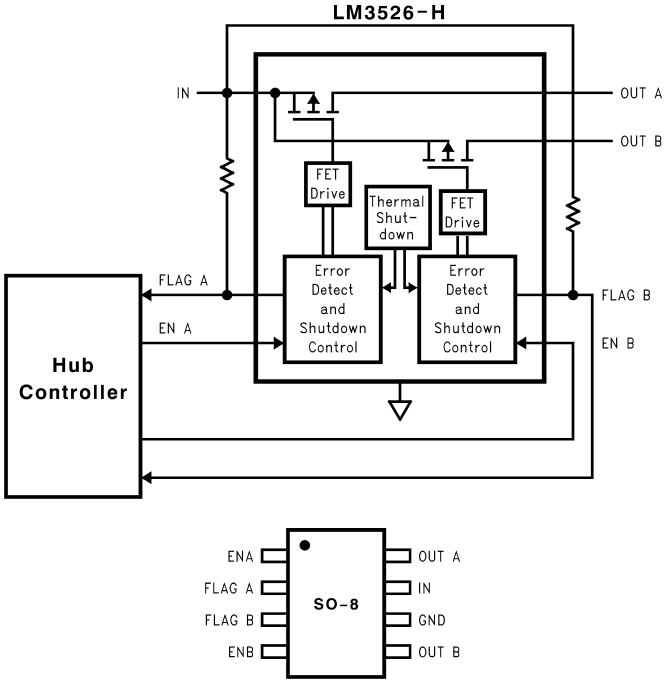


Figure 1. LM3526-H

UL Recognized Component

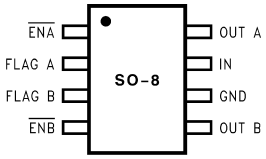


Figure 2. LM3526-L

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Absolute Maximum Ratings[1][2]

Supply Voltage	−0.3V to 6V
Output Voltage	−0.3V to 6V
Voltage at All Other Pins	−0.3V to 5.5V
Power Dissipation (T_A = 25°C)[3]	700 mW
T_{JMAX}[3]	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} (Maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, which ever is lower. θ_{JA} = 150°C/W.

Operating Ratings

Supply Voltage Range	2.7V to 5.5V
Operating Ambient Range	−40°C to 85°C
Operating Junction Temperature Range	−40°C to 125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 5 seconds)	260°C
ESD Rating[1]	2kV
ESD Rating Output Only	8kV

(1) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. Enable pin ESD threshold is 1.7kV.

DC Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface** type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 5.0V, $V_{\overline{EN}}$ = 0V (LM3526-L) or V_{EN} = V_{IN} (LM3526-H).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{ON}	On Resistance	V_{IN} = 5V, I_{OUT} = 500mA, each switch		100	140	mΩ
		V_{IN} = 2.7V, I_{OUT} = 500mA, each switch		110	180	
I_{OUT}	OUT pins continuous output current	Each Output	**0.5**			A
I_{SC}	Short Circuit Output Current	Each Output (enable into Load)[1]				A
		V_{OUT} = 4.0V	0.5	1.2	1.9	
		V_{OUT} = 0.1V		1	1.5	
OC_{THRESH}	Over-current Threshold			2.2	3.2	A
I_{LEAK}	OUT pins Output Leakage Current	$V_{\overline{EN}}$ = V_{IN} (LM3526-L) V_{EN} = 0V (LM3526-H)		0.01	10	µA
R_{FO}	FLAG Output Resistance	I_{FO} = 10 mA, V_{IN} = 5.0V		10	**25**	Ω
		I_{FO} = 10 mA, V_{IN} = 3.3V		11	**35**	
		I_{FO} = 10 mA, V_{IN} = 2.7V		12	**40**	
I_{EN}	$\overline{EN}$/EN Leakage Current	$V_{\overline{EN}}/V_{EN}$ = 0V or $V_{\overline{EN}}/V_{EN}$ = V_{IN}	−0.5		0.5	µA
V_{IH}	$\overline{EN}$/EN Input Logic High	See[2]	**2.4**	1.9		V
V_{IL}	$\overline{EN}$/EN Input Logic Low	See[2]		1.7	**0.8**	V
V_{UVLO}	Under-Voltage Lockout Threshold			1.8		V
I_{DDOFF}	Supply Current	Switch-Off −40°C ≤ T_J ≤ 85°C		0.2	1 **2**	µA
I_{DDON}	Supply Current	Switch-On		115	200	µA
Th_{SD}	Over-temperature Shutdown Threshold	T_J Increasing, with no shorted output T_J Increasing, with shorted output (s) T_J Decreasing[1]		150 145 135		°C

(1) Thermal Shutdown will protect the device from permanent damage.
(2) For LM3526-L, OFF is $\overline{EN}$ ≥ 2.4V and ON is $\overline{EN}$ ≤ 0.8V. For LM3526-H, OFF is EN ≤ 0.8V and ON is EN ≥ 2.4V.

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DC Electrical Characteristics (continued)

Limits in standard typeface are for T_J = 25°C, and limits in **boldface** type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 5.0V, $V_{\overline{EN}}$ = 0V (LM3526-L) or V_{EN} = V_{IN} (LM3526-H).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{FH}	Error Flag Leakage Current	V_{flag} = 5V		0.01	1	µA

AC Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface** type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 5.0V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_r	OUT Rise Time	R_L = 10Ω		100		µs
t_f	OUT Fall Time	R_L = 10Ω		5		µs
t_{ON}	Turn on Delay, $\overline{EN}$ to OUT	R_L = 10Ω		150		µs
t_{OFF}	Turn off Delay, $\overline{EN}$ to OUT	R_L = 10Ω		5		µs
t_{OC}	Over Current Flag Delay	R_L = 0		1		ms

TYPICAL APPLICATION CIRCUIT

PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Function
1, 4	$\overline{ENA}$, $\overline{ENB}$ (LM3526-L) ENA, ENB (LM3526-H)	Enable (Input): Logic-compatible enable inputs.
2, 3	FLAG A FLAG B	Fault Flag (Output): Active-low, open-drain outputs. Indicates overcurrent, UVLO or thermal shutdown. *See Application Information for more information.
6	GND	Ground
7	IN	Supply Input: This pin is the input to the power switch and the supply voltage for the IC.
8, 5	OUT A OUT B	Switch Output: These pins are the outputs of the high side switch.

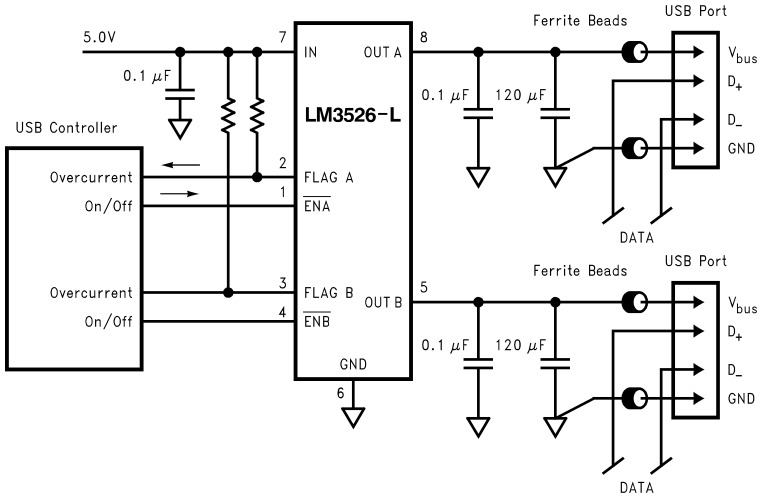


Figure 3. Typical Application Circuit

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Typical Performance Characteristics

V_{IN} = 5.0V, I_L = 500 mA, T_A = 25°C unless otherwise specified.

R_{ON} vs Temperature

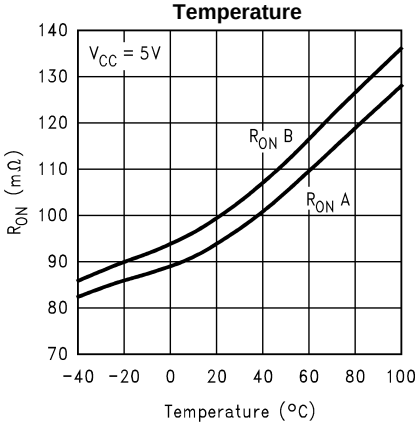


Figure 4.

R_{ON} vs Temperature

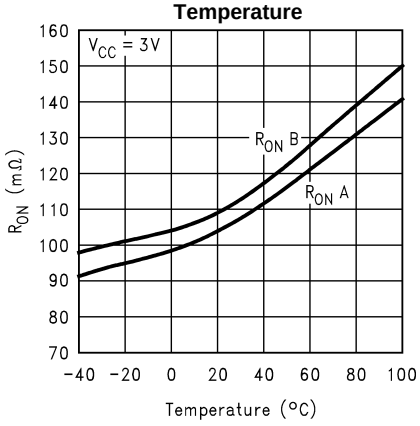


Figure 5.

Quiescent Current vs Input Voltage

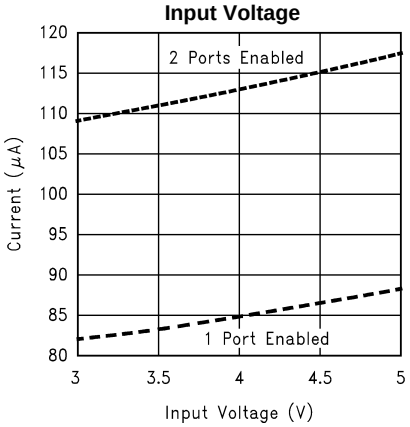


Figure 6.

Quiescent Current vs Temperature

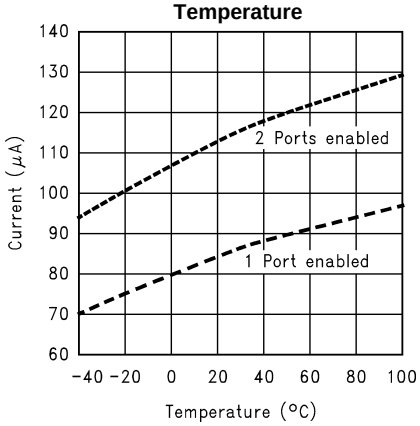


Figure 7.

Current Limit vs Output Voltage

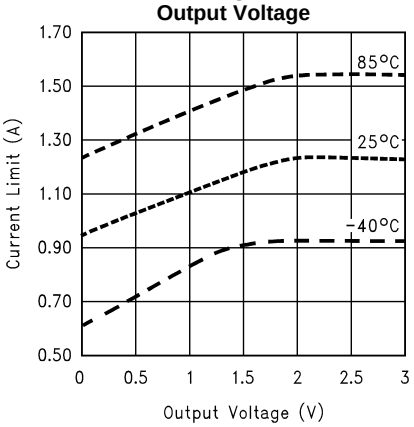


Figure 8.

OC Threshold vs Temperature

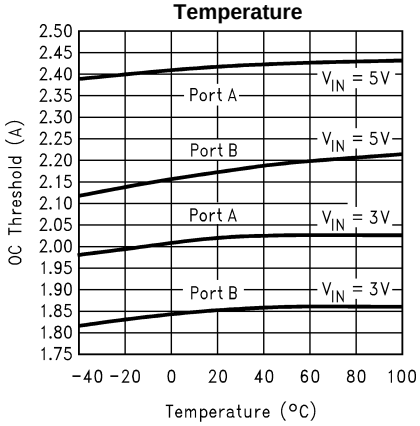


Figure 9.

Typical Performance Characteristics (continued)

V_{IN} = 5.0V, I_L = 500 mA, T_A = 25°C unless otherwise specified.

Fault Flag Delay vs Temperature

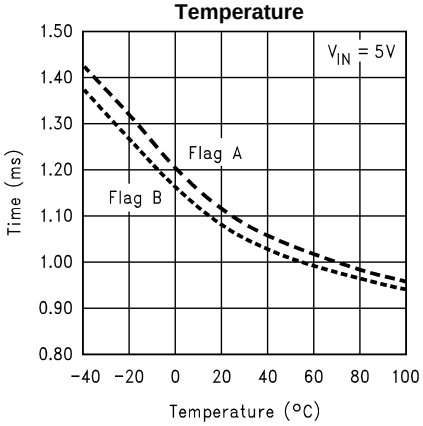


Figure 10.

Fault Flag Delay vs Temperature

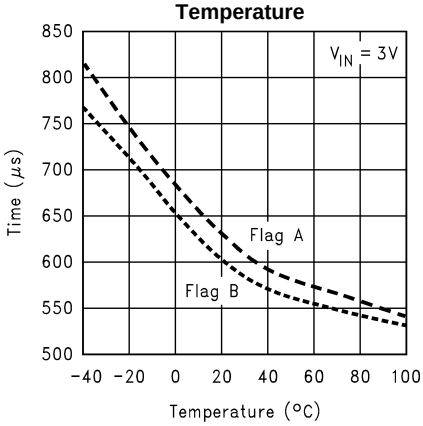


Figure 11.

Under Voltage Lockout (UVLO)

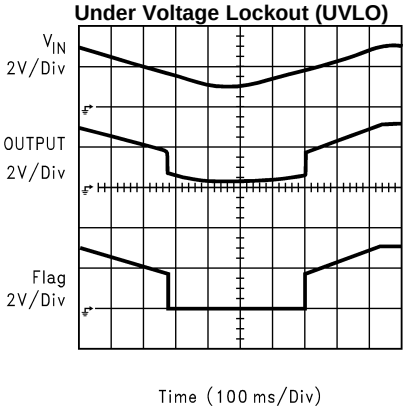


Figure 12.

Under Voltage Lockout Threshold vs Temperature

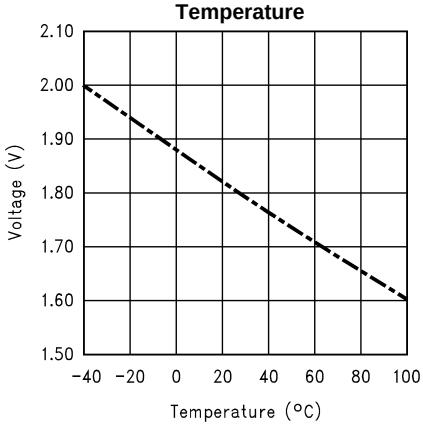
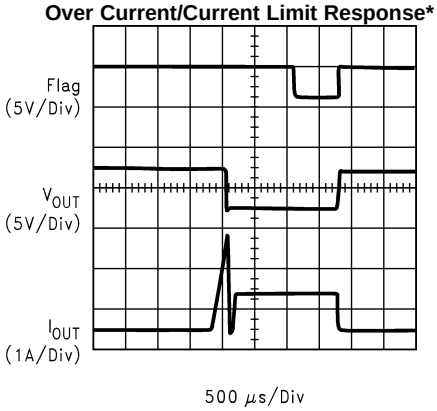


Figure 13.

Over Current/Current Limit Response*



* Output is shorted to Ground through a 100 mΩ resistor

Figure 14.

Short Circuit Response with Thermal Cycling*

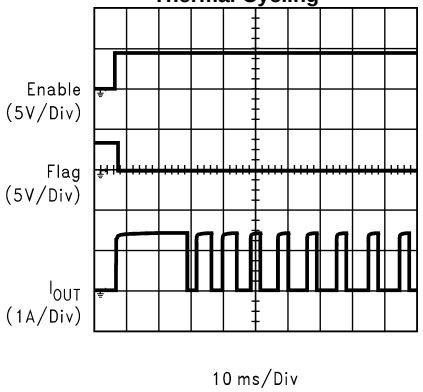


Figure 15.

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Typical Performance Characteristics (continued)

V_{IN} = 5.0V, I_L = 500 mA, T_A = 25°C unless otherwise specified.

Turn-ON/OFF Response with 47Ω/10µF Load

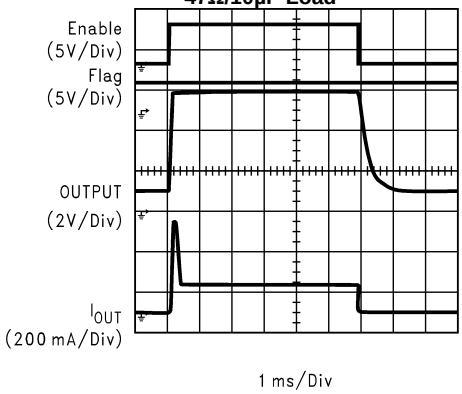


Figure 16.

Turn-ON/OFF Response with 47Ω/150µF Load

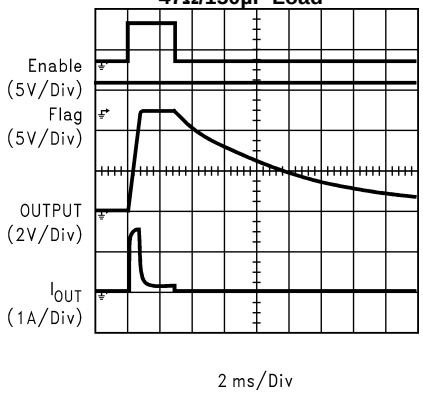
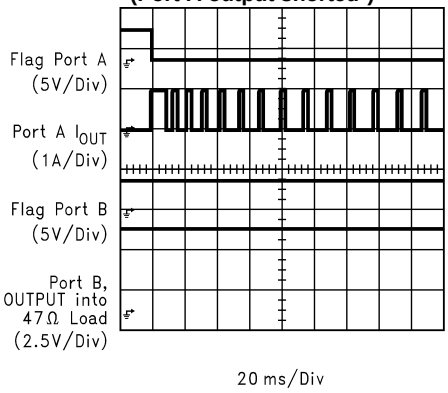


Figure 17.

Thermal Shutdown Response (Port A output shorted*)



* Port A is shorted to GND through a 100 mΩ resistor

Figure 18.

Thermal Shutdown Response (See Notes)

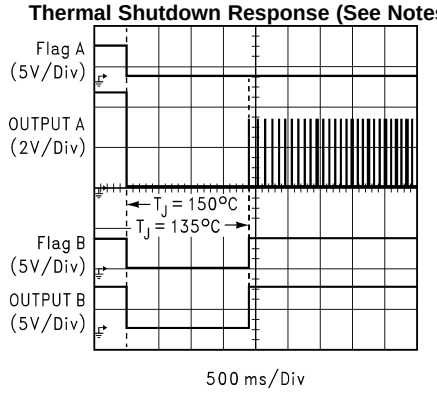


Figure 19.

Enable into a short

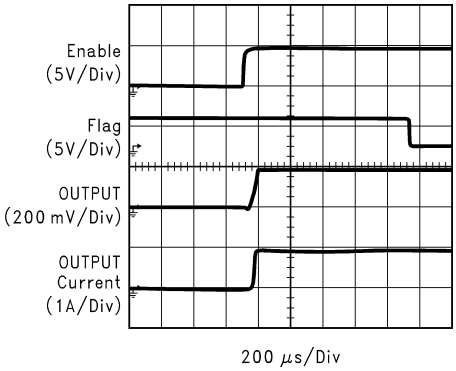


Figure 20.

FUNCTIONAL DESCRIPTION

The LM3526-H and LM3526-L are high side P-Channel switches with active-high and active-low enable inputs, respectively. Fault conditions turn-off and inhibit turn-on of the output transistor and activate the open-drain error flag transistor sinking current to the ground.

INPUT AND OUTPUT

IN (Input) is the power supply connection to the control circuitry and the source of the output MOSFET.

OUT (Output) is the connection to the drain of the output MOSFET. In a typical application circuit, current flows through the switch from IN to OUT towards the load.

If V_{OUT} is greater than V_{IN} when the switch is enabled, current will flow from OUT to IN since the MOSFET is bidirectional.

THERMAL SHUTDOWN

The LM3526 is internally protected against excessive power dissipation by a two-stage thermal protection circuit. If the device temperature rises to approximately 145°C, the thermal shutdown circuitry turns off any switch that is current limited. Non-overloaded switches continue to function normally. If the die temperature rises above 150°C, both switches are turned off and both fault flag outputs are activated. Hysteresis ensures that a switch turned off by thermal shutdown will not be turned on again until the die temperature is reduced to 135°C. Shorted switches will continue to cycle off and on, due to the rising and falling die temperature, until the short is removed.

UNDERVOLTAGE LOCKOUT

UVLO prevents the MOSFET switch from turning on until input voltage exceeds 1.8V (typical).

If input voltage drops below 1.8V (typical), UVLO shuts off the MOSFET switch and signals the fault flag. UVLO functions only when device is enabled.

CURRENT LIMIT

The current limit circuit is designed to protect the system supply, the MOSFET switches and the load from damage caused by excessive currents. The current limit threshold is set internally to allow a minimum of 500 mA through the MOSFET but limits the output current to approximately 1.0A typical.

FAULT FLAG

The fault flag is an open-drain output capable of sinking 10 mA load current to typically 100 mV above ground.

A parasitic diode exists between the flag pins and V_{IN} pin. Pulling the flag pins to voltages higher than V_{IN} will forward bias this diode and will cause an increase in supply current. This diode will also clamp the voltage on the flag pins to a diode drop above V_{IN}.

The fault flag is active (pulled low) when any of the following conditions are present: under-voltage, current limit, or thermal shutdown.

A 1ms (typ.) delay in reporting the fault condition prevents erroneous fault flags and eliminates the need for an external RC delay network.

Application Information

FILTERING

The USB specification indicates that “no less than 120 µF tantalum capacitors” must be used on the output of each downstream port. This bulk capacitance provides the short-term transient current needed during a hot plug-in. Current surges caused by the input capacitance of the down stream device could generate undesirable EMI signals. Ferrite beads in series with all power and ground lines are recommended to eliminate or significantly reduce EMI.

In selecting a ferrite bead, the DC resistance of the wire used must be kept to a minimum to reduce the voltage drop.

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A 0.01 µF ceramic capacitor is recommended on each port directly between the V_{bus} and ground pins to prevent EMI damage to other components during the hot-detachment.

Adequate capacitance must be connected to the input of the device to limit the input voltage drop during a hot-plug event to less than 330 mV. For a few tens of µs, the host must supply the in-rush current to the peripheral, charging its bulk capacitance to V_{bus}. This current is initially supplied by the input capacitor. A 33 µF 16V tantalum capacitor is recommended.

In choosing the capacitors, special attention must be paid to the Effective Series Resistance, ESR, of the capacitors to minimize the IR drop across the capacitor's ESR.

SOFT START

To eliminate the upstream voltage droop caused by the high in-rush current drawn by the output capacitors, the maximum in-rush current is internally limited to 1.5A.

TRANSIENT OVER-CURRENT DELAY

High transient current is also generated when the switch is enabled and large values of capacitance at the output have to be rapidly charged. The in-rush currents created could exceed the short circuit current limit threshold of the device forcing it into the current limit mode. The capacitor is charged with the maximum available short circuit current set by the LM3526. The duration of the in-rush current depends on the size of the output capacitance and load current. Since this is not a valid fault condition, the LM3526 delays the generation of the fault flag for 1 ms. If the condition persists due to other causes such as a short, a fault flag is generated after a 1 ms delay has elapsed.

The LM3526's 1 ms delay in issuing the fault flag is adequate for most applications. If longer delays are required, an RC filter as shown in Figure 21 may be used.

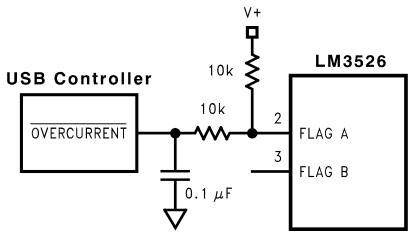


Figure 21.

PCB LAYOUT CONSIDERATIONS

In order to meet the USB requirements for voltage drop, droop and EMI, each component used in this circuit must be evaluated for its contribution to the circuit performance. The PCB layout rules and guidelines must be followed.

- Place the switch as close to the USB connector as possible. Keep all V_{bus} traces as short as possible and use at least 50-mil, 1 ounce copper for all V_{bus} traces. Solder plating the traces will reduce the trace resistance.
- Avoid vias as much as possible. If vias are used, use multiple vias in parallel and/or make them as large as possible.
- Place the output capacitor and ferrite beads as close to the USB connector as possible.
- If ferrite beads are used, use wires with minimum resistance and large solder pads to minimize connection resistance.

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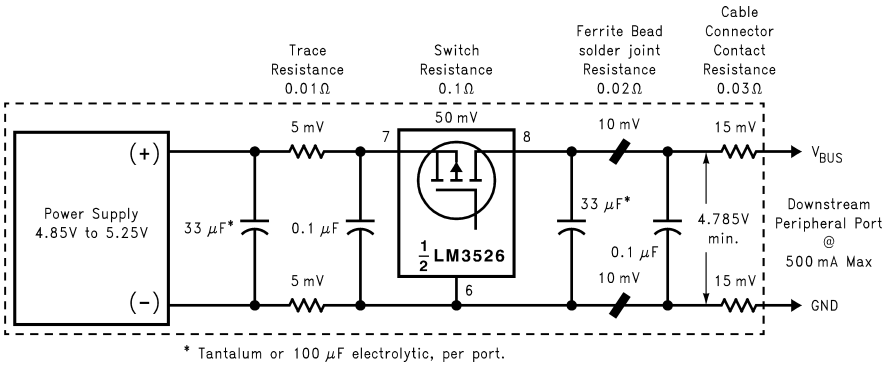


Figure 22. Self-Powered Hub Per-Port Voltage Drop

Typical Applications

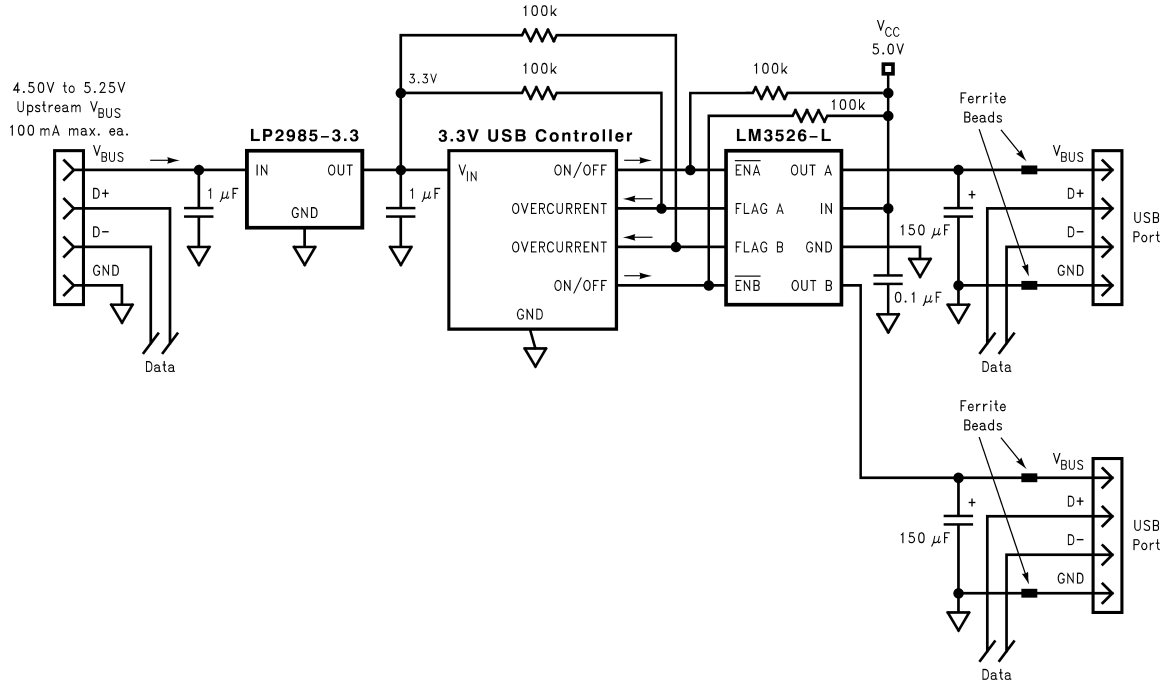


Figure 23. Dual-Port USB Self-Powered Hub

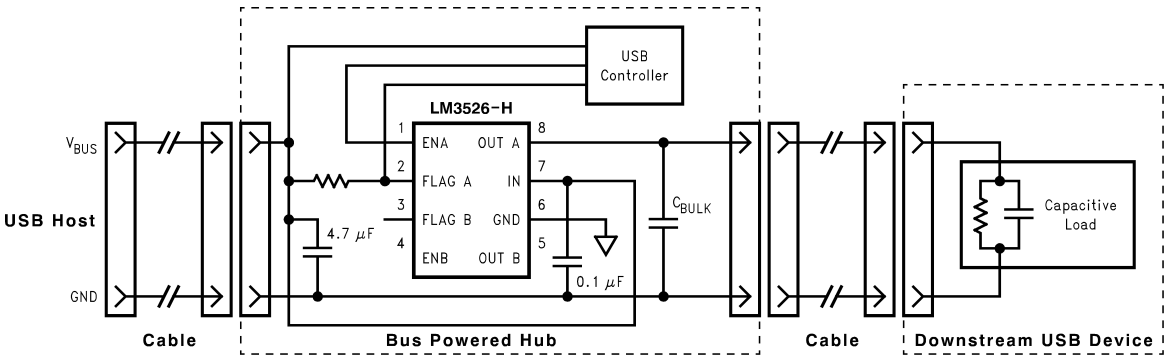


Figure 24. Soft-Start Application (Single port shown)

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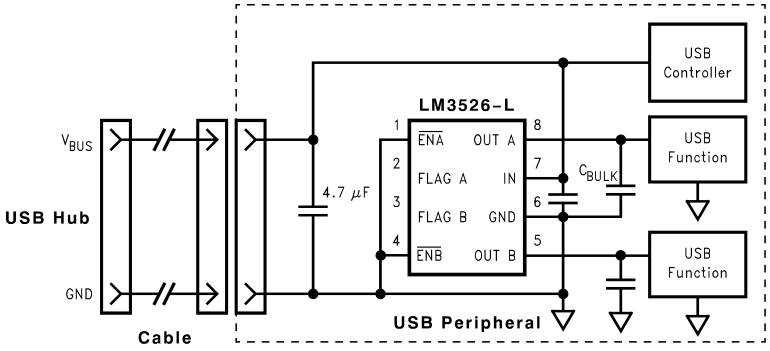


Figure 25. In-rush Current-limit Application

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	11

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3526M-H	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	3526 M-H
LM3526M-H/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3526 M-H
LM3526M-H/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3526 M-H
LM3526M-L/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3526 M-L
LM3526M-L/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3526 M-L
LM3526MX-H/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3526 M-H
LM3526MX-H/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3526 M-H
LM3526MX-L/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3526 M-L
LM3526MX-L/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3526 M-L

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

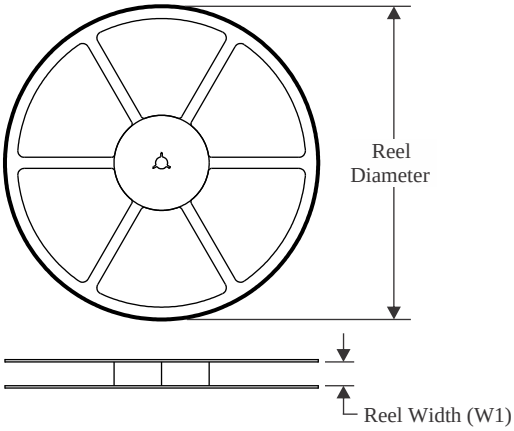
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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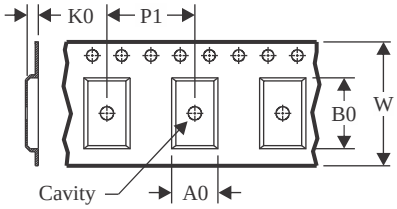
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

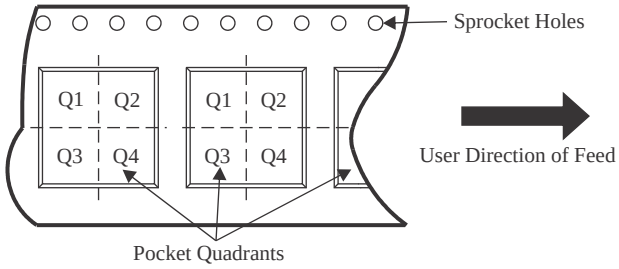


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

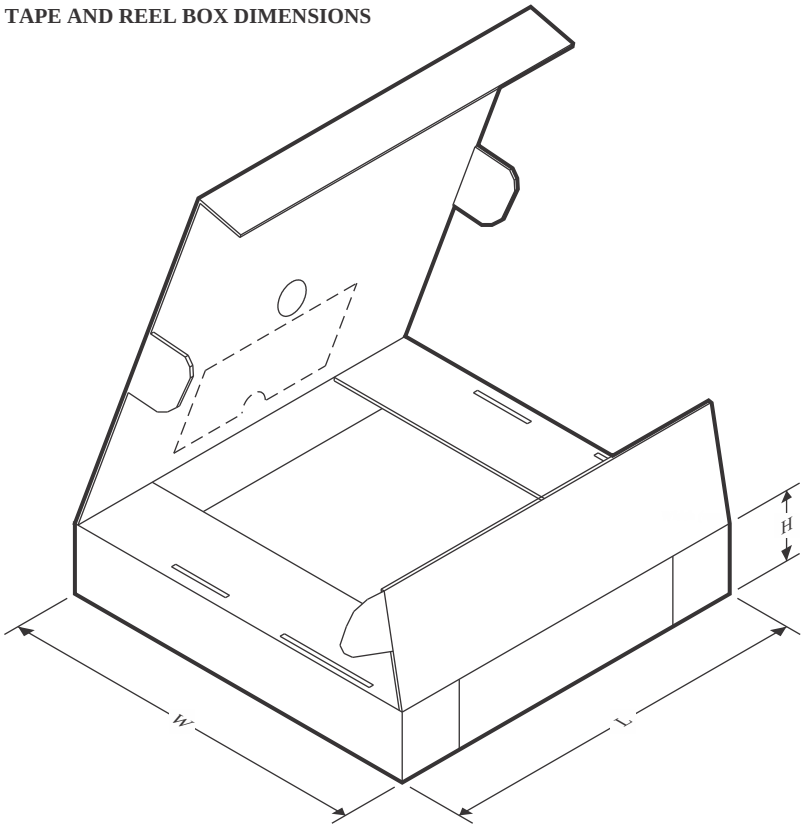
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3526MX-H/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM3526MX-L/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

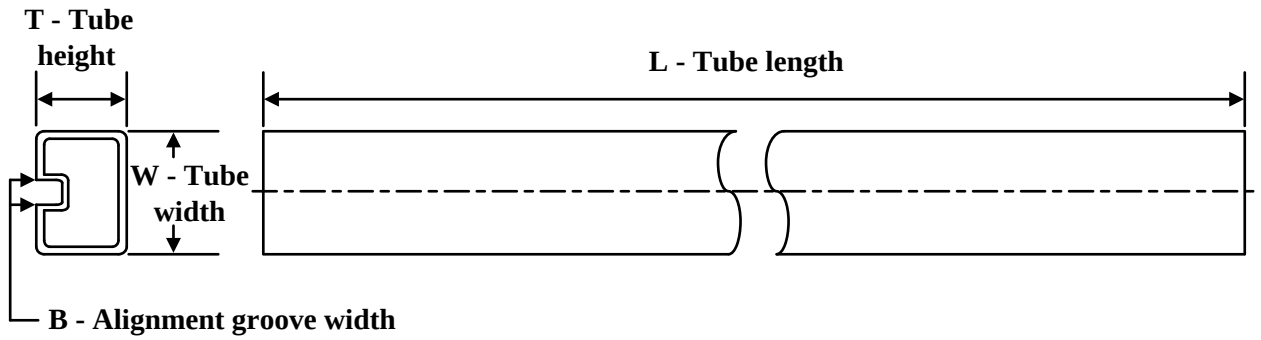
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

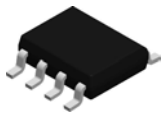
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3526MX-H/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM3526MX-L/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM3526M-H/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM3526M-H/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LM3526M-L/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM3526M-L/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

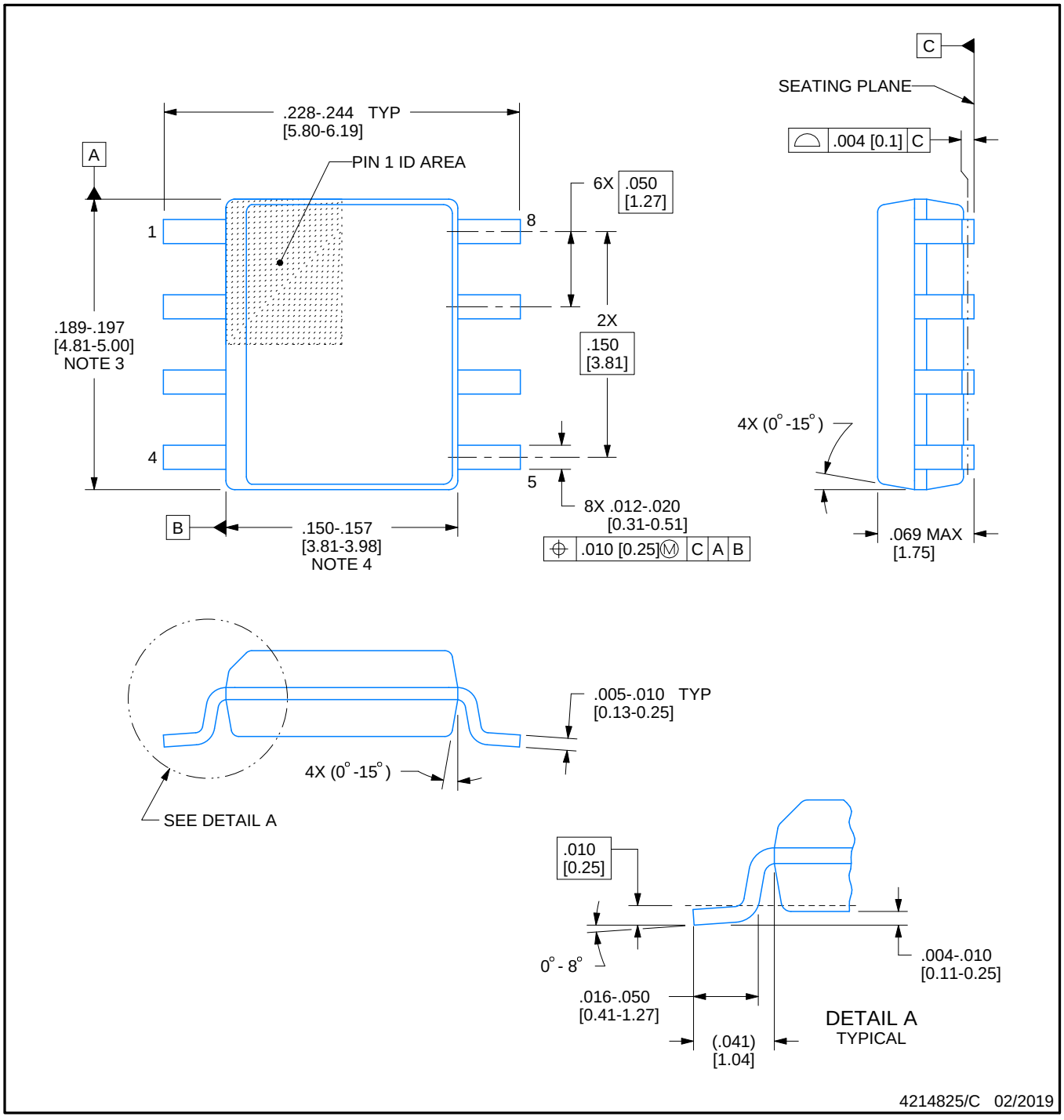


PACKAGE OUTLINE

D0008A

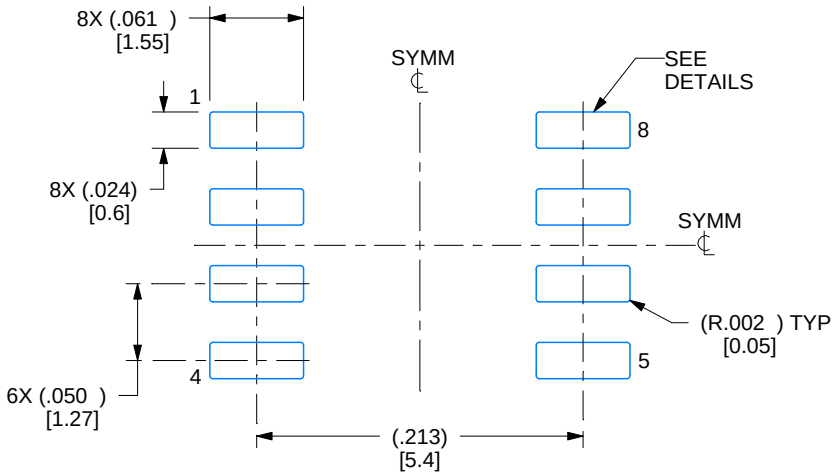
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

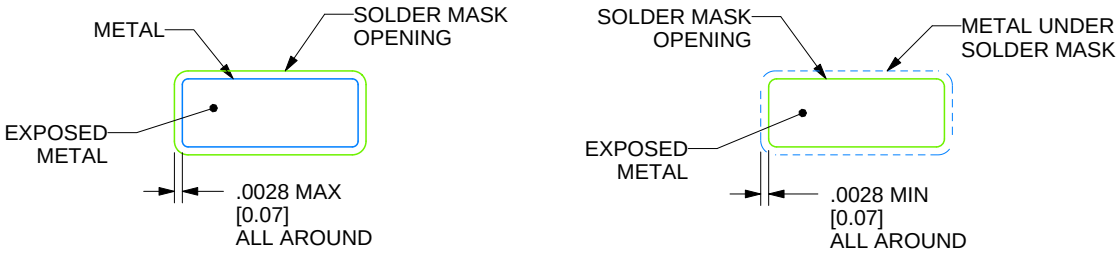


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

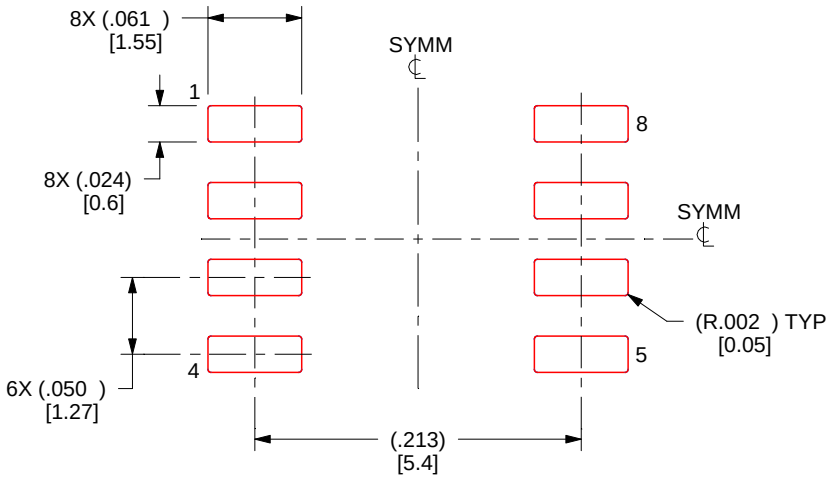
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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