LM317L 100mA Adjustable Floating Voltage Regulator

1 Features

- Output voltage range (V_O):
  - Adjustable 1.25V to 37V
- Output current: Up to 100mA
- No output capacitor required for stability
- Accuracy:
  - Input regulation typically 0.007% per input voltage change
  - Output regulation typically 0.5%
- Ripple rejection typically:
  - 71.5dB at 120Hz
- Package options:
  - SOIC
  - SOT-89
  - TO-92 (legacy chip only)
  - TSSOP (legacy chip only)
- For higher output current requirements, see LM317M (500mA) and LM317 (1.5A)

2 Applications

- Solar energy
- HVAC system
- Optical network terminal unit (ONT)
- AC inverter & VF drives
- Energy storage systems
- Analog input module

3 Description

The LM317L is an adjustable, 3-terminal, positive-voltage regulator capable of supplying up to 100mA over an output-voltage range of 1.25V to 37V. The device is exceptionally easy to use and requires only two external resistors to set the output voltage.

The LM317L uses floating topology and sees only the input-to-output differential voltage. Therefore, a supply of several hundred volts can be regulated, provided the maximum input-to-output differential is not exceeded.

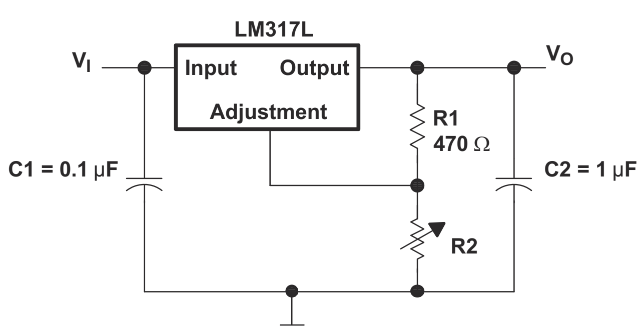
No capacitors are needed unless the LM317L is located far from the input filter capacitors, in which case an input bypass is needed. An optional output capacitor can be added to improve transient response.

The new chip is characterized for the junction temperature range of –40°C to +125°C for both the LM317LC and LM317LI series.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM317L	D (SOIC, 8)	4.9mm × 6mm
	LP (TO-92, 3)	4.8mm × 3.68mm
	PK (SOT-89, 3)	4.5mm × 4.095mm
	PW (TSSOP, 8)	3mm × 6.4mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

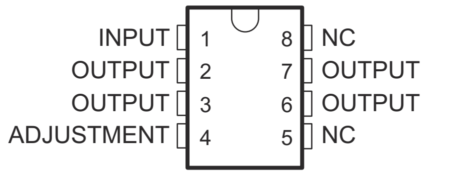


Simplified Schematic

Table of Contents

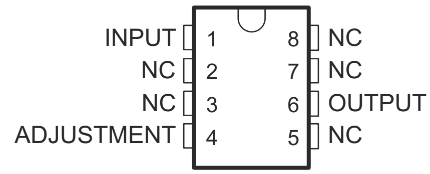
4 Pin Configuration and Functions

D PACKAGE (TOP VIEW)



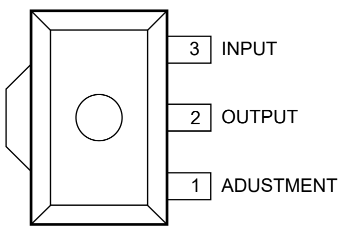
NC – No internal connection
OUTPUT terminals are all internally connected.

PW PACKAGE (TOP VIEW)



NC – No internal connection

PK PACKAGE (TOP VIEW)



LP PACKAGE (TOP VIEW)

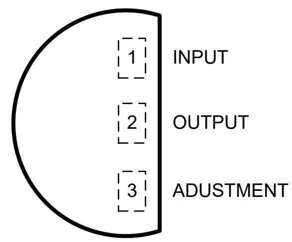


Table 4-1. Pin Functions

NAME	D	PW	LP	PK	TYPE(1)	DESCRIPTION
ADJUSTMENT	4	4	3	1	I	Output feedback voltage
INPUT	1	1	1	3	I	Input supply voltage
NC	5, 8	2, 3, 5, 7, 8	—	—	—	No connect. Recommended to ground pins for improved thermal performance but not required.
OUTPUT	2, 3, 6, 7	6	2	2	O	Regulated output voltage

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

			MIN	MAX	UNIT
V_I - V_O	Input-to-output differential voltage	Legacy chip (CSO:SHE)		35	V
		Legacy chip (CSO:TID)		40	
		New chip (CSO:RFB)		45	
T_J	Operating junction temperature			150	°C
T_{stg}	Storage temperature	Legacy chip (CSO:SHE)	–65	150	°C
		Legacy chip (CSO:TID)	–55	150	
		New chip (CSO:RFB)	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) CSO indicates the fabrication location of the chip.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	Legacy chip (CSO:SHE)	±3000	V
			Legacy chip (CSO:TID)	±2000	
			New chip (CSO:RFB)	±3000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	Legacy chip (CSO:SHE & CSO: TID)	±2000	
			New chip (CSO:RFB)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_o	Output voltage		Legacy chip (CSO:SHE)	1.25		32	V
			Legacy chip (CSO:TID)	1.25		37	
			New chip (CSO:RFB)	1.25		37	
V_I - V_o	Input-to-output differential voltage		Legacy chip (CSO:SHE)	2.5		32	V
			Legacy chip (CSO:TID)	2.5		37	
			New chip (CSO:RFB)	2.5		37	
I_O	Output current			2.5		100	mA
T_J	Operating junction temperature	LM317LC	Legacy chip (CSO:SHE)	0		125	°C
			Legacy chip (CSO:TID)	–40		125	
			New chip (CSO:RFB)	–40		125	
		LM317LI		–40		125	

5.4 Thermal Information (SOIC & SOT-89)

THERMAL METRIC[(1)] [(2)]		LM317L						UNIT
		SOIC (D, 8 PINS)			SOT-89 (PK, 3 PINS)			
		Legacy chip (CSO:SHE)	Legacy chip (CSO:TID)	New chip (CSO:RFB)	Legacy chip (CSO:SHE)	Legacy chip (CSO:TID)	New chip (CSO:RFB)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.1	96.5	98.18	51.5	44	43.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	–	48.6	48.44	–	86.9	124.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	–	34.8	31.90	–	8.5	4.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	–	5.9	6.38	–	4.5	5.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	–	34.2	31.59	–	8.5	4.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	–	6.9	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Limited thermal metrics are reported for legacy chip devices; additional metrics are included for the new chip (CSO:RFB).

5.5 Thermal Information (TO-92 & TSSOP)

THERMAL METRIC[(1)] [(2)]		TO-92 (LP)		TSSOP (PW)	UNIT
		3 PINS		8 PINS	
		Legacy chip (CSO: SHE)	Legacy chip (CSO: TID)	Legacy chip (CSO: SHE)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	139.5	156.7	149.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	–	80.6	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	–	–	–	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	–	24.7	–	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	–	135.8	–	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Limited thermal metrics are reported for legacy chip devices; additional metrics are included for the new chip (CSO:RFB) for SOIC and SOT-89 packages.

5.6 Electrical Characteristics

Over recommended operating virtual-junction temperature range. Unless otherwise noted, these specifications apply for the following test conditions: $V_I - V_O = 5V$ and $I_O = 40mA$. All characteristics are measured with a 0.1μF capacitor across the input and a 1μF capacitor across the output.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Line regulation	$V_I - V_O$ = 5V to 35V	T_J = 25°C	Legacy chip (CSO:SHE & CSO:TID)		0.01	0.02	%/V
		I_O = 2.5mA to 100mA			0.02	0.05	
		T_J = 25°C	New chip (CSO:RFB)		0.007	0.021	
		I_O = 2.5mA to 100mA			0.006	0.0275	

5.6 Electrical Characteristics (continued)

Over recommended operating virtual-junction temperature range. Unless otherwise noted, these specifications apply for the following test conditions: $V_I – V_O$ = 5V and I_O = 40mA. All characteristics are measured with a 0.1µF capacitor across the input and a 1µF capacitor across the output.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Ripple rejection	V_O = 10V, f = 120Hz				55		dB
Ripple rejection	V_O = 10V, 10µF capacitor between ADJUSTMENT and ground, f = 120Hz		Legacy chip (CSO:SHE & CSO:TID)	66	80		dB
Ripple rejection	V_O = 10V, 10µF capacitor between ADJUSTMENT and ground, f = 120Hz		New chip (CSO:RFB)	64	71.5		dB
Output voltage regulation	V_I - V_O = 5V to 35V, T_J = 25°C, I_O = 2.5mA to 100mA	V_O ≤ 5 V	Legacy chip (CSO:SHE & CSO:TID)		25		mV
Output voltage regulation	V_I - V_O = 5V to 35V, T_J = 25°C, I_O = 2.5mA to 100mA	V_O ≥ 5 V	Legacy chip (CSO:SHE & CSO:TID)		5		mV/V
Output voltage regulation	V_I - V_O= 5V to 35V, I_O = 2.5mA to 100mA	V_O ≤ 5 V	Legacy chip (CSO:SHE & CSO:TID)		50		mV
Output voltage regulation	V_I - V_O= 5V to 35V, I_O = 2.5mA to 100mA	V_O ≥ 5 V	Legacy chip (CSO:SHE & CSO:TID)		10		mV/V
Output voltage regulation	V_I - V_O = 5V to 35V, T_J = 25°C, I_O = 2.5mA to 100mA	V_O ≤ 5 V	New chip (CSO:RFB)		25		mV
Output voltage regulation	V_I - V_O = 5V to 35V, T_J = 25°C, I_O = 2.5mA to 100mA	V_O ≥ 5 V	New chip (CSO:RFB)		5		mV/V
Output voltage regulation	V_I - V_O = 5V to 35V, I_O = 2.5mA to 100mA	V_O ≤ 5 V	New chip (CSO:RFB)		25		mV
Output voltage regulation	V_I - V_O = 5V to 35V, I_O = 2.5mA to 100mA	V_O ≥ 5 V	New chip (CSO:RFB)		5		mV/V
Output voltage change with temperature	T_J = 0°C to 125°C		Legacy chip (CSO:SHE & CSO:TID)		10		mV/V
Output voltage change with temperature	T_J = –40°C to 125°C		New chip (CSO:RFB)		10		mV/V
Output voltage long-term drift	After 1000 hours at T_J = 125°C and $V_I – V_O$ = 35V				3	10	mV/V
Output noise voltage	f = 10Hz to 10kHz, T_J = 25°C				10		µV/V
Minimum output current to maintain regulation	$V_I – V_O$ = 35V		Legacy chip (CSO:SHE)		1.5	2.5	mA
Minimum output current to maintain regulation	$V_I – V_O$ = 35V		Legacy chip (CSO:TID)		3.5	5	mA
Minimum output current to maintain regulation	$V_I – V_O$ = 35V		New chip (CSO:RFB)		1.28	1.72	mA
Peak output current	$V_I – V_O$ ≤ 35V		Legacy chip (CSO:SHE)	100	200		mA
Peak output current	3V ≤ $V_I – V_O$ ≤ 13V		Legacy chip (CSO:TID)	100	200		mA
Peak output current	$V_I – V_O$ = 35V		Legacy chip (CSO:TID)	25	50	150	mA
Peak output current	$V_I – V_O$ ≤ 35V		New chip (CSO:RFB)	160	290		mA
ADJUSTMENT current			Legacy chip (CSO:SHE & CSO:TID)		50	100	µA
ADJUSTMENT current			New chip (CSO:RFB)		44	57	µA
Change in ADJUSTMENT current	$V_I – V_O$ = 2.5V to 35V, I_O = 2.5mA to 100mA		Legacy chip (CSO:SHE & CSO:TID)		0.2	5	µA
Change in ADJUSTMENT current	$V_I – V_O$ = 2.8V to 35V, I_O = 2.5mA to 100mA		New chip (CSO:RFB)		0.8	2.5	µA
Reference voltage (output to ADJUSTMENT)	$V_I – V_O$ = 5.0V to 35V, I_O = 2.5mA to 100mA, P ≤ rated dissipation		Legacy chip (CSO:SHE & CSO:TID)	1.2	1.25	1.3	V
Reference voltage (output to ADJUSTMENT)	$V_I – V_O$ = 5.0V to 35V, I_O = 2.5mA to 100mA, P ≤ rated dissipation		New chip (CSO:RFB)	1.22	1.256	1.292	V

5.7 Typical Characteristics

Unless otherwise noted, specifications over recommended operating virtual-junction temperature range, $V_I - V_O$ = 5V and I_O = 40mA, P ≤ rated dissipation.

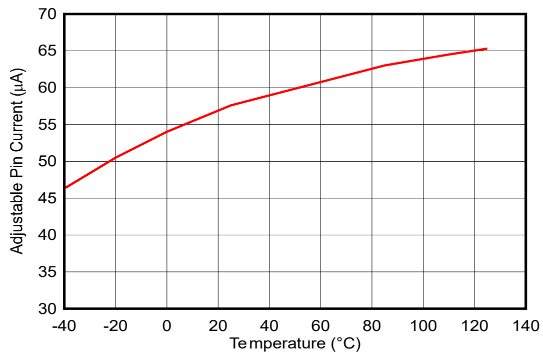


Figure 5-1. Change in Adjustment Current Over Temperature (Legacy Chip, CSO: SHE)

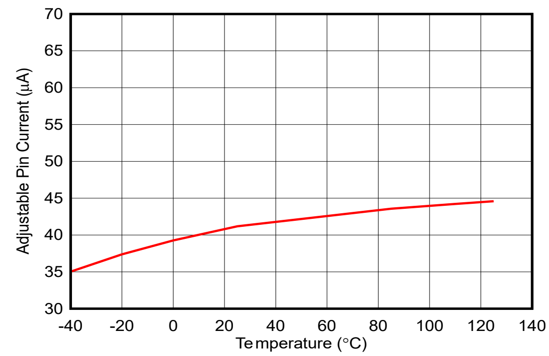


Figure 5-2. Change in Adjustment Current Over Temperature (Legacy Chip, CSO: TID)

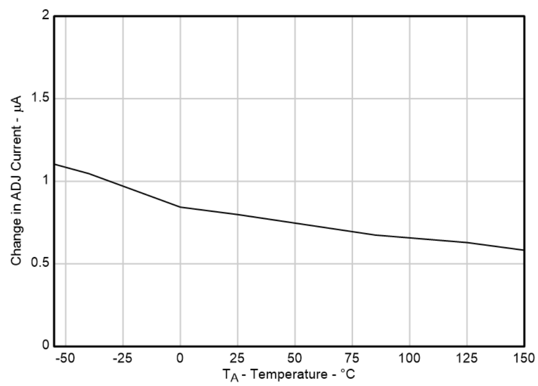
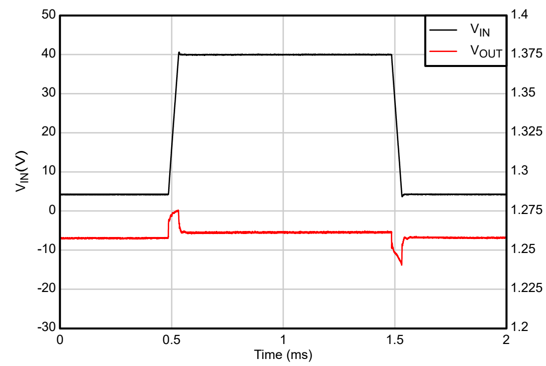
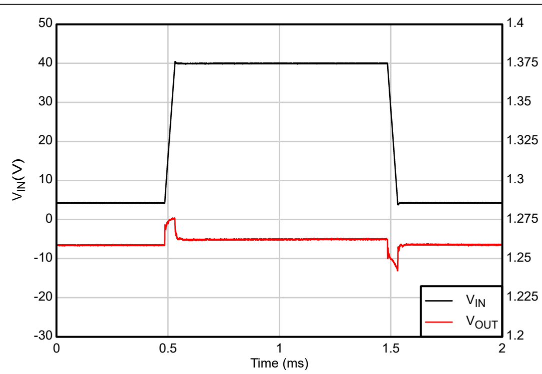


Figure 5-3. Change in Adjustment Current Over Temperature (New Chip, CSO: RFB)



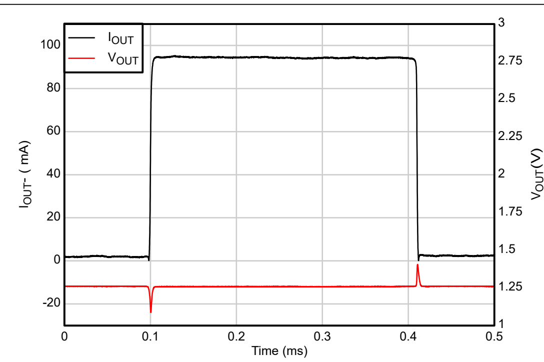
I_O = 2.5mA, C_{OUT} = 0µF, C_{IN} = 1µF

Figure 5-4. Line Transient (New Chip, CSO: RFB)



I_O = 100mA, C_{OUT} = 0µF, C_{IN} = 1µF

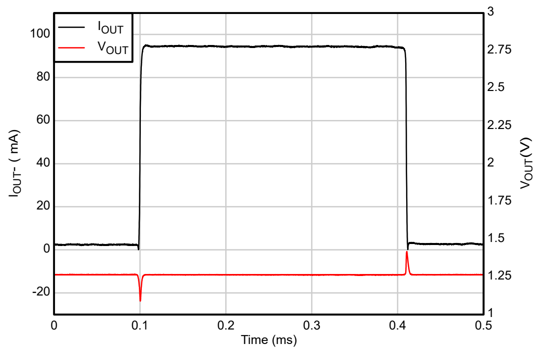
Figure 5-5. Line Transient (New Chip, CSO: RFB)



V_I - V_O = 3V, C_{OUT} = 0µF, C_{IN} = 1µF

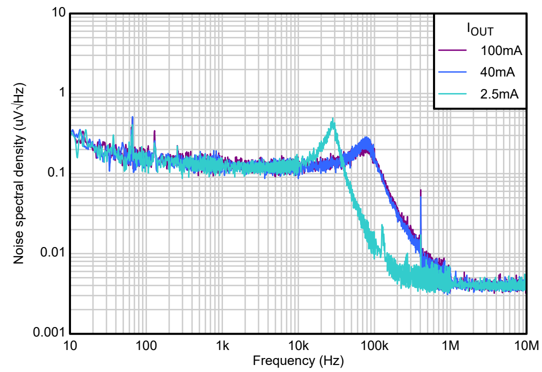
Figure 5-6. Load Transient (New Chip, CSO: RFB)

5.7 Typical Characteristics (continued)



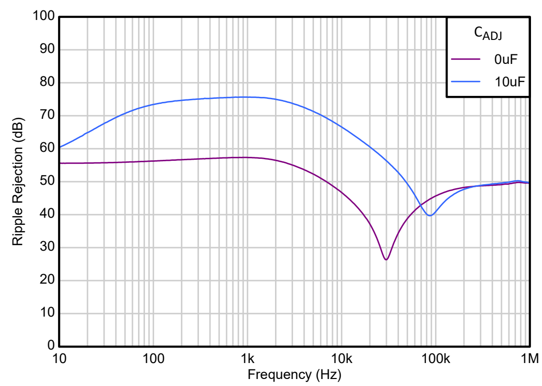
$V_I - V_O = 40V$, $C_{OUT} = 0\mu F$, $C_{IN} = 1\mu F$

Figure 5-7. Load Transient (New Chip, CSO: RFB)



$C_{OUT} = 1\mu F$, $C_{IN} = 0.1\mu F$

Figure 5-8. Output Noise (New Chip, CSO: RFB)



$C_{OUT} = 1\mu F$, $C_{IN} = 0.1\mu F$

Figure 5-9. Ripple Rejection (New Chip, CSO: RFB)

6 Detailed Description

6.1 Overview

The LM317L is a 100mA linear regulator with high voltage tolerance up to 37V (CSO: TID & CSO: RFB). The device has a feedback voltage that is relative to the output instead of ground. This ungrounded design allows the LM317L to have superior line and load regulation. This design also allows the device to be used as a current source or current sink using a single resistor. Any output voltage within the recommended output range can be obtained by using two resistors. The bias current of the device flows to the output; this current must be used by the load or the feedback resistors. Refer to the minimum output current to maintain regulation in the *Electrical Characteristics*.

The power dissipation is the product of pass transistor voltage and current, which is calculated as shown in Equation 1.

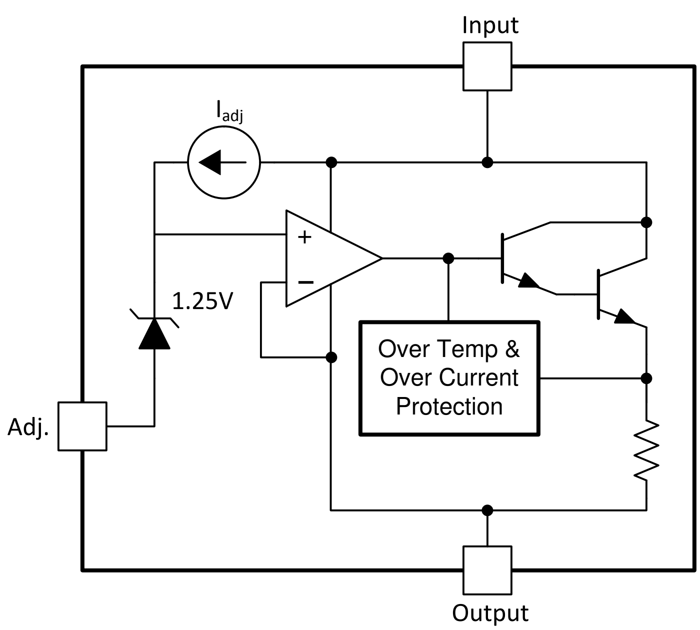
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

The application heat sink must be able to absorb the power calculated in Equation 1.

The LM317L regulator offers current-limiting and thermal-overload protection. All overload-protection circuitry remains fully functional even when ADJUSTMENT is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. ADJUSTMENT can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard three-terminal regulators.

In addition to replacing fixed regulators, the LM317L regulator is useful in a wide variety of other applications. Because the regulator is floating and observes only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. The primary application is that of a programmable output regulator, but by connecting a fixed resistor between ADJUSTMENT and OUTPUT, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping ADJUSTMENT to ground, programming the output to 1.25V, where most loads draw little current.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 NPN Darlington Output Drive

The NPN Darlington output topology provides naturally low output impedance and an output capacitor is optional. To support maximum current and lowest temperature, a 2.5V headroom is recommended (V_I – V_O), refer to the *Recommended Operating Conditions*.

6.3.2 Overload Block

Overcurrent and overtemperature shutdown protects the device against overload or damage from operating in excessive heat.

6.3.3 Programmable Feedback

An op amp with a 1.25V offset input at the ADJUST pin provides easy output voltage or current (not both) programming. For current regulation applications, use a single resistor whose resistance value is 1.25V / I_{OUT} and power rating is greater than $(1.25V)^2$ / R. For voltage regulation applications, two resistors set the output voltage. See the *Typical Application* section for a schematic and the resistor formula.

6.4 Device Functional Modes

6.4.1 Normal operation

The device OUTPUT pin sources current necessary to make the OUTPUT pin 1.25V greater than the ADJUST terminal to provide output regulation.

6.4.2 Operation With Low Input Voltage

The device requires up to a 2.5V headroom (V_I – V_O) to operate in regulation, refer to the *Recommended Operating Conditions*. With less headroom, the device can drop out. In dropout operation, the OUTPUT voltage is the INPUT voltage minus the dropout voltage.

6.4.3 Operation at Light Loads

The device passes the bias current to the OUTPUT pin. The load or feedback must consume this minimum current for regulation or the output can be too high. Refer to the minimum output current to maintain regulation in the *Electrical Characteristics*.

6.4.4 Operation In Self Protection

When an overload occurs, the device shuts down the Darlington NPN output stage or reduces the output current to prevent device damage. The device automatically restarts when the over current is removed. Until the overload condition is removed, the output of the LM317L can be reduced or the device can cycle in and out of thermal shutdown, which can impact the long-term reliability of the device.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The two output resistors are the only components required to adjust V_{OUT}.

7.2 Typical Application

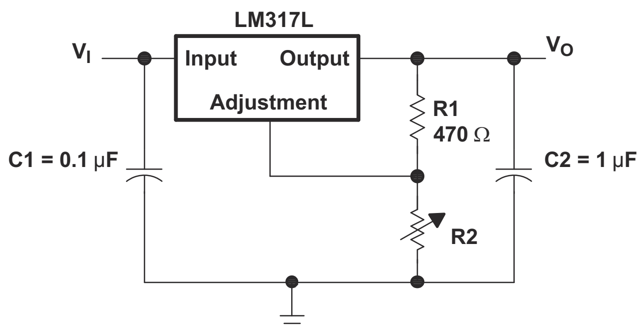


Figure 7-1. Typical Application Schematic

7.2.1 Design Requirements

1. Use an input bypass capacitor if the regulator is far from the filter capacitors.
2. For this design example, use the parameters listed in Table 7-1.
3. Using an output capacitor improves transient response, but is optional.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	(Output voltage + 2.5V) to 37V
Output voltage	$V_{REF} \times (1 + R_2 / R_1) + I_{ADJ} \times R_2$

7.2.2 Detailed Design Procedure

7.2.2.1 Input Capacitor

An input capacitor is not required, but is recommended, particularly if the regulator is not in close proximity to the power-supply filter capacitors. A 0.1μF ceramic or 1μF tantalum provides sufficient bypassing for most applications, especially when adjustment and output capacitors are used.

7.2.2.2 Output Capacitor

An output capacitor improves transient response, but is not needed for stability.

7.2.2.3 Feedback Resistors

The feedback resistor sets the output voltage using Equation 2.

$$V_{REF} \times (1 + R_2 / R_1) + I_{ADJ} \times R_2 \quad (2)$$

7.2.2.4 Adjustment Terminal Capacitor

The optional adjustment pin capacitor (C_{ADJ}) improves ripple rejection by preventing the amplification of the ripple. When this capacitor is used and V_{OUT} > 6V, a protection diode from adjust to output is recommended.

7.2.2.5 Design Options and Parameters

Common linear regulator designs are concerned with the following parameters:

- Input voltage range
- Input capacitor range
- Output voltage
- Output current rating
- Output capacitor range
- Input short protection
- Stability
- Ripple rejection

7.2.2.6 Output Voltage

V_O is calculated as shown in Equation 3.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right) + (I_{ADJ} \times R_2) \tag{3}$$

Because I_{ADJ} typically is 44µA, this parameter is negligible in most applications.

7.2.2.7 Input Short Protection

If the input is shorted to ground during a fault condition, protection diodes provide measures to prevent the possibility of external capacitors discharging through low-impedance paths in the device. By providing low-impedance discharge paths for C_3 and C_2, respectively, a protection diode across the input to the output and a protection diode across ADJ to the output prevent the capacitors from discharging into the output of the regulator.

7.2.2.8 Ripple Rejection

C_{ADJ} is used to improve ripple rejection. This capacitor prevents amplification of the ripple when the output voltage is adjusted higher. If C_{ADJ} is used, include protection diodes to prevent ADJ from reverse-biasing when VOUT collapses quickly. Refer to the *Adjustment Terminal Capacitor* section for more details.

7.2.3 Application Curve

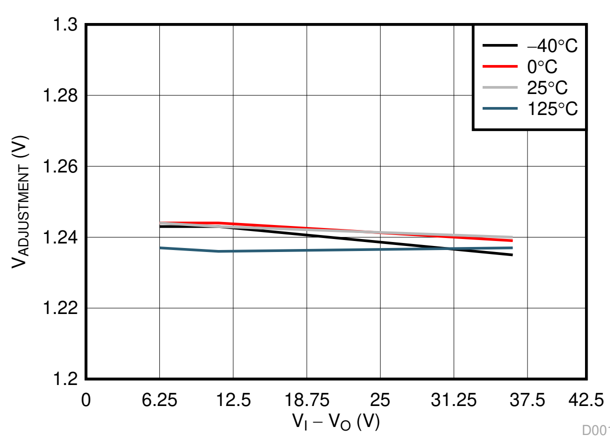


Figure 7-2. Adjustment Voltage Relative to Output Over Temperature (Legacy Chip, CSO:SHE)

7.3 System Examples

7.3.1 Regulator Circuit With Improved Ripple Rejection

C2 helps stabilize the voltage at the adjustment pin, which helps reject noise. Diode D1 exists to discharge C2 in case the output is shorted to ground.

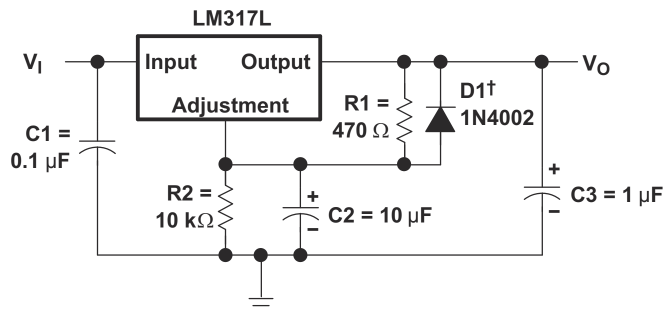


Figure 7-3. Regulator Circuit With Improved Ripple Rejection

7.3.2 0V to 30V Regulator Circuit

In the 0V to 30V regulator circuit application, the output voltage is determined by Equation 4.

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2 + R_3}{R_1}\right) - 10\,V \quad (4)$$

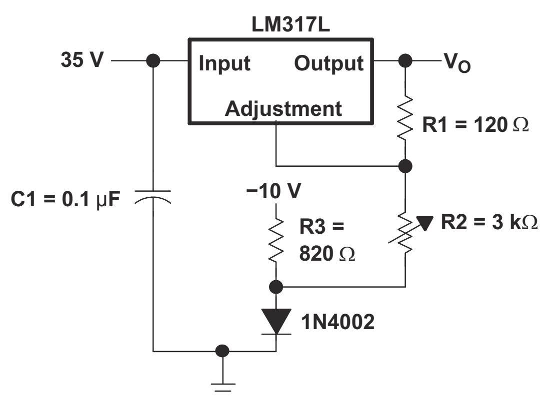


Figure 7-4. 0V to 30V Regulator Circuit

Note

This application circuit tested with legacy chips only (CSO: SHE & CSO: TID); TI's customers are responsible for validating and testing their design implementation to confirm system functionality.

7.3.3 Precision Current-Limiter Circuit

This application limits the output current to the I_{LIMIT} shown in Figure 7-5.

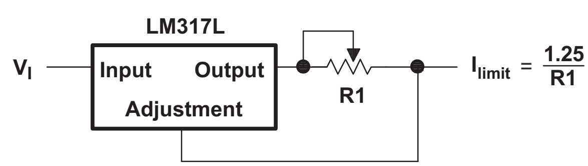


Figure 7-5. Precision Current-Limiter Circuit

7.3.4 Tracking Preregulator Circuit

The tracking preregulator circuit application keeps a constant voltage across the second LM317L in the circuit.

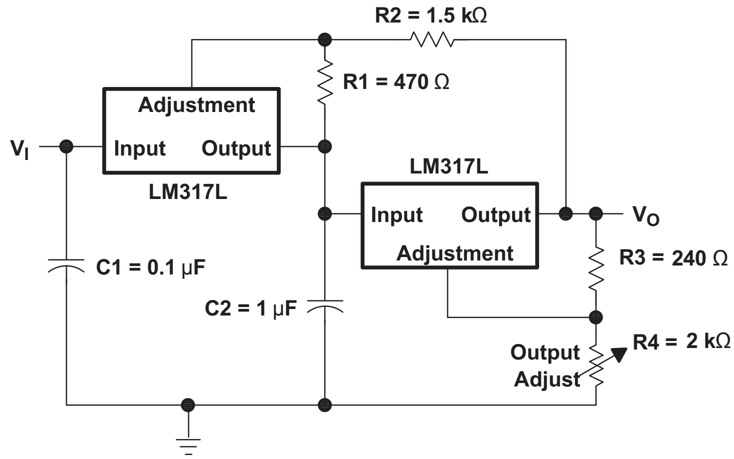


Figure 7-6. Tracking Preregulator Circuit

7.3.5 Slow-Turn On 15V Regulator Circuit

The capacitor C1, in combination with the PNP transistor, helps the circuit to slowly start supplying voltage. In the beginning, the capacitor is not charged. Therefore, output voltage starts at 1.9V, as determined by Equation 5. As the capacitor voltage rises, V_{OUT} rises at the same rate. When the output voltage reaches the value determined by R1 and R2, the PNP is turned off.

$$V_{C1} + V_{BE} + 1.25V = 0V + 0.65V + 1.25V = 1.9V \tag{5}$$

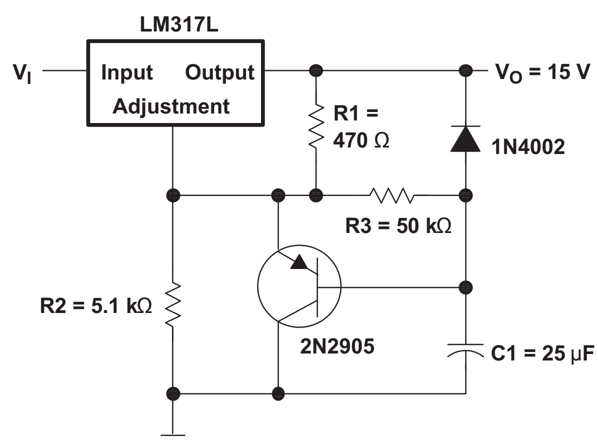


Figure 7-7. Slow-Turn On of the 15V Regulator Circuit

Note

This application circuit tested with legacy chips only (CSO: SHE & CSO: TID); TI's customers are responsible for validating and testing their design implementation to confirm system functionality.

7.3.6 50mA Constant-Current, Battery-Charger Circuit

The current-limit operation mode can be used to trickle charge a battery at a fixed current as determined by Equation 6. V_I must be greater than V_{BAT} + 3.75V.

$$I_{CHG} = 1.25V \div 24\Omega \quad (6)$$

$$(1.25V\ [V_{REF}] + 2.5V\ [\text{headroom}]) \quad (7)$$

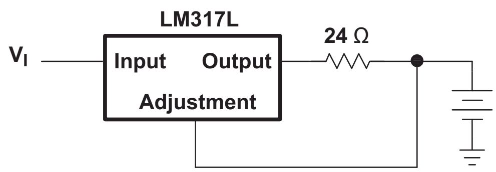


Figure 7-8. 50mA Constant-Current, Battery-Charger Circuit

7.3.7 Current-Limited 6V Charger

As the charge current increases, the voltage at the bottom resistor increases until the NPN starts sinking current from the adjustment pin. The voltage at the adjustment pin drops, and consequently the output voltage decreases until the NPN stops conducting.

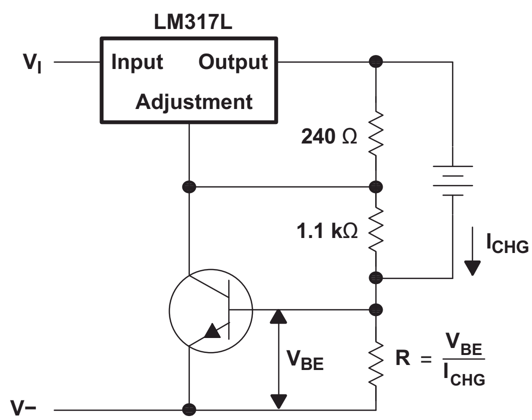


Figure 7-9. Current-Limited 6V Charger

Note

This application circuit tested with legacy chips only (CSO: SHE & CSO: TID); TI's customers are responsible for validating and testing their design implementation to confirm system functionality.

7.3.8 High-Current Adjustable Regulator

This application allows higher currents at V_{OUT} than the LM317L can provide, while still keeping the output voltage at levels determined by the adjustment-pin resistor divider of the LM317L.

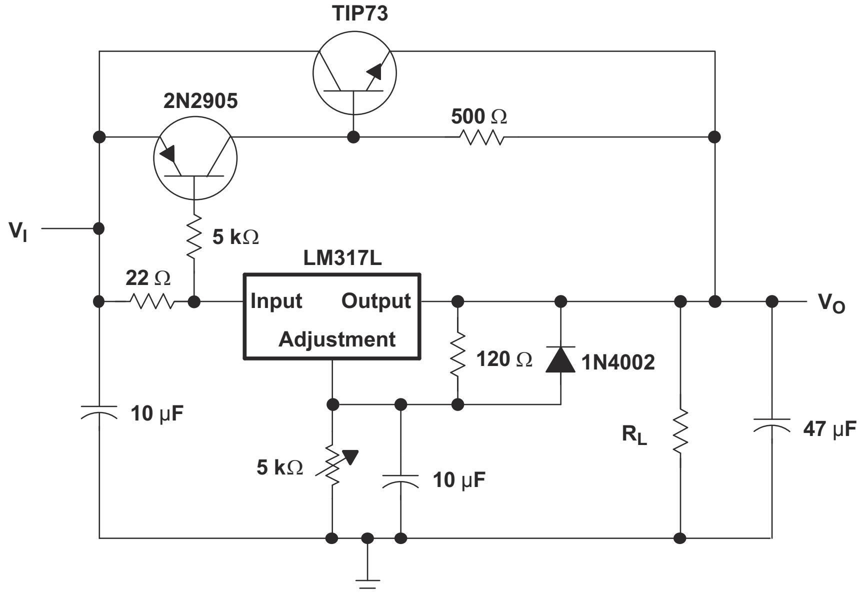


Figure 7-10. High-Current Adjustable Regulator

Note

This application circuit tested with legacy chips only (CSO: SHE & CSO: TID); TI's customers are responsible for validating and testing their design implementation to confirm system functionality.

7.4 Power Supply Recommendations

The LM317L is designed to operate from an input voltage supply range between 2.5V to 37V greater than the output voltage (CSO: TID & CSO: RFB; see the *Recommended Operating Conditions*). If the device is more than six inches from the input filter capacitors, an input bypass capacitor of 0.1µF or greater, of any type, is needed for stability.

7.5 Layout

7.5.1 Layout Guidelines

- Bypass the input pin to ground with a bypass capacitor.
  - This is required only if the regulator is located more than 6 inches from input filter capacitors. However, good analog design practice is to connect a bypass capacitor from IN to GND (C_{IN}); C_{IN} counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR.
  - Place C_{IN} as close to the V_{IN} of the device and the GND of the system as possible. Care must be taken to minimize the loop area formed by the bypass capacitor connection, the INPUT pin, and the GND pin of the system.
- Connect an output capacitor from the output pin to ground.
  - The output capacitor (C_{OUT}) is not required for stability. However, adding C_{OUT} improves transient response.
  - Place C_{OUT} as close to the V_{OUT} of the device and the GND of the system as possible. Care must be taken to minimize the loop area formed by the bypass capacitor connection, the OUTPUT pin, and the GND pin of the system.
- For operation at a full-rated load, use wide trace lengths to minimize IR drop and heat dissipation.

7.5.2 Layout Example

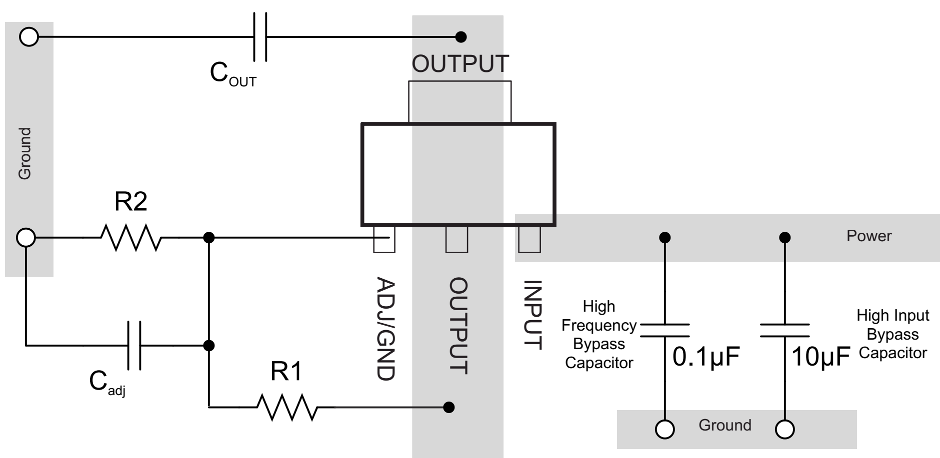


Figure 7-11. Layout Diagram, SOT-89

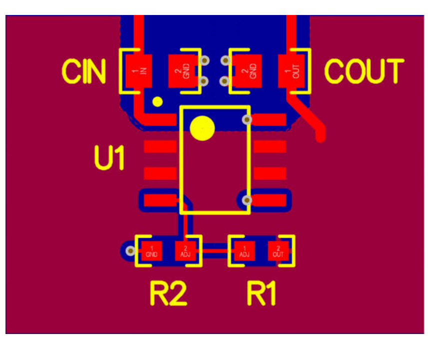


Figure 7-12. Layout Diagram, SOIC with NC Pins Grounded

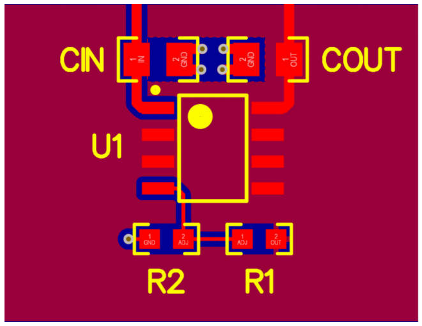


Figure 7-13. Layout Diagram, SOIC with NC Pins Connected to OUTPUT

7.6 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \Psi_{JT} \times P_D \tag{8}$$

$$T_J = T_T + \psi_{JT} \times P_D \tag{9}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \Psi_{JB} \times P_D \tag{10}$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Device Nomenclature

PRODUCT [(1)]	VERSION	V_{OUT}
LM317L**x y(y) (z) (G4)**	Legacy chip **CSO: SHE**	**x** is the operating temperature range designator (C = 0°C to 125°C, I = -40°C to 125°C). **y(y)** is the package designator (D = SOIC, PK = SOT-89, PW = TSSOP, LP= TO-92). **(z)** is the package quantity designator (R = large reel, no designator = tube packing for SOIC and TSSOP, bulk packing for TO-92, large reel for SOT-89). **(G4)** if present, indicates NiPdAu lead finish.
	Legacy chip **CSO: TID**	**x** is the operating temperature range designator (C and I = -40°C to 125°C). **y(y)** is the package designator (D = SOIC, PK = SOT-89). **(z)** is the package quantity designator (R = large reel, no designator = tube packing for SOIC, large reel for SOT-89). **(G4)** if present, indicates NiPdAu lead finish.
	New chip **CSO: RFB**	**x** is the operating temperature range designator (C and I = -40°C to 125°C). **y(y)** is the package designator (D = SOIC, PK = SOT-89). **(z)** is the package quantity designator (R = large reel, no designator = tube packing for SOIC, large reel for SOT-89). **(G4)** if present, indicates NiPdAu lead finish.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

Note

Devices ship with either the legacy chip (CSO: SHE or CSO: TID) or the new chip (CSO: RFB). CSO, or chip source origin, indicates the fabrication site at which the chip was manufactured. CSO can be found on the packaging label of material received. Device performance for new and legacy chips is denoted throughout the data sheet.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (December 2024) to Revision G (August 2026) **Page**

- Updated legacy and new chip information throughout the document.....1
- Removed output voltage range of the legacy chip from the *Features* section.....1
- Changed the input regulation per input voltage change from 0.01% to 0.007% in the *Features* section to reflect new chip (CSO: RFB) specs.....1
- Changed the typical ripple rejection at 120Hz spec from 80dB to 71.5dB in the *Features* section to reflect new chip (CSO: RFB) specs.....1
- Removed ripple rejection at 100kHz spec from the *Features* section.....1
- Added device package options to the *Features* section.....1
- Updated *Applications* section.....1
- Updated the *Description* section to reflect new chip (CSO: RFB) specs.....1
- Changed output voltage maximum from 32V to 37V in the *Description* section to reflect new chip (CSO: RFB) specs.....1
- Added new chip (CSO: RFB) specs to the Absolute Maximum Ratings.....4
- Added new chip (CSO: RFB) specs to the ESD Ratings.....4
- Added new chip (CSO: RFB) specs to the Recommended Operating Conditions.....4
- Added new chip (CSO: RFB) specs to the Thermal Information.....5
- Updated Thermal Information to two tables for clarity.....5
- Added new chip (CSO: RFB) specs to the Electrical Characteristics.....5
- Updated titles of *Typical Characteristics* graphs for legacy chip (CSO: SHE & CSO: TID).....7
- Added *Typical Characteristics* graphs for new chip (CSO: RFB).....7
- Updated *Overview* section to reflect new chip (CSO: RFB) specs.....9
- Removed mention of specific output voltage range and bias current in the *Overview* section, instead added a reference the *Electrical Characteristics* table, where the specs can be found.....9
- Updated *NPN Darlington Output Drive* with link to the *Recommended Operating Conditions* 10
- Updated *Operation With Low Input Voltage* with a link to the *Recommended Operating Conditions* 10
- Updated *Operation at Light Loads* with a link to the *Electrical Characteristics* 10
- Updated *Operation in Self Protection* for clarity.....10
- Updated the maximum input range example value from 32V to 37V in the *Design Requirements* to reflect new chip (CSO: RFB) specs.....11
- Updated *Adjustment Terminal Capacitor* section to mention C_{ADJ} 12
- Updated adjustment current from 50µA to 44µA in the *Output Voltage* section to reflect new chip (CSO: RFB) specs.....12
- Changed position of *Input Short Protection* to before *Ripple Rejection* within the *Detailed Design Procedure* 12
- Updated *Ripple Rejection* with a link to the *Adjustment Terminal Capacitor* section.....12
- Updated *Application Curve* to specify legacy chip performance.....12
- Added note to *0V to 30V Regulator Circuit* 13
- Added note to *Slow-Turn On 15V Regulator Circuit* 14
- Added note to *Current-Limited 6V Charger* 15
- Added note to *High-Current Adjustable Regulator* 16
- Updated the maximum input voltage from 32V to 37V in the *Power Supply Recommendations* section to reflect new chip (CSO: RFB) specs.....17
- Added a link to the *Recommended Operating Conditions* table in the *Power Supply Recommendations* section.....17
- Updated *Layout Guidelines* to give more detailed guidance about capacitor placement.....17
- Added SOIC layouts to the *Layout Example* section.....17
- Updated the *Device Nomenclature* for clarity, included distinction based on CSO.....19

Changes from Revision E (October 2014) to Revision F (December 2024) **Page**

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM317LCD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCLP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	L317LC
LM317LCLP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	0 to 125	L317LC
LM317LCLPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	L317LC
LM317LCLPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	L317LC
LM317LCLPRE3	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	0 to 125	L317LC
LM317LCPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	LA
LM317LCPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	LA
LM317LCPK.B	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	LA
LM317LCPKG3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 125	LA
LM317LCPW	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCPW.A	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCPWE4	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LCPWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 125	L317LC
LM317LID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI
LM317LID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI
LM317LIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L317LI
LM317LIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI
LM317LIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI
LM317LIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI
LM317LIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM317LIDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI
LM317LILP	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	L317LI
LM317LILP.A	Active	Production	TO-92 (LP) | 3	1000 | BULK	Yes	SN	N/A for Pkg Type	-40 to 125	L317LI
LM317LILPR	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	L317LI
LM317LILPR.A	Active	Production	TO-92 (LP) | 3	2000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-40 to 125	L317LI
LM317LIPK	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LB
LM317LIPK.A	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LB
LM317LIPK.B	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LB
LM317LIPKG3	Active	Production	SOT-89 (PK) | 3	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	LB
LM317LIPW	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI
LM317LIPW.A	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI
LM317LIPWR	NRND	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI
LM317LIPWR.A	NRND	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L317LI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

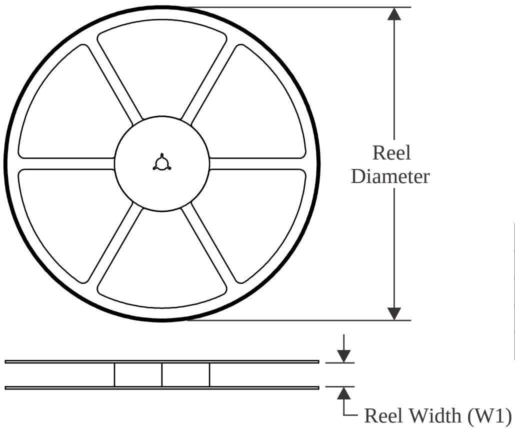
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

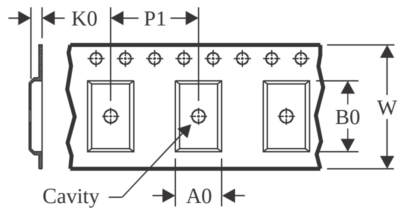
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

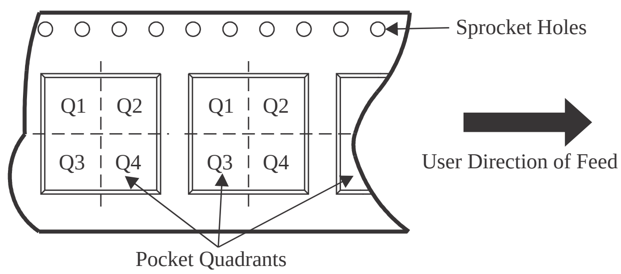


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

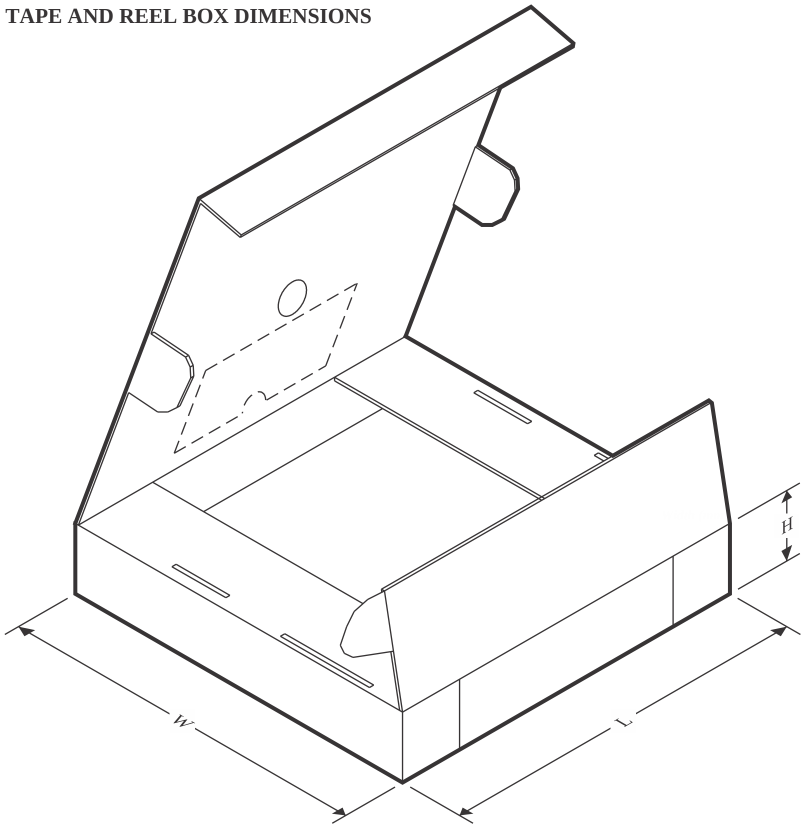
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM317LCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LCDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LCPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
LM317LCPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM317LIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM317LIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
LM317LIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

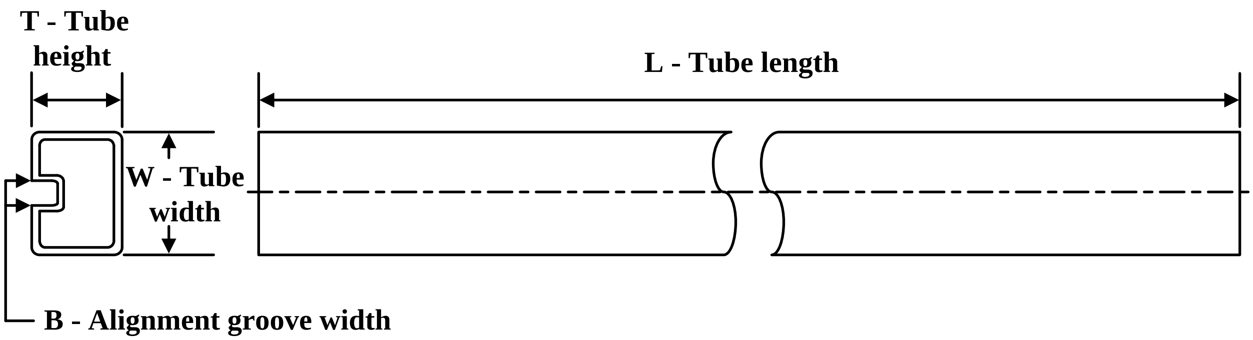
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM317LCDR	SOIC	D	8	2500	340.5	338.1	20.6
LM317LCDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM317LCPK	SOT-89	PK	3	1000	340.0	340.0	38.0
LM317LCPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
LM317LIDR	SOIC	D	8	2500	353.0	353.0	32.0
LM317LIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
LM317LIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
LM317LIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0

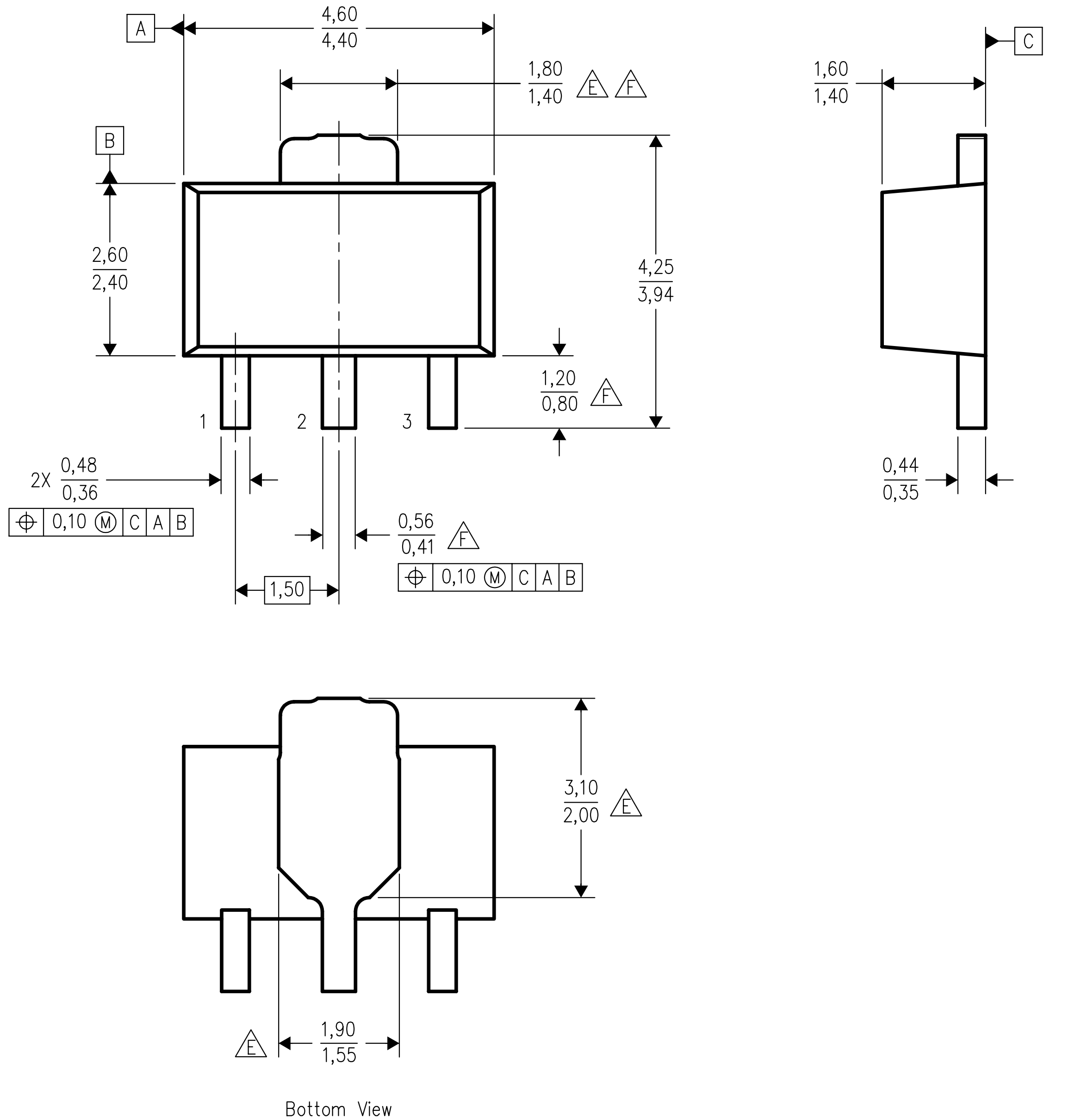
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM317LCD	D	SOIC	8	75	507	8	3940	4.32
LM317LCD.A	D	SOIC	8	75	507	8	3940	4.32
LM317LCPW	PW	TSSOP	8	150	530	10.2	3600	3.5
LM317LCPW.A	PW	TSSOP	8	150	530	10.2	3600	3.5
LM317LCPWE4	PW	TSSOP	8	150	530	10.2	3600	3.5
LM317LID	D	SOIC	8	75	507	8	3940	4.32
LM317LID.A	D	SOIC	8	75	507	8	3940	4.32
LM317LIPW	PW	TSSOP	8	150	530	10.2	3600	3.5
LM317LIPW.A	PW	TSSOP	8	150	530	10.2	3600	3.5

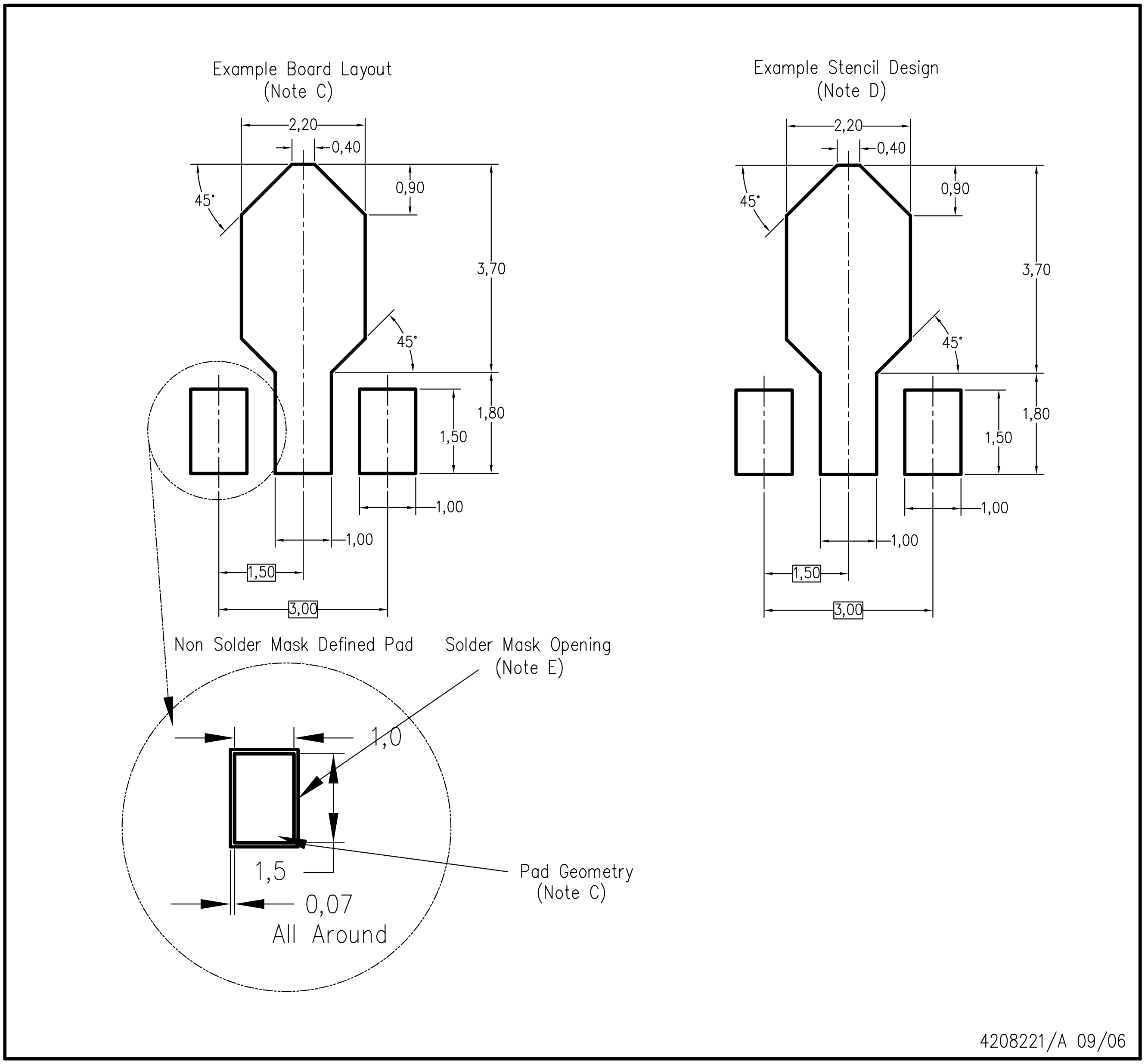
PK (R-PSSO-F3) PLASTIC SINGLE-IN-LINE PACKAGE



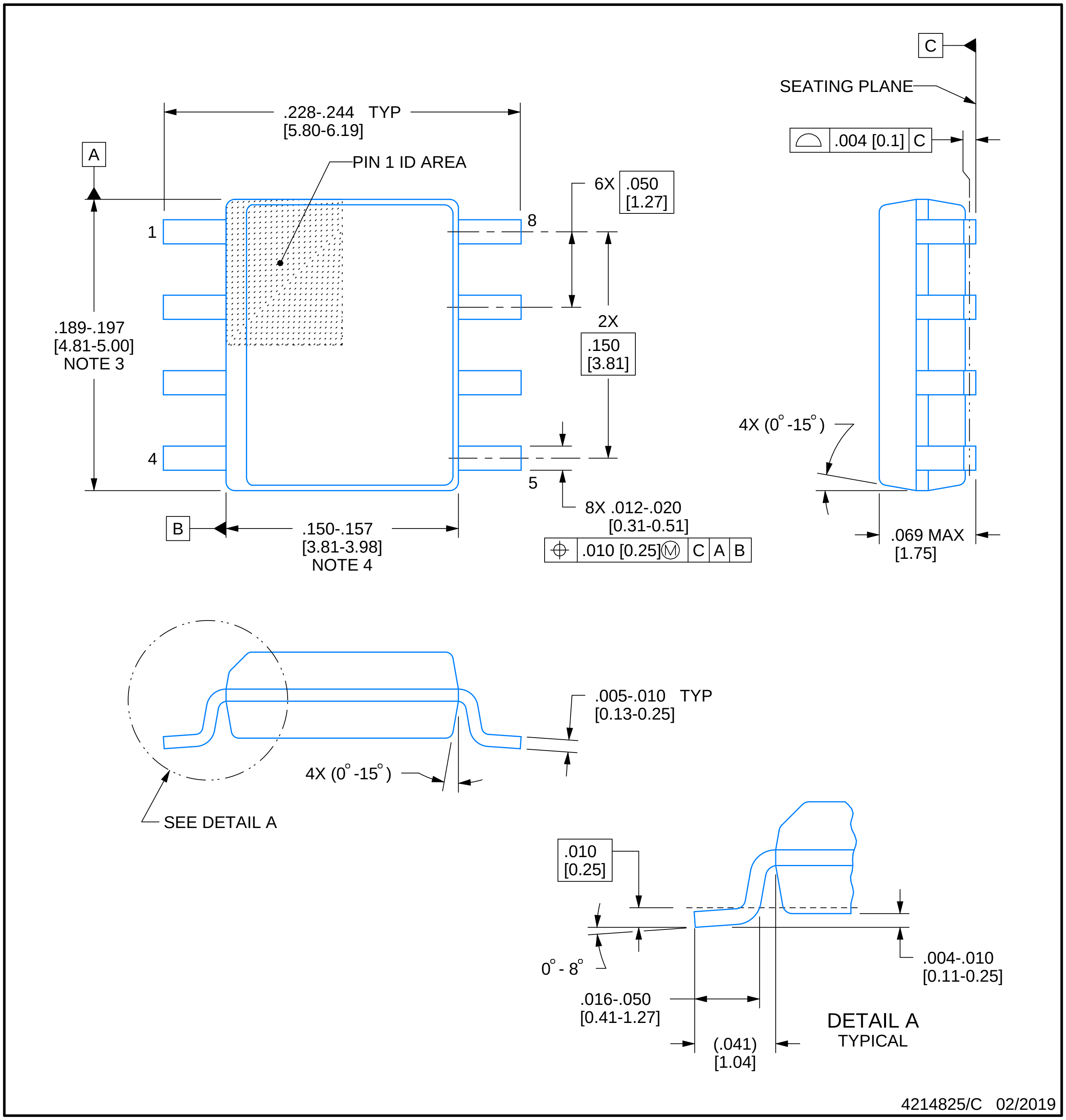
4040234/D 02/2006

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO-243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

PK (R–PDSO–G3)

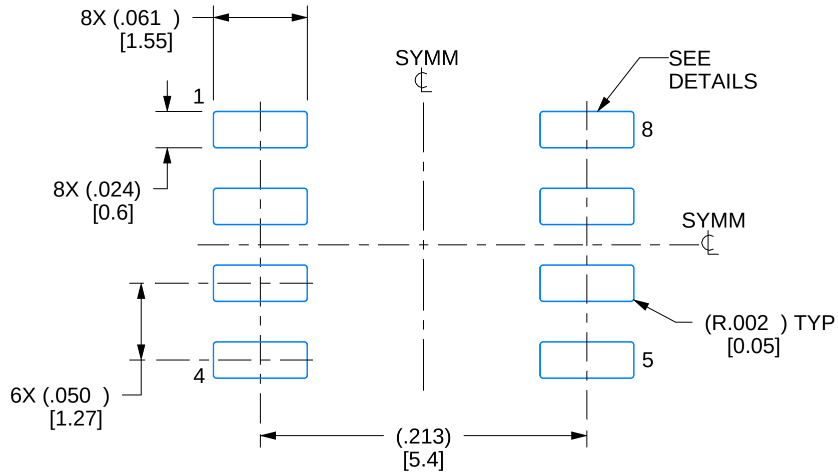


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

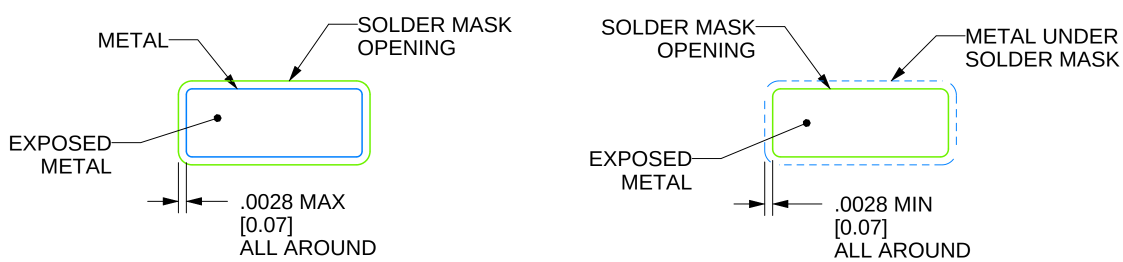


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

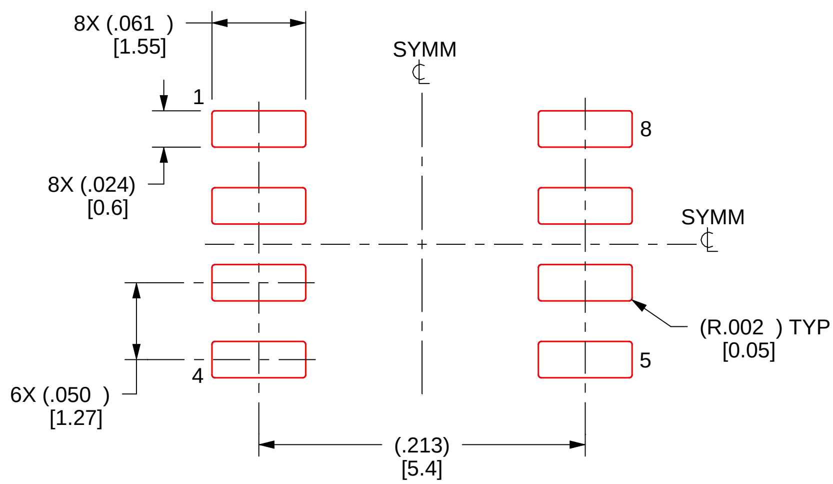
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

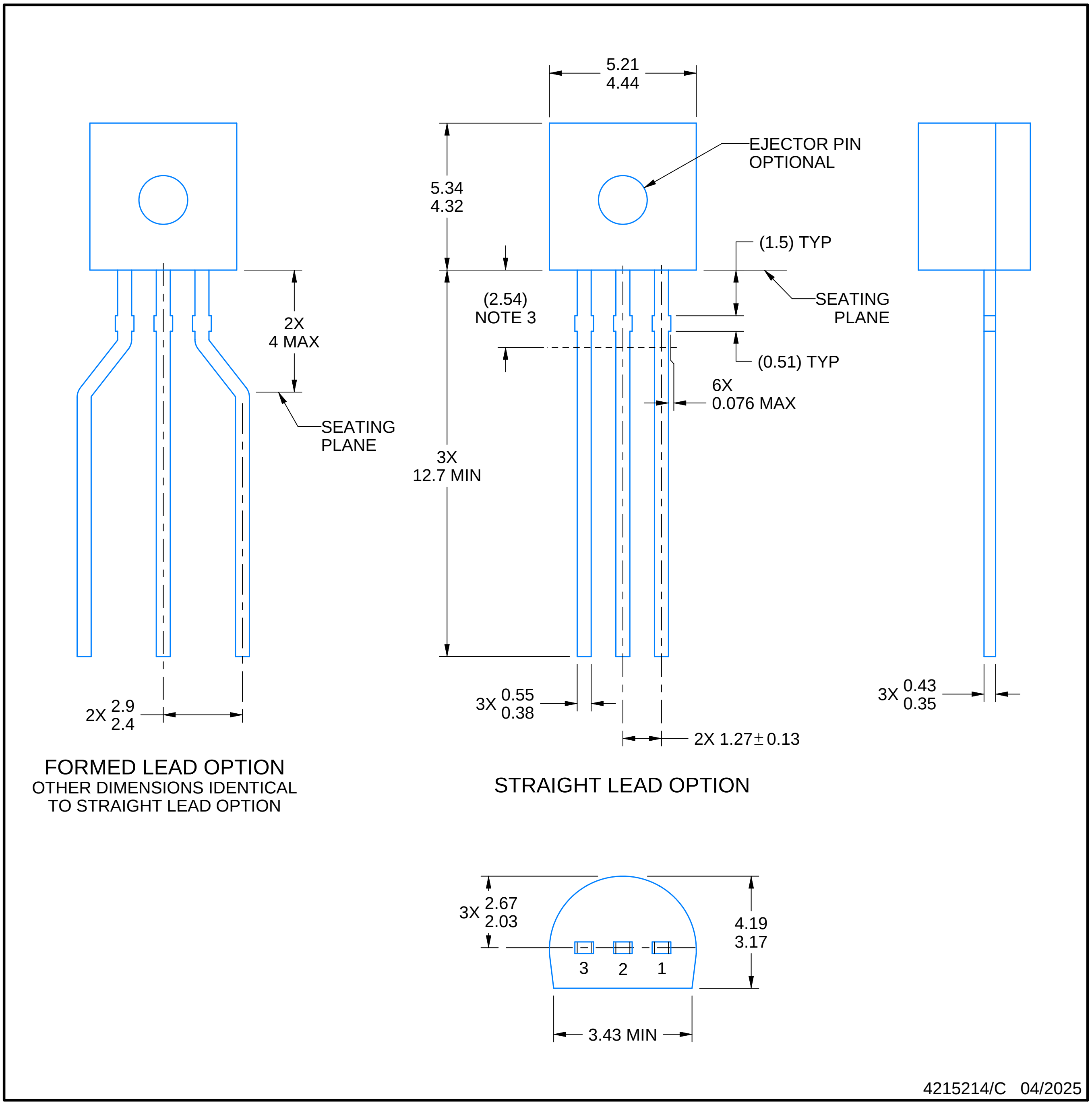


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

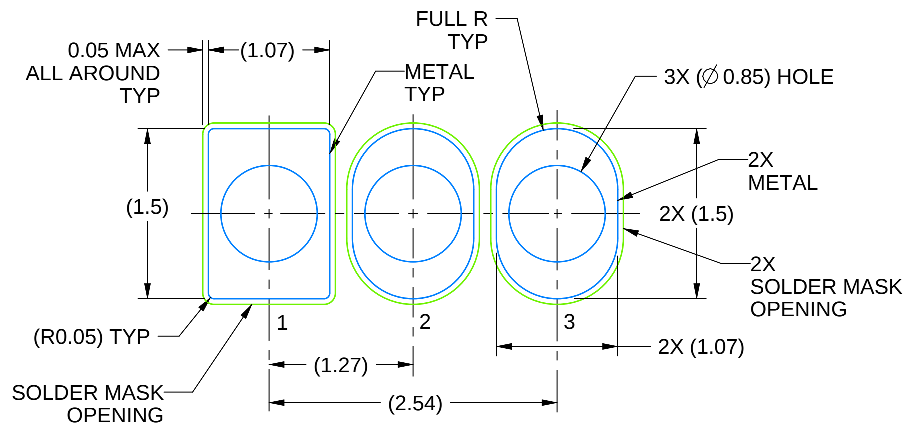
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

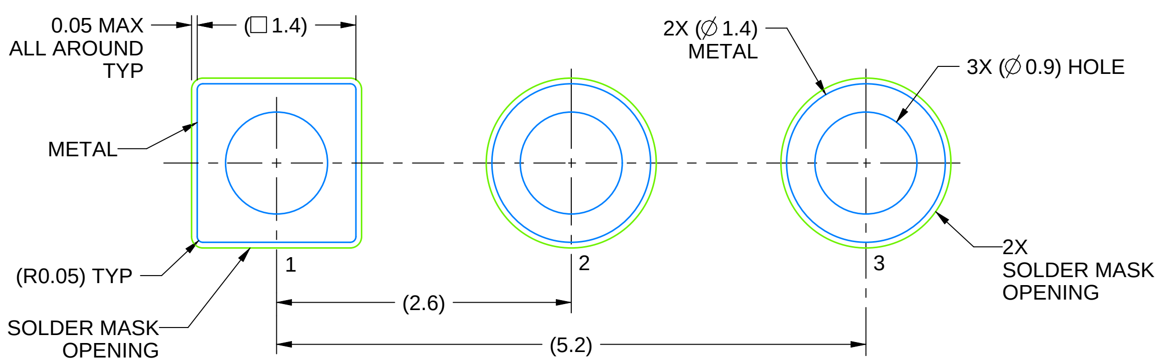


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.

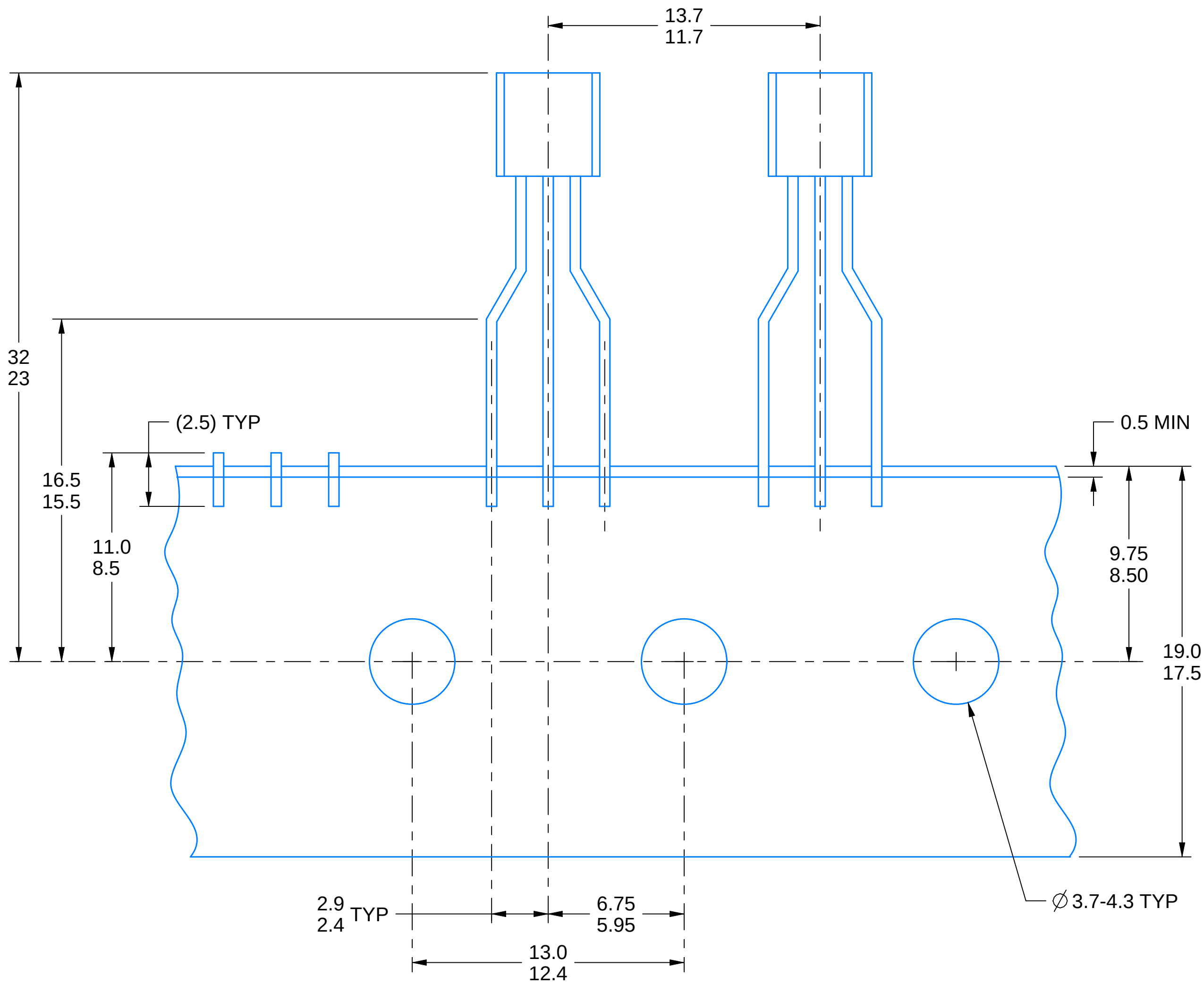


LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



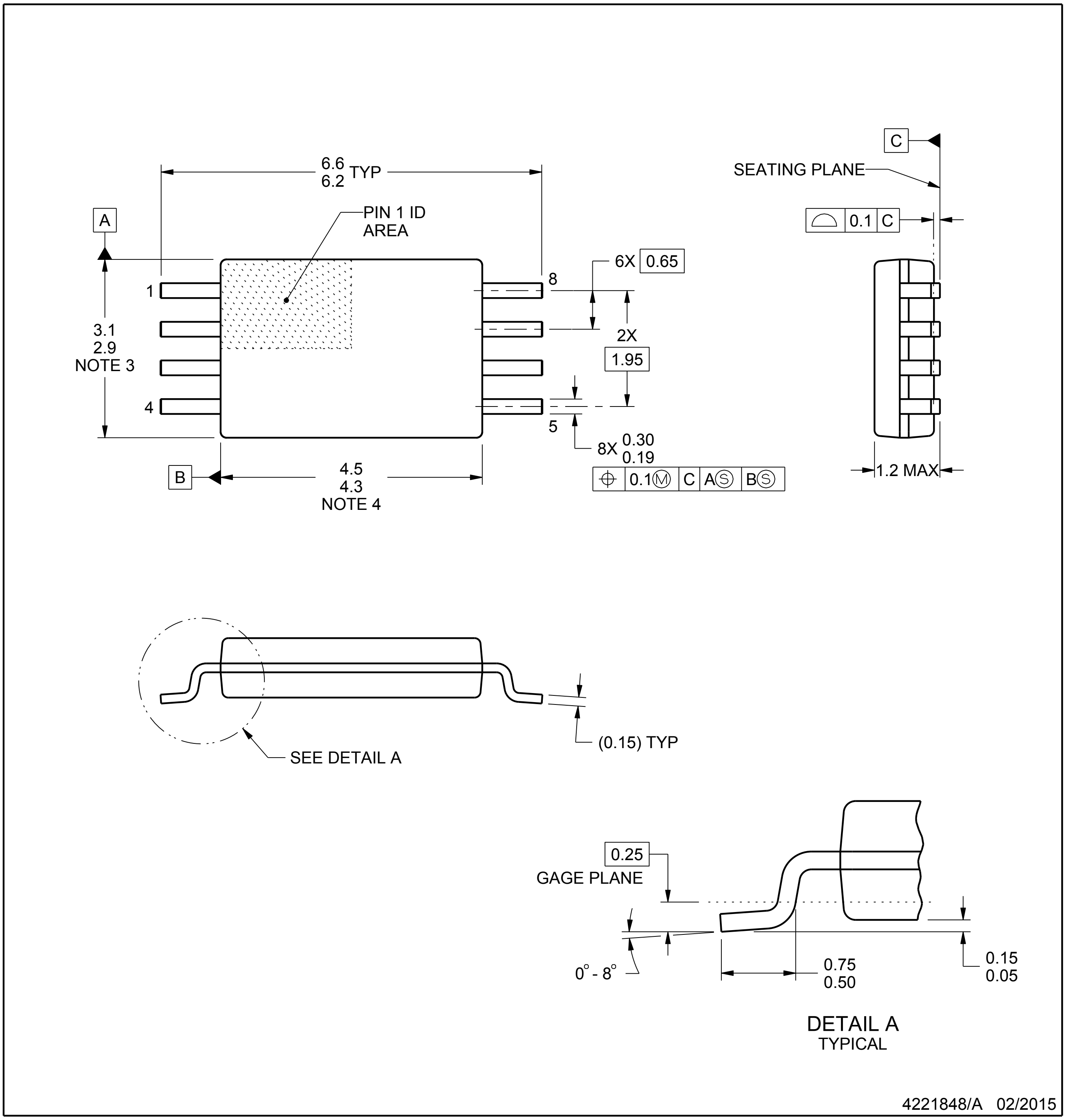
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/C 04/2025



FOR FORMED LEAD OPTION PACKAGE

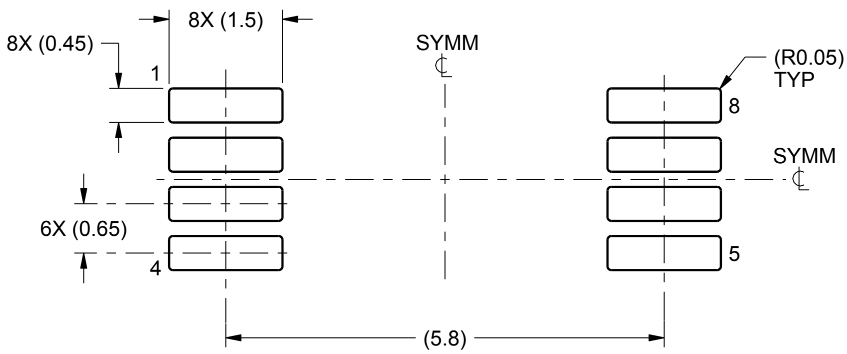
4215214/C 04/2025



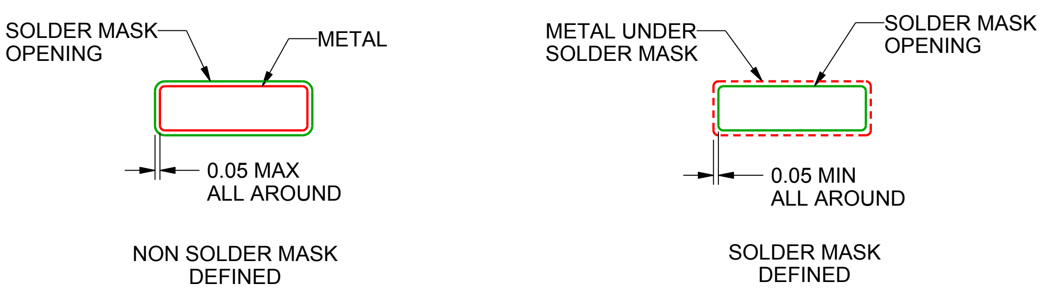
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

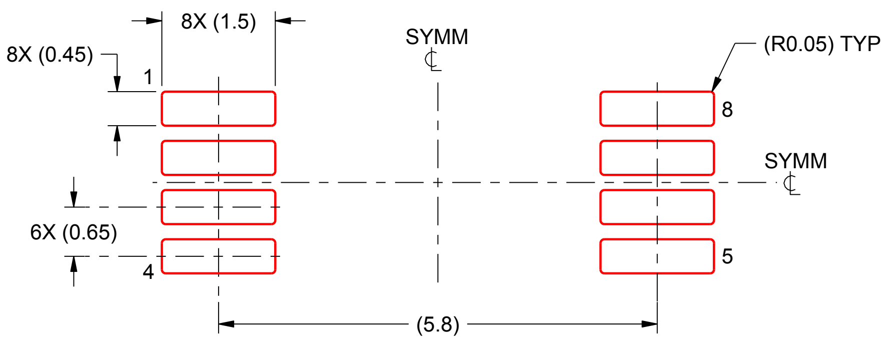


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.