LM25115A Secondary Side Post Regulator/DC-DC Converter with Power-Up/Power-Down Tracking

Check for Samples: LM25115A

FEATURES

- **Power-up/Power-down Tracking**
- **Self-synchronization to Main Channel Output**
- **Leading Edge Pulse Width Modulation**
- **Valley Current Mode Control**
- **Standalone DC/DC Synchronous Buck Mode**
- **Operates from AC or DC Input up to 42V**
- **Wide 4.5V to 30V Bias Supply Range**
- **Wide 0.75V to 13.5V Output Range.**
- **Top and Bottom Gate Drivers Sink 2.5A Peak**
- **Adaptive Gate Driver Dead-time Control**
- **Wide Bandwidth Error Amplifier (4MHz)**
- **Programmable Soft-start**
- **Thermal Shutdown Protection**
- **TSSOP-16 package**

DESCRIPTION

The LM25115A controller contains all of the features necessary to produce multiple tracking outputs using the Secondary Side Post Regulation (SSPR) technique. The SSPR technique develops a highly efficient and well regulated auxiliary output from the secondary side switching waveform of an isolated power converter. LM25115A can be also used as a standalone DC/DC synchronous buck controller (**Refer to Standalone DC/DC Synchronous Buck Mode section**). Regulation of the auxiliary output voltage is achieved by leading edge pulse width modulation (PWM) of the main channel duty cycle. Leading edge modulation is compatible with either current mode or voltage mode control of the main output. The LM25115A drives external high-side and low-side NMOS power switches configured as a synchronous buck regulator. A current sense amplifier provides overload protection and operates over a wide common mode input range. Additional features include a low dropout (LDO) bias regulator, error amplifier, precision reference, adaptive dead time control of the gate signals and thermal shutdown.

Typical Application Circuit

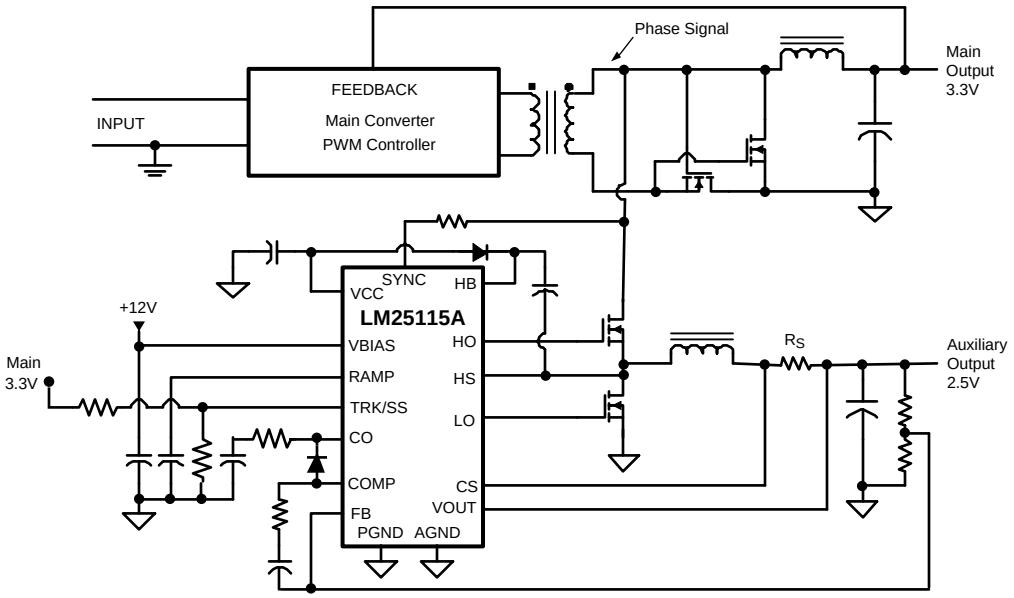


Figure 1. Simplified Multiple Output Power Converter Utilizing SSPR Technique

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Connection Diagram

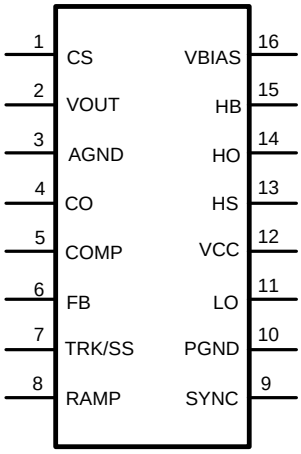


Figure 2. 16-Lead TSSOP
See Package Numbers PW0016A

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PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	CS	Current Sense amplifier positive input	A low inductance current sense resistor is connected between CS and VOUT. Current limiting occurs when the differential voltage between CS and VOUT exceeds 45mV (typical).
2	VOUT	Current sense amplifier negative input	Connected directly to the output voltage. The current sense amplifier operates over a voltage range from 0V to 13.5V at the VOUT pin.
3	AGND	Analog ground	Connect directly to the power ground pin (PGND).
4	CO	Current limit output	For normal current limit operation, connect the CO pin to the COMP pin through a diode. CO pin is connected to ground through a resistor in series with a capacitor to provide adequate control loop compensation for the current limit gm amplifier. Leave this pin open to disable the current limit function.
5	COMP	Compensation. Error amplifier output	COMP pin pull-up is provided by an internal 300uA current source.
6	FB	Feedback. Error amplifier inverting input	Connected to the regulated output through the feedback resistor divider and compensation components. The non-inverting input of the error amplifier is internally connected to the SS pin.
7	TRK/SS	Tracking/Soft-start control	Non-inverting input to error amp with 15 µA pull-up current source. Can be used with capacitor for soft-start or tied to external divider of a master output for tracking. TRK/SS is the reference input to the amplifier when the voltage applied to the pin is < 0.75V. For higher inputs, the internal reference controls the amplifier.
8	RAMP	PWM Ramp signal	An external capacitor connected to this pin sets the ramp slope for the voltage mode PWM. The RAMP capacitor is charged with a current that is proportional to current into the SYNC pin. The capacitor is discharged at the end of every cycle by an internal MOSFET.
9	SYNC	Synchronization input	A low impedance current input pin. The current into this pin sets the RAMP capacitor charge current and the frequency of an internal oscillator that provides a clock for the free-run (DC input) mode .
10	PGND	Power Ground	Connect directly to the analog ground pin (AGND).
11	LO	Low-side gate driver output	Connect to the gate of the low-side synchronous MOSFET through a short low inductance path.
12	VCC	Output of bias regulator	Nominal 7V output from the internal LDO bias regulator. Locally decouple to PGND using a low ESR/ESL capacitor located as close to controller as possible.
13	HS	High-side MOSFET source connection	Connect to negative terminal of the bootstrap capacitor and the source terminal of the high-side MOSFET.
14	HO	High-side gate driver output	Connect to the gate of high-side MOSFET through a short low inductance path.
15	HB	High-side gate driver bootstrap rail	Connect to the cathode of the bootstrap diode and the positive terminal of the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high-side MOSFET gate and should be placed as close to controller as possible.
16	VBIAS	Supply Bias Input	Input to the LDO bias regulator and current sense amplifier that powers internal blocks. Input range of VBIAS is 4.5V to 30V.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

VBIAS to GND	–0.3V to 32V
VCC to GND	–0.3V to 9V
HS to GND	–1V to 45V
VOUT, CS to GND	– 0.3V to 15V
All other inputs to GND	−0.3V to 7.0V
Storage Temperature Range	–55°C to +150°C
Junction Temperature	+150°C
ESD Rating HBM (3)	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

OPERATING RATINGS

VBIAS supply voltage	5V to 30V
VCC supply voltage	5V to 7.5V
HS voltage	0V to 42V
HB voltage	VCC + HS
Operating Junction Temperature	–40°C to +125°C

TYPICAL OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply Voltage, VBIAS	4.5		30	V
Supply Voltage, VCC	4.5		7	V
Supply voltage bypass, CVBIAS	0.1	1		µF
Reference bypass capacitor, CVCC	0.1	1	10	µF
HB-HS bootstrap capacitor	0.047			µF
SYNC Current Range (VCC = 4.5V)	50		150	µA
RAMP Saw Tooth Amplitude	1		1.75	V
VOUT regulation voltage (VBIAS min = 3V + VOUT)	0.75		13.5	V

ELECTRICAL CHARACTERISTICS(1)

Unless otherwise specified, T_J = –40°C to +125°C, VBIAS = 12V, No Load on LO or HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VBIAS SUPPLY						
Ibias	VBIAS Supply Current	F_{SYNC} = 200kHz			**4**	mA
VCC LOW DROPOUT BIAS REGULATOR						
VccReg	VCC Regulation	VCC open circuit. Outputs not switching	**6.65**	7	**7.15**	V
	VCC Current Limit	(2)		40		mA
	VCC Under-voltage Lockout Voltage	Positive going VCC	**4**		**4.5**	V
	VCC Under-voltage Hysteresis		**0.2**	0.25	**0.3**	V

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Device thermal limitations may limit usable range.

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ELECTRICAL CHARACTERISTICS[1] (continued)

Unless otherwise specified, T_J = –40°C to +125°C, VBIAS = 12V, No Load on LO or HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRACK / SOFT-START						
	SS Pull-up Source		**10**	15	**20**	µA
	SS Discharge Impedance			140		Ω
ERROR AMPLIFIER and FEEDBACK REFERENCE						
VREF	FB Reference Voltage	Measured at FB pin	**.737**	.750	**.763**	V
	FB Input Bias Current	FB = 2V		0.2	**0.5**	µA
	COMP Source Current			300		µA
	Open Loop Voltage Gain			60		dB
GBW	Gain Bandwidth Product			4		MHz
Vio	Input Offset Voltage			22		mV
	COMP Offset	Threshold for V_{HO} = high RAMP = CS = VOUT = 0V		2		V
	RAMP Offset	Threshold for V_{HO} = high COMP = 1.5V, CS = VOUT = 0V		1.0		V
CURRENT SENSE AMPLIFIER						
	Current Sense Amplifier Headroom	Headroom = V_{bias} – Vout V_{bias}= 4.5 V and Vout= 1.5 V	**3**			V
	Current Sense Amplifier Gain			16		V/V
	Output DC Offset			1.27		V
	Amplifier Bandwidth			500		kHz
CURRENT LIMIT						
	Slow ILIMIT Amp Transconductance			5		mA / V
	Overall Transconductance			90		mA / V
	Slow ILimit Threshold	$V_{CL} = V_{CS} - V_{VOUT}$ VOUT = 6V and CO/COMP = 1.5V	**39**	45	**51**	mV
	Slow ILimit Foldback	$V_{CL} = V_{CS} - V_{VOUT}$ VOUT = 0V and CO/COMP = 1.5V	**34**	39	**46**	mV
	Fast ILimit Pull-Down Current	Vds = 2V		45		mA
	Fast ILimit Threshold			60		mV
V_{CLNEG}	Negative Current Limit	VOUT = 6V $V_{CL} = V_{CS} - V_{VOUT}$ to cause LO to shutoff		-17		mV
	CO Clamp Voltage		**5.5**	6	**6.5**	V
	ICO Pull-Up Current			15		µA
RAMP GENERATOR						
	SYNC Input Impedance			2.5		kΩ
	SYNC Threshold	End of cycle detection threshold		20		µA
	Free Run Mode Peak Threshold	RAMP peak voltage with dc current applied to SYNC.			**2.35**	V
	Current Mirror Gain	Ratio of RAMP charge current to SYNC input current.	**2.7**		**3.3**	A/A
	Discharge Impedance			100		Ω
LOW-SIDE GATE DRIVER						
V_{OLL}	LO Low-state Output Voltage	I_{LO} = 100mA		0.15	**0.5**	V
V_{OHL}	LO High-state Output Voltage	I_{LO} = -100mA, $V_{OHL} = V_{CC} - V_{LO}$		0.35	**0.8**	V
	LO Rise Time	C_{LOAD} = 1000pF		15		ns
	LO Fall Time	C_{LOAD} = 1000pF		12		ns
I_{OHL}	Peak LO Source Current	V_{LO} = 0V		2		A
I_{OLL}	Peak LO Sink Current	V_{LO} = 12V		2.5		A

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ELECTRICAL CHARACTERISTICS[1] (continued)

Unless otherwise specified, T_J = –40°C to +125°C, VBIAS = 12V, No Load on LO or HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
HIGH-SIDE GATE DRIVER						
V_{OLH}	HO Low-state Output Voltage	I_{HO} = 100mA		0.15	**0.5**	V
V_{OHH}	HO High-state Output Voltage	I_{HO} = -100mA, $V_{OHH} = V_{HB} – V_{HO}$		0.35	**0.8**	V
	HO Rise Time	C_{LOAD} = 1000pF		15		ns
	HO High-side Fall Time	C_{LOAD} = 1000pF		12		ns
I_{OHH}	Peak HO Source Current	V_{HO} = 0V		2		A
I_{OLH}	Peak HO Sink Current	V_{HO} = 12V		2.5		A
SWITCHING CHARACTERISITCS						
	LO Fall to HO Rise Delay	C_{LOAD} = 0		40		ns
	HO Fall to LO Rise Delay	C_{LOAD} = 0		50		ns
	SYNC Fall to HO Fall Delay	C_{LOAD} = 0		120		ns
	SYNC Rise to LO Fall Delay	C_{LOAD} = 0		80		ns
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Temp.		**150**	165		°C
	Thermal Shutdown Hysteresis			25		°C
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	PW Package		125		°C/W
θ_{JA}	Junction to Ambient	SDA Package		32		°C/W

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TYPICAL PERFORMANCE CHARACTERISTICS

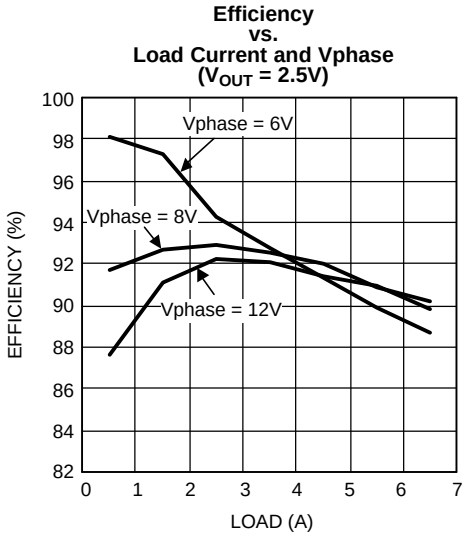


Figure 3.

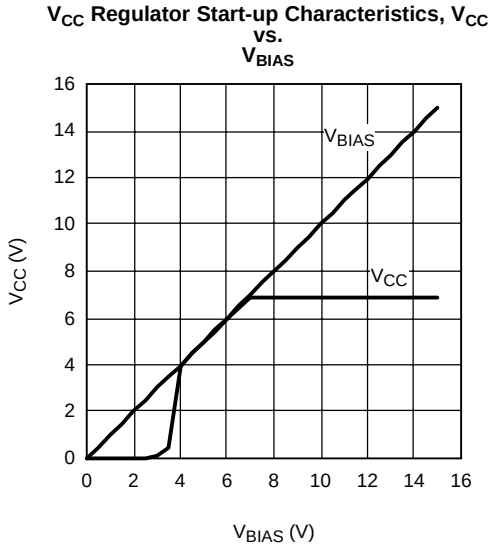


Figure 4.

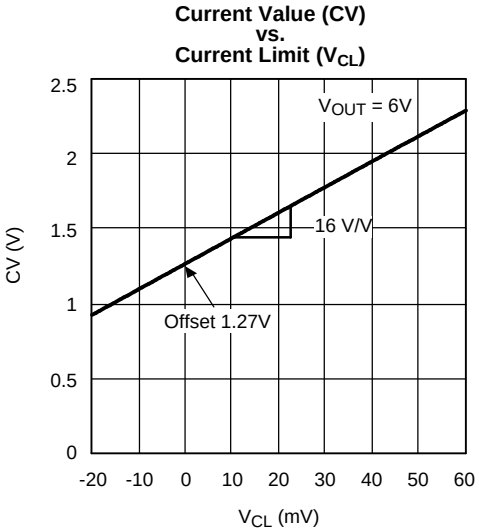


Figure 5.

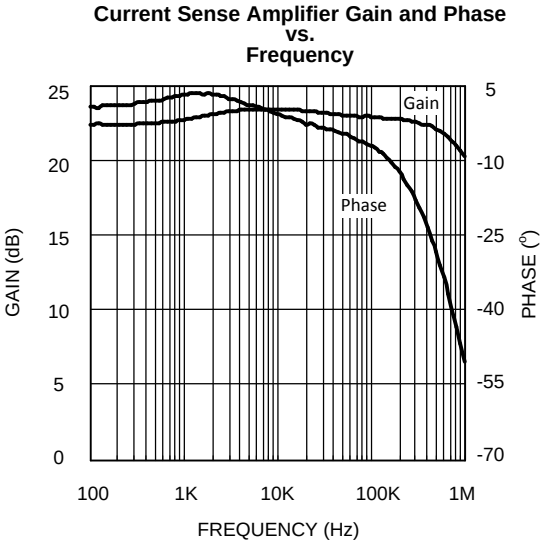


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Current Error Amplifier Transconductance

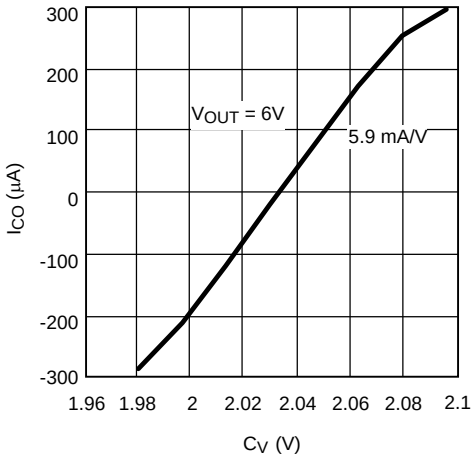


Figure 7.

Overall Current Amplifier Transconductance

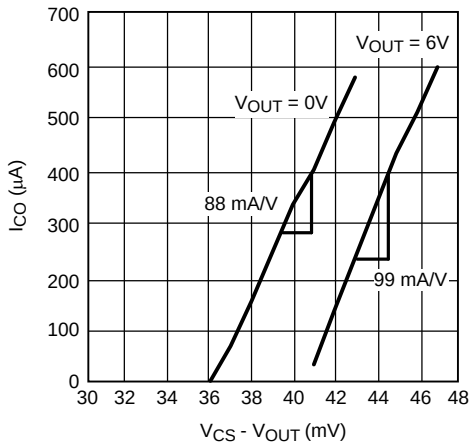


Figure 8.

Common Mode Output Voltage vs. Positive Current Limit

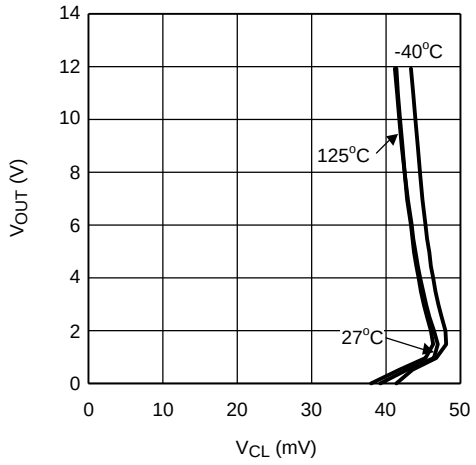


Figure 9.

Common Mode Output Voltage vs. Negative Current Limit (Room Temp)

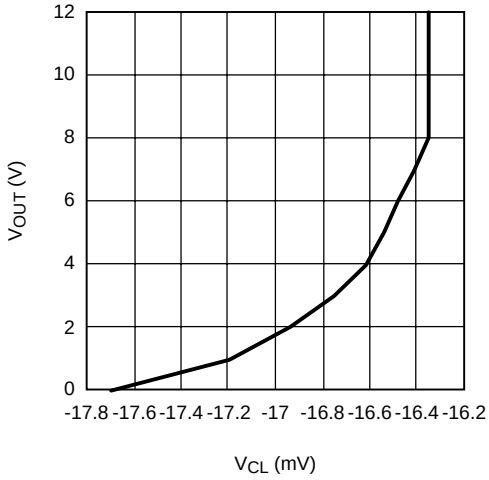


Figure 10.

V_{CC} Load Regulation to Current Limit

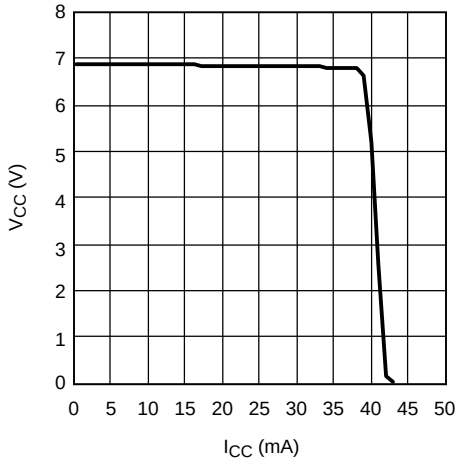
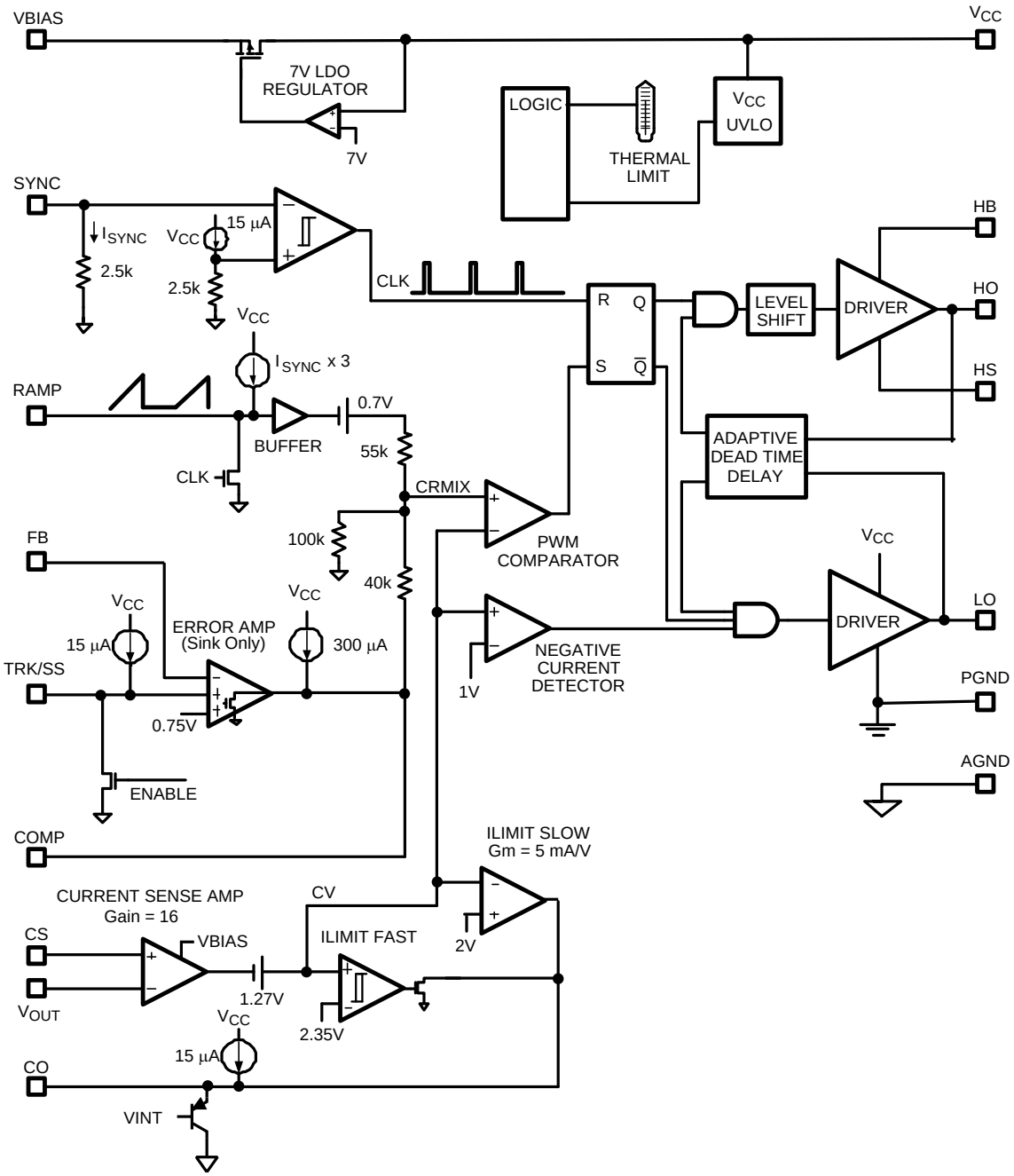


Figure 11.

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BLOCK DIAGRAM



DETAILED OPERATING DESCRIPTION

The LM25115A controller contains all of the features necessary to implement multiple output power converters utilizing the Secondary Side Post Regulation (SSPR) technique. The SSPR technique develops a highly efficient and well regulated auxiliary output from the secondary side switching waveform of an isolated power converter. Regulation of the auxiliary output voltage is achieved by leading edge pulse width modulation (PWM) of the main channel duty cycle. Leading edge modulation is compatible with either current mode or voltage mode control of the main output. The LM25115A drives external high-side and low-side NMOS power switches configured as a synchronous buck regulator. A current sense amplifier provides overload protection and operates over a wide common mode input range from 0V to 13.5V. Additional features include a low dropout (LDO) bias regulator, error amplifier, precision reference, adaptive dead time control of the gate driver signals and thermal shutdown.

Low Drop-Out Bias Regulator (VCC)

The LM25115A contains an internal LDO regulator that operates over an input supply range from 4.5V to 30V. The output of the regulator at the VCC pin is nominally regulated at 7V and is internally current limited to 40mA. VCC is the main supply to the internal logic, PWM controller, and gate driver circuits. When power is applied to the VBIAS pin, the regulator is enabled and sources current into an external capacitor connected to the VCC pin. The recommended output capacitor range for the VCC regulator is 0.1uF to 100uF. When the voltage at the VCC pin reaches the VCC under-voltage lockout threshold of 4.25V, the controller is enabled. The controller is disabled if VCC falls below 4.0V (250mV hysteresis). In applications where an appropriate regulated dc bias supply is available, the LM25115A controller can be powered directly through the VCC pin instead of the VBIAS pin. In this configuration, it is recommended that the VCC and the VBIAS pins be connected together such that the external bias voltage is applied to both pins. The allowable VCC range when biased from an external supply is 4.5V to 7V.

Synchronization (SYNC) and Feed-Forward (RAMP)

The pulsing “phase signal” from the main converter synchronizes the PWM ramp and gate drive outputs of the LM25115A. The phase signal is the square wave output from the transformer secondary winding before rectification (Figure 1). A resistor connected from the phase signal to the low impedance SYNC pin produces a square wave current (I_{SYNC}) as shown in Figure 12. A current comparator at the SYNC input monitors I_{SYNC} relative to an internal 15µA reference. When I_{SYNC} exceeds 15µA, the internal clock signal (CLK) is reset and the capacitor connected to the RAMP begins to charge. The current source that charges the RAMP capacitor is equal to 3 times the I_{SYNC} current. The falling edge of the phase signal sets the CLK signal and discharges the RAMP capacitor until the next rising edge of the phase signal. The RAMP capacitor is discharged to ground by a low impedance (100Ω) n-channel MOSFET. The input impedance at SYNC pin is 2.5kΩ which is normally much smaller than the external SYNC pin resistance.

The RAMP and SYNC functions illustrated in Figure 12 provide line voltage feed-forward to improve the regulation of the auxiliary output when the input voltage of the main converter changes. Varying the input voltage to the main converter produces proportional variations in amplitude of the phase signal. The main channel PWM controller adjusts the pulse width of the phase signal to maintain constant volt*seconds and a regulated main output as shown in Figure 13. The variation of the phase signal amplitude and duration are reflected in the slope and duty cycle of the RAMP signal of the LM25115A (I_{SYNC} α phase signal amplitude). As a result, the duty cycle of the LM25115A is automatically adjusted to regulate the auxiliary output voltage with virtually no change in the PWM threshold voltage. Transient line regulation is improved because the PWM duty cycle of the auxiliary converter is immediately corrected, independent of the delays of the voltage regulation loop.

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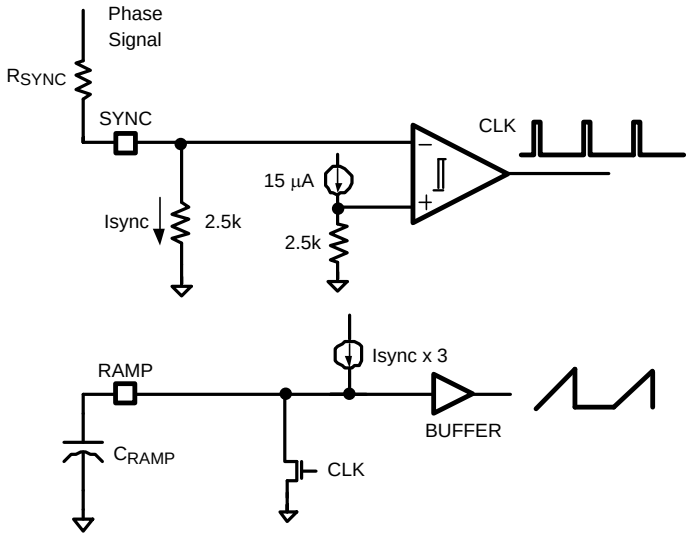


Figure 12. Line Feed-Forward Diagram

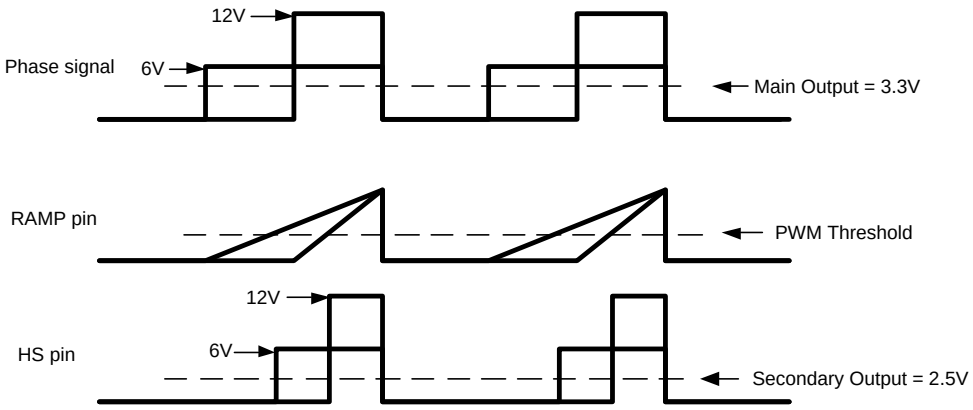


Figure 13. Line Feed-Forward Waveforms

The recommended SYNC input current range is 50µA to 150µA. The SYNC pin resistor (R_{SYNC}) should be selected to set the SYNC current (I_{SYNC}) to 150µA with the maximum phase signal amplitude, $V_{PHASE(max)}$. This will ensure that I_{SYNC} stays within the recommended range over a 3:1 change in phase signal amplitude. The SYNC pin resistor is therefore:

$$R_{SYNC} = (V_{PHASE(max)} / 150\mu A) - 2.5k\Omega$$

Once I_{SYNC} has been established by selecting R_{SYNC}, the RAMP signal slope/amplitude may be programmed by selecting the proper RAMP pin capacitor value. The RAMP signal slope should be selected to provide adequate slope compensation for the Valley current mode control scheme (Please refer to the Valley Current Mode Control section). The recommended peak amplitude of the ramp waveform is 1.75V.

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Error Amplifier and Soft-Start (FB, CO, COMP & TRK/SS)

An internal wide bandwidth error amplifier is provided within the LM25115A for voltage feedback to the PWM controller. The amplifier's inverting input is connected to the FB pin. The output of the auxiliary converter is regulated by connecting a voltage setting resistor divider between the output and the FB pin. Loop compensation networks are connected between the FB pin and the error amplifier output (COMP). The amplifier has two non-inverting inputs. The first non-inverting input connects to a 0.75V bandgap reference while the second non-inverting input connects to the TRK/SS pin and it has 15 µA pull-up current source. The TRK/SS pin can be tied to an external resistor divider from the master output for tracking, or it can be tied to a capacitor for soft-start . TRK/SS is the reference input to the amplifier when the voltage applied to the pin is < 0.75V. For higher inputs, the internal reference controls the amplifier. When the VCC voltage is below the UVLO threshold, the TRK/SS pin is discharged to ground. When VCC rises and exceeds the positive going UVLO threshold (4.25V), the TRK/SS pin is released and allowed to rise. If an external capacitor is connected to the TRK/SS pin, it will be charged by the internal 15uA pull-up current source to gradually increase the non-inverting input of the error amplifier to 0.75V. During start-up, the output of the LM25115A converter will follow the following equation:

VOUT(t) = VOUT(final) x15 µA x t /(.75 Vx Css)

where

- Css = external Soft-Start capacitor
- VOUT(final) = regulator output set point

Pull-up current for the error amplifier output is provided by an internal 300µA current source. The PWM threshold signal at the COMP pin can be controlled by either the open drain error amplifier or the open drain current amplifier connected through the CO pin to COMP. Since the internal error amplifier is configured as an open drain output it can be disabled by connecting FB to ground. The current sense amplifier and current limiting function will be described in a later section.

Power-Up/Power-Down Tracking

The LM25115A can track the output of a master power supply during soft start by connecting a resistor divider to the TRACK pin (Figure 14). Therefore, the output voltage slew rate of the LM25115A will be controlled by the master supply for loads that require precise sequencing. In order to track properly the output voltage of the LM25115A must be lower than the output voltage of the master supply.

One way to use the tracking feature is to design the tracking resistor divider so that the master supply output voltage (VOUT1) and the LM25115A output voltage (VOUT2) both rise together and reach their target values at the same time. For this case, the equation governing the values of the tracking divider resistors RT1 and RT2 is:

$$R_{T1} = \frac{0.8 \times R_{T2}}{V_{OUT1} - 0.8}$$

A value of 10kΩ (1%) is recommended for RT2 as a good compromise between high precision and low quiescent current through the divider. If the master supply voltage was 3.3V and the LM25115A output voltage was 2.5 V, then the value of RT1 needed to give the two supplies identical soft start times would be 2.94 kΩ (1%). The timing diagram and waveforms for the equal soft start time configuration are shown in Figure 15 and Figure 16.

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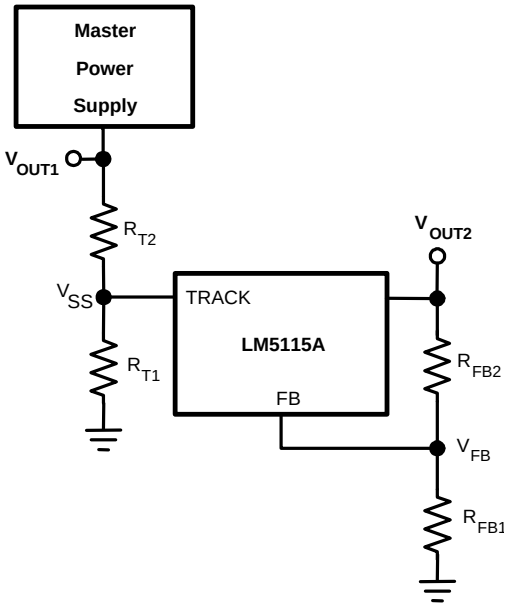


Figure 14.

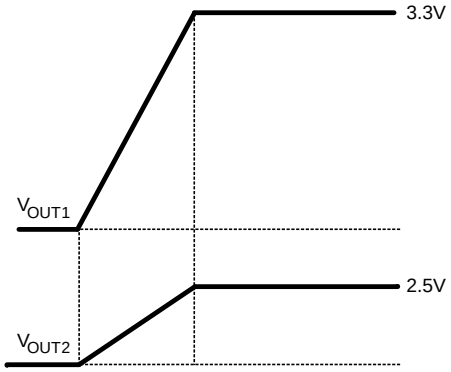
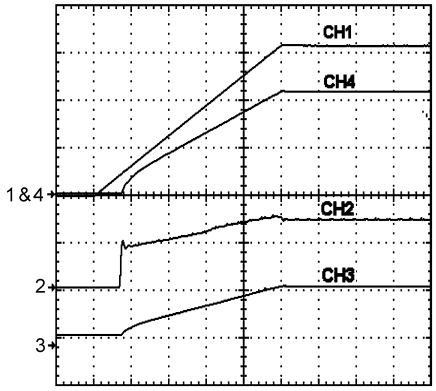


Figure 15.



Vphase = 10V
CH1 = Master output, 1V/Div
CH2 = COMP, 5/Div
CH3 = Iout, 1A/Div
CH4 = SSPR Output (Slave), 1V/Div
Horizontal Resolution= 200 µs/Div

Figure 16. Tracking with Equal Soft Start Time

Alternatively, the tracking feature can be used to create equal slew rates between the output voltages of the master supply and the LM25115A. This method ensures that the output voltage of the LM25115A always reaches regulation before the output voltage of the master supply. In this case, the tracking resistors can be determined based on the following equation:

$$R_{T1} = \frac{0.8 \times R_{T2}}{V_{OUT2} - 0.8}$$

Again, a value of 10kΩ 1% is recommended for RT2. For the case of VOUT1 = 3.3V and VOUT2 = 2.5V, RT1 should be 4.32 kΩ 1%. The timing diagram and the waveforms for equal slew rates configuration are shown in Figure 17 and Figure 18.

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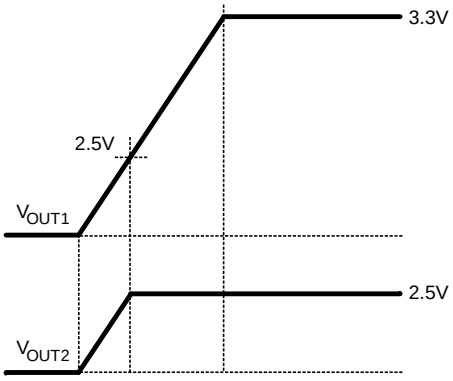
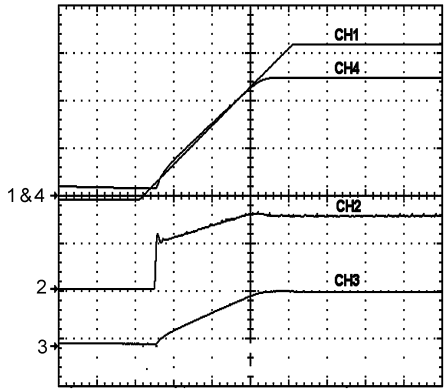


Figure 17.



Vphase = 10V
CH1 = Master output, 1V/Div
CH2 = COMP, 5/Div
CH3 = Iout, 1A/Div
CH4 = SSPR Output (Slave), 1V/Div
Horizontal Resolution= 200 µs/Div

Figure 18. Tracking with Equal Slew Rate

Leading Edge Pulse Width Modulation

Unlike conventional voltage mode controllers, the LM25115A implements leading edge pulse width modulation. A current source equal to 3 times the I_{SYNC} current is used to charge the capacitor connected to the RAMP pin as shown in Figure 19. The ramp signal and the output of the error amplifier (COMP) are combined through a resistor network to produce a voltage ramp with variable dc offset (CRMIX in Figure 19). The high-side MOSFET which drives the HS pin is held in the off state at the beginning of the phase signal. When the voltage of CRMIX exceeds the internal threshold voltage CV, the PWM comparator turns on the high-side MOSFET. The HS pin rises and the MOSFET delivers current from the main converter phase signal to the output of the auxiliary regulator. The PWM cycle ends when the phase signal falls and power is no longer supplied to the drain of the high-side MOSFET.

Leading edge modulation of the auxiliary PWM controller is required if the main converter uses peak current mode control. If trailing edge modulation were used, the additional load on the transformer secondary from the auxiliary channel would be drawn only during the first portion of the phase signal pulse. Referring to Figure 20, the turn-off of the high- side MOSFET of the auxiliary regulator would create a non-monotonic negative step in the transformer current. This negative current step would produce instability in a peak current mode controller. With leading edge modulation, the additional load presented by the auxiliary regulator on the transformer secondary will be present during the latter portion of the phase signal. This positive step in the phase signal current can be accommodated by a peak current mode controller without instability.

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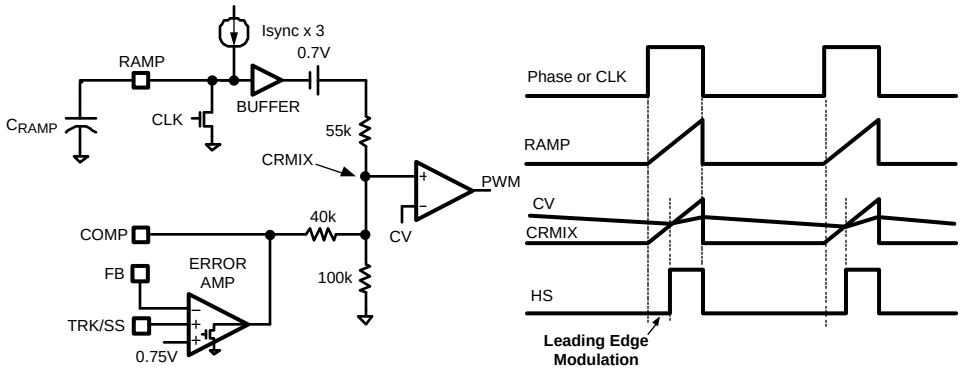


Figure 19. Synchronization and Leading Edge Modulation

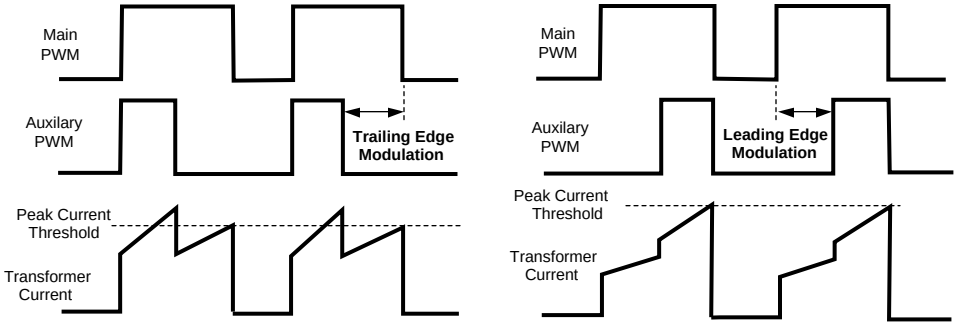


Figure 20. Leading versus Trailing Edge Modulation

Valley Current Mode Control

The LM25115A controller uniquely utilizes the elements and benefits of valley current mode control in conjunction with leading edge modulation to correct changes in output voltage due to line and load transients. Contrary to peak current mode control, valley current mode control turns on the high-side MOSFET when the inductor valley current reaches a programmable threshold. This programmable threshold (CRMIX) is the sum of the output of voltage error amplifier and the RAMP signal generated at the RAMP pin. Valley current mode control experiences sub-harmonic oscillation when the duty ratio, D, is less than or equal to 50%. Therefore, adequate slope compensation is needed for the proper operation across the full range of the duty ratio. The RAMP signal is proportional to the input voltage and it provides the required slope compensation for the valley current mode scheme. The desired RAMP pin capacitance can be calculated from the following equation:

$$C_{RAMP} = (0.05 \times L) / (R_{SYNC} \times R_{SENSE})$$

where

- L is the power inductor
- R_{SYNC} is the SYNC pin resistor
- R_{SENSE} is the current sense resistor

The current sense amplifier shown in Figure 21 monitors the inductor current as it flows through a sense resistor connected between CS and VOUT. The voltage gain of the sense amplifier is nominally equal to 16. The current sense output signal is shifted by 1.27V to produce the internal CV reference signal. The CV signal is applied to the negative input of the PWM comparator and compared to CRMIX as illustrated in Figure 21. Therefore when CRMIX exceeds the PWM threshold (CV), the PWM comparator turns on the high-side MOSFET. Insure that the Vbias voltage is at least 3V above the regulated output voltage (VOUT) to provide enough headroom for the current sense amplifier.

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Valley current mode control improves the control loop stability and bandwidth. It also eliminates the R-C lead network in the feedback path that is normally required with voltage mode control (Figure 22). Eliminating the lead network not only simplifies the compensation, but also reduces sensitivity to output noise that could pass through the lead network to the error amplifier.

The design of the voltage feedback path through the error amp begins with the selection of R1 and R2 in Figure 22 to set the regulated output voltage. The steady state output voltage after soft-start is determined by the following equation:

$$VOUT(final) = 0.75V \times (1+R1/R2)$$

The parallel impedance of the R1, R2 resistor divider should be approximately 2kΩ (between 0.5kΩ and 5kΩ). Lower resistance values may not be properly driven by the error amplifier output and higher feedback resistances can introduce noise sensitivity. The next step in the design process is selection of R3, which sets the ac gain of the error amplifier.

The capacitor C1 is connected in series with R3 to increase the dc gain of the voltage regulation loop and improve output voltage accuracy. The corner frequency set by R3 x C1 should be less than 1/10th of the cross-over frequency of the overall converter such that capacitor C1 does not add phase lag at the crossover frequency.

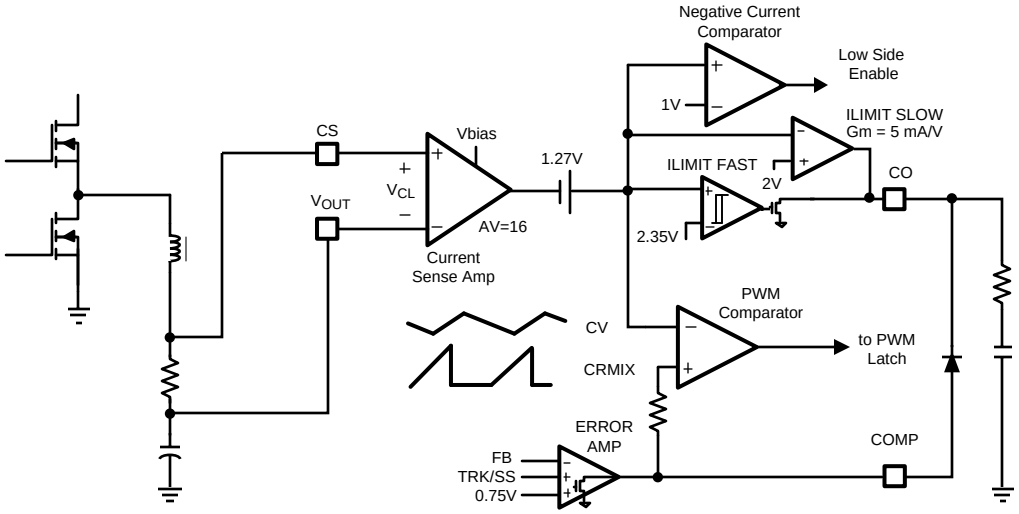


Figure 21. Current Sensing and Limiting

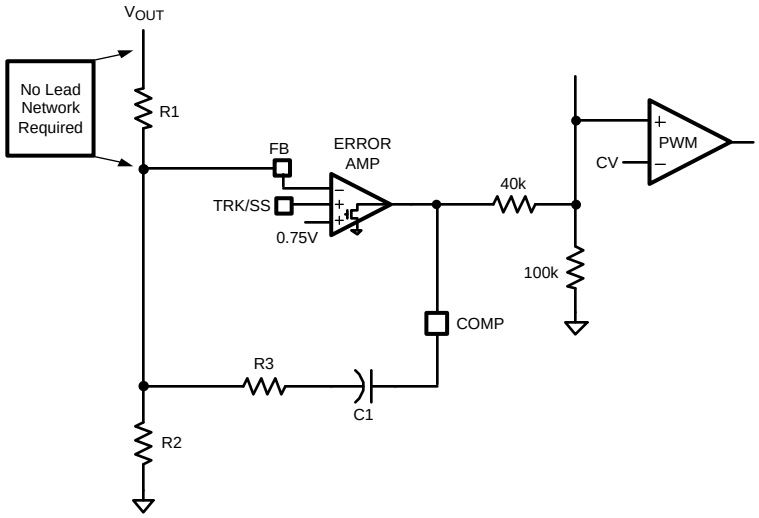


Figure 22. Voltage Sensing and Feedback

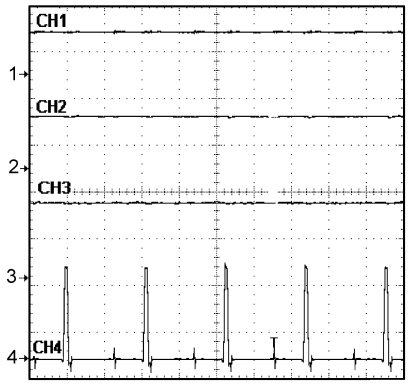
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Current Limiting (CS, CO and VOUT)

Current limiting is implemented through the current sense amplifier as illustrated in Figure 21. The current sense amplifier monitors the inductor current that flows through a sense resistor connected between CS and VOUT. The voltage gain of the current sense amplifier is nominally equal to 16. The output of current sense signal is shifted by 1.27V to produce the internal CV reference signal. The CV signal drives two current limit amplifiers. Both of the current limit amplifiers have open drain (sink only) output stages which are connected to the CO pin. The CO pin is typically connected to the COMP pin through a diode (the cathode is connected to the CO pin and the anode is connected to the COMP pin). The slow current limit amplifier has a nominal transconductance of 5 mA/V and provides constant current mode operation at the desired current limit set point. The fast current limit amplifier has nominal current pull-down capability of 100mA and provides protection against fast over-current conditions. During normal operation, the voltage error amplifier controls the COMP pin voltage which adjusts the PWM duty cycle by varying the internal CRMIX level. However when the current sense input voltage, V_{CL}, exceeds 45mV, the slow current limit amplifier gradually pulls down on COMP through the CO pin. Pulling COMP low reduces the CRMIX signal and thereby reducing the operating duty cycle. By controlling the operating duty cycle, the slow current limit amplifier will force a constant current mode of operation at the desired current limit set point (Figure 23). A resistor in series with a capacitor are connected from the CO Pin to ground to provide adequate control loop compensation for the slow current limit (Figure 21). The desired current limit set point, ILimit, can be programmed by selecting the proper current sense resistor, R_{SENSE},using the following equation:

$$R_{SENSE} = 0.045\ V / ILimit$$

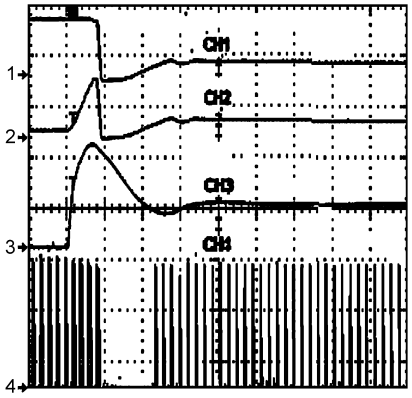
In the event that the current sense input voltage, V_{CL}, exceeds 60mV, the fast current limit amplifier will pull down hard on COMP through the CO pin. This will reduce the CRMIX signal to a voltage below the CV signal level. Therefore, the PWM comparator will inhibit output pulses. Once the fault condition is removed, the fast current limit amplifier will release COMP. Therefore, the CRMIX signal will increase to a normal operating threshold and the switching will resume (Figure 24). A current limit fold-back feature is provided by the LM25115A to reduce the peak output current delivered to a shorted load. When the common mode input voltage to the current sense amplifier (CS and VOUT pins) falls below 2V, the current limit threshold is reduced from the normal level. At common mode voltages > 2V, the current limit threshold is nominally 45mV. When VOUT is reduced to 0 V the current limit threshold drops to 39mV to reduce stress on the inductor and power MOSFETs.



Vphase=10V
CH1 = CO, 5V/Div
CH2 = COMP, 5/Div
CH3 = Iout, 5A/Div
CH4 = SSPR Switch Signal, 5V/Div
Horizontal Resolution= 2 µs/Div

Figure 23. SSPR Steady State Current Limit (Output Shorted)

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Vphase=10V
CH1 = CO, 5V/Div
CH2 = COMP, 5/Div
CH3 = Iout, 10A/Div
CH4 = SSPR Switch Signal, 4V/Div
Horizontal Resolution= 20 µs/Div

Figure 24. SSPR Short Circuit Transient (No-Load to Short-Circuit)

Negative Current Limit

Under certain conditions synchronous buck regulators are capable of sinking current from the output capacitors. This energy is stored in the inductor and returned to the input source. The LM25115A detects this current reversal by detecting a negative voltage being developed across the current sense resistor. The intent of this negative current comparator is to protect the low-side MOSFET from excessive currents. Excessive negative current can also lead to a large positive voltage spike on the HS pin at the turn-off of the low-side MOSFET. This voltage spike may damage the chip if its magnitude exceeds the maximum voltage rating of the part. The negative current comparator threshold is sufficiently negative to allow inductor current to reverse at no load or light load conditions. It is not intended to support discontinuous conduction mode with diode emulation by the low-side MOSFET. The negative current comparator shown in Figure 21 monitors the CV signal and compares this signal to a fixed 1V threshold. This corresponds to a negative V_{CL} voltage between CS and VOUT of -17mV. The negative current limit comparator turns off the low-side MOSFET for the remainder of the cycle when the V_{CL} input falls below this threshold.

Gate Driver Outputs (HO & LO)

The LM25115A provides two gate driver outputs, the floating high-side gate driver HO and the synchronous rectifier low-side driver LO. The low-side driver is powered directly by the VCC regulator. The high-side gate driver is powered from a bootstrap capacitor connected between HB and HS. An external diode connected between VCC and HB charges the bootstrap capacitor when the HS is low. When the high-side MOSFET is turned on, HB rises with HS to a peak voltage equal to VCC + V_{HS} - V_D where V_D is the forward drop of the external bootstrap diode. Both output drivers have adaptive dead-time control to avoid shoot through currents. The adaptive dead-time control circuit monitors the state of each driver to ensure that one MOSFET is turned off before the other is turned on. The HB and VCC capacitors should be placed close to the pins of the LM25115A to minimize voltage transients due to parasitic inductances and the high peak output currents of the drivers. The recommended range of the HB capacitor is 0.047µF to 0.22µF.

Both drivers are controlled by the PWM logic signal from the PWM latch. When the phase signal is low, the outputs are held in the reset state with the low-side MOSFET on and the high-side MOSFET off. When the phase signal switches to the high state, the PWM latch reset signal is de-asserted. The high-side MOSFET remains off until the PWM latch is set by the PWM comparator (CRMIX > CV as shown in Figure 19). When the PWM latch is set, the LO driver turns off the low-side MOSFET and the HO driver turns on the high-side MOSFET. The high-side pulse is terminated when the phase signal falls and SYNC input comparator resets the PWM latch.

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Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature limit is exceeded. When activated, typically at 165 degrees Celsius, the controller is forced into a low power standby state with the output drivers and the bias regulator disabled. The device will restart when the junction temperature falls below the thermal shutdown hysteresis, which is typically 25 degrees. The thermal protection feature is provided to prevent catastrophic failures from accidental device overheating.

Standalone DC/DC Synchronous Buck Mode

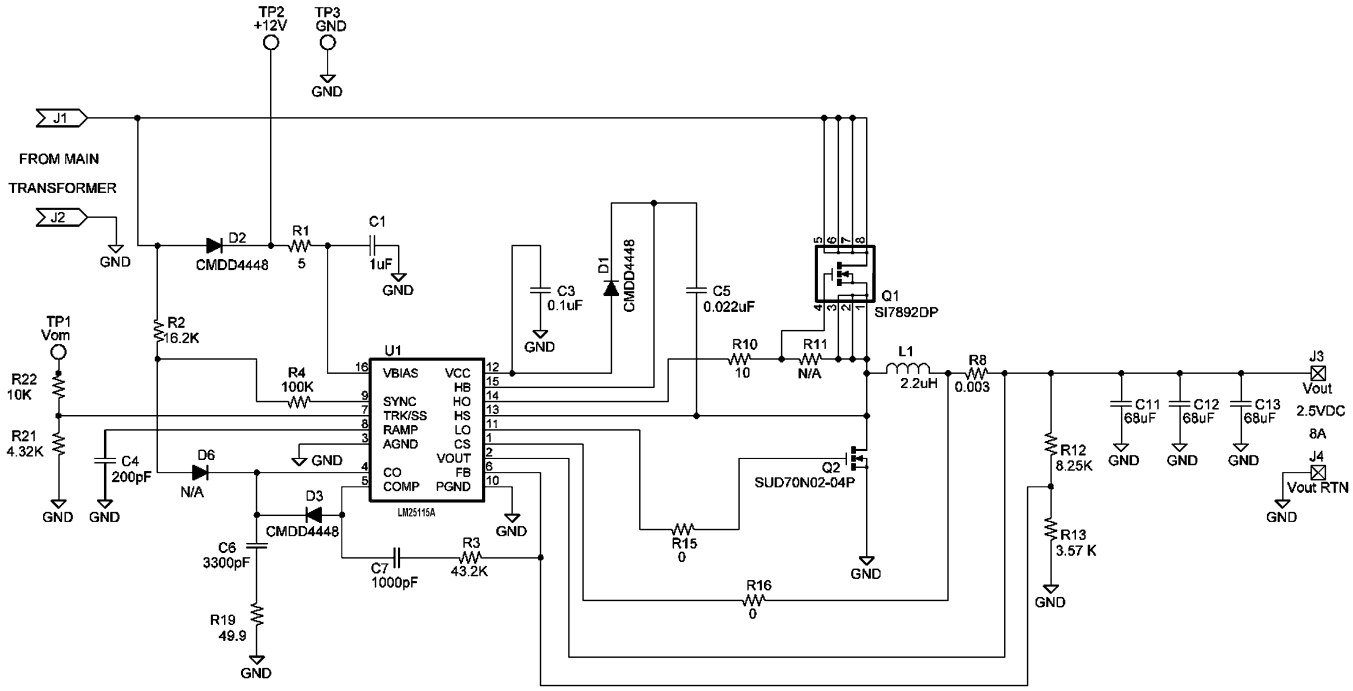
The LM25115A can be configured as a standalone DC/DC synchronous buck controller. In this mode the LM25115A uses leading edge modulation in conjunction with valley current mode control to control the synchronous buck power stage. The internal oscillator within the LM25115A sets the clock frequency for the high and low-side drivers of the external synchronous buck power MOSFETs . The clock frequency in the synchronous buck mode is programmed by the SYNC pin resistor and RAMP pin capacitor. Connecting a resistor between a dc bias supply and the SYNC pin produces a current, I_{SYNC}, which sets the charging current of the RAMP pin capacitor. The RAMP capacitor is charged until its voltage reaches the peak ramp threshold of 2.25V. The RAMP capacitor is then discharged for 300ns before beginning a new PWM cycle. The 300ns reset time of the RAMP pin sets the minimum off-time of the PWM controller in this mode. The internal clock frequency in the synchronous buck mode is set by I_{SYNC}, the ramp capacitor, the peak ramp threshold, and the 300ns deadtime.

$$F_{CLK} \cong 1 / ((C_{RAMP} \times 2.25V) / (I_{SYNC} \times 3) + 300ns)$$

See the LM5115 dc evaluation board application note (AN-1367, literature number SNVA106) for more details on the synchronous buck mode. Please note that LM25115A is similar to LM5115 except for the tracking feature.

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Application Circuit



(Inputs from LM5025 Forward Active Clamp Converter, 36V to 78V)

Figure 25. LM25115A Secondary Side Post Regulator

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REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	19

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25115AMT/NOPB	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25115 AMT
LM25115AMT/NOPB.A	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25115 AMT
LM25115AMT/NOPB.B	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25115 AMT
LM25115AMTX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25115 AMT
LM25115AMTX/NOPB.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25115 AMT
LM25115AMTX/NOPB.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L25115 AMT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

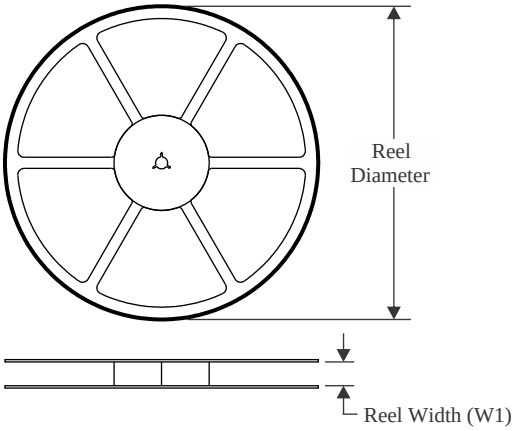
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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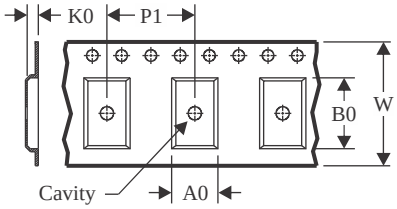
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

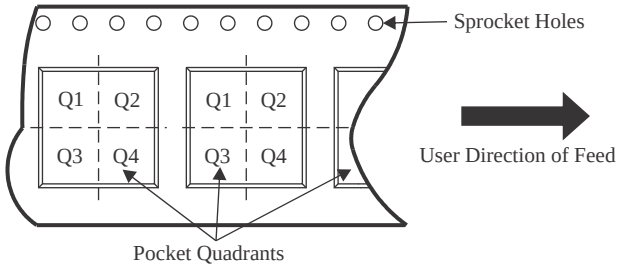


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

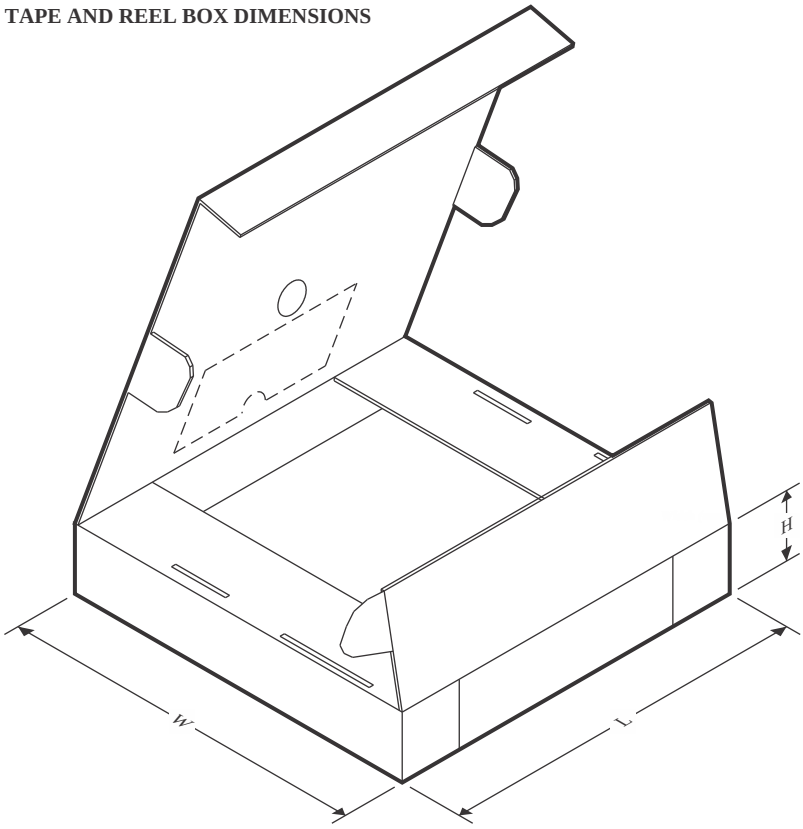
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25115AMTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

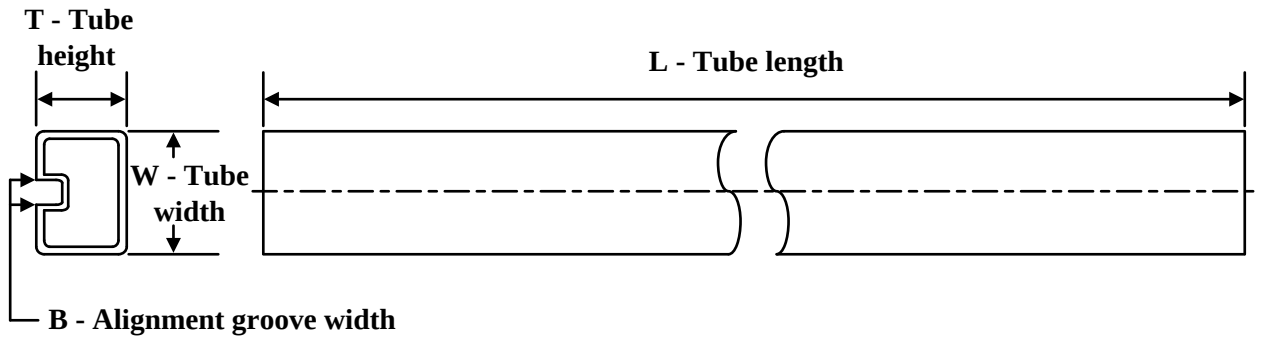
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25115AMTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

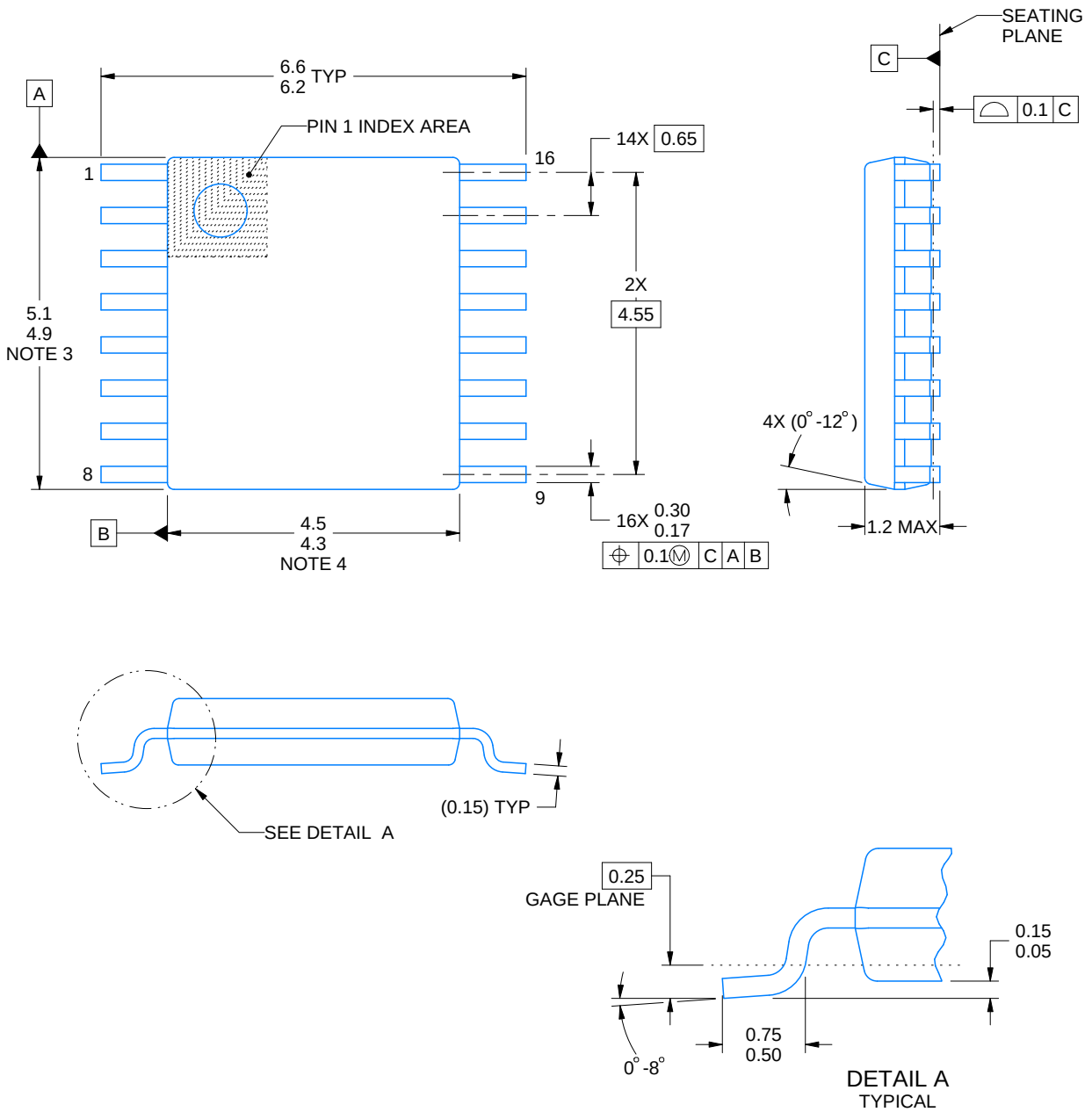
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM25115AMT/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06
LM25115AMT/NOPB.A	PW	TSSOP	16	92	495	8	2514.6	4.06
LM25115AMT/NOPB.B	PW	TSSOP	16	92	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0016A

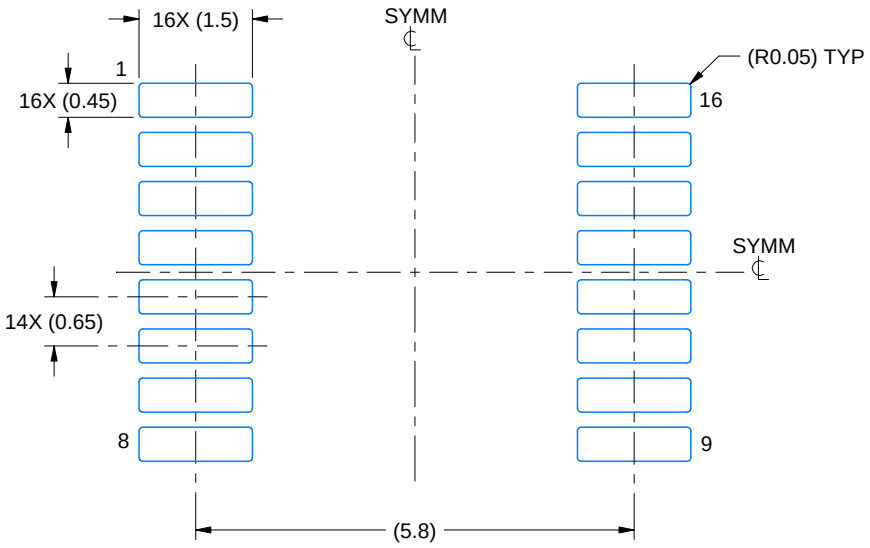
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

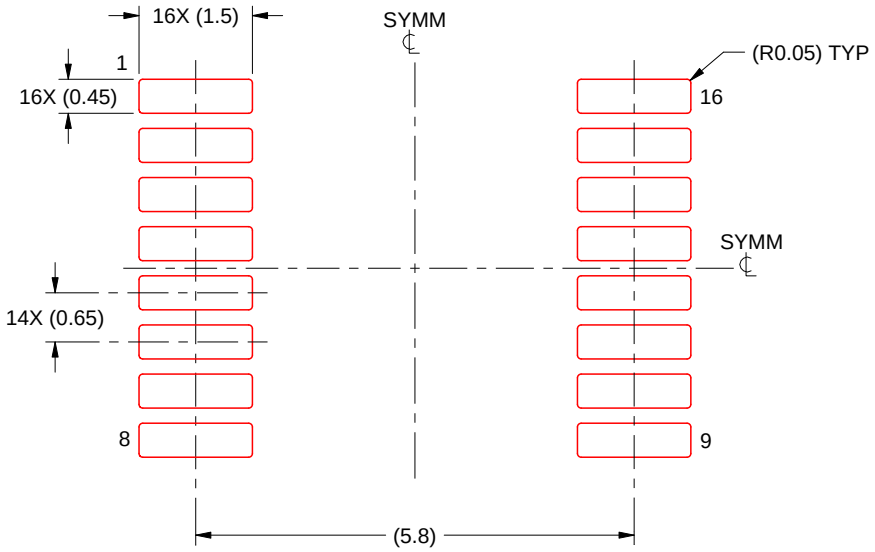


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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