LM193A/LM193QML Low Power Low Offset Voltage Dual Comparators

Check for Samples: LM193A, LM193QML

FEATURES

- **Available with Radiation Guarantee**
  - **Total Ionizing Dose 100 krad(Si)**
  - **ELDRS Free 100 krad(Si)**
- **Wide Supply**
  - **Voltage Range: 2.0V_{DC} to 36V_{DC}**
  - **Single or Dual Supplies: ±1.0V to ±18V**
- **Very Low Supply Current Drain (0.4 mA) — Independent of Supply Voltage**
- **Low Input Biasing Current: 25 nA typ**
- **Low Input Offset Current: ±5 nA typ**
- **Input Common-Mode Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to the Power Supply Voltage**
- **Low Output Saturation Voltage,: 250 mV at 4 mA typ**
- **Output Voltage Compatible with TTL, DTL, ECL, MOS and CMOS Logic Systems**

ADVANTAGES

- **High Precision Comparators**
- **Reduced V_{OS} Drift Over Temperature**
- **Eliminates Need for Dual Supplies**
- **Allows Sensing Near Ground**
- **Compatible with All Forms of Logic**
- **Power Drain Suitable for Battery Operation**

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

Schematic and Connection Diagrams

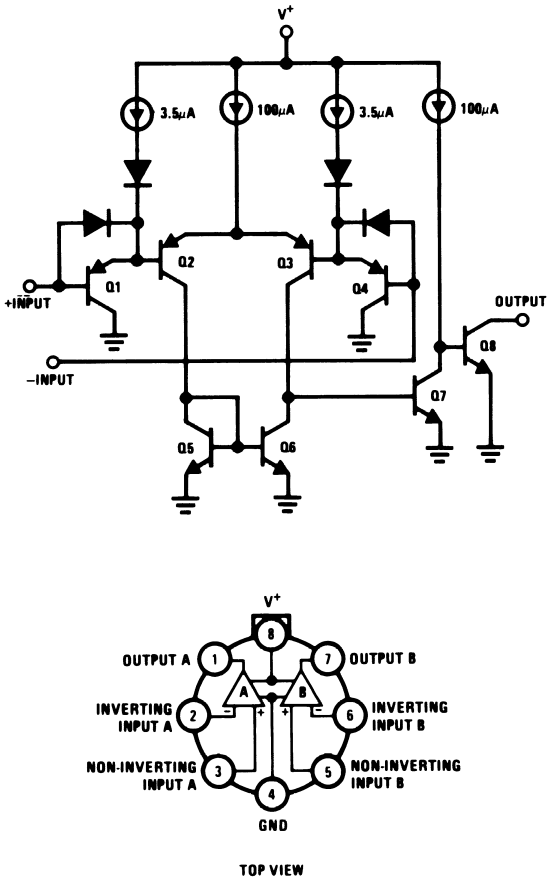


Figure 1. TO-99 Package
See Package Number LMC

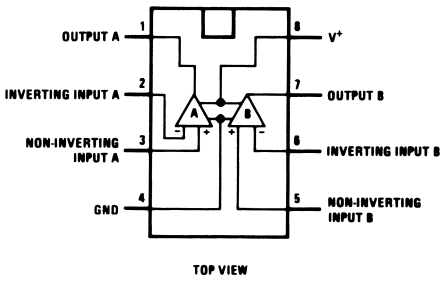


Figure 2. CDIP Package
See Package Number NAB0008A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage, V^+			$36V_{DC}$ or $\pm 18V_{DC}$
Differential Input Voltage(2)			36V
Input Voltage			$-0.3V_{DC}$ to $+36V_{DC}$
Input Current ($V_{IN} < -0.3V_{DC}$)(3)			50 mA
Maximum Junction Temperature			150°C
Power Dissipation(4)(5)		TO-99	660 mW
		CDIP	780 mW
Output Short-Circuit to Ground(6)			Continuous
Operating Temperature Range			$-55°C \le T_A \le +125°C$
Storage Temperature Range			$-65°C \le T_A \le +150°C$
Thermal Resistance	θ_{JA}	TO-99 (Still Air)	174°C/W
		TO-99 (500LF/Min Air flow)	99°C/W
		CDIP (Still Air)	146°C/W
		CDIP (500LF/Min Air flow)	85°C/W
	θ_{JC}	TO-99	44°C/W
		CDIP	33°C/W
Lead Temperature (Soldering, 10 seconds)			260°C
ESD Tolerance(7)			500V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

(3) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$.

(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(5) The LM193A must be derated based on a 150°C, T_{Jmax}. The low bias dissipation and the ON-OFF characteristic of the outputs keep the chip dissipation very small ($P_D \le 100mV$), provided the output transistors are allowed to saturate.

(6) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

(7) Human body model, 1.5KΩ in series with 100pF.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp°C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55

Quality Conformance Inspection (continued)

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp°C
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

LM193 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current				1.0	mA	1, 2, 3
		+V = 36V			2.5	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, $+V_I$ = 1V, V_O = 30V, $-V_I$ = 0V		-0.65	0.65	µA	1
				-1.0	1.0	µA	2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V, $-V_I$ = 1V, $+V_I$ = 0V		6.0		mA	1
V_{Sat}	Output Saturation Voltage	I_{Sink} = 4mA, $-V_I$ = 1V, $+V_I$ = 0V			0.4	V	1
					0.7	V	2, 3
V_{IO}	Input Offset Voltage			-5.0	5.0	mV	1
				-9.0	9.0	mV	2, 3
		+V = 30V		-5.0	5.0	mV	1
				-9.0	9.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V		-5.0	5.0	mV	1
		+V = 30V, V_{CM} = 28.0V		-9.0	9.0	mV	2, 3
$\pm I_{IB}$	Input Bias Current			-100	-1.0	nA	1
				-300	-1.0	nA	2, 3
I_{IO}	Input offset Current	R_S = 50Ω		-25	25	nA	1
				-100	100	nA	2, 3
V_{CM}	Common Mode Voltage	+V = 30V	See (1)		28.5	V	1
			See (1)		28	V	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V, R_S = 50Ω		60		dB	1
CMRR	Common Mode Rejection Ratio	+V = 30V, R_S = 50Ω V_{CM} = 0V to 28.5V,		60		dB	1
V_{Diff}	Differential Input Voltage	+V = 30V, $+V_I$ = 36V, $-V_I$ = 0V	See (2)		500	nA	1, 2, 3
		+V = 30V, $+V_I$ = 0V, $-V_I$ = +36V	See (2)		500	nA	1, 2, 3
A_{VS}	Voltage Gain	+V = 15V, R_{PullUp} = 15KΩ 1V ≤ V_O ≤ 11V,	See (3)	50		V/mV	4

(1) Parameter specified by the V_{IO} tests.
(2) The value for V_{Diff} is not datalogged during Read and Record.
(3) Datalog reading in K = V/mV.

LM193 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified. +V = 5V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	9
		V_{OD} = 50mV			0.8	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	9
		V_{OD} = 50mV			0.8	µS	9

LM193A Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	R_L = Infinity			1.0	mA	1, 2, 3
		+V = 36V, R_L = Infinity			2.5	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, $+V_I$ = 1V, V_O = 30, $-V_I$ = 0		-0.65	0.65	µA	1
				-1.0	1.0	µA	2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V, $-V_I$ = 1V, $+V_I$ = 0V		6.0		mA	1
				4.0		mA	2, 3
V_{Sat}	Output Saturation Voltage	I_{Sink} = 4mA, $-V_I$ = 1V, $+V_I$ = 0V			0.4	V	1
					0.7	V	2, 3
V_{IO}	Input Offset Voltage			-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V		-2.0	2.0	mV	1
		+V = 30V, V_{CM} = 28.0V		-4.0	4.0	mV	2, 3
$\pm I_{IB}$	Input Bias Current	V_O = 1.5V		-100	-1.0	nA	1
				-300	-1.0	nA	2, 3
I_{IO}	Input offset Current	R_S = 50Ω, V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
V_{CM}	Common Mode Voltage	+V = 30V	See (1)		28.5	V	1
			See (1)		28	V	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V, R_S = 50Ω		60		dB	1
CMRR	Common Mode Rejection Ratio	+V = 30V, R_S = 50Ω V_{CM} = 0V to 28.5V,		60		dB	1
V_{Diff}	Differential Input Voltage	+V = 30V, $+V_I$ = 36V, $-V_I$ = 0V	See (2)		500	nA	1, 2, 3
		+V = 30V, $+V_I$ = 0V, $-V_I$ = +36V	See (2)		500	nA	1, 2, 3
A_{VS}	Voltage Gain	+V = 15V, R_{PullUp} = 15KΩ 1V ≤ V_O ≤ 11V,	See (3)	50		V/mV	4
			See (3)	25		V/mV	5, 6

(1) Parameter specified by the V_{IO} tests.
(2) The value for V_{Diff} is not datalogged during Read and Record.
(3) Datalog reading in K = V/mV.

LM193A Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	9
		V_{OD} = 50mV			0.8	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	9
		V_{OD} = 50mV			0.8	µS	9

LM193A Electrical Characteristics DC Drift Parameters

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V
Delta calculations performed on QMLV devices at Group B, Subgroup 5 only

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V = 30V		-1.0	1.0	mV	1
$\pm I_{IB}$	Input Bias Current			-15	15	nA	1

LM193A - 100K Radiation Electrical Characteristics DC Parameters(1)(2)

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	R_L = Infinity			1.0	mA	1, 2, 3
		+V = 36V, R_L = Infinity			2.5	mA	1, 2, 3
I_{CEX}	Output Leakage Current	+V = 30V, $+V_I$ = 1V, V_O = 30, $-V_I$ = 0		-0.65	0.65	µA	1
				-1.0	1.0	µA	2, 3
I_{Sink}	Output Sink Current	V_O = 1.5V, $-V_I$ = 1V, $+V_I$ = 0V		6.0		mA	1
				4.0		mA	2, 3
V_{Sat}	Output Saturation Voltage	I_{Sink} = 4mA, $-V_I$ = 1V, $+V_I$ = 0V			0.4	V	1
					0.7	V	2, 3
V_{IO}	Input Offset Voltage			-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		+V = 30V, V_{CM} = 28.5V		-2.0	2.0	mV	1
		+V = 30V, V_{CM} = 28.0V		-4.0	4.0	mV	2, 3
$\pm I_{IB}$	Input Bias Current	V_O = 1.5V		-100	-1.0	nA	1
				-300	-1.0	nA	2, 3
I_{IO}	Input offset Current	R_S = 50Ω, V_O = 1.5V		-25	25	nA	1
				-100	100	nA	2, 3
V_{CM}	Common Mode Voltage	+V = 30V	See(3)		28.5	V	1
			See(3)		28	V	2, 3
PSRR	Power Supply Rejection Ratio	+V = 5V to 30V, R_S = 50Ω		60		dB	1
CMRR	Common Mode Rejection Ratio	+V = 30V, R_S = 50Ω V_{CM} = 0V to 28.5V,		60		dB	1

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in MIL-STD-883, Method 1019

(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

(3) Parameter specified by the V_{IO} tests.

LM193A - 100K Radiation Electrical Characteristics DC Parameters[1][2] (continued)

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{Diff}	Differential Input Voltage	+V = 30V, $+V_I$ = 36V, $-V_I$ = 0V	See[4]		500	nA	1, 2, 3
		+V = 30V, $+V_I$ = 0V, $-V_I$ = +36V	See[4]		500	nA	1, 2, 3
A_{VS}	Voltage Gain	+V = 15V, R_{PullUp} = 15KΩ 1V ≤ V_O ≤ 11V,	See[3]	50		V/mV	4
			See[5]	25		V/mV	5, 6

(4) The value for V_{Diff} is not datalogged during Read and Record.
(5) Datalog reading in K = V/mV.

LM193A - 100K Radiation Electrical Characteristics AC Parameters[1][2]

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 5mV			5.0	µS	9
		V_{OD} = 50mV			0.8	µS	9
t_{RHL}	Response Time	V_{OD} = 5mV			2.5	µS	9
		V_{OD} = 50mV			0.8	µS	9

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in MIL-STD-883, Method 1019
(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

LM193A - 100K Radiation Electrical Characteristics (Continued) DC Drift Parameters[1][2]

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V
Delta calculations performed on QMLV devices at Group B, Subgroup 5 only

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	+V = 30V		-1.0	1.0	mV	1
$\pm I_{IB}$	Input Bias Current			-15	15	nA	1

(1) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.
(2) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in MIL-STD-883, Method 1019

LM193A - 100K Radiation Electrical Characteristics (Continued) AC Parameters - Post Radiation Limits @ +25°C[1][2]

The following conditions apply, unless otherwise specified. +V = 5V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{RLH}	Response Time	V_{OD} = 50mV			1.0	µS	9

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in MIL-STD-883, Method 1019
(2) Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

Typical Performance Characteristics

Supply Current

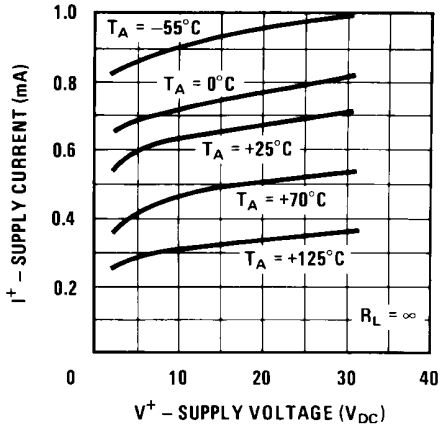


Figure 3.

Input Current

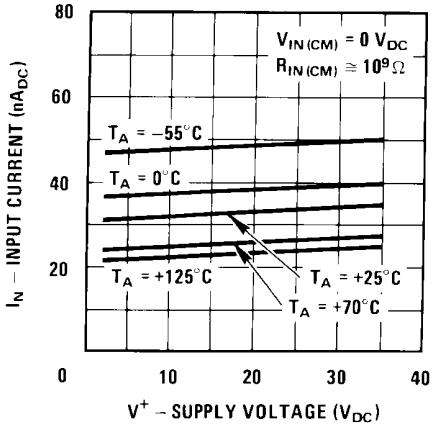


Figure 4.

Output Saturation Voltage

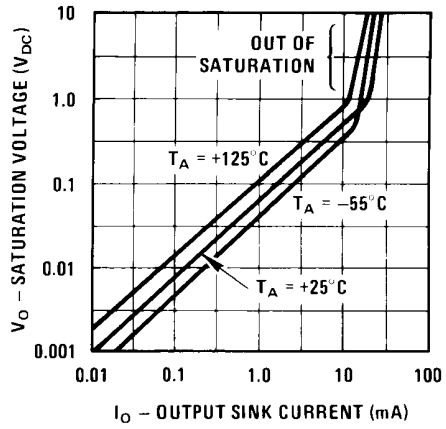


Figure 5.

Response Time for Various Input Overdrives—Negative Transition

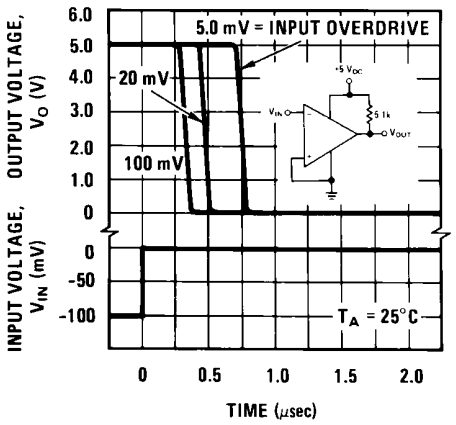


Figure 6.

Response Time for Various Input Overdrives—Positive Transition

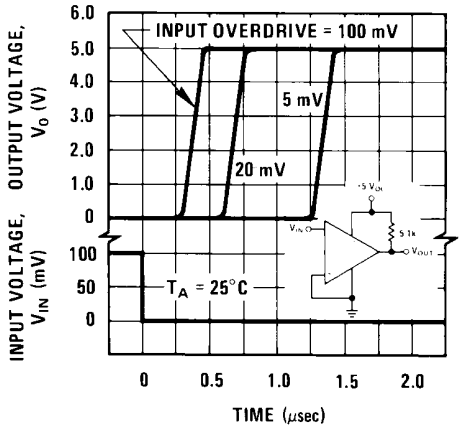


Figure 7.

APPLICATION HINTS

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 KΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All input pins of any unused comparators should be tied to the negative supply.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device (see following note).

NOTE

Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

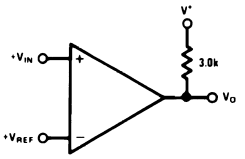
Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0mV) allows the output to clamp essentially to ground level for small load currents.

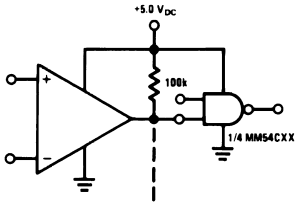
Typical Applications

(V^+=5.0 V_{DC})

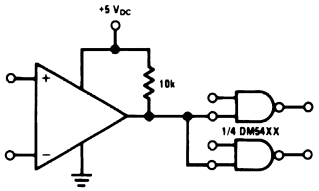
Basic Comparator



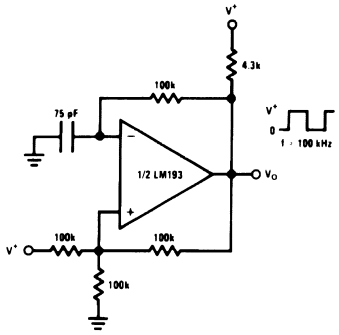
Driving CMOS



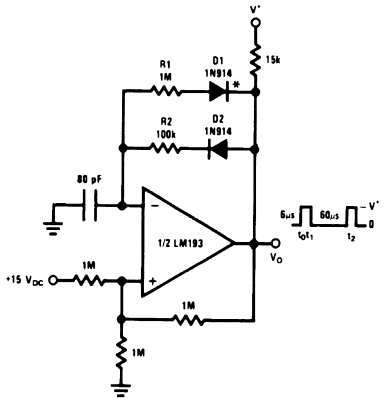
Driving TTL



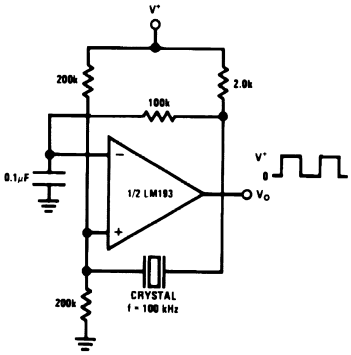
Squarewave Oscillator



Pulse Generator

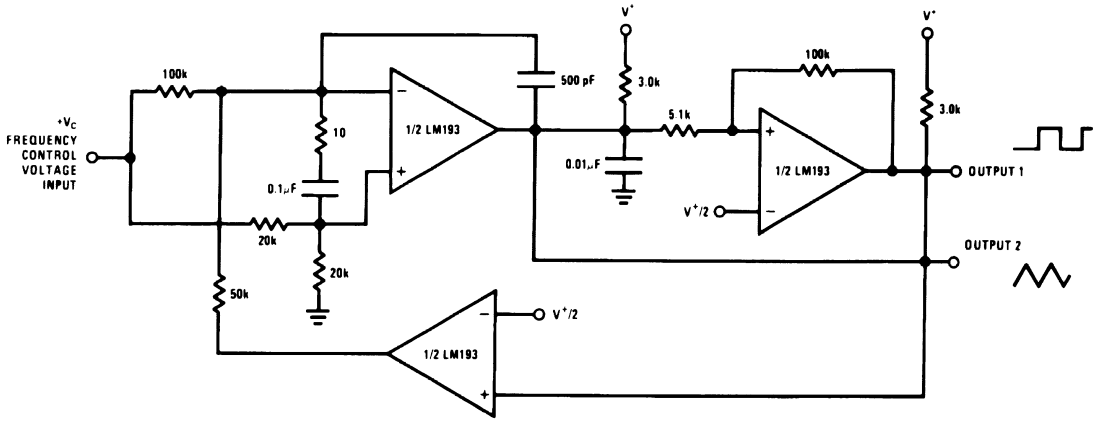


Crystal Controlled Oscillator



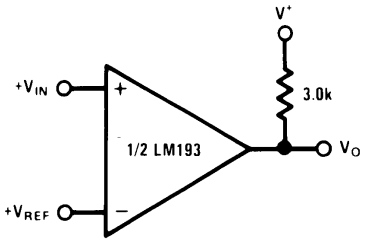
* For large ratios of R1/R2,
D1 can be omitted.

Figure 8. Two-Decade High Frequency VCO

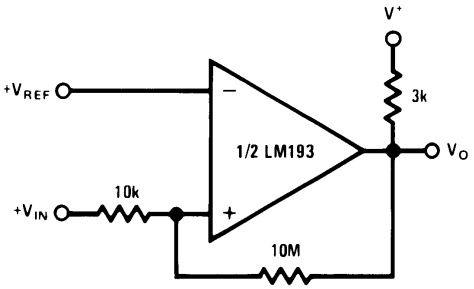


V* = +30 V_{DC}
+250 mV_{DC} ≤ V_C ≤ +50 V_{DC}
700Hz ≤ f_o ≤ 100kHz

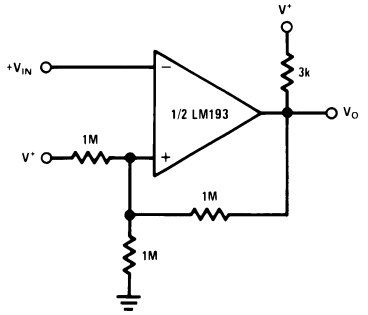
Basic Comparator



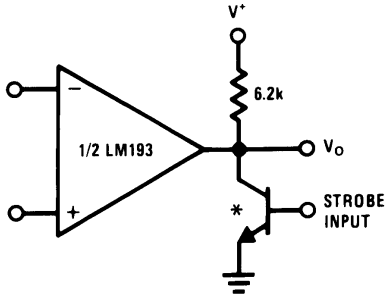
Non-Inverting Comparator with Hysteresis



Inverting Comparator with Hysteresis

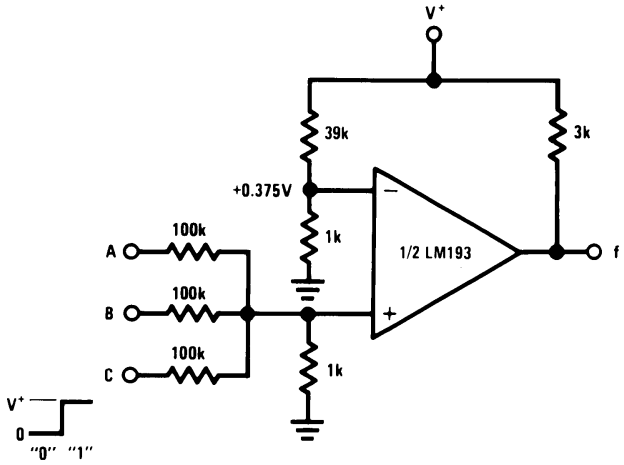


Output Strobing

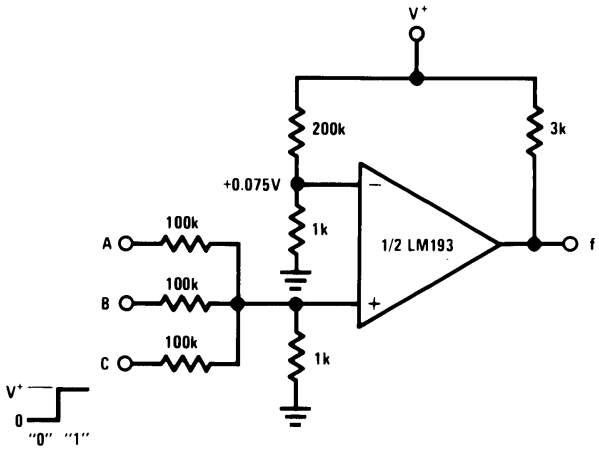


* OR LOGIC GATE
WITHOUT PULL-UP RESISTOR

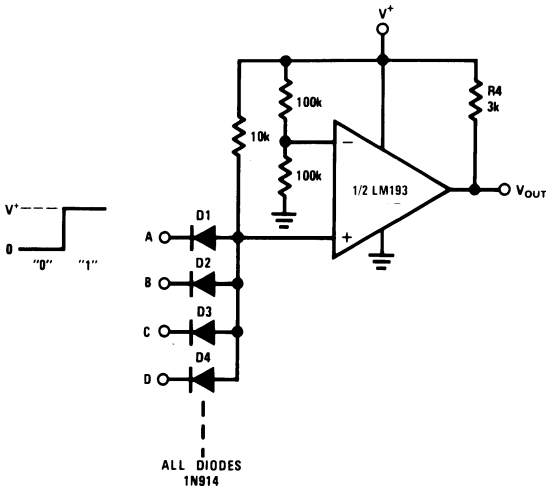
AND Gate



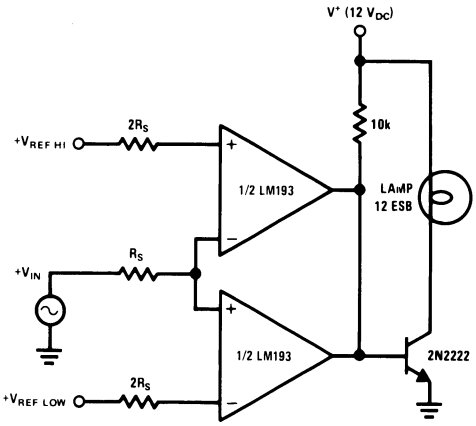
OR Gate



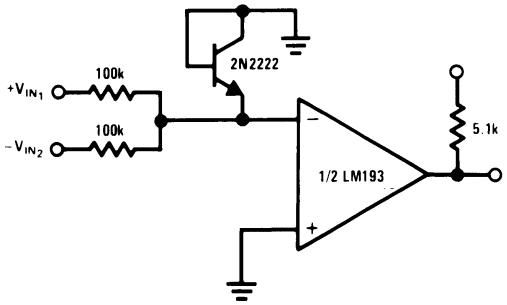
Large Fan-in AND Gate



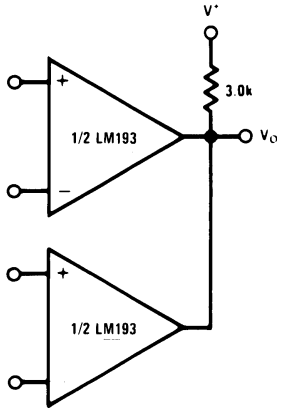
Limit Comparator



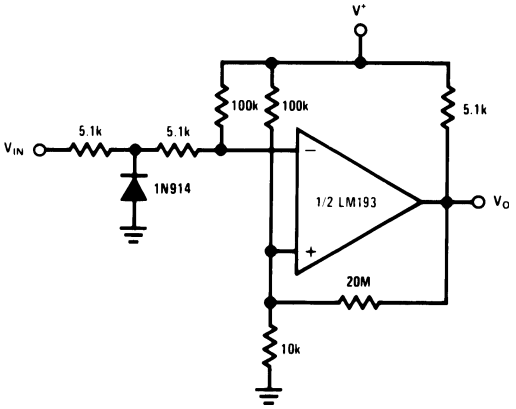
Comparing Input Voltages of Opposite Polarity



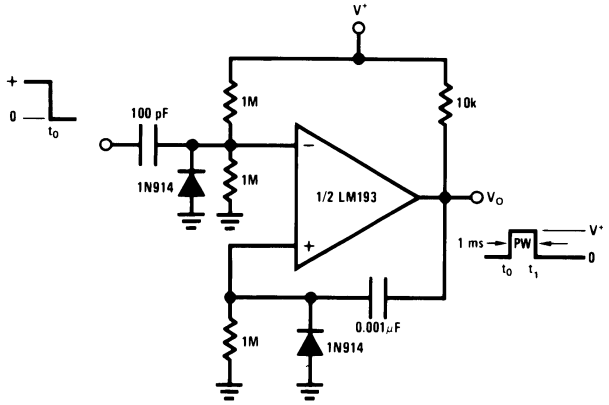
ORing the Outputs



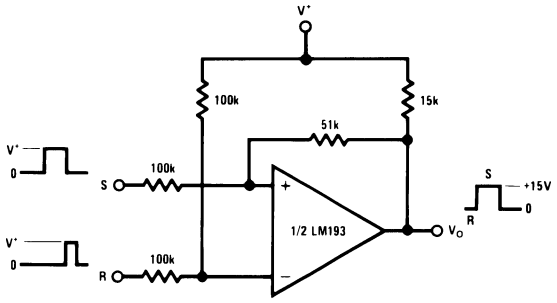
Zero Crossing Detector (Single Power Supply)



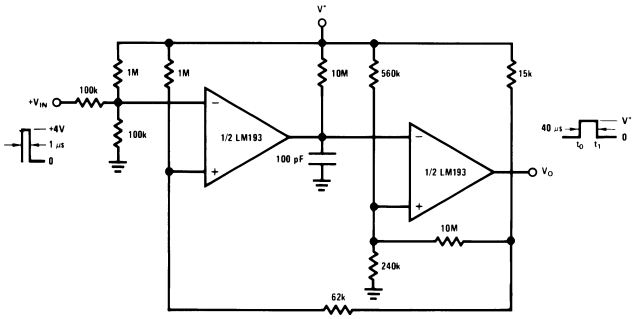
One-Shot Multivibrator



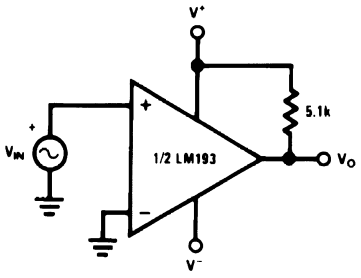
Bi-Stable Multivibrator



One-Shot Multivibrator with Input Lock Out



Zero Crossing Detector



Comparator With a Negative Reference

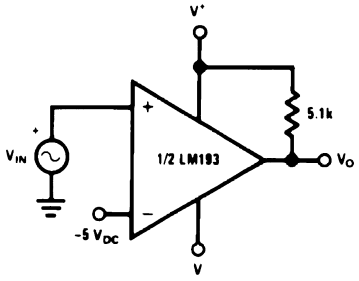
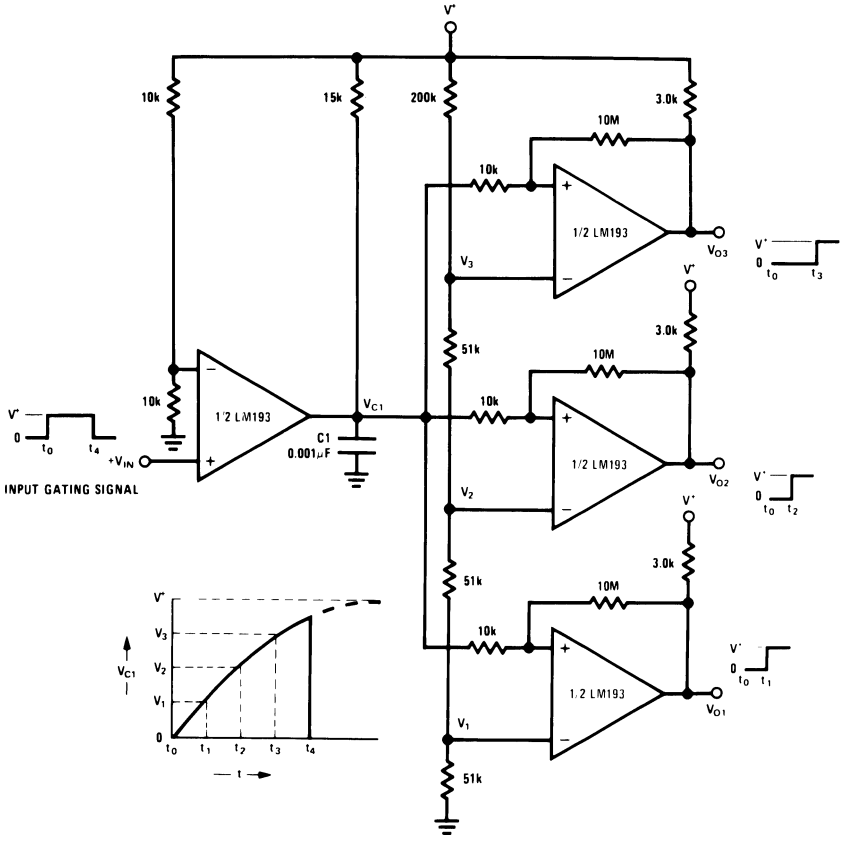


Figure 9. Time Delay Generator



Split-Supply Applications

(V^+=+15 V_{DC} and V^-=−15 V_{DC})

Figure 10. MOS Clock Driver

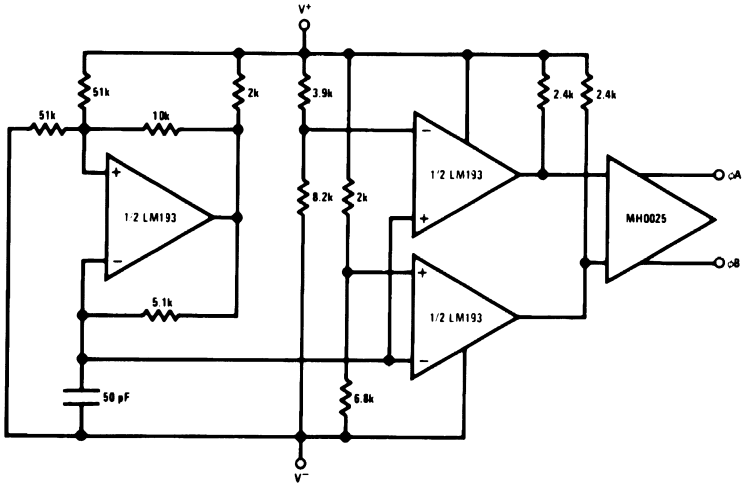


Table 1. Revision History

Date Released	Revision	Section	Originator	Changes
05/09/05	A	New Release. Corporate format	L. Lytle	2 MDS datasheets converted into one Corp. datasheet format. MNLM193A-X Rev 1B3 & MNLM193–X Rev 0E1. The Iout Vsat condition for LM193 was changed to Isink for consistency with the LM193A and JAN electrical conditions. Also, redundant parameters were removed from conditions that were defined at beginning of the table. MDS data sheets will be archived.
05/07/07	B	Features, Ordering Information, LM193A Electricals	Larry McGee	Added Radiation Electrical information for LM193A Device. Revision A will be archived.
10/29/07	C	Features, Ordering Information, Notes	Larry McGee	Added reference to New ELDS NSID and SMD Device 03, ELDRS Note 12. Revision B will be archived.
03/20/13	C	All		Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9452602MGA	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM193AH/883 5962-9452602MGA Q ACO 5962-9452602MGA Q >T
5962-9452602MPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJ/883 5962-94526 02MPA Q ACO 02MPA Q >T
5962-9452602VPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJ-QMLV 5962-94526 02VPA Q ACO 02VPA Q >T
5962R9452602V9A	Active	Production	DIESALE (Y) | 0	40 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
5962R9452602VGA	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM193AHRQMLV 5962R9452602VGA Q ACO 5962R9452602VGA Q >T
5962R9452602VPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJRQMLV 5962R94526 02VPA Q ACO 02VPA Q >T
5962R9452603V9A	Active	Production	DIESALE (Y) | 0	40 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
5962R9452603VGA	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM193AHRLQMLV 5962R9452603VGA Q ACO 5962R9452603VGA Q >T
5962R9452603VPA	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJRLV 5962R94526 03VPA Q ACO 03VPA Q >T
LM193 MD8	Active	Production	DIESALE (Y) | 0	400 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM193 MDE	Active	Production	DIESALE (Y) | 0	40 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM193 MDR	Active	Production	DIESALE (Y) | 0	40 | NOT REQUIRED	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
LM193AH/883	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM193AH/883 5962-9452602MGA Q ACO 5962-9452602MGA Q >T
LM193AHRLQMLV	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM193AHRLQMLV 5962R9452603VGA Q ACO 5962R9452603VGA Q >T
LM193AHRQMLV	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	No	Call TI	Level-1-NA-UNLIM	-55 to 125	LM193AHRQMLV 5962R9452602VGA Q ACO 5962R9452602VGA Q >T
LM193AJ-QMLV	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJ-QMLV 5962-94526 02VPA Q ACO 02VPA Q >T
LM193AJ/883	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJ/883 5962-94526 02MPA Q ACO 02MPA Q >T
LM193AJRLQMLV	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJRLV 5962R94526 03VPA Q ACO 03VPA Q >T
LM193AJRQMLV	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM193AJRQMLV 5962R94526 02VPA Q ACO 02VPA Q >T
LM193H/883	Active	Production	TO-99 (LMC) | 8	20 | JEDEC TRAY (5+1)	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM193H/883 Q ACO LM193H/883 Q >T
LM193J/883	Active	Production	CDIP (NAB) | 8	40 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	LM193J /883 Q ACO /883 Q >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

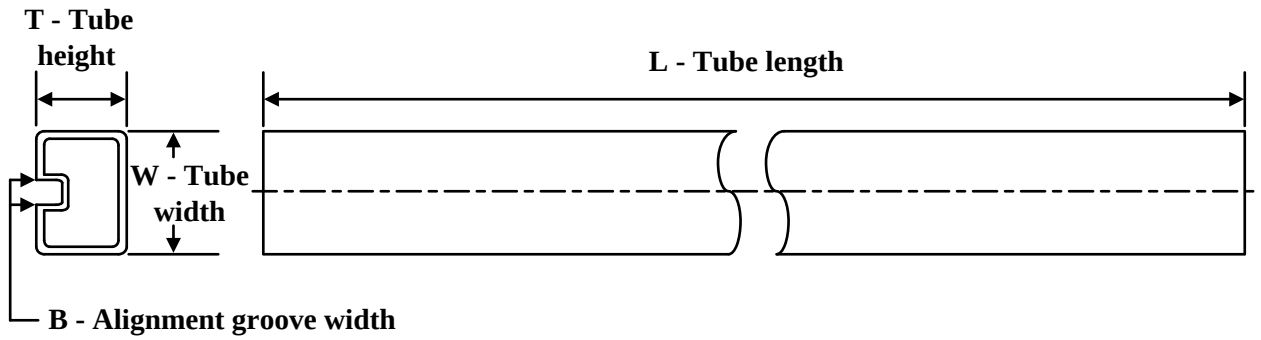
OTHER QUALIFIED VERSIONS OF LM193QML, LM193QML-SP :

- Military : LM193QML
- Space : LM193QML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

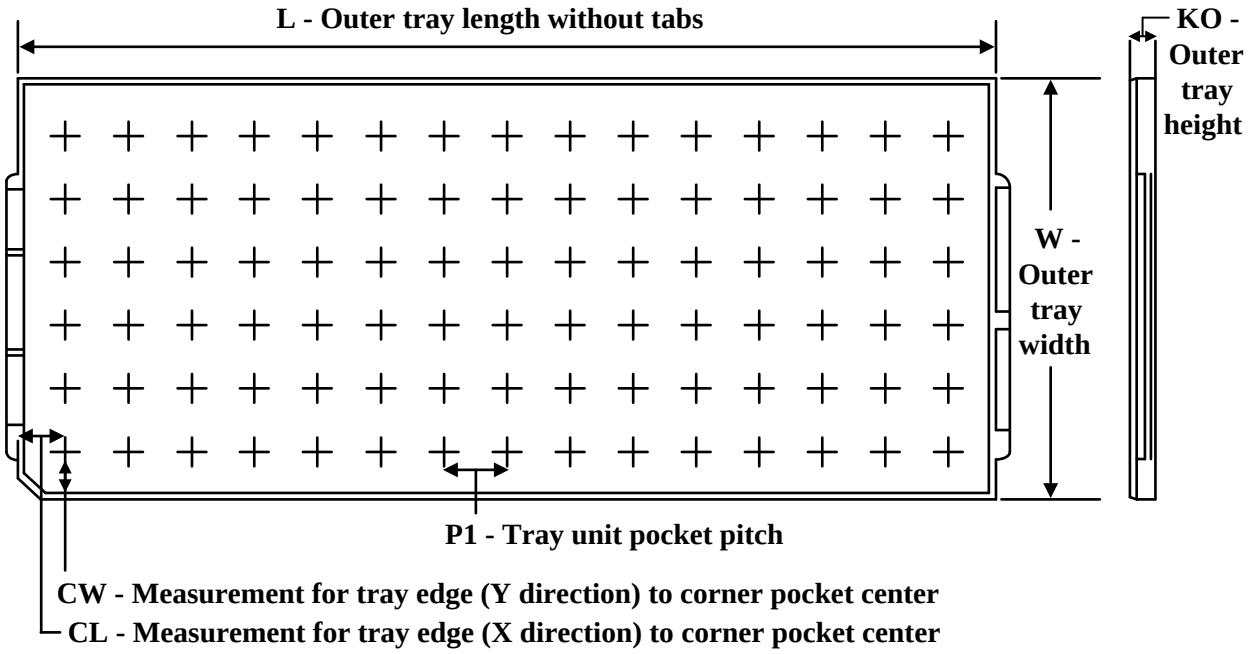
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9452602MPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
5962-9452602VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
5962R9452602VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
5962R9452603VPA	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM193AJ-QMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM193AJ/883	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM193AJRLQMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM193AJRQMLV	NAB	CDIP	8	40	506.98	15.24	13440	NA
LM193J/883	NAB	CDIP	8	40	506.98	15.24	13440	NA

TRAY

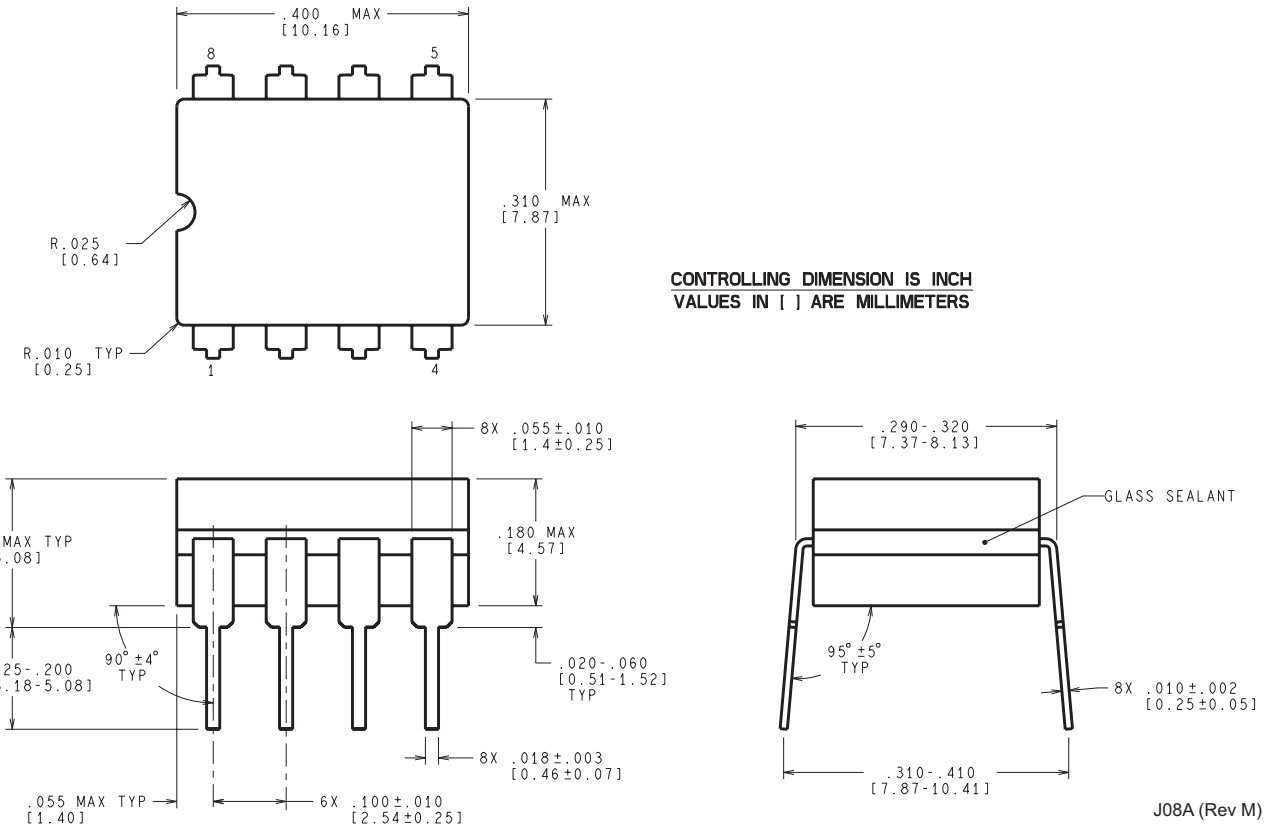


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-9452602MGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
5962R9452602VGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
5962R9452603VGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LM193AH/883	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LM193AHRLQMLV	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LM193AHRQMLV	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
LM193H/883	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

NAB0008A

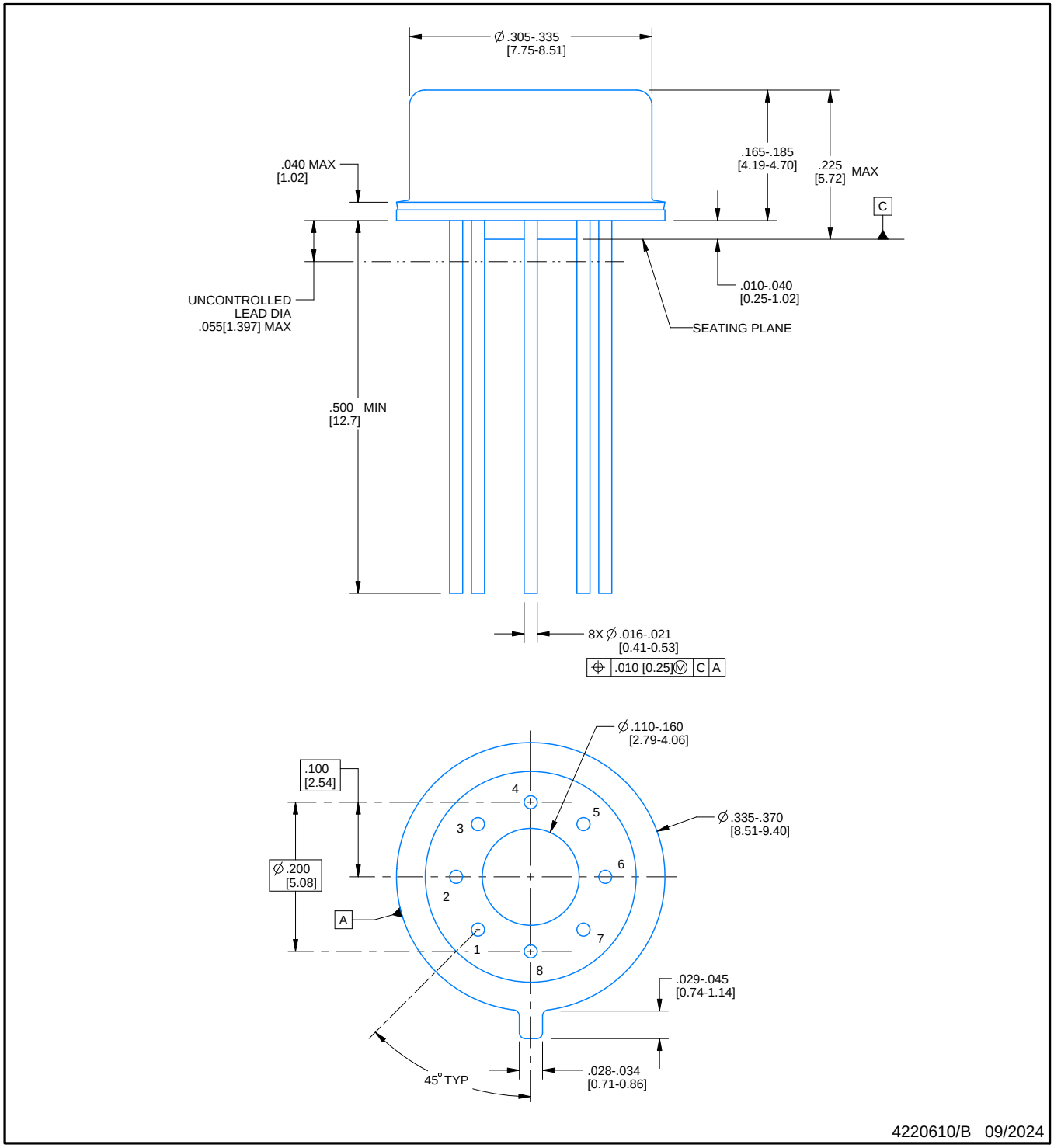

.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

PACKAGE OUTLINE

LMC0008A

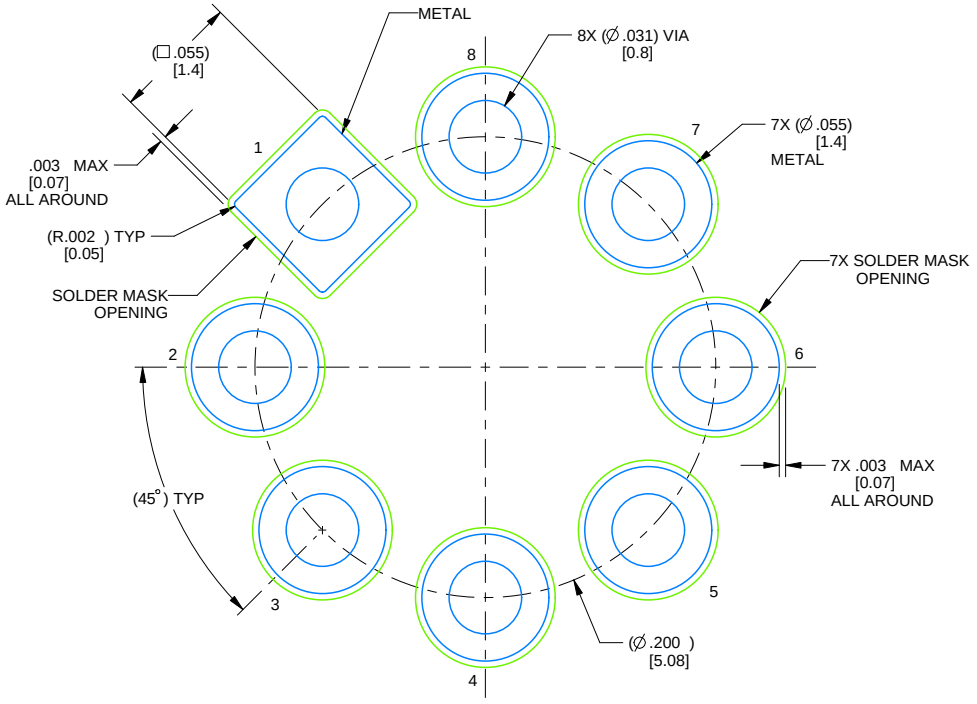
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

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Last updated 10/2025