# LM119QML High Speed Dual Comparator

**Check for Samples: LM119QML**

## FEATURES

- **Available with radiation ensured**
  - **High Dose Rate 100 krad(Si)**
  - **ELDRS Free 100 krad(Si)**
- **Two independent comparators**
- **Operates from a single 5V supply**
- **Typically 80 ns response time at ±15V**
- **Minimum fan-out of 2 each side**
- **Maximum input current of 1 µA over temperature**
- **Inputs and outputs can be isolated from system ground**
- **High common mode slew rate**

## DESCRIPTION

The LM119 is a precision high speed dual comparator fabricated on a single monolithic chip. It is designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, it has higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA.

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 is fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

## Connection Diagrams

**CDIP Package**

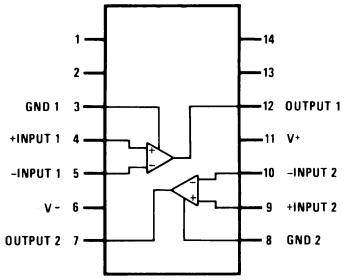



**Figure 1. Top View**
**Package Number J0014A**

**LCCC Package**

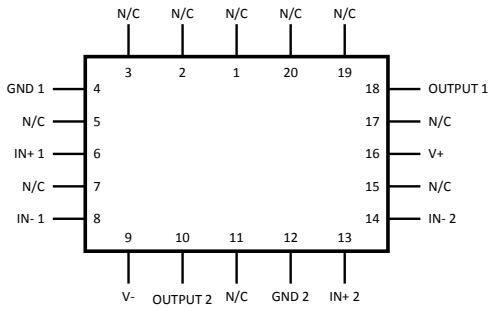
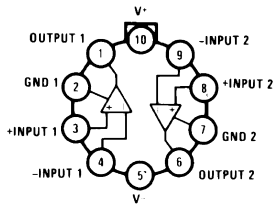



**Figure 2. Top View**
**Package Number NAJ0020A**

**TO-100 Package**




Case is connected to pin 5 ($V^-$).

**Figure 3. Top View**
**Package Number LME0010C**

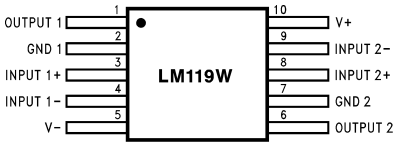



**Figure 4. Top View**
**Package Number NAD0010A, NAC0010A**

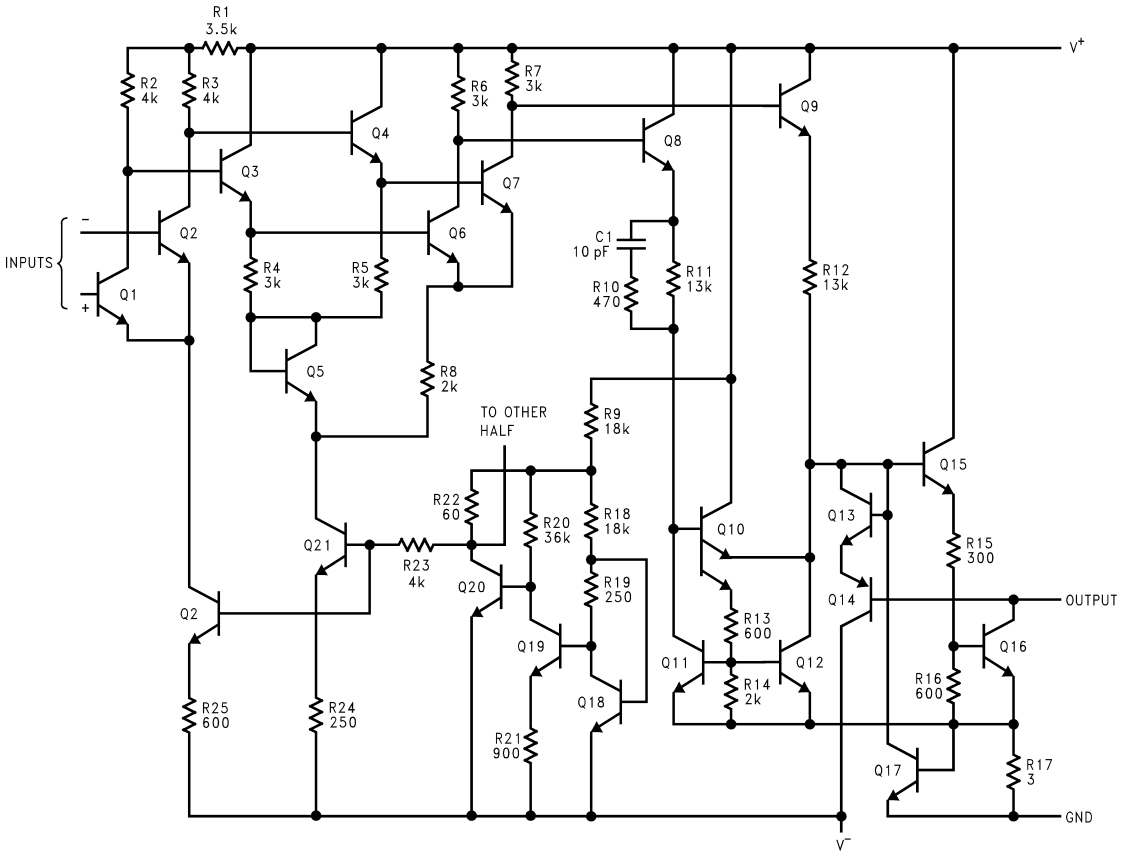
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2008–2013, Texas Instruments Incorporated

## Schematic Diagram




*Do not operate the LM119 with more than 16V between GND and $V^+$

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.


Copyright © 2008–2013, Texas Instruments Incorporated

## Absolute Maximum Ratings (1)

| | |
|---|---|
| Total Supply Voltage | 36V |
| Output to Negative Supply Voltage | 36V |
| Ground to Negative Supply Voltage | 25V |
| Ground to Positive Supply Voltage | 18V |
| Differential Input Voltage | ±5V |
| Input Voltage (2) | ±15V |
| Power Dissipation (3) | 500 mW |
| Output Short Circuit Duration | 10 sec |
| Storage Temperature Range | $-65°C \le T_A \le 150°C$ |
| Operating Ambient Temperature Range | $-55°C \le T_A \le 125°C$ |
| Maximum Junction Temperature ($T_J$) | 150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Thermal Resistance | |
| $\theta_{JA}$ | |
| LCCC Package (Still Air) | 89°C/W |
| LCCC Package (500LF/Min Air flow) | 63°C/W |
| TO-100 Package (Still Air) | 162°C/W |
| TO-100 Package (500LF/Min Air flow) | 88°C/W |
| CDIP Package (Still Air) | 94°C/W |
| CDIP Package (500LF/Min Air flow) | 52°C/W |
| CLGA Package (Still Air) | 215°C/W |
| CLGA Package (500LF/Min Air flow) | 132°C/W |
| CLGA Package (Still Air) | 215°C/W |
| CLGA Package (500LF/Min Air flow) | 132°C/W |
| $\theta_{JC}$ | |
| LCCC Package | 5°C/W |
| TO-100 Package | 31°C/W |
| CDIP Package | 11°C/W |
| CLGA Package | 13°C/W |
| CLGA Package | 13°C/W |
| Package Weight | |
| LCCC Package | TBD |
| TO-100 Package | TBD |
| CDIP Package | TBD |
| CLGA Package | TBD |
| CLGA Package | 225mg |
| ESD rating (4) | 800V |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{Jmax}$ (maximum junction temperature), $\theta_{JA}$ (package junction to ambient thermal resistance), and $T_A$ (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(4) Human Body model, 1.5KΩ in series with 100pF.

Copyright © 2008–2013, Texas Instruments Incorporated

**Table 1. Quality Conformance Inspection(1)**

| Subgroup | Description | Temp °C |
|---|---|---|
| 1 | Static tests at | 25 |
| 2 | Static tests at | 125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | 25 |
| 5 | Dynamic tests at | 125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | 25 |
| 8A | Functional tests at | 125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | 25 |
| 10 | Switching tests at | 125 |
| 11 | Switching tests at | -55 |
| 12 | Settling time at | 25 |
| 13 | Settling time at | 125 |
| 14 | Settling time at | -55 |

(1) Mil-Std-883, Method 5005 - Group 5


Copyright © 2008–2013, Texas Instruments Incorporated

## LM119/883 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. $V_{CM}$ = 0V

| Symbol | Parameter | Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $+I_{CC}$ | Positive Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low<br>$V^+$ = 5.6V thru 1.4KΩ | | | 11 | mA | 1 |
| | | | | | 11.5 | mA | 2 |
| $-I_{CC}$ | Negative Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low<br>$V^+$ = 5.6V thru 1.4KΩ | | -4.2 | | mA | 1 |
| | | | | -4.5 | | mA | 2 |
| $I_{Leak}$ | Output Leakage Current | $^+V_{CC}$ = 15V, $^-V_{CC}$ = -1V,<br>$V_{Gnd}$ = 0V, $V_O$ = 35V,<br>$V_I$ = 5mV | | | 1.8 | µA | 1 |
| | | | | | 9.5 | µA | 2 |
| | | | | | 10.0 | µA | 3 |
| $I_{IB}$ | Input Bias Current | $\pm V_{CC}$ = ±15V | | | 0.475 | µA | 1 |
| | | | | | 0.95 | µA | 2, 3 |
| | | $^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V,<br>$V_{CM}$ = 1.5V | | | 0.475 | µA | 1 |
| | | | | | .95 | µA | 2, 3 |
| $V_{IO}$ | Input Offset Voltage | $^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V,<br>$V_{CM}$ = 1V, $R_S$ ≤ 5KΩ | | -3.8 | 3.8 | mV | 1 |
| | | | | -6.8 | 6.8 | mV | 2, 3 |
| | | $^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V,<br>$V_{CM}$ = 3V, $R_S$ ≤ 5KΩ | | -3.8 | 3.8 | mV | 1 |
| | | | | -6.8 | 6.8 | mV | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = 12V,<br>$R_S$ ≤ 5KΩ | | -3.8 | 3.8 | mV | 1 |
| | | | | -6.8 | 6.8 | mV | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = -12V,<br>$R_S$ ≤ 5KΩ | | -3.8 | 3.8 | mV | 1 |
| | | | | -6.8 | 6.8 | mV | 2, 3 |
| $I_{IO}$ | Input Offset Current | $^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V, $V_{CM}$ = 1V | | -75 | 75 | nA | 1 |
| | | | | -100 | 100 | nA | 2, 3 |
| | | $^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V, $V_{CM}$ = 3V | | -75 | 75 | nA | 1 |
| | | | | -100 | 100 | nA | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = 12V | | -75 | 75 | nA | 1 |
| | | | | -100 | 100 | nA | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = -12V | | -75 | 75 | nA | 1 |
| | | | | -100 | 100 | nA | 2, 3 |
| $V_{Sat}$ | Output Saturation Voltage | $\pm V_{CC}$ = ±15V, $I_O$ = 25mA,<br>$V_I$ = -5mV | | | 1.5 | V | 1 |
| | | $^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V,<br>$I_O$= 4.0mA | (1) | | 0.4 | V | 1, 2 |
| | | | (1) | | 0.6 | V | 3 |
| $A_V$ | Voltage Gain | $\pm V_{CC}$ = ±15V, Delta $V_O$ = 12V,<br>$R_L$ = 1.4KΩ | (2), (3) | 10.5 | | K | 4 |
| | | | (2), (3) | 10 | | K | 5, 6 |
| | | $^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V,<br>Delta $V_O$ = 4.5V, $R_L$ = 1.4KΩ | (2), (4) | 8.0 | | K | 4 |
| | | | (2), (4) | 5.0 | | K | 5 |
| | | | (2), (4) | 5.8 | | K | 6 |

(1) Output is monitored by measuring $V_I$ with limits from 0 to 6mV at all temperatures
(2) K = V/mV.
(3) Gain is computed with an output swing from +13.5V to +1.5V.
(4) Gain is computed with an output swing from +5.0V to +0.5V.

Copyright © 2008–2013, Texas Instruments Incorporated

## LM119-SMD Electrical Characteristics SMD 8601401 DC Parameters

The following conditions apply, unless otherwise specified. $V_{CM}$ = 0V

| Symbol | Parameter | Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $+I_{CC}$ | Positive Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low<br>$V^+$ = 5.6V thru 1.4KΩ | | | 11 | mA | 1 |
| | | | | | 11.5 | mA | 2, 3 |
| $-I_{CC}$ | Negative Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low<br>$V^+$ = 5.6V thru 1.4KΩ | | -4.2 | | mA | 1 |
| | | | | -4.5 | | mA | 2 |
| | | | | -6.0 | | mA | 3 |
| $I_{Leak}$ | Output Leakage Current | $^+V_{CC}$ = 15V, $^-V_{CC}$ = -1V,<br>$V_{Gnd}$ = 0V, $V_O$ = 35V | (1) | | 1.8 | µA | 1 |
| | | | (1) | | 10 | µA | 2, 3 |
| $I_{IB}$ | Input Bias Current | $\pm V_{CC}$ = ±15V | | | 0.475 | µA | 1 |
| | | | | | 0.95 | µA | 2, 3 |
| | | $^+V_{CC}$ = 5V | (2) | | 0.475 | µA | 1 |
| | | | (2) | | .95 | µA | 2, 3 |
| $V_{IO}$ | Input Offset Voltage | $^+V_{CC}$ = 5V, $V_{CM}$ = 1V, $R_S$ ≤ 5KΩ | (2) | -3.8 | 3.8 | mV | 1 |
| | | | (2) | -6.8 | 6.8 | mV | 2, 3 |
| | | $^+V_{CC}$ = 5V, $V_{CM}$ = 3V,<br>$R_S$ ≤ 5KΩ | (2) | -3.8 | 3.8 | mV | 1 |
| | | | (2) | -6.8 | 6.8 | mV | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = 12V,<br>$R_S$ ≤ 5KΩ | | -3.8 | 3.8 | mV | 1 |
| | | | | -6.8 | 6.8 | mV | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = -12V,<br>$R_S$ ≤ 5KΩ | | -3.8 | 3.8 | mV | 1 |
| | | | | -6.8 | 6.8 | mV | 2, 3 |
| $I_{IO}$ | Input Offset Current | $^+V_{CC}$ = 5V, $V_{CM}$ = 1V | (2) | -75 | 75 | nA | 1 |
| | | | (2) | -100 | 100 | nA | 2, 3 |
| | | $^+V_{CC}$ = 5V, $V_{CM}$ = 3V | (2) | -75 | 75 | nA | 1 |
| | | | (2) | -100 | 100 | nA | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = 12V | | -75 | 75 | nA | 1 |
| | | | | -100 | 100 | nA | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = -12V | | -75 | 75 | nA | 1 |
| | | | | -100 | 100 | nA | 2, 3 |
| $V_I$ | Input Voltage Range | $^+V_{CC}$ = 5V | (2), (3) | 1.0 | 3.0 | V | 1, 2, 3 |
| | | $\pm V_{CC}$ = ±15V | (3) | -12 | 12 | V | 1, 2, 3 |
| $V_{Sat}$ | Output Saturation Voltage | $\pm V_{CC}$ = ±15V, $I_O$ = 25mA,<br>$V_I$ ≤ -5mV | (1) | | 1.5 | V | 1, 2, 3 |
| | | $^+V_{CC}$ = 3.5V, $^-V_{CC}$ = -1V,<br>$V_I$ ≤ -6mV, $I_O$ ≤ 3.2mA | | | 0.4 | V | 1, 2 |
| | | | | | 0.6 | V | 3 |
| $A_V$ | Voltage Gain | $\pm V_{CC}$ = ±15V, Delta $V_O$ = 12V,<br>$R_L$ = 1.4KΩ | (4) | 10.5 | | K | 4 |
| | | | (4) | 10 | | K | 5, 6 |
| | | $^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V,<br>Delta $V_O$ = 4.5V, $R_L$ = 1.4KΩ | (2), (4) | 8.0 | | K | 4 |
| | | | (2), (4) | 5.0 | | K | 5 |
| | | | (2), (4) | 5.8 | | K | 6 |
| CMRR | Common Mode Rejection Ratio | $\pm V_{CC}$ = ±15V, $V_{CM}$ = ±12V | | 80 | | dB | 4 |

(1) $V_I$ ≥ 8mV at extremes for $I_{Leak}$ and $V_I$ ≤ −8mV at extremes for $V_{Sat}$ ($V_I$ to exceed $V_{OS}$.
(2) 5V differential across $+V_{CC}$ and $-V_{CC}$.
(3) Parameter ensured by $V_{IO}$ and $I_{IO}$ tests.
(4) K = V/mV.


Copyright © 2008–2013, Texas Instruments Incorporated

## LM119 Electrical Characteristics SMD 5962-9679801, HIGH DOSE RATE DC Parameters

The following conditions apply, unless otherwise specified. $V_{CM}$ = 0V

| Symbol | Parameter | Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $+I_{CC}$ | Positive Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low<br>$V^+$ = 5.6V thru 1.4KΩ | | | 11 | mA | 1 |
| | | | | | 11.5 | mA | 2, 3 |
| $-I_{CC}$ | Negative Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low<br>$V^+$ = 5.6V thru 1.4KΩ | | -4.2 | | mA | 1 |
| | | | | -4.5 | | mA | 2 |
| | | | | -6.0 | | mA | 3 |
| $I_{Leak}$ | Output Leakage Current | $^+V_{CC}$ = 15V, $^-V_{CC}$ = -1V,<br>$V_{Gnd}$ = 0V, $V_O$ = 35V | (1) | | 1.8 | µA | 1 |
| | | | (1) | | 10 | µA | 2, 3 |
| $I_{IB}$ | Input Bias Current | $\pm V_{CC}$ = ±15V | | | 0.475 | µA | 1 |
| | | | | | 0.95 | µA | 2, 3 |
| | | $^+V_{CC}$ = 5V | (2) | | 0.475 | µA | 1 |
| | | | (2) | | .95 | µA | 2, 3 |
| $V_{IO}$ | Input Offset Voltage | $^+V_{CC}$ = 5V, $V_{CM}$ = 1V, $R_S \le 5K\Omega$ | (2) | -3.8 | 3.8 | mV | 1 |
| | | | (2) | -6.8 | 6.8 | mV | 2, 3 |
| | | $^+V_{CC}$ = 5V, $V_{CM}$ = 3V,<br>$R_S \le 5K\Omega$ | (2) | -3.8 | 3.8 | mV | 1 |
| | | | (2) | -6.8 | 6.8 | mV | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = 12V,<br>$R_S \le 5K\Omega$ | | -3.8 | 3.8 | mV | 1 |
| | | | | -6.8 | 6.8 | mV | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = -12V,<br>$R_S \le 5K\Omega$ | | -3.8 | 3.8 | mV | 1 |
| | | | | -6.8 | 6.8 | mV | 2, 3 |
| $I_{IO}$ | Input Offset Current | $^+V_{CC}$ = 5V, $V_{CM}$ = 1V | (2) | -75 | 75 | nA | 1 |
| | | | (2) | -100 | 100 | nA | 2, 3 |
| | | $^+V_{CC}$ = 5V, $V_{CM}$ = 3V | (2) | -75 | 75 | nA | 1 |
| | | | (2) | -100 | 100 | nA | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = 12V | | -75 | 75 | nA | 1 |
| | | | | -100 | 100 | nA | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = -12V | | -75 | 75 | nA | 1 |
| | | | | -100 | 100 | nA | 2, 3 |
| $V_I$ | Input Voltage Range | $^+V_{CC}$ = 5V | (2), (3) | 1.0 | 3.0 | V | 1, 2, 3 |
| | | $\pm V_{CC}$ = ±15V | (3) | -12 | 12 | V | 1, 2, 3 |
| $V_{Sat}$ | Output Saturation Voltage | $\pm V_{CC}$ = ±15V, $I_O$ = 25mA,<br>$V_I \le$ -5mV | (1) | | 1.5 | V | 1, 2, 3 |
| | | $^+V_{CC}$ = 3.5V, $^-V_{CC}$ = -1V,<br>$V_I \le$ -6mV, $I_O \le$ 3.2mA | | | 0.4 | V | 1, 2 |
| | | | | | 0.6 | V | 3 |
| $A_V$ | Voltage Gain | $\pm V_{CC}$ = ±15V, Delta $V_O$ = 12V,<br>$R_L$ = 1.4KΩ | (4) | 10.5 | | K | 4 |
| | | | (4) | 10 | | K | 5, 6 |
| | | $^+V_{CC}$ = 5V, $^-V_{CC}$ = 0V,<br>Delta $V_O$ = 4.5V, $R_L$ = 1.4KΩ | (2), (4) | 8.0 | | K | 4 |
| | | | (2), (4) | 5.0 | | K | 5 |
| | | | (2), (4) | 5.8 | | K | 6 |
| CMRR | Common Mode Rejection Ratio | $\pm V_{CC}$ = ±15V, $V_{CM}$ = ±12V | | 80 | | dB | 4 |

(1) $V_I \ge$ 8mV at extremes for $I_{Leak}$ and $V_I \le$ −8mV at extremes for $V_{Sat}$ ($V_I$ to exceed $V_{OS}$.
(2) 5V differential across $+V_{CC}$ and $-V_{CC}$.
(3) Parameter ensured by $V_{IO}$ and $I_{IO}$ tests.
(4) K = V/mV.

Copyright © 2008–2013, Texas Instruments Incorporated

## SMD 5962-9679801, HIGH DOSE RATE DC DELTA Parameters

The following conditions apply, unless otherwise specified.

$V_{CM}$ = 0V, Delta calculations performed on QMLV devices at group B, subgroup 5 only.

| Symbol | Parameter | Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $+I_{CC}$ | Positive Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low<br>$V^+$ = 5.6V thru 1.4KΩ | | -1.0 | 1.0 | mA | 1 |
| $-I_{CC}$ | Negative Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low<br>$V^+$ = 5.6V thru 1.4KΩ | | -0.5 | 0.5 | mA | 1 |
| $V_{IO}$ | Input Offset Voltage | $^+V_{CC}$ = 5V, $V_{CM}$ = 1V, $R_S \leq$ 5KΩ | | -0.4 | 0.4 | mV | 1 |

## SMD 5962-9679801, High Dose Rate 100K Post Radiation Parameters @ 25°C (1)

The following conditions apply, unless otherwise specified. $V_{CM}$ = 0V

| Symbol | Parameter | Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $I_{IB}$ | Input Bias Current | $\pm V_{CC}$ = ±15V | | | 1.0 | µA | 1 |
| | | $V_{CC}$ = 5V | | | 1.0 | µA | 1 |
| $V_{IO}$ | Input Offset Voltage | $^+V_{CC}$ = 5V, $V_{CM}$ = 1V, $R_S \leq$ 5KΩ | | -4.0 | 4.0 | mV | 1 |
| | | $^+V_{CC}$ = 5V, $V_{CM}$ = 3V, $R_S \leq$ 5KΩ | | -4.0 | 4.0 | mV | 1 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = 12V, $R_S \leq$ 5KΩ | | -4.0 | 4.0 | mV | 1 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = −12V, $R_S \leq$ 5KΩ | | -4.0 | 4.0 | mV | 1 |

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate sensitivity. Radiation end point limits for the noted parameters are ensured only for the conditions as specified in MIL-STD-883, per Test Method 1019, Condition A.

## LM119 Electrical Characteristics SMD 5962-9679802, ELDRS FREE DC Parameters

The following conditions apply, unless otherwise specified. $V_{CM}$ = 0V

| Symbol | Parameter | Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $+I_{CC}$ | Positive Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low<br>$V^+$ = 5.6V thru 1.4KΩ | | | 11 | mA | 1 |
| | | | | | 11.5 | mA | 2, 3 |
| $-I_{CC}$ | Negative Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low<br>$V^+$ = 5.6V thru 1.4KΩ | | -4.2 | | mA | 1 |
| | | | | -4.5 | | mA | 2 |
| | | | | -6.0 | | mA | 3 |
| $I_{Leak}$ | Output Leakage Current | $^+V_{CC}$ = 15V, $^-V_{CC}$ = -1V,<br>$V_{Gnd}$ = 0V, $V_O$ = 35V | (1) | | 1.8 | µA | 1 |
| | | | (1) | | 10 | µA | 2, 3 |
| $I_{IB}$ | Input Bias Current | $\pm V_{CC}$ = ±15V | | | 0.475 | µA | 1 |
| | | | | | 0.95 | µA | 2, 3 |
| | | $^+V_{CC}$ = 5V | (2) | | 0.475 | µA | 1 |
| | | | (2) | | .95 | µA | 2, 3 |

(1) $V_I \geq$ 8mV at extremes for $I_{Leak}$ and $V_I \leq$ −8mV at extremes for $V_{Sat}$ ($V_I$ to exceed $V_{OS}$.

(2) 5V differential across $+V_{CC}$ and $-V_{CC}$.


Copyright © 2008–2013, Texas Instruments Incorporated

## LM119 Electrical Characteristics SMD 5962-9679802, ELDRS FREE DC Parameters (continued)

The following conditions apply, unless otherwise specified. $V_{CM}$ = 0V

| Symbol | Parameter | Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input Offset Voltage | $^{+}V_{CC}$ = 5V, $V_{CM}$ = 1V, $R_S \le 5K\Omega$ | (2) | -3.8 | 3.8 | mV | 1 |
| | | | (2) | -6.8 | 6.8 | mV | 2, 3 |
| | | $^{+}V_{CC}$ = 5V, $V_{CM}$ = 3V, $R_S \le 5K\Omega$ | (2) | -3.8 | 3.8 | mV | 1 |
| | | | (2) | -6.8 | 6.8 | mV | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = 12V, $R_S \le 5K\Omega$ | | -3.8 | 3.8 | mV | 1 |
| | | | | -6.8 | 6.8 | mV | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = -12V, $R_S \le 5K\Omega$ | | -3.8 | 3.8 | mV | 1 |
| | | | | -6.8 | 6.8 | mV | 2, 3 |
| $I_{IO}$ | Input Offset Current | $^{+}V_{CC}$ = 5V, $V_{CM}$ = 1V | (2) | -75 | 75 | nA | 1 |
| | | | (2) | -100 | 100 | nA | 2, 3 |
| | | $^{+}V_{CC}$ = 5V, $V_{CM}$ = 3V | (2) | -75 | 75 | nA | 1 |
| | | | (2) | -100 | 100 | nA | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = 12V | | -75 | 75 | nA | 1 |
| | | | | -100 | 100 | nA | 2, 3 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = -12V | | -75 | 75 | nA | 1 |
| | | | | -100 | 100 | nA | 2, 3 |
| $V_I$ | Input Voltage Range | $^{+}V_{CC}$ = 5V | (3), (3) | 1.0 | 3.0 | V | 1, 2, 3 |
| | | $\pm V_{CC}$ = ±15V | (3) | -12 | 12 | V | 1, 2, 3 |
| $V_{Sat}$ | Output Saturation Voltage | $\pm V_{CC}$ = ±15V, $I_O$ = 25mA, $V_I \le$ -5mV | (1) | | 1.5 | V | 1, 2, 3 |
| | | $^{+}V_{CC}$ = 3.5V, $^{-}V_{CC}$ = -1V, $V_I \le$ -6mV, $I_O \le$ 3.2mA | | | 0.4 | V | 1, 2 |
| | | | | | 0.6 | V | 3 |
| $A_V$ | Voltage Gain | $\pm V_{CC}$ = ±15V, Delta $V_O$ = 12V, $R_L$ = 1.4KΩ | (4) | 10.5 | | K | 4 |
| | | | (4) | 10 | | K | 5, 6 |
| | | $^{+}V_{CC}$ = 5V, $^{-}V_{CC}$ = 0V, Delta $V_O$ = 4.5V, $R_L$ = 1.4KΩ | (5), (4) | 8.0 | | K | 4 |
| | | | (5), (4) | 5.0 | | K | 5 |
| | | | (5), (4) | 5.8 | | K | 6 |
| CMRR | Common Mode Rejection Ratio | $\pm V_{CC}$ = ±15V, $V_{CM}$ = ±12V | | 80 | | dB | 4 |

(3) Parameter ensured by $V_{IO}$ and $I_{IO}$ tests.
(4) K = V/mV.
(5) 5V differential across $+V_{CC}$ and $-V_{CC}$.

## SMD 5962-9679802, ELDRS FREE DC DELTA Parameters

The following conditions apply, unless otherwise specified.
$V_{CM}$ = 0V, Delta calculations performed on QMLV devices at group B, subgroup 5 only.

| Symbol | Parameter | Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $+I_{CC}$ | Positive Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low $V^+$ = 5.6V thru 1.4KΩ | | -1.0 | 1.0 | mA | 1 |
| $-I_{CC}$ | Negative Supply Current | $\pm V_{CC}$ = ±15V, $V_O$ = Low $V^+$ = 5.6V thru 1.4KΩ | | -0.5 | 0.5 | mA | 1 |
| $V_{IO}$ | Input Offset Voltage | $^{+}V_{CC}$ = 5V, $V_{CM}$ = 1V, $R_S \le 5K\Omega$ | | -0.4 | 0.4 | mV | 1 |

Copyright © 2008–2013, Texas Instruments Incorporated

## SMD 5962-9679802, ELDRS FREE 100K Post Radiation Parameters @ 25°C (1)

The following conditions apply, unless otherwise specified. $V_{CM}$ = 0V

| Symbol | Parameter | Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $I_{IB}$ | Input Bias Current | $\pm V_{CC}$ = ±15V | | | 1.0 | µA | 1 |
| | | $V_{CC}$ = 5V | | | 1.0 | µA | 1 |
| $V_{IO}$ | Input Offset Voltage | $^{+}V_{CC}$ = 5V, $V_{CM}$ = 1V, $R_S \leq 5K\Omega$ | | -4.0 | 4.0 | mV | 1 |
| | | $^{+}V_{CC}$ = 5V, $V_{CM}$ = 3V, $R_S \leq 5K\Omega$ | | -4.0 | 4.0 | mV | 1 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = 12V, $R_S \leq 5K\Omega$ | | -4.0 | 4.0 | mV | 1 |
| | | $\pm V_{CC}$ = ±15V, $V_{CM}$ = −12V, $R_S \leq 5K\Omega$ | | -4.0 | 4.0 | mV | 1 |

(1) Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. Low dose rate testing has been performed on a wafer-by-wafer basis, per Test Method 1019, Condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS).


Copyright © 2008–2013, Texas Instruments Incorporated

## Typical Performance Characteristics

**Input Currents**

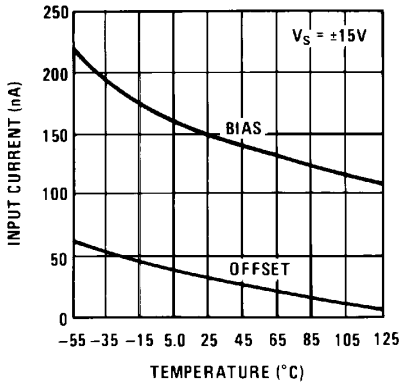



Figure 5.

**Common Mode Limits**

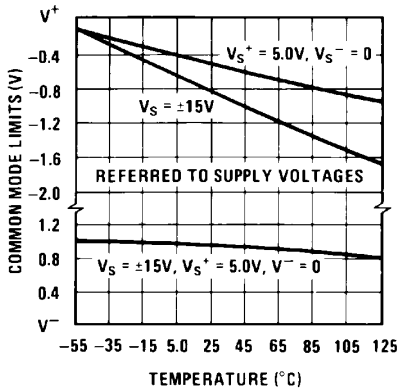



Figure 6.

**Transfer Function**

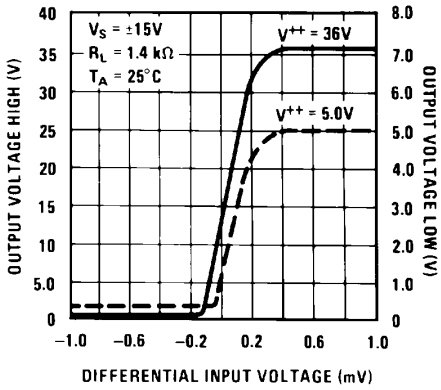



Figure 7.

**Response Time for Various Input Overdrives**

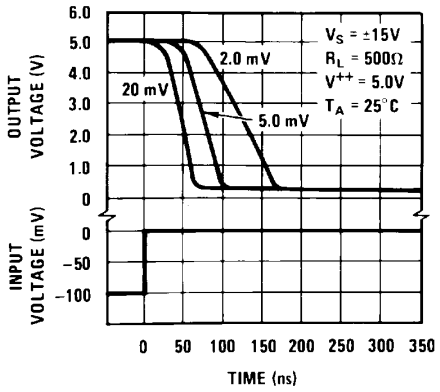



Figure 8.

**Response Time for Various Input Overdrives**

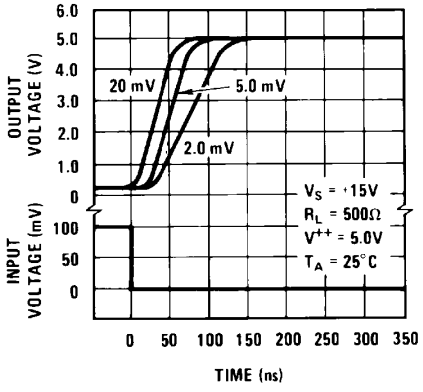



Figure 9.

**Input Characteristics**

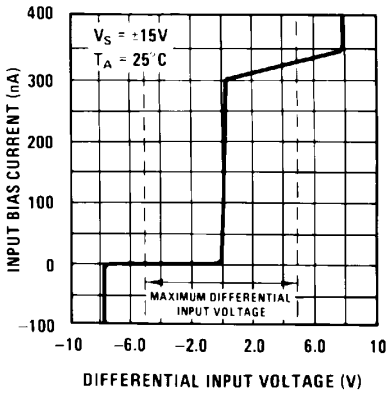



Figure 10.

Copyright © 2008–2013, Texas Instruments Incorporated

## Typical Performance Characteristics (continued)

**Response Time for Various Input Overdrives**

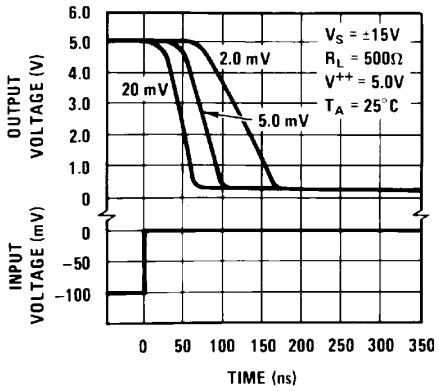



Figure 11.

**Response Time for Various Input Overdrives**

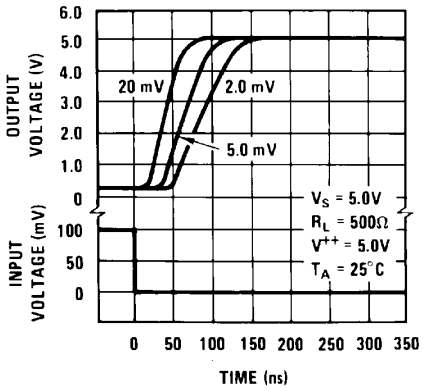



Figure 12.

**Output Saturation Voltage**

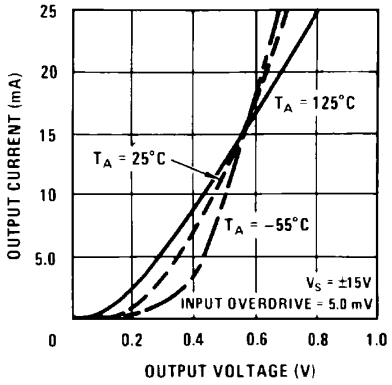



Figure 13.

**Supply Current**

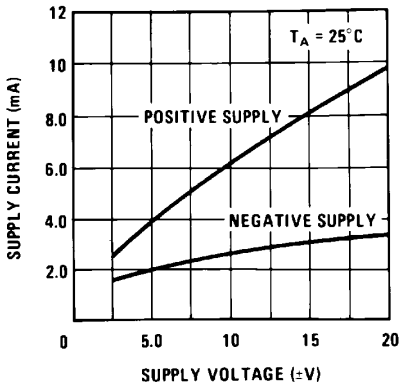



Figure 14.

**Supply Current**

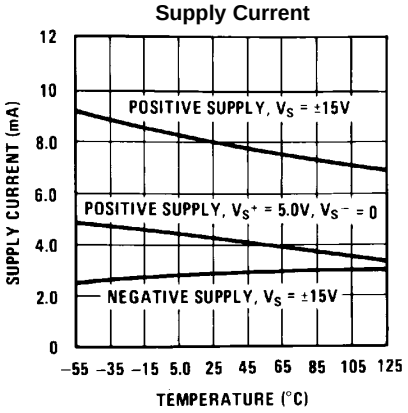



Figure 15.

**Output Limiting Characteristics**

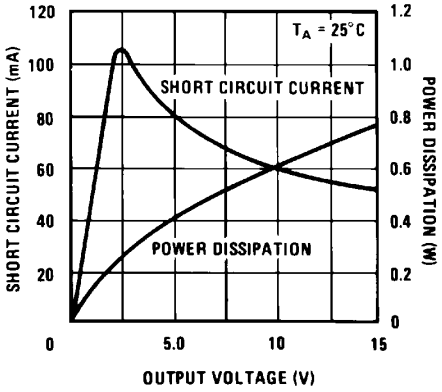
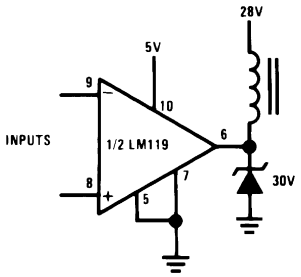



Figure 16.


Copyright © 2008–2013, Texas Instruments Incorporated

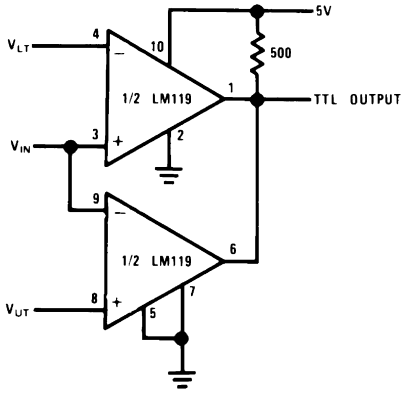
## TYPICAL APPLICATIONS

**Relay Driver**




Pin numbers are for LME0010C package.

**Window Detector**




$V_{OUT}$ = 5V for $V_{LT} \le V_{IN} \le V_{UT}$
$V_{OUT}$ = 0 for $V_{IN} \le V_{LT}$or $V_{IN} \ge V_{UT}$

## REVISION HISTORY

| Date Released | Revision | Section | Originator | Changes |
|---|---|---|---|---|
| 07/24/08 | A | New release to corporate format | L. Lytle | 2 MDS datasheets converted into one corporate data sheet format. Added Radiation information. MDS data sheets MNLM119-X Rev. 0F1 & MDLM119-X Rev 2A2 will be archived. |
| 01/13/09 | B | Features, Ordering Info., Electrical Section, Notes 13 and 14 | Larry McGee | Added reference to ELDRS and Die NSID's to data sheet. Correction from: 100k rd(Si) to 100 krad(Si) in ordering info. Changed wording in Notes 13 and 14 Revision A will be Archived. |
| 03/26/2013 | B | All Sections | | Changed layout of National Data Sheet to TI format |


Copyright © 2008–2013, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9679801VCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119J-QMLV 5962-9679801VCA Q |
| 5962R9679801V9A | Active | Production | DIESALE (Y) \| 0 | 32 \| NOT REQUIRED | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | |
| 5962R9679801VCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119JRQMLV 5962R9679801VCA Q |
| 5962R9679801VHA | Active | Production | CFP (NAD) \| 10 | 19 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119W RQMLV Q 5962R96798 01VHA ACO 01VHA >T |
| 5962R9679801VIA | Active | Production | TO-100 (LME) \| 10 | 20 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | LM119HRQMLV 5962R9679801VIA Q ACO 5962R9679801VIA Q >T |
| 5962R9679801VXA | Active | Production | CFP (NAC) \| 10 | 124 \| JEDEC TRAY (5+1) | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119WG RQMLV Q 5962R96798 01VXA ACO 01VXA >T |
| 5962R9679802V9A | Active | Production | DIESALE (Y) \| 0 | 32 \| NOT REQUIRED | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | |
| 5962R9679802VCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119JRLQMLV 5962R9679802VCA Q |
| 5962R9679802VHA | Active | Production | CFP (NAD) \| 10 | 19 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119W RLQMLV Q 5962R96798 02VHA ACO (LM111W, LM119W) 02VHA >T |
| 5962R9679802VIA | Active | Production | TO-100 (LME) \| 10 | 20 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | LM119HRLQMLV 5962R9679802VIA Q ACO 5962R9679802VIA Q >T |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962R9679802VXA | Active | Production | CFP (NAC) \| 10 | 124 \| JEDEC TRAY (5+1) | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119WG RLQMLV Q 5962R96798 02VXA ACO 02VXA >T |
| 86014012A | Active | Production | LCCC (NAJ) \| 20 | 50 \| TUBE | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | LM119E -SMD Q 5962-86014 012A ACO 012A >T |
| 8601401CA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119J-SMD 5962-8601401CA Q |
| 8601401HA | Active | Production | CFP (NAD) \| 10 | 19 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119W -SMD Q 5962-86014 01HA ACO 01HA >T |
| 8601401IA | Active | Production | TO-100 (LME) \| 10 | 20 \| TRAY NON-STD | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | LM119H-SMD 5962-8601401IA Q A CO 5962-8601401IA Q > T |
| LM119 MD8 | Active | Production | DIESALE (Y) \| 0 | 192 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | |
| LM119 MDE | Active | Production | DIESALE (Y) \| 0 | 32 \| NOT REQUIRED | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | |
| LM119 MDR | Active | Production | DIESALE (Y) \| 0 | 32 \| NOT REQUIRED | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | |
| LM119E-SMD | Active | Production | LCCC (NAJ) \| 20 | 50 \| TUBE | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | LM119E -SMD Q 5962-86014 012A ACO 012A >T |
| LM119E/883 | Active | Production | LCCC (NAJ) \| 20 | 50 \| TUBE | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | LM119E /883 Q ACO /883 Q >T |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM119H-SMD | Active | Production | TO-100 (LME) \| 10 | 20 \| TRAY NON-STD | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | LM119H-SMD 5962-8601401IA Q A CO 5962-8601401IA Q > T |
| LM119H/883 | Active | Production | TO-100 (LME) \| 10 | 20 \| TRAY NON-STD | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | LM119H/883 Q ACO LM119H/883 Q >T |
| LM119HRLQMLV | Active | Production | TO-100 (LME) \| 10 | 20 \| JEDEC TRAY (5+1) | Yes | Call TI | Level-1-NA-UNLIM | -55 to 125 | LM119HRLQMLV 5962R9679802VIA Q ACO 5962R9679802VIA Q >T |
| LM119HRQMLV | Active | Production | TO-100 (LME) \| 10 | 20 \| JEDEC TRAY (5+1) | No | Call TI | Level-1-NA-UNLIM | -55 to 125 | LM119HRQMLV 5962R9679801VIA Q ACO 5962R9679801VIA Q >T |
| LM119J-QMLV | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119J-QMLV 5962-9679801VCA Q |
| LM119J-SMD | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119J-SMD 5962-8601401CA Q |
| LM119J/883 | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119J/883 Q |
| LM119JRLQMLV | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119JRLQMLV 5962R9679802VCA Q |
| LM119JRQMLV | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119JRQMLV 5962R9679801VCA Q |
| LM119W-SMD | Active | Production | CFP (NAD) \| 10 | 19 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119W -SMD Q 5962-86014 01HA ACO 01HA >T |
| LM119W/883 | Active | Production | CFP (NAD) \| 10 | 19 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119W /883 Q ACO /883 Q >T |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM119WGRLQMLV | Active | Production | CFP (NAC) \| 10 | 124 \| JEDEC TRAY (5+1) | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119WG RLQMLV Q 5962R96798 02VXA ACO 02VXA >T |
| LM119WGRQMLV | Active | Production | CFP (NAC) \| 10 | 124 \| JEDEC TRAY (5+1) | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119WG RQMLV Q 5962R96798 01VXA ACO 01VXA >T |
| LM119WRLQMLV | Active | Production | CFP (NAD) \| 10 | 19 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119W RLQMLV Q 5962R96798 02VHA ACO (LM111W, LM119W) 02VHA >T |
| LM119WRQMLV | Active | Production | CFP (NAD) \| 10 | 19 \| TUBE | No | SNPB | Level-1-NA-UNLIM | -55 to 125 | LM119W RQMLV Q 5962R96798 01VHA ACO 01VHA >T |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

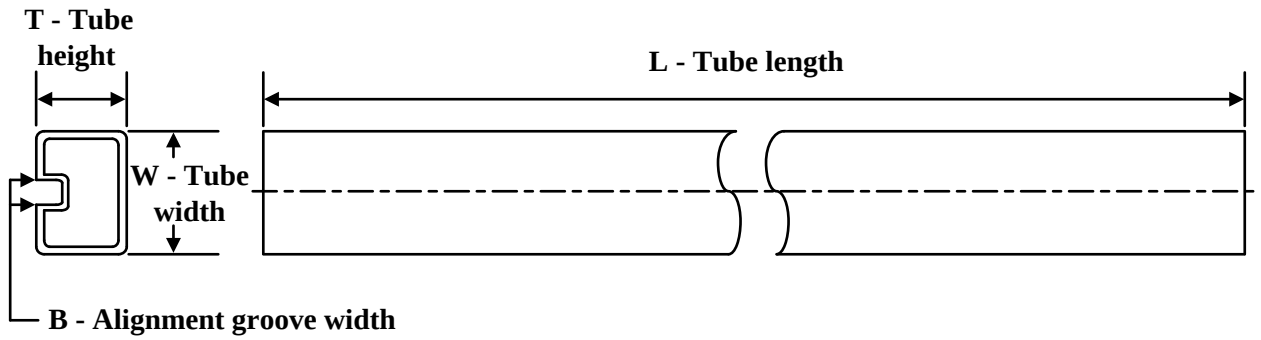
**OTHER QUALIFIED VERSIONS OF LM119QML, LM119QML-SP :**

- Military : LM119QML
- Space : LM119QML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

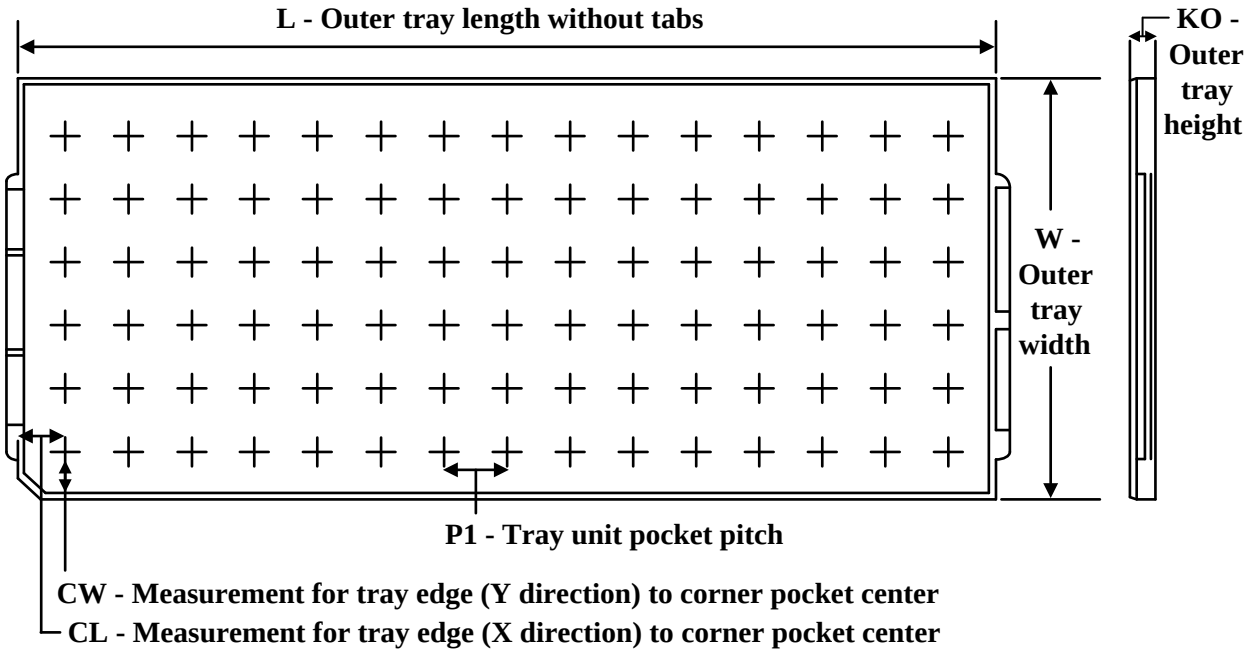
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9679801VCA | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| 5962R9679801VCA | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| 5962R9679801VCA | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| 5962R9679801VHA | NAD | CFP | 10 | 19 | 502 | 23 | 9398 | 9.78 |
| 5962R9679802VCA | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| 5962R9679802VCA | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| 5962R9679802VHA | NAD | CFP | 10 | 19 | 502 | 23 | 9398 | 9.78 |
| 86014012A | NAJ | LCCC | 20 | 50 | 470 | 11 | 3810 | 0 |
| 8601401CA | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| 8601401HA | NAD | CFP | 10 | 19 | 502 | 23 | 9398 | 9.78 |
| LM119E-SMD | NAJ | LCCC | 20 | 50 | 470 | 11 | 3810 | 0 |
| LM119E/883 | NAJ | LCCC | 20 | 50 | 470 | 11 | 3810 | 0 |
| LM119J-QMLV | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| LM119J-SMD | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| LM119J/883 | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| LM119JRLQMLV | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| LM119JRLQMLV | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| LM119JRQMLV | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| LM119JRQMLV | J | CDIP | 14 | 25 | 506.98 | 15.24 | 13440 | NA |
| LM119W-SMD | NAD | CFP | 10 | 19 | 502 | 23 | 9398 | 9.78 |
| LM119W/883 | NAD | CFP | 10 | 19 | 502 | 23 | 9398 | 9.78 |
| LM119WRLQMLV | NAD | CFP | 10 | 19 | 502 | 23 | 9398 | 9.78 |
| LM119WRQMLV | NAD | CFP | 10 | 19 | 502 | 23 | 9398 | 9.78 |

## TRAY

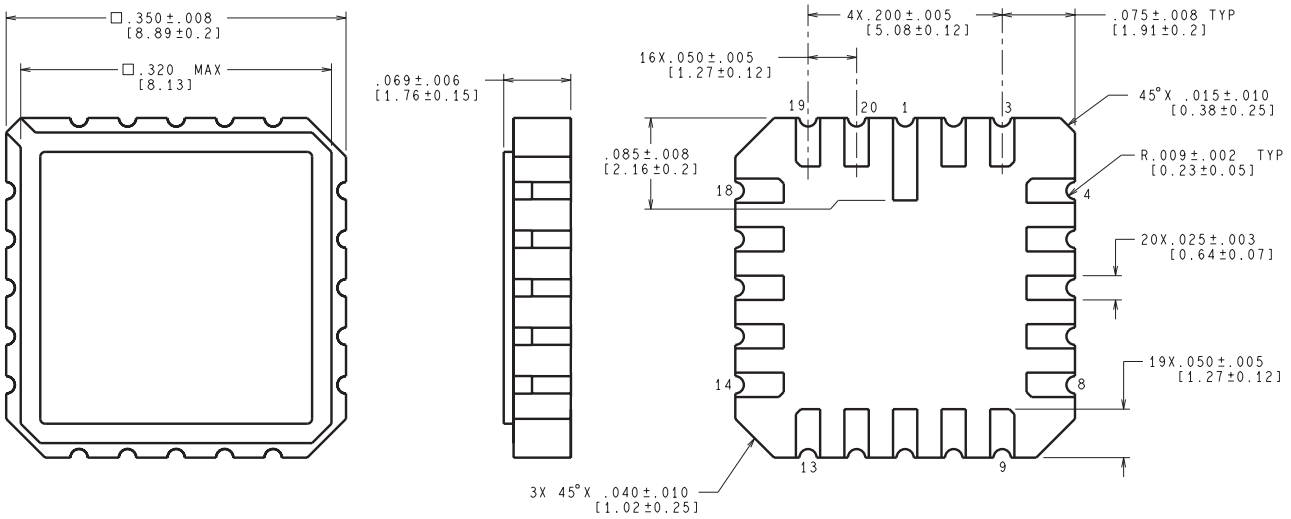



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962R9679801VIA | LME | TO-CAN | 10 | 20 | 2 X 10 | 150 | 126.49 | 61.98 | 8890 | 11.18 | 12.95 | 18.54 |
| 5962R9679802VIA | LME | TO-CAN | 10 | 20 | 2 X 10 | 150 | 126.49 | 61.98 | 8890 | 11.18 | 12.95 | 18.54 |
| 8601401IA | LME | TO-CAN | 10 | 20 | 2 X 10 | 150 | 126.49 | 61.98 | 8890 | 11.18 | 12.95 | 18.54 |
| LM119H-SMD | LME | TO-CAN | 10 | 20 | 2 X 10 | 150 | 126.49 | 61.98 | 8890 | 11.18 | 12.95 | 18.54 |
| LM119H/883 | LME | TO-CAN | 10 | 20 | 2 X 10 | 150 | 126.49 | 61.98 | 8890 | 11.18 | 12.95 | 18.54 |
| LM119HRLQMLV | LME | TO-CAN | 10 | 20 | 2 X 10 | 150 | 126.49 | 61.98 | 8890 | 11.18 | 12.95 | 18.54 |
| LM119HRQMLV | LME | TO-CAN | 10 | 20 | 2 X 10 | 150 | 126.49 | 61.98 | 8890 | 11.18 | 12.95 | 18.54 |

NAJ0020A




CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

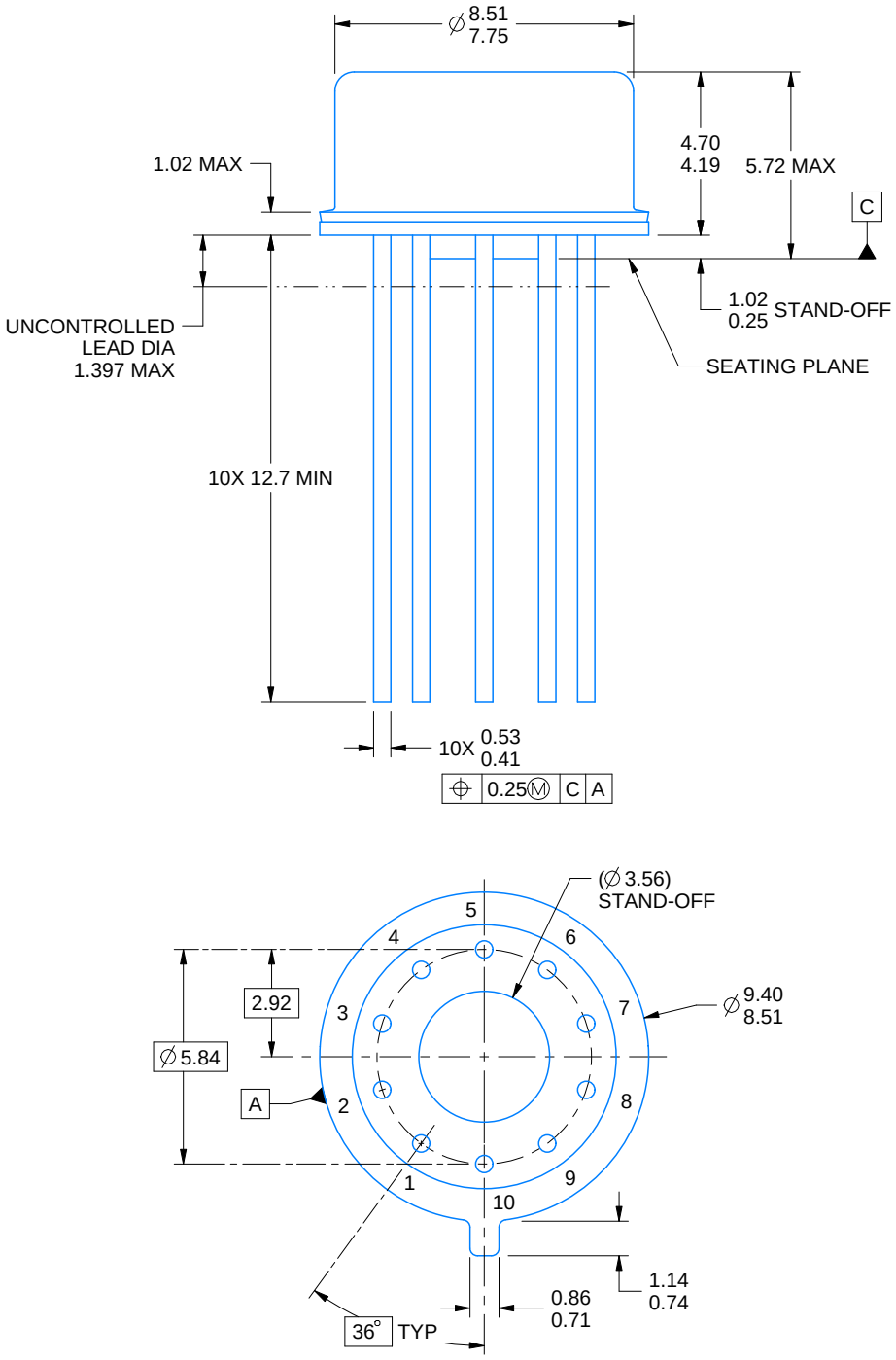
E20A (Rev F)

# PACKAGE OUTLINE

## LME0010A

## TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE




4220604/B 09/2024

NOTES:

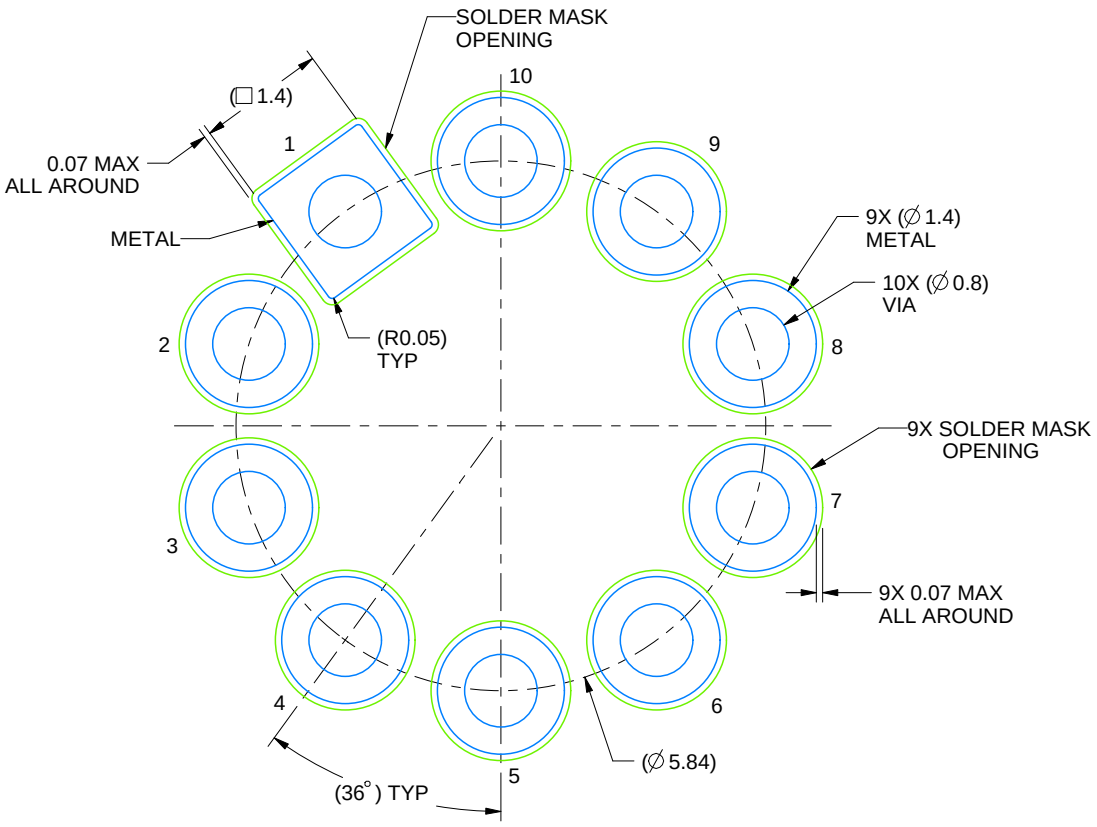
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-006/TO-100.

# EXAMPLE BOARD LAYOUT

## LME0010A

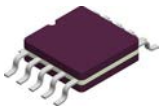
## TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220604/B 09/2024

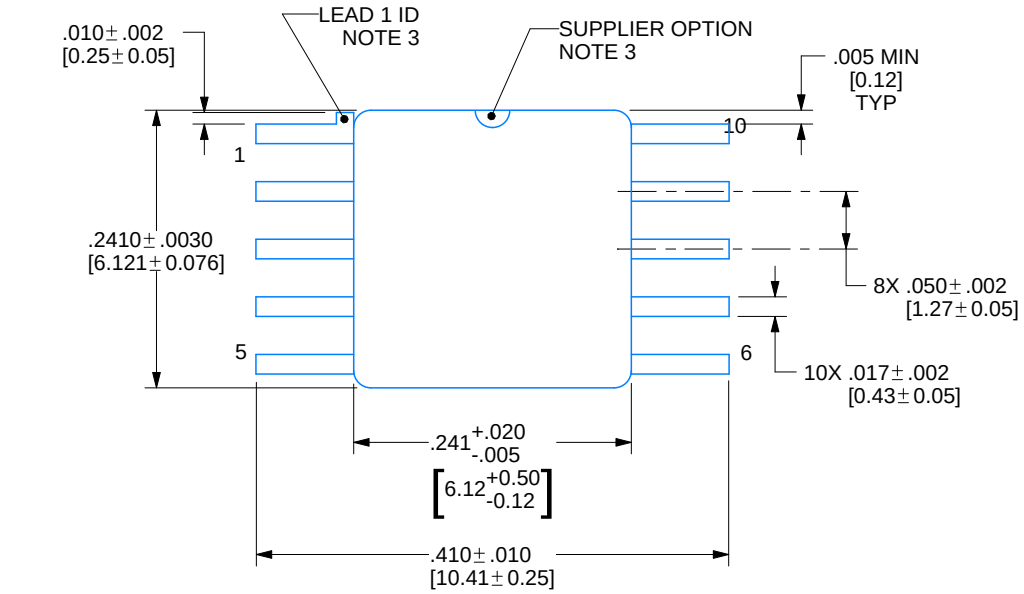


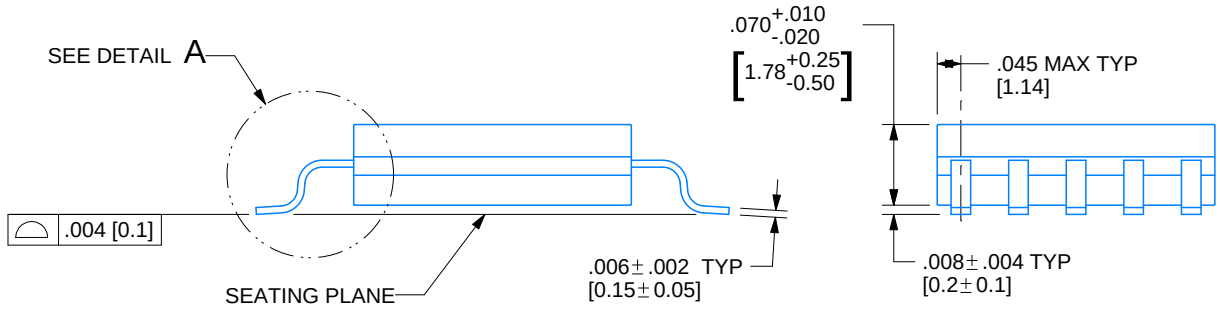
# PACKAGE OUTLINE

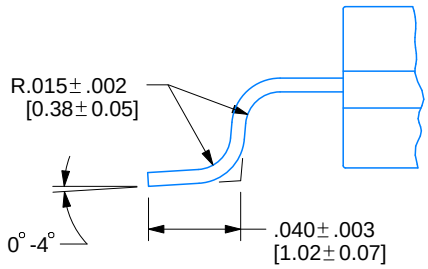
## NAC0010A

## CFP - 2.33mm max height

CERAMIC FLATPACK




DETAIL A
TYPICAL

4215196/D 08/2022

NOTES:

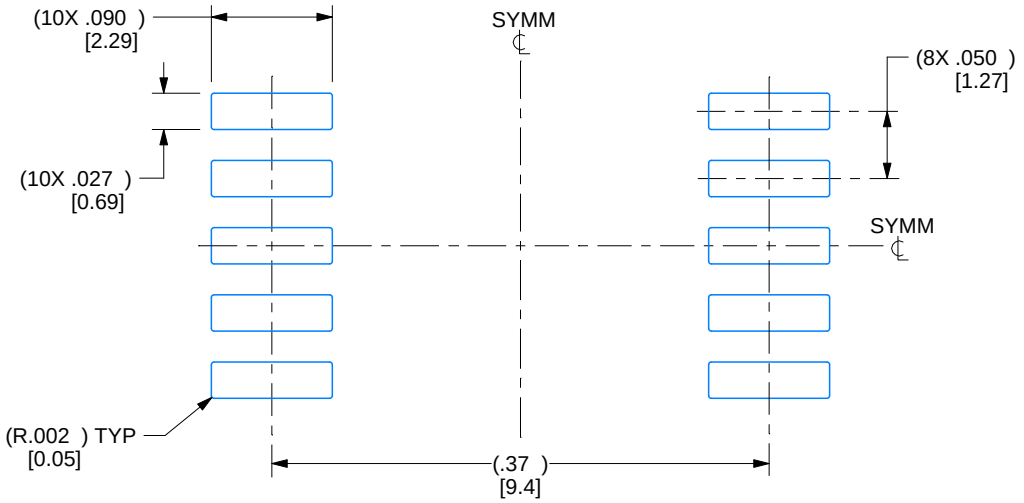
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

# EXAMPLE BOARD LAYOUT

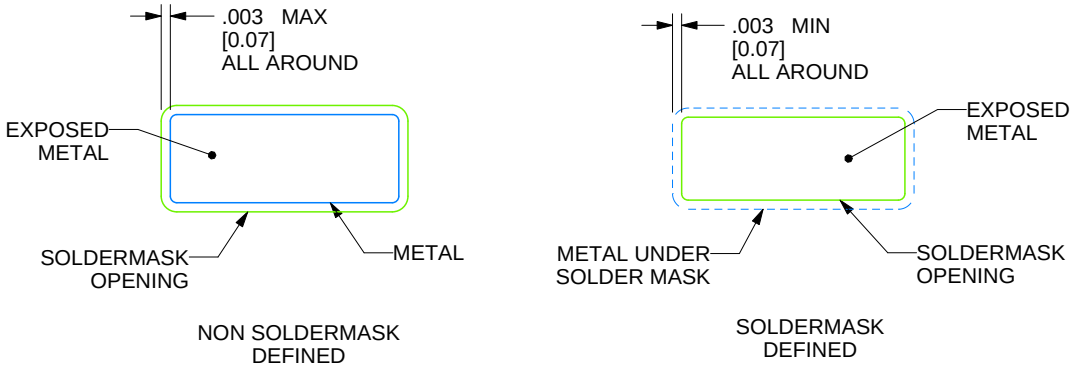
## NAC0010A

## CFP - 2.33mm max height

CERAMIC FLATPACK




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X




4215196/D 08/2022

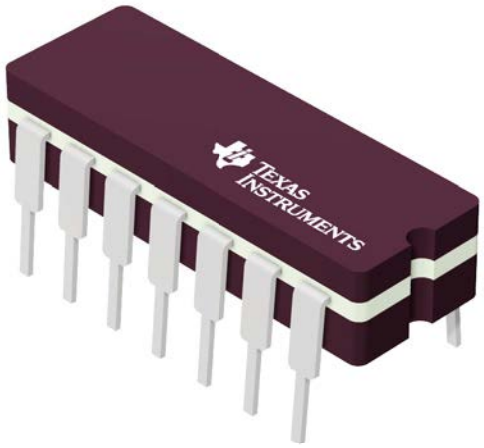
## REVISIONS

| REV | DESCRIPTION | E.C.N. | DATE | BY/APP'D |
|---|---|---|---|---|
| A | RELEASE TO DOCUMENT CONTROL | 2197877 | 12/30/2021 | DAVID CHIN / ANIS FAUZI |
| B | NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE; | 2198820 | 02/14/2022 | K. SINCERBOX |
| C | CHANGE PIN 1 ID LOCATION ON PIN | 2198845 | 02/18/2022 | D. CHIN / K. SINCERBOX |
| D | .2410± .0030 WAS .2700 +.0012/-.0002; | 2200915 | 08/08/2022 | D. CHIN / K. SINCERBOX |

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

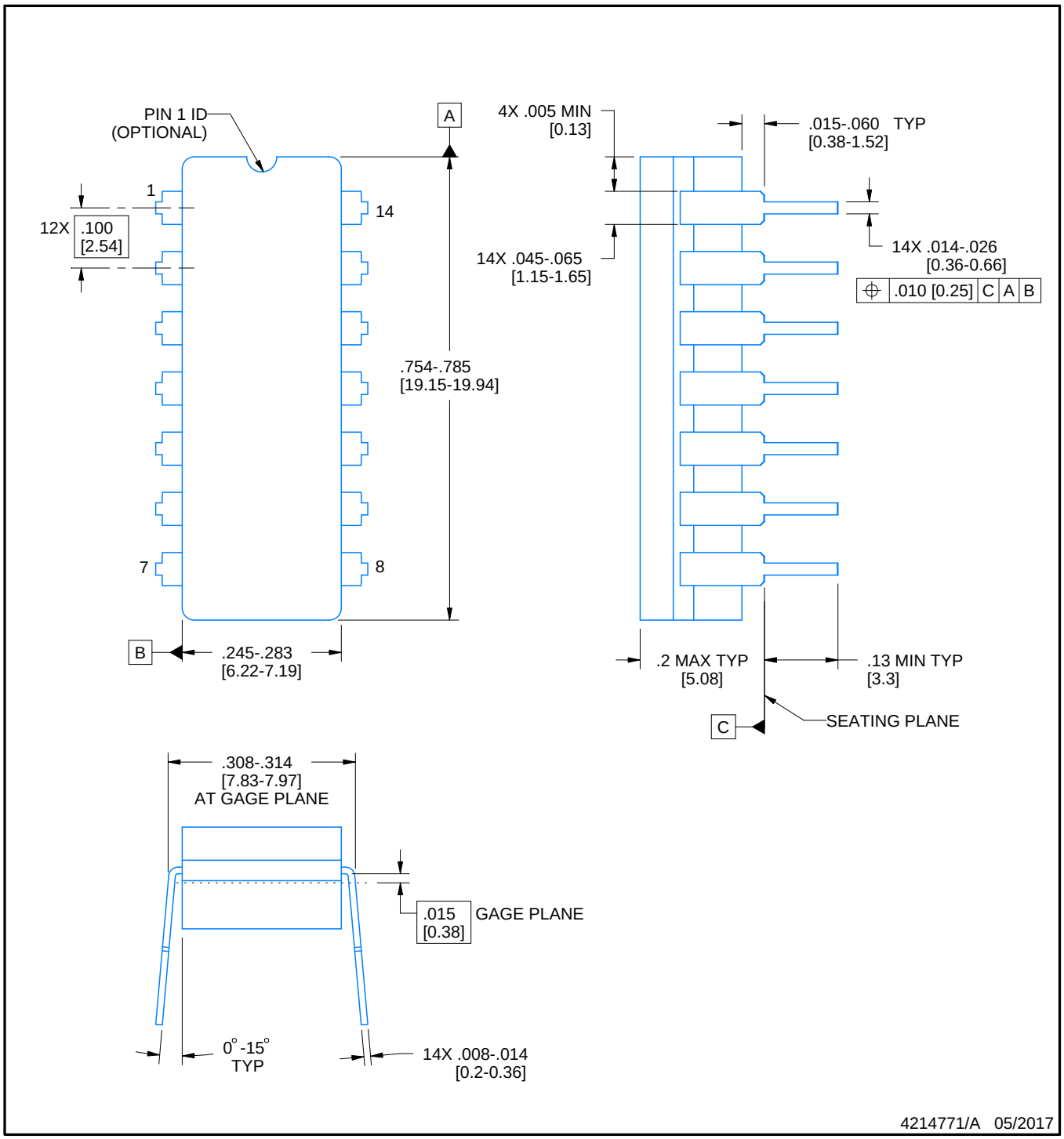


# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

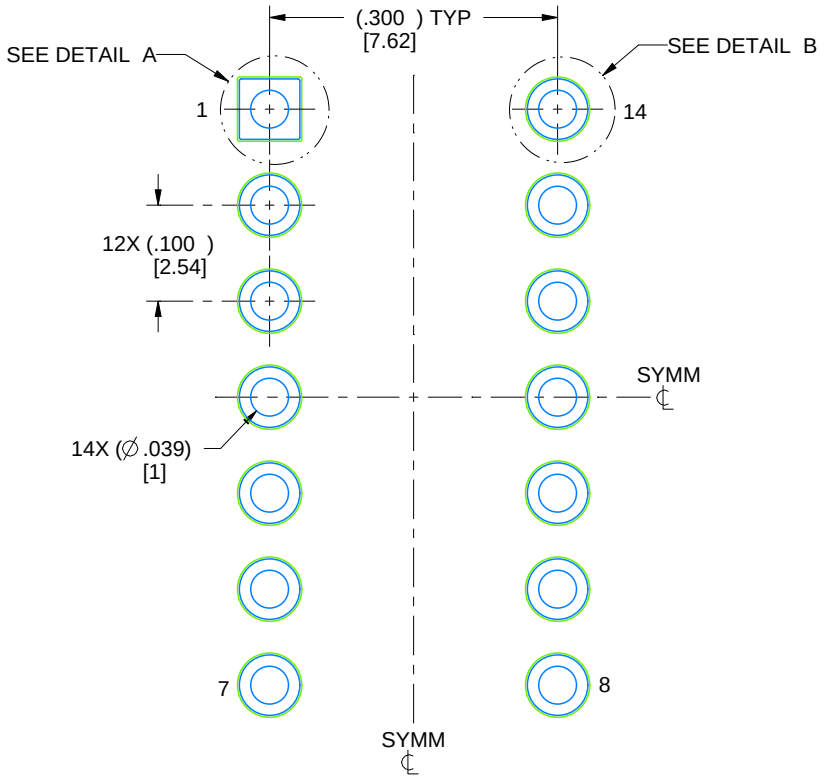
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

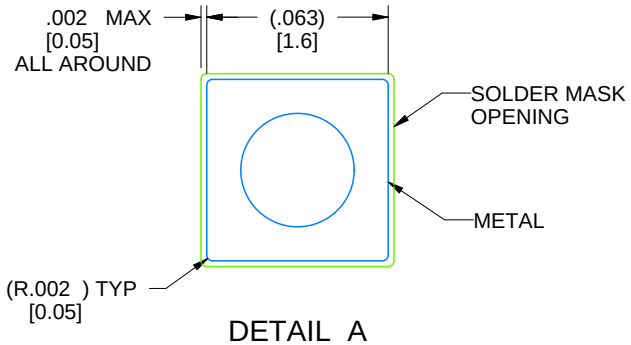
## J0014A

## CDIP - 5.08 mm max height

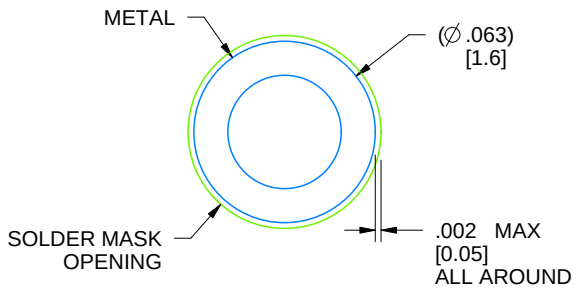
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X




DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

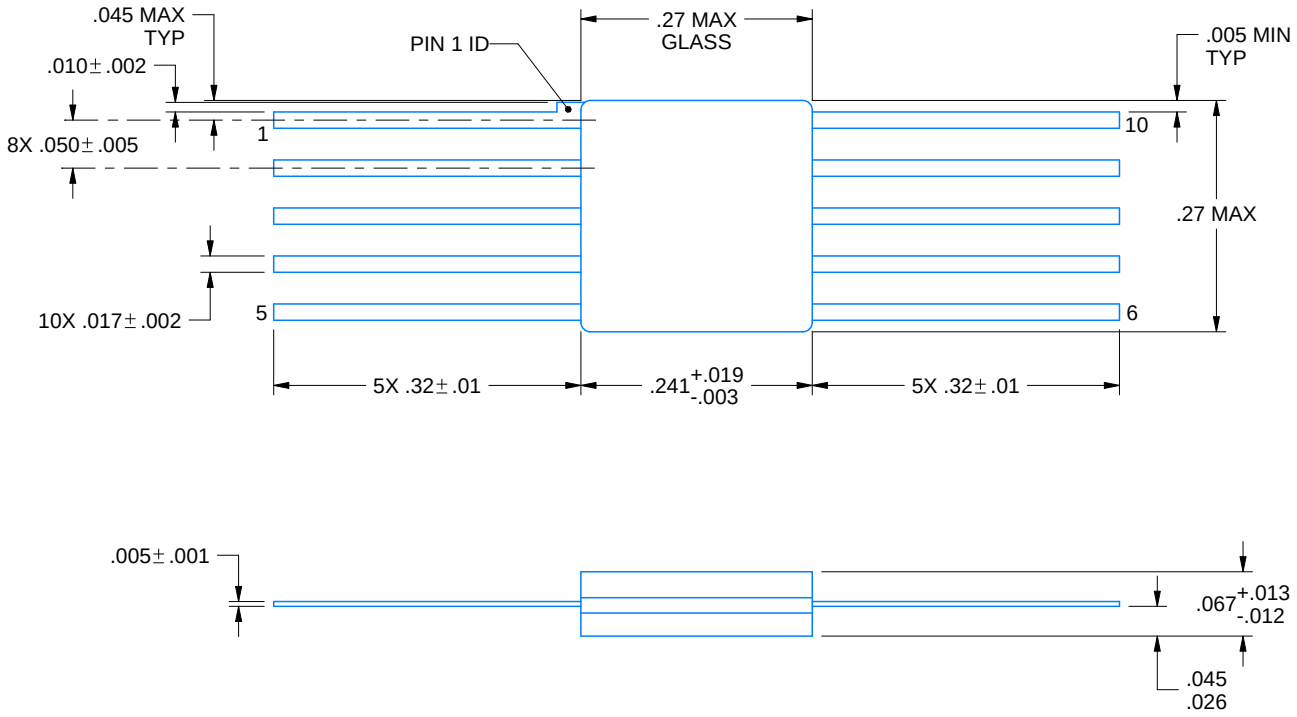
# NAD0010A



# PACKAGE OUTLINE

## CFP - 2.03 mm max height

CERAMIC FLATPACK







4215191/A 06/2021

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025