

ISOW14x2 Isolated RS-485/RS-422 Transceiver with Integrated Low-Emissions, Low-Noise, High-Efficiency DC-DC Converter

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard
- Data rates
 - ISOW1412 : 500kbps
 - ISOW1432 : 12Mbps
- Integrated low-emissions DC-DC converter with low-emissions, low-noise
 - Meets CISPR 32 Class B and EN 55032 Class B with margin on a two-layer PCB
 - Low frequency power converter at 25MHz enabling low noise performance
- Additional 2Mbps GPIO channel
- High efficiency output power
 - Typical efficiency: 46%
 - V_{ISOOUT} accuracy: $\pm 5\%$
 - Additional output current: 20mA
- Independent power supply for RS-485 and DC-DC
 - Logic supply (V_{IO}): 1.71V to 5.5V
 - Power converter supply (V_{DD}): 3V to 5.5V
- RS-485 with PROFIBUS compatibility
 - Open, short, and idle bus failsafe
 - 1/8 unit load: up to 256 nodes on bus
 - Glitch-free power up and power down
- Reinforced and Basic isolation options
- High CMTI: 100kV/ μ s (typical)
- High ESD bus protection
 - HBM: ± 16 kV
 - IEC 61000-4-2 contact discharge: ± 8 kV
- Operating temperature range: -40°C to 125°C
- Current limit and thermal shutdown
- 20-pin wide SOIC package
- **Safety-Related Certifications:**
 - VDE reinforced and basic insulation per DIN EN IEC 60747-17 (VDE 0884-17)
 - UL 1577 component recognition program
 - IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1 certifications

2 Applications

- [Factory automation](#)
- [Building automation](#)
- [Industrial transport](#)
- [Solar inverters, protection relay](#)
- [Motor drives](#)

Table 2-1. Device Information

DEVICE	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM)
ISOW1412 ISOW1432	DFM (SOIC, 20)	12.83mm × 10.30mm	12.83mm × 7.5mm
ISOW1412B ISOW1432B			

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.

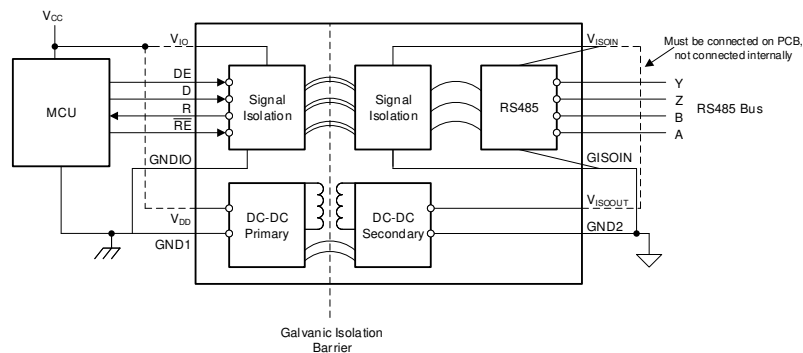


3 Description

The ISOW14x2 devices are galvanically-isolated RS-485/RS-422 transceivers with a built-in isolated DC-DC converter, that eliminates the need for a separate isolated power supply in space constrained isolated designs. The low-emissions, isolated DC-DC converter meets CISPR 32 radiated emissions Class B standard with just two ferrite beads on a simple two-layer PCB. Additional 20mA output current can be used to power other circuits on the board. An integrated 2Mbps GPIO channel helps remove any additional digital isolator or optocoupler for diagnostics, LED indication or supply monitoring.

Two options of data rates are provided: ISOW1412 is optimized for maximum 500kbps and ISOW1432 is designed for maximum 12Mbps data rate. These devices do not require any external components other than bypass capacitors to realize an isolated RS-485 port, designed for long distance communications. Isolation breaks the ground loop between the communicating nodes, allowing for a much larger common mode voltage range. Both signal and power paths are 5kV_{RMS} isolated per UL1577 and are qualified for reinforced and basic isolation per VDE, TUV, CSA and CQC.

The ISOW14x2 can operate from a single supply voltage of 3V to 5.5V by connecting V_{IO} and V_{DD} together on PCB. If lower logic levels are required, 1.71V to 5.5V logic supply (V_{IO}) can be separated and independent from the power converter supply (V_{DD}) of 3V to 5.5V. These devices support a wide operating ambient temperature range from -40°C to +125°C and are available in 20-pin DFM (SOIC-20 footprint compatible package) offering a minimum of 8mm creepage and clearance.



Simplified Schematic

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4 Device Comparison Table

Part number	Isolation	Duplex	Data Rate	Package
ISOW1412/ISOW1412B	Reinforced/Basic	Full	500Kbps	20-DFM(SOIC)
ISOW1432/ISOW1432B	Reinforced/Basic	Full	12Mbps	20-DFM(SOIC)

5 Pin Configuration and Functions

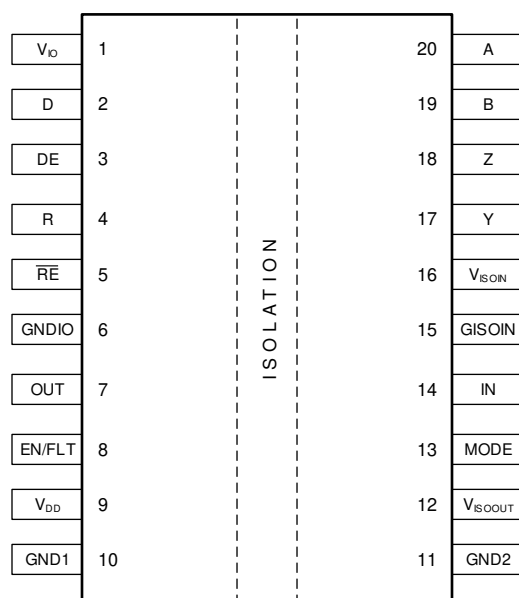


Figure 5-1. ISOW14x2 20-pin DFM Top View

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
V _{IO}	1	--	Side 1 logic supply
D	2	I	Data input
DE	3	I	Driver enable. If pin is floating, driver is disabled (internal pull-down resistor)
R	4	O	Received data output
RE	5	I	Receiver enable. If pin is floating, receiver buffer is disabled (internal pull-up resistor)
GNDIO	6	--	Ground connections for V _{IO} . GNDIO and GND1 need be shorted directly on PCB.
OUT	7	O	General purpose logic output
EN/FLT	8	I/O	Multi-function power converter enable input pin or fault output pin. Can only be used as either an input pin or an output pin. - If the pin is used as a Power converter enable input pin, the pin enables and disables the integrated DC-DC power converter. Connect directly to microcontroller or through a series current limiting resistor to use as an enable input pin. DC-DC power converted is enabled when EN is high (connected to V_{IO}) and disabled when low (connected to GND1). If EN is floating, DC-DC converter is enabled (internal pull-up resistor) - If the pin is used as a Fault output pin, the pin gives an alert signal if power converter is not operating properly. This pin is active low. Connect to microcontroller through a 5kΩ or greater pullup resistor to use as a fault output pin.
V _{DD}	9	--	Side 1 DC-DC converter power supply
GND1	10	--	Ground connection for V _{IO} . GNDIO and GND1 need be shorted directly on PCB.
GND2	11	--	Ground connection for V _{ISOOUT} . GND2 and GISOIN need be shorted directly on PCB, or connected through a ferrite bead.
V _{ISOOUT}	12	--	Isolated power converter output voltage. V _{ISOOUT} and V _{ISOIN} need be shorted directly on PCB, or connected through a ferrite bead.
MODE	13	I	Mode select. For RS-485 transceiver to operate at 3.3V supply, connect MODE to GND2. For RS-485 transceiver to operate in 5V supply PROFIBUS mode, connect MODE to V _{ISOOUT} (internal pull-down resistor)
IN	14	I	General purpose logic input
GISOIN	15	--	Ground connections for V _{ISOIN} . GND2 and GISOIN need be shorted directly on PCB, or connected through a ferrite bead.
V _{ISOIN}	16	--	Side 2 supply voltage for RS485. V _{ISOOUT} and V _{ISOIN} need be shorted directly on PCB, or connected through a ferrite bead.
Y	17	O	RS-485 driver non-inverting output
Z	18	O	RS-485 driver inverting output
B	19	I	RS-485 receiver inverting input
A	20	I	RS-485 receiver non-inverting input

(1) I = Input; O = Output; I/O = Input or Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{DD}	Power converter supply voltage	−0.5	6	V
V _{ISOIN}	Isolated supply voltage, input supply for RS-485 transceiver	−0.5	6	V
V _{ISOOUT}	Isolated supply voltage, Power converter output at RS485 mode (MODE = GND2)	−0.5	4	V
V _{ISOOUT}	Isolated supply voltage, Power converter output at Profibus mode (MODE = V _{ISOOUT})	−0.5	6	V
V _{IO}	Logic supply voltage	−0.5	6	V
V _{BUS}	Voltage on bus pins (A, B, Y, Z with respect to GND2)	−12	15	V
V _{LOGIC_IO}	Logic I/O voltage level (D, DE, $\overline{RE}$, R, EN, OUT)	−0.5	V _{IO} + 0.5 ⁽³⁾	V
	IN	−0.5	V _{ISOIN} + 0.5	V
	MODE	−0.5	V _{ISOOUT} + 0.5	V
I _O	Output current on R and OUT pins	−15	15	mA
T _J	Junction temperature	−40	150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground pin (GND1 or GND2). All voltage values except differential I/O bus voltages are peak voltage values.
- (3) The maximum voltage must not be greater than 6 V.

6.2 ESD Ratings

				VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins except bus pins	±3000	V
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Bus pins with respect to GND2 (same side)	±16000	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1500	V
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 contact discharge	Bus pins and GND1 (across barrier)	±8000	V
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 contact discharge	Bus pins and GND2 (same side)	±8000	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{IO}	Logic supply voltage	1.8V operation	1.71		1.89	V
		2.5V, 3.3V, and 5V operation	2.25		5.5	
V _{DD}	Power converter supply voltage		3		5.5	V
V _{DD(UVLO+)}	Positive threshold when power converter supply is rising			2.8	2.93	V
V _{DD(UVLO-)}	Positive threshold when power converter supply is falling		2.40	2.55		V
V _{HYS1(UVLO)}	Power converter supply voltage hysteresis		0.15	0.25		V
V _{IO(UVLO+)}	Rising threshold of logic supply voltage				1.7	V
V _{IO(UVLO-)}	Falling threshold of logic supply voltage		1			V
V _{HYS2(UVLO)}	Logic supply voltage hysteresis		75	125		mV
V _{BUS}	Input voltage at any bus terminal (separately with respect to GND2 or common mode)		-7		12	V
V _{IH}	High-level input voltage (D, DE, EN, and $\overline{RE}$ inputs)		$0.7 \times V_{IO}$		V _{IO}	V
	High-level input voltage (IN input)		$0.7 \times V_{ISOIN}$		V _{ISOIN}	V
V _{IL}	Low-level input voltage (D, DE, EN, and $\overline{RE}$ inputs)		0		$0.3 \times V_{IO}$	V
	Low-level input voltage (IN input)		0		$0.3 \times V_{ISOIN}$	V
V _{ID}	Differential input voltage (receiver terminals A with respect to B)		-12		12	V
I _{O(DRV)}	Output current, driver (Y, Z)		-60		60	mA
I _O	Output current, R and OUT pins	V _{IO} = 4.5 to 5.5V	-4		4	mA
		V _{IO} = 3 to 3.6 V	-2		2	mA
		V _{IO} = 2.25 to 2.75V, 1.71 to 1.89V	-1		1	mA
R _L	Differential load resistance on bus		54			Ω
1/t _{UI}	Signaling rate	ISOW1412			500	kbps
1/t _{UI}	Signaling rate	ISOW1432			12	Mbps
DR	Data rate for GPIO channel				2	Mbps
t _{pwrap}	Power up time after applying input supply (Isolated output supply reaches 90% of set point and data transmission can start after this)		5			ms
T _A	Ambient operating temperature (MODE= GND2), no extra current available on V _{ISOUT} ⁽¹⁾		-40		125	°C
	Ambient operating temperature (MODE= GND2), 20mA extra current available on V _{ISOUT} ⁽¹⁾		-40		105	°C
	Ambient operating temperature (MODE= V _{ISOOUT}), 50% duty cycle on DE, no extra current available on V _{ISOUT} ⁽¹⁾		-40		125	°C
	Ambient operating temperature (MODE= V _{ISOOUT}), no extra current available on V _{ISOUT} ⁽¹⁾		-40		105	°C
	Ambient operating temperature (MODE= V _{ISOOUT}), 20mA extra current available on V _{ISOUT} ⁽¹⁾		-40		85	°C

(1) Extra current is only available at VDD=5 V ± 10% mode

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISOW14x2	UNIT
		DFM	
		20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	68.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	20.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	44.8	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	13	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	44	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	--	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _D	Maximum power dissipation (both sides)	ISOW1412: V _{DD} = V _{IO} = 5.5V, MODE = V _{ISOOUT} , T _J = 150°C, Y-Z load = 54Ω 50pF, Y shorted to A, Z shorted to B(loopback), Load on R = 15pF, Input a 250kHz 50% duty cycle square wave to D pin with V _{DE} = V _{IO} , V _{RE} = GND1			1060	mW
P _{D1}	Maximum power dissipation (side-1)				490	mW
P _{D2}	Maximum power dissipation (side-2)				570	mW
P _D	Maximum power dissipation (both sides)	ISOW1432: V _{DD} = V _{IO} = 5.5V, MODE = V _{ISOOUT} , T _J = 150°C, Y-Z load = 54Ω 50pF, Y shorted to A, Z shorted to B(loopback), Load on R = 15pF, Input a 6MHz 50% duty cycle square wave to D pin with V _{DE} = V _{IO} , V _{RE} = GND1			1110	mW
P _{D1}	Maximum power dissipation (side-1)				510	mW
P _{D2}	Maximum power dissipation (side-2)				600	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – capacitive signal isolation)	>17	μm
		Minimum internal gap (internal clearance- transformer power isolation)	>120	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150V _{RMS}	I-IV	
		Rated mains voltage ≤ 300V _{RMS}	I-IV	
		Rated mains voltage ≤ 600V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000V _{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) ⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V _{PK}
V _{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDb) test	1000	V _{RMS}
		DC voltage	1500	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t = 1s (100% production)	7071	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ISOW14x2 ⁽³⁾	Test method per IEC 62368-1, 1.2/50μs waveform	10000	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ISOW14x2B ⁽³⁾	Test method per IEC 62368-1, 1.2/50μs waveform	7800	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a: After I/O safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10s	≤5	pC
		Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; ISOW14x2: V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10s ISOW14x2B: V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10s	≤5	
		Method b1: At routine test (100% production) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1s; ISOW14x2: V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1s (method b1) ISOW14x2B: V _{pd(m)} = 1.5 × V _{IORM} , t _m = 1s (method b1), or V _{pd(m)} = V _{ini} , t _m = t _{ini} (method b2)	≤5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.4 sin (2πft), f = 1MHz	≈3.5	pF
R _{IO}	Isolation resistance, input to output ⁽⁵⁾	V _{IO} = 500V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	Ω
		V _{IO} = 500V at T _S = 150°C	>10 ⁹	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} = 5000V _{RMS} , t = 60s (qualification); V _{TEST} = 1.2 × V _{ISO} = 6000V _{RMS} , t = 1s (100% production)	5000	V _{RMS}

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
- (2) ISOW14x2 is suitable for *safe electrical insulation* and ISOW14x2B is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device

6.7 Safety-Related Certifications

VDE	CSA	UL	TUV	CQC
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1, IEC 61010-1 and IEC 60601-1	Certified under UL 1577 Component Recognition Program	Certified according to EN 61010-1 and EN 62368-1	Certified according to GB 4943.1
Certificate number: 40040142 (Reinforced) 40047657 (Basic)	Master contract number: 220991	File number: E181974	Client ID number: 77311	Certificate number: CQC21001297517

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S	Safety input, output, or supply current ⁽¹⁾	R _{θJA} = 68.5°C/W, V _I = 5.5V, T _J = 150°C, T _A = 25°C, See Figure 6-1			332	mA
		R _{θJA} = 68.5°C/W, V _I = 3.6V, T _J = 150°C, T _A = 25°C, See Figure 6-1			507	
P _S	Safety input, output, or total power ⁽¹⁾	R _{θJA} = 68.5°C/W, T _J = 150°C, T _A = 25°C, See Figure 6-2			1826	mW
T _S	Safety temperature ⁽¹⁾				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, R_{θJA}, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
T_J = T_A + R_{θJA} × P, where P is the power dissipated in the device.
T_{J(max)} = T_S = T_A + R_{θJA} × P_S, where T_{J(max)} is the maximum allowed junction temperature.
P_S = I_S × V_I, where V_I is the maximum input voltage.

6.9 Electrical Characteristics

Over recommended operating conditions, typical values are at $V_{DD} = V_{IO} = 3.3V$ and $T_A = 25^\circ C$, GND1 = GNDIO, GND2 = GISOIN (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Device							
V _{ISOOUT}	Isolated output supply voltage	MODE=GND2, DE=GND1, D, $\overline{RE}$ and IN floating	3.135	3.3V	3.465	V	
	Isolated output supply voltage	MODE=V _{ISOOUT} , DE=GND1, D, $\overline{RE}$ and IN floating	4.75	5	5.25	V	
V _{OH}	Output high voltage on OUT pin	V _{IO} = 5V ± 10%, I _{OH} = −4mA, IN=V _{ISOIN}	V _{IO} − 0.4			V	
	Output high voltage on OUT pin	V _{IO} = 3.3V ± 10% , I _{OH} = −2mA, IN=V _{ISOIN}	V _{IO} − 0.3			V	
	Output high voltage on OUT pin	V _{IO} = 2.5V ± 10% , I _{OH} = −1mA, IN=V _{ISOIN}	V _{IO} − 0.2			V	
	Output high voltage on OUT pin	V _{IO} = 1.8V ± 5%, I _{OH} = −1mA, IN=V _{ISOIN}	V _{IO} − 0.2			V	
V _{OL}	Output low voltage on OUT pin	V _{IO} = 5V ± 10%, I _{OL} = 4mA, IN=GND2				0.4	V
	Output low voltage on OUT pin	V _{IO} = 3.3V ± 10% , I _{OL} = 2mA, IN=GND2				0.3	V
	Output low voltage on OUT pin	V _{IO} = 2.5V ± 10%, I _{OL} = 1mA, IN=GND2				0.2	V
	Output low voltage on OUT pin	V _{IO} = 1.8V ± 5%, I _{OL} = 1mA, IN=GND2				0.2	V
I _I	Input current, IN	IN at 0V or V _{ISOIN}	−25			25	μA
I _I	Input current, EN	EN at 0V or V _{IO}	−25			25	μA
CM _H	High-level common-mode transient immunity	Driver and receiver path, V _{CM} = 1000V, see Figure 7-4	100			kV/μs	
CM _L	Low-level common-mode transient immunity	Driver and receiver path, V _{CM} = 1000V, see Figure 7-4	100			kV/μs	
Driver							
V _{OD}	Differential output voltage magnitude	Unloaded bus, V _{DD} = 3V to 3.6V with MODE=GND2, or 4.5V to 5.5V with MODE=V _{ISOOUT}	1.5	V _{ISOIN}		V	
		R _L = 60Ω, −7V ≤ V _{TEST} ≤ 12V (see Figure 7-1), V _{DD} = 3V to 3.6V, MODE = GND2	1.5	V _{ISOIN}			
		R _L = 100Ω (see Figure 7-2) (RS-422 load), V _{DD} = 3V to 3.6V, MODE = GND2	2	V _{ISOIN}			
		R _L = 54 Ω (see Figure 7-2) (RS-485 load), V _{DD} = 3V to 3.6V, MODE = GND2	1.5	V _{ISOIN}			
V _{OD}	Differential output voltage magnitude	R _L = 54Ω, V _{DD} = 4.5V to 5.5V, MODE = V _{ISOOUT} , see Figure 7-2	2.1	V _{ISOIN}		V	
V _{OD}	Differential output voltage magnitude	R _L = 100Ω (see Figure 7-2) (RS-422 load), V _{DD} = 4.5V to 5.5V, MODE = V _{ISOOUT}	2.1	V _{ISOIN}		V	
V _{OD}	Differential output voltage magnitude	R _L = 60Ω, −7V ≤ V _{TEST} ≤ 12V (see Figure 7-1), V _{DD} = 4.5V to 5.5V, MODE = V _{ISOOUT}	2.1	V _{ISOIN}		V	
Δ V _{OD}	Change in differential output voltage between the two states	R _L = 54 Ω or 100 Ω (see Figure 7-2)	−200	200		mV	
V _{OC}	Common-mode output voltage	R _L = 54Ω or 100Ω (see Figure 7-2)	1	0.5 × V _{ISOIN}		3	V
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between the two states	R _L = 54Ω or 100Ω (see Figure 7-2)	−200	200		mV	
V _{OC(PP)}	Peak-to-peak common mode output voltage	R _L = 54Ω or 100Ω, V _{ISOIN} =V _{ISOOUT} =3.3V, see Figure 7-2	400			mV	
I _{OS}	Short-circuit output current	V _{DE} = V _{IO} , V _D =V _{IO} or GND1, −7V ≤ Y or Z ≤ 12V, or Y shorted to Z, see Figure 7-10	180			mA	
I _I	Input current , D, DE	V _D , V _{DE} at 0V or V _{IO}	−25	25		μA	

Over recommended operating conditions, typical values are at $V_{DD} = V_{IO} = 3.3V$ and $T_A = 25^\circ C$, GND1 = GNDIO, GND2 = GISOIN (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
I _{I1}	Bus input current	V _{DE} = 0V, V _{ISOIN} = 0V or 3.3V or 5V, ISOW1412 or ISOW1432, V _A or V _B = −7V to 12V, other input at 0V	−100		125	μA
V _{TH+}	Positive-going input-threshold voltage	−7V ≤ V _{CM} ≤ 12V	See ⁽¹⁾	−78	−20	mV
V _{TH−}	Negative-going input-threshold voltage	−7V ≤ V _{CM} ≤ 12V	−200	−141	See ⁽¹⁾	mV
V _{hys}	Input hysteresis (V _{TH+} − V _{TH−})	−7V ≤ V _{CM} ≤ 12V	40	63		mV
V _{OH}	Output high voltage on R pin	V _{IO} = 5V ± 10%, I _{OH} = −4mA, V _{ID} ≥ 200mV	V _{IO} − 0.4			V
		V _{IO} = 3.3V ± 10%, I _{OH} = −2mA, V _{ID} ≥ 200mV	V _{IO} − 0.3			
		V _{IO} = 2.5V ± 10% , I _{OH} = −1mA, V _{ID} ≥ 200mV	V _{IO} − 0.2			
		V _{IO} = 1.8V ± 5%, I _{OH} = −1mA, V _{ID} ≥ 200mV	V _{IO} − 0.2			
V _{OL}	Output low voltage on R pin	V _{IO} = 5V ± 10%, I _{OL} = 4mA, V _{ID} ≤ −200mV			0.4	V
		V _{IO} = 3.3V ± 10%, I _{OL} = 2mA, V _{ID} ≤ −200mV			0.3	
		V _{IO} = 2.5V ± 10% , I _{OL} = 1mA, V _{ID} ≤ −200mV			0.2	
		V _{IO} = 1.8V ± 5%, I _{OL} = 1mA, V _{ID} ≤ −200mV			0.2	
I _{OZ}	Output high-impedance current on R pin	V _R = 0V or V _{IO} , V _{RE} = V _{IO}	−1		1	μA
I _{I(RE)}	Input current on RE pin	V _{RE} at 0V or V _{IO}	−25		25	μA

(1) The V_{TH+} voltage is specified to be greater than the V_{TH-} voltage by at least the V_{hys} voltage under any specific conditions.

6.10 Supply Current Characteristics at $V_{ISOOUT} = 3.3\text{ V}$

over recommended operating conditions, $V_{DD} = V_{IO} = 3\text{ to }5.5\text{ V}$, $MODE = GND2$, $GND1 = GNDIO$, $GND2 = GISOIN$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power converter disabled						
I _{DD}	Power converter supply current	EN=GND1, D, DE, $\overline{RE}$ floating		0.23	0.45	mA
I _{IO}	Logic supply current	EN=GND1, D, DE, $\overline{RE}$ floating		0.24	0.55	mA
Power converter supply current: Driver enabled, receiver disabled						
I _{DD}	Power converter supply current	V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 120Ω, V _D = V _{IO} , V _{DD} = 5V ± 10%, A and B floating		56	77	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 120Ω, V _D = V _{IO} , V _{DD} = 3.3V ± 10%, A and B floating		69	125	mA
I _{DD}	Power converter supply current, ISOW1412	V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 120Ω 50pF, D = 500kbps square wave 50% duty, V _{DD} = 5V ± 10%		62	86	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 100Ω 50pF, D = 500kbps square wave 50% duty, V _{DD} = 5V ± 10%		69	88	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 54Ω 50pF, D = 500kbps square wave 50% duty, V _{DD} = 5V ± 10%		90	122	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 120Ω 50pF, D = 500kbps square wave 50% duty, V _{DD} = 3.3V ± 10%		76	131	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 100Ω 50pF, D = 500kbps square wave 50% duty, V _{DD} = 3.3V ± 10%		84	131	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 54Ω 50pF, D = 500kbps square wave 50% duty, V _{DD} = 3.3V ± 10%		111	158	mA
I _{DD}	Power converter supply current, ISOW1432	V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 120Ω 50pF, D = 12Mbps square wave 50% duty, V _{DD} = 5V ± 10%		87	99	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 100Ω 50pF, D = 12Mbps square wave 50% duty, V _{DD} = 5V ± 10%		69	96	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 54Ω 50pF, D = 12Mbps square wave 50% duty, V _{DD} = 5V ± 10%		114	130	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 120Ω 50pF, D = 12Mbps square wave 50% duty, V _{DD} = 3.3V ± 10%		105	135	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 100Ω 50pF, D = 12Mbps square wave 50% duty, V _{DD} = 3.3V ± 10%		84	140	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 54Ω 50pF, D = 12Mbps square wave 50% duty, V _{DD} = 3.3V ± 10%		137	163	mA
Power converter supply current: Driver disabled, receiver enabled						
I _{DD}	Power converter supply current, ISOW1412	V _{DE} = V _{GND1} , V _{RE} = V _{GND1} , Y and Z bus loaded and unloaded, A-B = square wave 500kbps 50% duty V _D = V _{GND1} , V _{DD} = 5V ± 10%, C _L on R = 15pF		16	28	mA
		V _{DE} = V _{GND1} , V _{RE} = V _{GND1} , Y and Z bus loaded and unloaded, A-B = square wave 500kbps 50% duty V _D = V _{GND1} , V _{DD} = 3.3V ± 10%, C _L on R = 15pF		18	30	
I _{DD}	Power converter supply current, ISOW1432	V _{DE} = V _{GND1} , V _{RE} = V _{GND1} , Y and Z bus loaded and unloaded, A-B = square wave 12Mbps 50% duty V _D = V _{GND1} , V _{DD} = 5V ± 10%, C _L on R = 15pF		15	22	mA
		V _{DE} = V _{GND1} , V _{RE} = V _{GND1} , Y and Z bus loaded and unloaded, A-B = square wave 12Mbps 50% duty V _D = V _{GND1} , V _{DD} = 3.3V ± 10%, C _L on R = 15pF		17	27	
Power converter supply current: Driver enabled, receiver enabled						

over recommended operating conditions, $V_{DD} = V_{IO} = 3$ to $5.5V$, MODE=GND2, GND1 = GNDIO, GND2 = GISOIN (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD}	Power converter supply current, ISOW1412	V _{DE} = V _{IO} , V _{RE} = V _{GND1} , Y and Z bus load = 120Ω 50pF, loopback ⁽¹⁾ , D = 500kbps 50% duty, V _{DD} = 5V ± 10%, C _L on R = 15pF		63	102	mA
		V _{DE} = V _{IO} , V _{RE} = V _{GND1} , Y and Z bus load = 120Ω 50pF, loopback ⁽¹⁾ , D = 500kbps 50% duty, V _{DD} = 3.3V ± 10%, C _L on R = 15pF		77	129	
I _{DD}	Power converter supply current, ISOW1432	V _{DE} = V _{IO} , V _{RE} = V _{GND1} , Y and Z bus load = 120Ω 50pF, loopback ⁽¹⁾ , D = 12Mbps 50% duty, V _{DD} = 5V ± 10%, C _L on R = 15pF		90	105	mA
		V _{DE} = V _{IO} , V _{RE} = V _{GND1} , Y and Z bus load = 120Ω 50pF, loopback ⁽¹⁾ , D = 12Mbps 50% duty, V _{DD} = 3.3V ± 10%, C _L on R = 15pF		109	138	
Logic supply current: Driver disabled, receiver disabled						
I _{IO}	Logic supply current	V _{DE} = V _{GND1} , V _{RE} = V _{IO} , V _D = V _{IO} , V _{IO} = 3.3V ± 10%		3.2	6.0	mA
Logic supply current: Driver enabled, Receiver enabled, static						
I _{IO}	Logic supply current	V _{DE} = V _{IO} , V _{RE} = V _{GND1} , V _D = V _{IO} , loopback ⁽¹⁾ , V _{IO} = 3.3V ± 10%		4	6.8	mA
Logic supply current: Driver enabled, receiver enabled, dynamic						
I _{IO}	Logic supply current, ISOW1412	V _{DE} = V _{IO} , V _{RE} = V _{GND1} , D = 500kbps 50% duty square wave, loopback ⁽¹⁾ , V _{IO} = 3.3V ± 10%		4.6	7.2	mA
I _{IO}	Logic supply current, ISOW1432	V _{DE} = V _{IO} , V _{RE} = V _{GND1} , D = 12Mbps 50% duty square wave, loopback ⁽¹⁾ , V _{IO} = 3.3V ± 10%		4.6	7.2	mA

(1) The output of the driver is connected to the input of a receiver in a loop back mode.

6.11 Supply Current Characteristics at $V_{ISOOUT} = 5\text{ V}$

over recommended operating conditions, $V_{DD} = V_{IO} = 4.5\text{ V to } 5.5\text{ V}$, $MODE = V_{ISOOUT}$, $GND1 = GNDIO$, $GND2 = GISOIN$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power converter disabled						
I _{DD}	Power converter supply current	EN=GND1, D, DE, $\overline{RE}$ floating		0.23	0.45	mA
I _{IO}	Logic supply current	EN=GND1, D, DE, $\overline{RE}$ floating		0.24	0.55	mA
Power converter supply current: Driver enabled, receiver disabled						
I _{DD}	Power converter supply current	V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 120Ω, V _D = V _{IO} , V _{DD} = 5V ± 10%, A and B floating		97	160	mA
I _{DD}	Power converter supply current, ISOW1412	V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 120Ω 50pF, D = 500kbps square wave 50% duty, V _{DD} = 5V ± 10%		123	161	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 54Ω 50pF, D = 500kbps square wave 50% duty, V _{DD} = 5V ± 10%		175	227	mA
I _{DD}	Power converter supply current, ISOW1432	V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 120Ω 50pF, D = 12Mbps square wave 50% duty, V _{DD} = 5V ± 10%		146	185	mA
		V _{DE} = V _{IO} , V _{RE} = V _{IO} , bus load = 54Ω 50pF, D = 12Mbps square wave 50% duty, V _{DD} = 5V ± 10%		202	240	mA
Power converter supply current: Driver disabled, receiver enabled						
I _{DD}	Power converter supply current	V _{DE} = V _{GND1} , V _{RE} = V _{GND1} , Y and Z bus loaded and unloaded, A-B = square wave 500kbps 50% duty V _D = V _{IO} , V _{DD} = 5V ± 10%, C _L on R = 15pF		17	31	mA
I _{DD}	Power converter supply current	V _{DE} = V _{GND1} , V _{RE} = V _{GND1} , Y and Z bus loaded and unloaded, A-B = square wave 12Mbps 50% duty (ISOW1432) V _D = V _{IO} , V _{DD} = 5V ± 10%, C _L on R = 15pF		24	36	mA
Power converter supply current: Driver enabled, receiver enabled						
I _{DD}	Power converter supply current, ISOW1412	V _{DE} = V _{IO} , V _{RE} = V _{GND1} , Y and Z bus load = 120Ω 50pF, loopback ⁽¹⁾ , D = 500kbps 50% duty, V _{DD} = 5V ± 10%, C _L on R = 15pF		123	207	mA
I _{DD}	Power converter supply current, ISOW1432	V _{DE} = V _{IO} , V _{RE} = V _{GND1} , Y and Z bus load = 120Ω 50pF, loopback ⁽¹⁾ , D = 12Mbps 50% duty, V _{DD} = 5V ± 10%, C _L on R = 15pF		145	210	mA

(1) The output of the driver is connected to the input of a receiver in a loop back mode.

6.12 Switching Characteristics at $V_{ISOOUT} = 3.3\text{ V}$

Min / Max specifications are over recommended operating conditions, typical values are at $V_{DD} = V_{IO} = 3.3\text{V}$, $\text{MODE} = \text{GND2}$ ($V_{ISOOUT} = 3.3\text{V}$), $\text{GND1} = \text{GNDIO}$, $\text{GND2} = \text{GISOIN}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver: 500-kbps device (ISOW1412)						
t _r , t _f	Differential output rise time and fall time	R _L = 54Ω, C _L = 50pF, see Figure 7-3	190	300	600	ns
t _{PHL} , t _{PLH}	Propagation delay	R _L = 54Ω, C _L = 50pF, see Figure 7-3		450	610	ns
PWD	Pulse width distortion ⁽¹⁾ , t _{PHL} - t _{PLH}	R _L = 54Ω, C _L = 50pF, see Figure 7-3		3	40	ns
t _{PHZ} , t _{PLZ}	Disable time	See Figure 7-5 and Figure 7-6		56	200	ns
t _{PZH} , t _{PZL}	Enable time	See Figure 7-5 and Figure 7-6		280	600	ns
Receiver: 500-kbps device (ISOW1412)						
t _r , t _f	Output rise time and fall time	C _L = 15pF, see Figure 7-7			4	ns
t _{PHL} , t _{PLH}	Propagation delay	C _L = 15pF, see Figure 7-7		60	135	ns
PWD	Pulse width distortion ⁽¹⁾ , t _{PHL} - t _{PLH}	C _L = 15pF, see Figure 7-7		2	15	ns
t _{PHZ} , t _{PLZ}	Disable time	See Figure 7-8 and Figure 7-9		9	30	ns
t _{PZH} , t _{PZL}	Enable time	See Figure 7-8 and Figure 7-9		8	30	ns
Driver: 12-Mbps device (ISOW1432)						
t _r , t _f	Differential output rise time and fall time	R _L = 54Ω, C _L = 50pF, see Figure 7-3	6	15	25	ns
t _{PHL}	Propagation delay	R _L = 54Ω, C _L = 50pF, see Figure 7-3		49	125	ns
t _{PLH}	Propagation delay	R _L = 54Ω, C _L = 50pF, see Figure 7-3		49	125	ns
t _{PHL} , t _{PLH}	Propagation delay	R _L = 54Ω, C _L = 50pF, see Figure 7-3		52	125	ns
PWD	Pulse width distortion ⁽¹⁾ , t _{PHL} - t _{PLH}	R _L = 54Ω, C _L = 50pF, see Figure 7-3		1	10	ns
t _{PHZ}	Disable time	See Figure 7-5 and Figure 7-6		35	125	ns
t _{PLZ}	Disable time	See Figure 7-5 and Figure 7-6		35	125	ns
t _{PHZ} , t _{PLZ}	Disable time	See Figure 7-5 and Figure 7-6		36	125	ns
t _{PZH}	Enable time	See Figure 7-5 and Figure 7-6		46	150	ns
t _{PZL}	Enable time	See Figure 7-5 and Figure 7-6		36	150	ns
t _{PZH} , t _{PZL}	Enable time	See Figure 7-5 and Figure 7-6		48	110	ns
Receiver: 12-Mbps device (ISOW1432)						
t _r , t _f	Output rise time and fall time	C _L = 15pF, see Figure 7-7			4	ns
t _{PHL}	Propagation delay	C _L = 15pF, see Figure 7-7		59	120	ns
t _{PLH}	Propagation delay	C _L = 15pF, see Figure 7-7		59	120	ns
t _{PHL} , t _{PLH}	Propagation delay	C _L = 15pF, see Figure 7-7		42	120	ns
PWD	Pulse width distortion ⁽¹⁾ , t _{PHL} - t _{PLH}	C _L = 15pF, see Figure 7-7		1.7	10	ns
t _{PHZ}	Disable time	See Figure 7-8 and Figure 7-9		7	30	ns
t _{PLZ}	Disable time	See Figure 7-8 and Figure 7-9		6	30	ns
t _{PHZ} , t _{PLZ}	Disable time	See Figure 7-8 and Figure 7-9		9	30	ns
t _{PZH}	Enable time	See Figure 7-8 and Figure 7-9		6	30	ns
t _{PZL}	Enable time	See Figure 7-8 and Figure 7-9		5	30	ns
t _{PZH} , t _{PZL}	Enable time	See Figure 7-8 and Figure 7-9		8	30	ns
GPIO channel						
t _{PHL} , t _{PLH}	Propagation delay time	See Figure 7-11		227	347	ns
PWD	Pulse width distortion, t _{PHL} - t _{PLH}			20	110	ns
t _r	Output signal rise time			1	4	ns
t _f	Output signal fall time			1	4	ns

(1) Also known as pulse skew.

6.13 Switching Characteristics at $V_{ISOOUT} = 5\text{ V}$

Min / Max specifications are over recommended operating conditions, typical values are at $V_{DD} = V_{IO} = 5\text{ V}$, $MODE = V_{ISOOUT}$ ($V_{ISOOUT} = 5\text{ V}$), $GND1 = GNDIO$, $GND2 = GISOIN$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver: 500-kbps device (ISOW1412)						
t _r , t _f	Differential output rise time and fall time	R _L = 54Ω, C _L = 50pF, see Figure 7-3	200	300	600	ns
t _{PHL} , t _{PLH}	Propagation delay	R _L = 54Ω, C _L = 50pF, see Figure 7-3		400	610	ns
PWD	Pulse width distortion ⁽¹⁾ , t _{PHL} – t _{PLH}	R _L = 54Ω, C _L = 50pF, see Figure 7-3		2	40	ns
t _{PHZ} , t _{PLZ}	Disable time	See Figure 7-5 and Figure 7-6		30	200	ns
t _{PZH} , t _{PZL}	Enable time	See Figure 7-5 and Figure 7-6		115	600	ns
Receiver: 500-kbps device (ISOW1412)						
t _r , t _f	Output rise time and fall time	C _L = 15pF, see Figure 7-7			4	ns
t _{PHL} , t _{PLH}	Propagation delay	C _L = 15pF, see Figure 7-7		49	135	ns
PWD	Pulse width distortion ⁽¹⁾ , t _{PHL} – t _{PLH}	C _L = 15pF, see Figure 7-7		2	20	ns
t _{PHZ} , t _{PLZ}	Disable time	See Figure 7-8 and Figure 7-9		8	30	ns
t _{PZH} , t _{PZL}	Enable time	See Figure 7-8 and Figure 7-9		7	30	ns
Driver: 12-Mbps device (ISOW1432)						
t _r , t _f	Differential output rise time and fall time	R _L = 54Ω, C _L = 50pF, see Figure 7-3	4	10	18	ns
t _{PHL}	Propagation delay	R _L = 54Ω, C _L = 50pF, see Figure 7-3		40	125	ns
t _{PLH}	Propagation delay	R _L = 54Ω, C _L = 50pF, see Figure 7-3		40	125	ns
t _{PHL} , t _{PLH}	Propagation delay	R _L = 54Ω, C _L = 50pF, see Figure 7-3		40	125	ns
PWD	Pulse width distortion ⁽¹⁾ , t _{PHL} – t _{PLH}	R _L = 54Ω, C _L = 50pF, see Figure 7-3		2	10	ns
t _{PHZ}	Disable time	See Figure 7-5 and Figure 7-6		30	125	ns
t _{PLZ}	Disable time	See Figure 7-5 and Figure 7-6		30	125	ns
t _{PHZ} , t _{PLZ}	Disable time	See Figure 7-5 and Figure 7-6		28	40	ns
t _{PZH}	Enable time	See Figure 7-5 and Figure 7-6		34	150	ns
t _{PZL}	Enable time	See Figure 7-5 and Figure 7-6		25	150	ns
t _{PZH} , t _{PZL}	Enable time	See Figure 7-5 and Figure 7-6		33	150	ns
Receiver: 12-Mbps device (ISOW1432)						
t _r , t _f	Output rise time and fall time	C _L = 15pF, see Figure 7-7			6	ns
t _{PHL}	Propagation delay	C _L = 15pF, see Figure 7-7		55	120	ns
t _{PLH}	Propagation delay	C _L = 15pF, see Figure 7-7		55	120	ns
t _{PHL} , t _{PLH}	Propagation delay	C _L = 15pF, see Figure 7-7		52	120	ns
PWD	Pulse width distortion ⁽¹⁾ , t _{PHL} – t _{PLH}	C _L = 15pF, see Figure 7-7		2.5	10	ns
t _{PHZ}	Disable time	See Figure 7-8 and Figure 7-9		5	30	ns
t _{PLZ}	Disable time	See Figure 7-8 and Figure 7-9		5	30	ns
t _{PHZ} , t _{PLZ}	Disable time	See Figure 7-8 and Figure 7-9		8	30	ns
t _{PZH}	Enable time	See Figure 7-8 and Figure 7-9		4	30	ns
t _{PZL}	Enable time	See Figure 7-8 and Figure 7-9		4	30	ns
t _{PZH} , t _{PZL}	Enable time	See Figure 7-8 and Figure 7-9		7	30	ns
GPIO channel						
t _{PHL} , t _{PLH}	Propagation delay time	See Figure 7-11		227	347	ns
PWD	Pulse width distortion, t _{PHL} - t _{PLH}			20	110	ns
t _r	Output signal rise time			2.2	4	ns
t _f	Output signal fall time			2.2	4	ns

(1) Also known as pulse skew.

6.14 Insulation Characteristics Curves

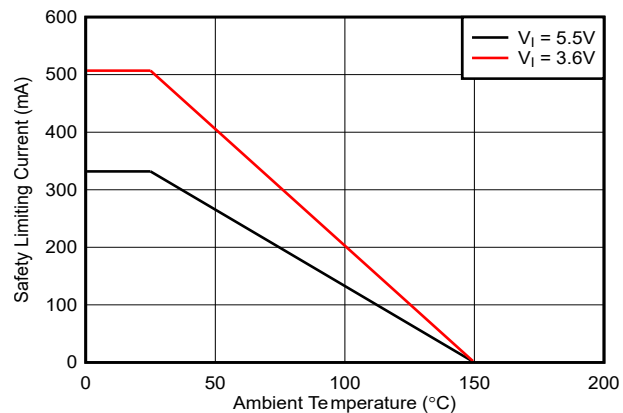


Figure 6-1. Thermal Derating Curve for Limiting Current per VDE

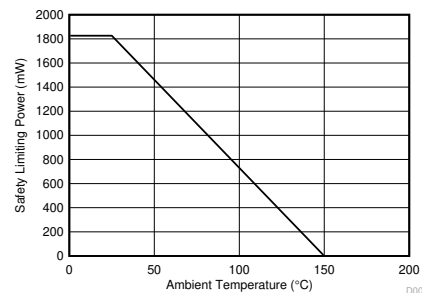


Figure 6-2. Thermal Derating Curve for Limiting Power per VDE

6.15 Typical Characteristics

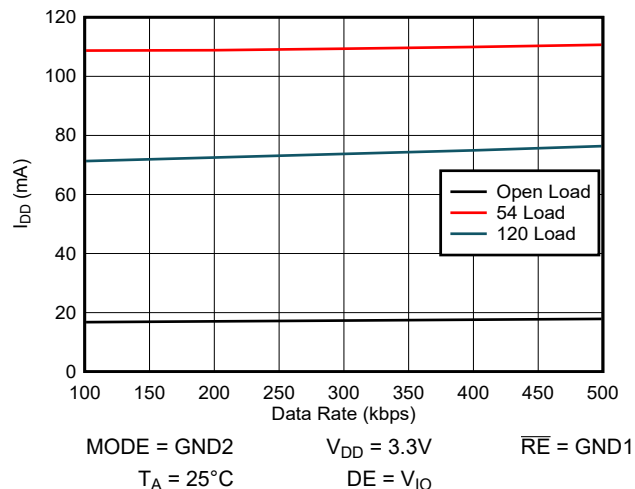


Figure 6-3. ISOW1412 V_{DD} Supply Current vs Data Rate - RS485 Mode

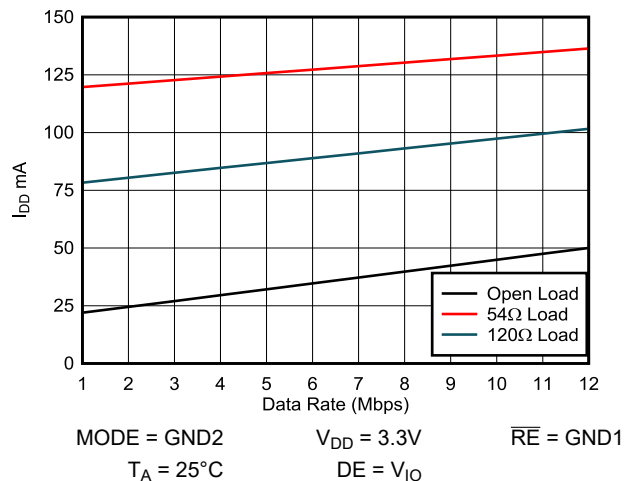


Figure 6-4. ISOW1432 V_{DD} Supply Current vs Data Rate - RS485 Mode

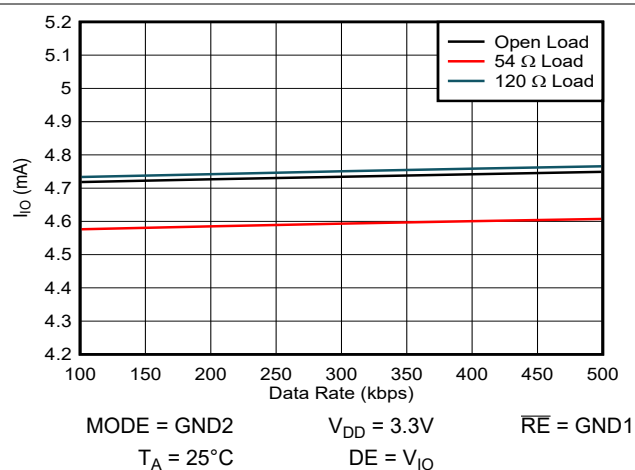


Figure 6-5. ISOW1412 V_{IO} Supply Current vs Data Rate - RS485 Mode

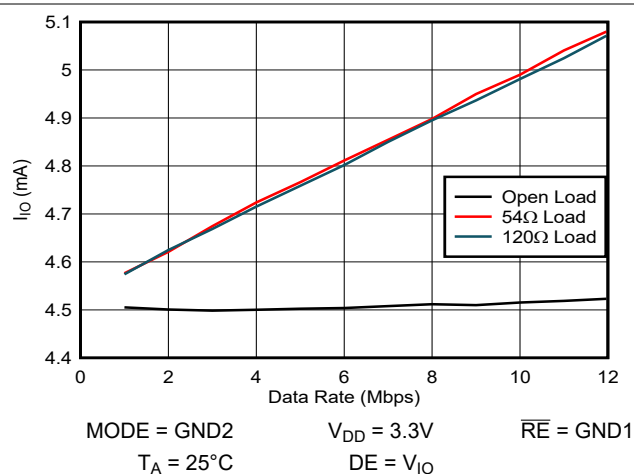


Figure 6-6. ISOW1432 V_{IO} Supply Current vs Data Rate - RS485 Mode

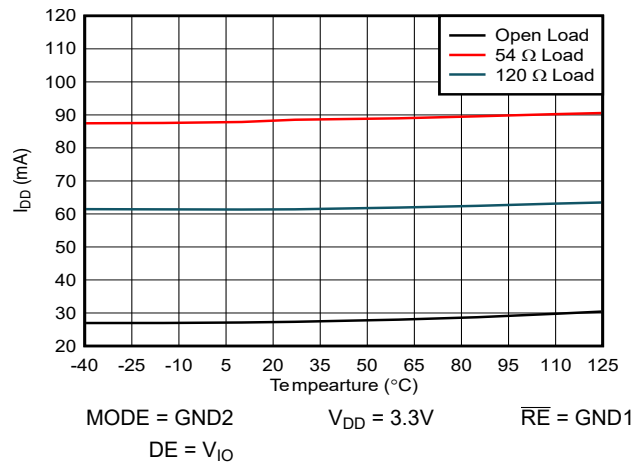


Figure 6-7. ISOW1412 V_{DD} Current vs Temperature - RS485 Mode

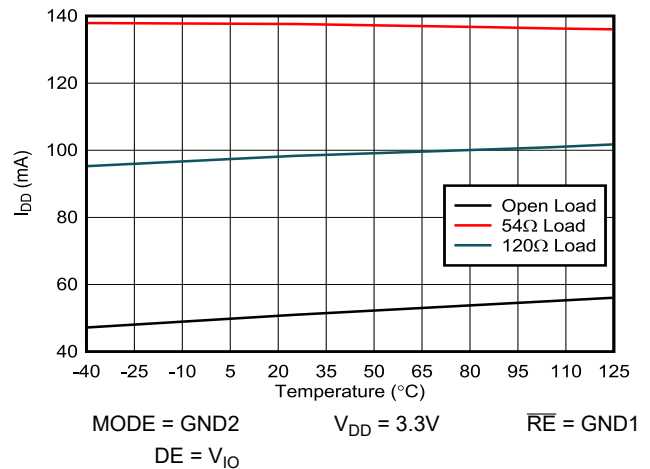


Figure 6-8. ISOW1432 V_{DD} Current vs Temperature - RS485 Mode

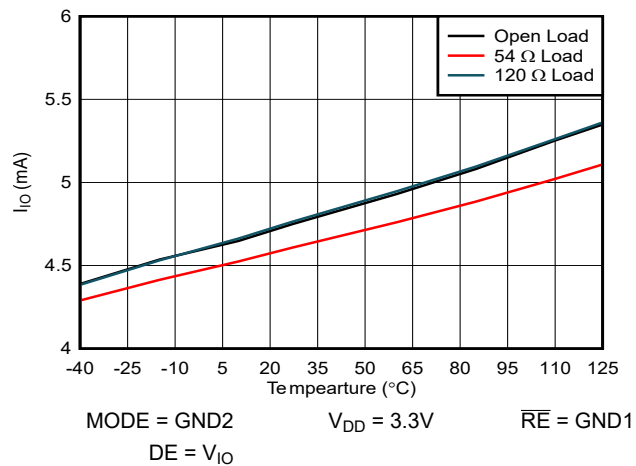


Figure 6-9. ISOW1412 V_{IO} Current vs Temperature - RS485 Mode

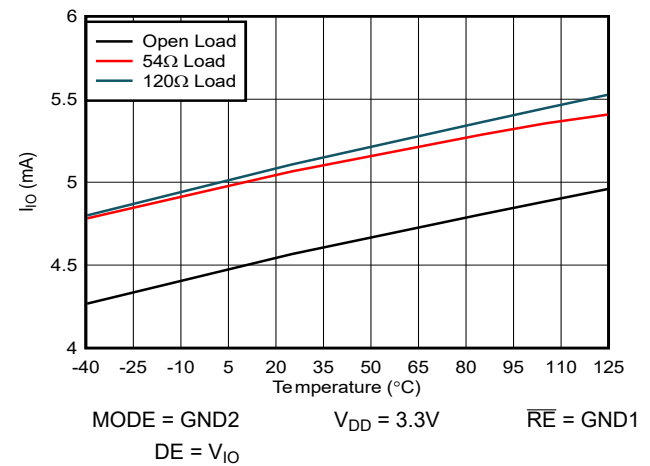


Figure 6-10. ISOW1432 V_{IO} Current vs Temperature - RS485 Mode

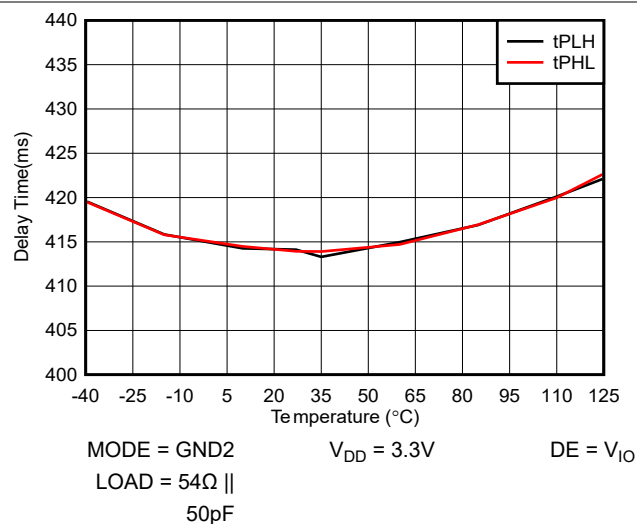


Figure 6-11. ISOW1412 Driver Propagation Delay vs Temperature - RS485 Mode

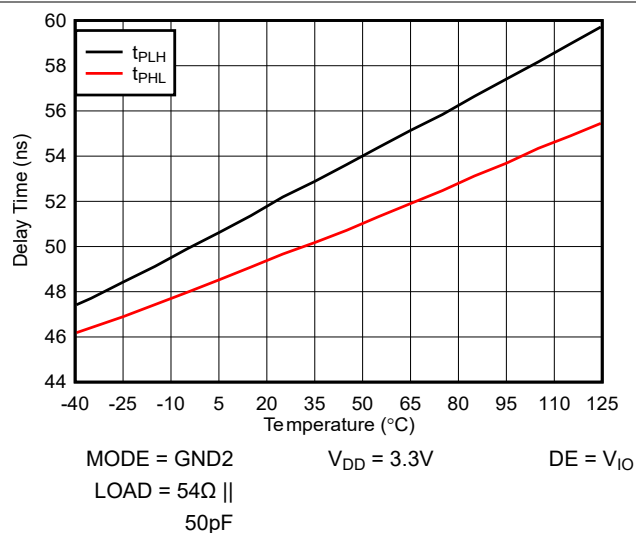


Figure 6-12. ISOW1432 Driver Propagation Delay vs Temperature - RS485 Mode

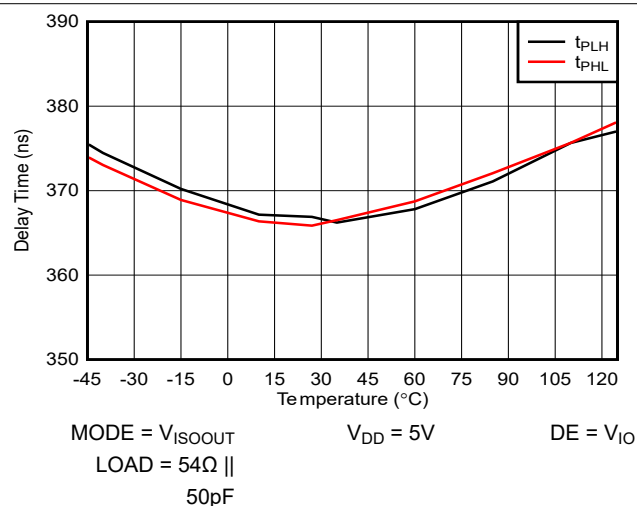


Figure 6-13. ISOW1412 Driver Propagation Delay vs Temperature - Profibus Mode

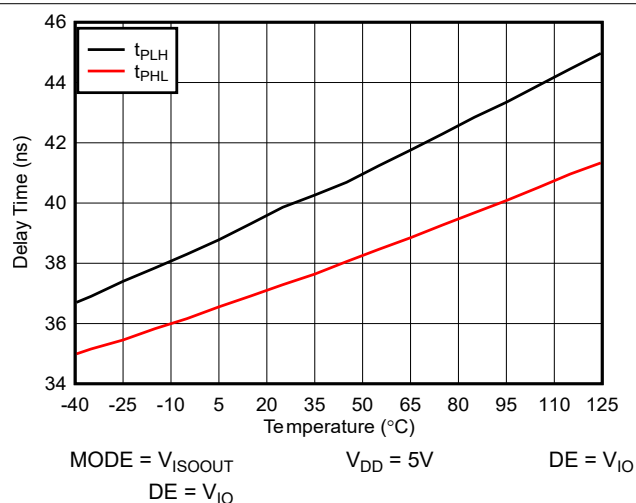


Figure 6-14. ISOW1432 Driver Propagation Delay vs Temperature - Profibus Mode

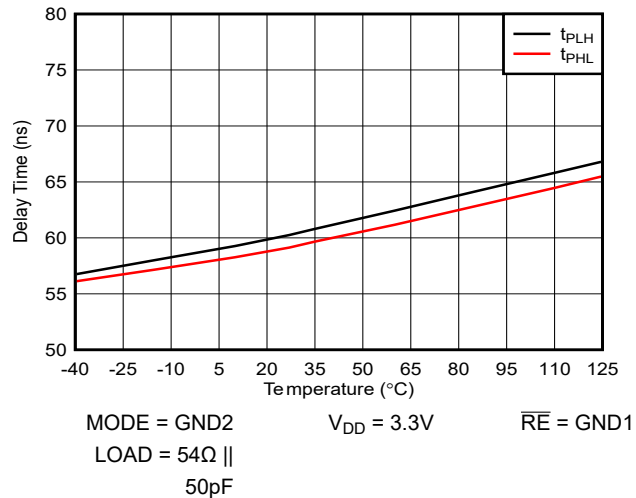


Figure 6-15. ISOW1412 Receiver Propagation Delay vs Temperature - RS485 Mode

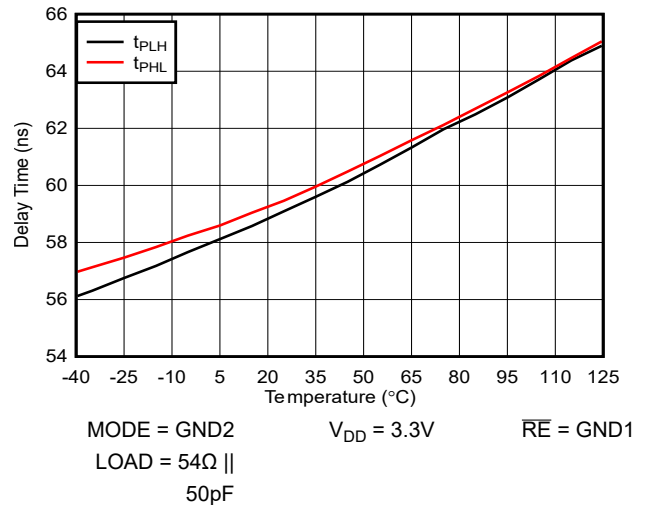


Figure 6-16. ISOW1432 Receiver Propagation Delay vs Temperature - RS485 Mode

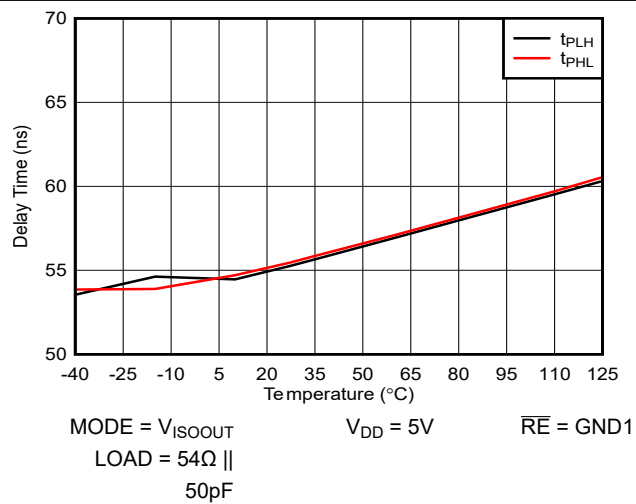


Figure 6-17. ISOW1412 Receiver Propagation Delay vs Temperature - Profibus Mode

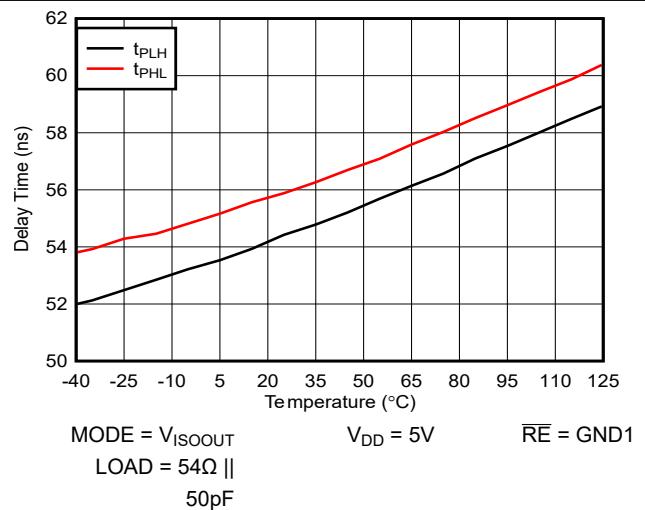
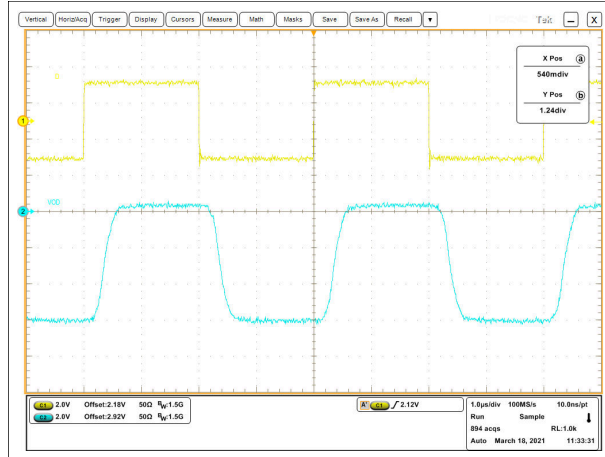
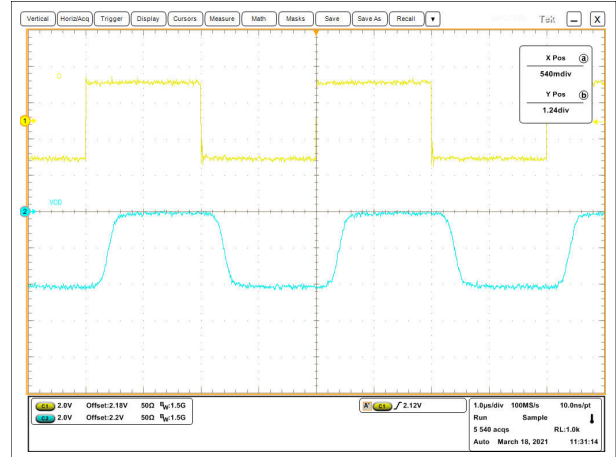


Figure 6-18. ISOW1432 Receiver Propagation Delay vs Temperature - Profibus Mode



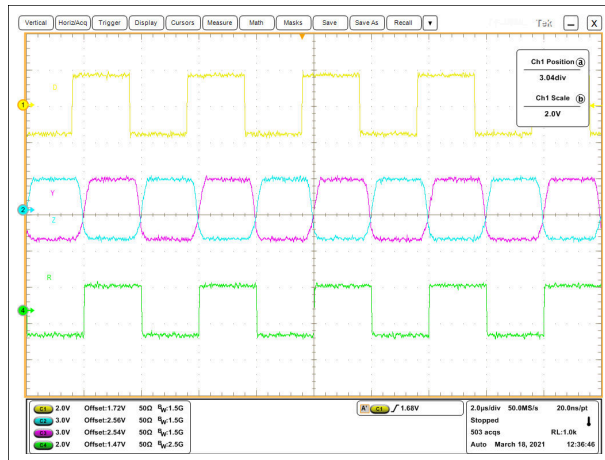
MODE = V_{ISOOUT} $V_{DD} = 5V$ $DE = V_{IO}$
LOAD = $54\Omega \parallel 50pF$ $T_A = 25^\circ C$

Figure 6-19. ISOW1412 Driver Propagation Delay - Profibus Mode



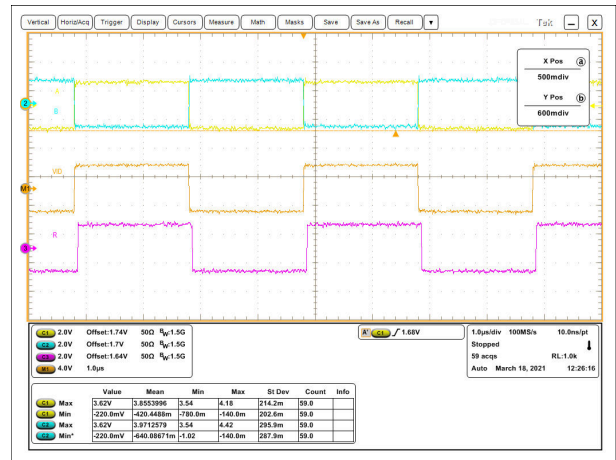
MODE = GND2 $V_{DD} = 3.3V$ $DE = V_{IO}$
LOAD = $54\Omega \parallel 50pF$ $T_A = 25^\circ C$

Figure 6-20. ISOW1412 Driver Propagation Delay - RS485 Mode



MODE = V_{ISOOUT} $V_{DD} = 5V$ $\overline{RE} = GND1$
LOAD = $54\Omega \parallel 50pF$ $T_A = 25^\circ C$

Figure 6-21. ISOW1412 Receiver Propagation Delay - Profibus Mode



MODE = GND2 $V_{DD} = 3.3V$ $\overline{RE} = GND1$
LOAD = $54\Omega \parallel 50pF$ $T_A = 25^\circ C$

Figure 6-22. ISOW1412 Receiver Propagation Delay - RS485 Mode

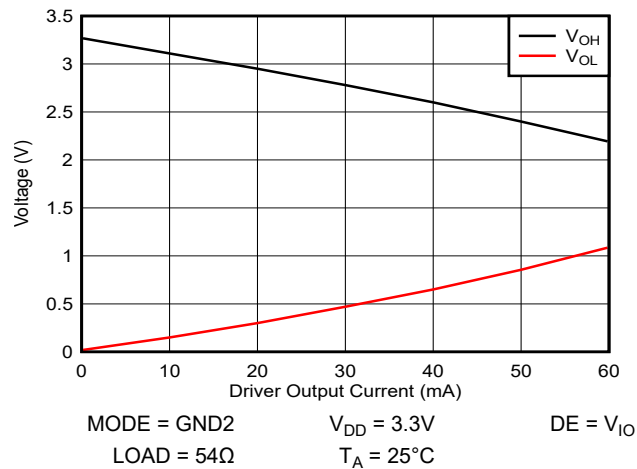


Figure 6-23. ISOW1412 Driver Output Voltage vs Driver Output Current - RS485 Mode

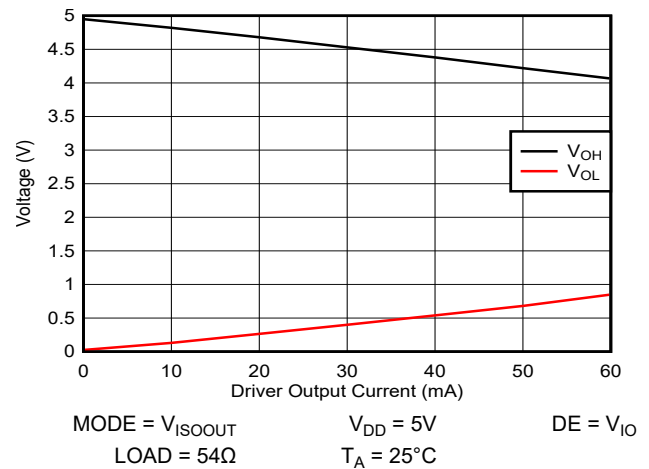


Figure 6-24. ISOW1412 Driver Output Voltage vs Driver Output Current - Profibus Mode

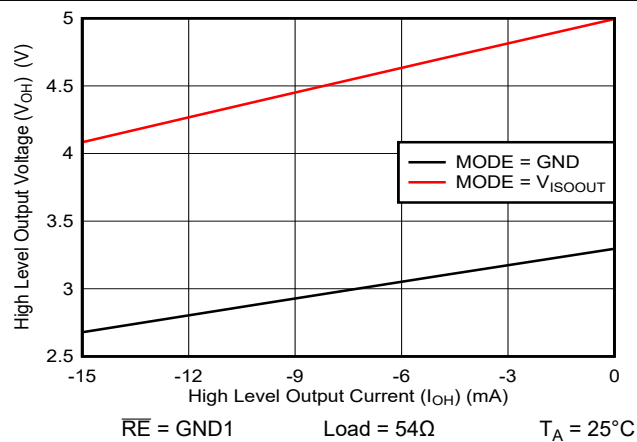


Figure 6-25. ISOW1412 Receiver Buffer High Level Output Voltage vs High Level Output Current - RS485 and Profibus Mode

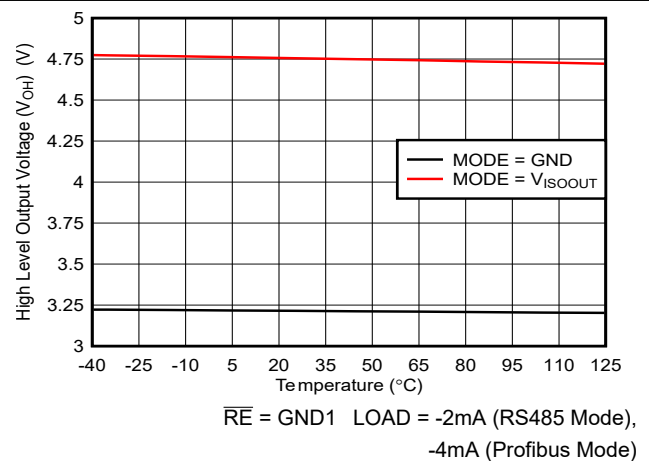


Figure 6-26. ISOW1412 Receiver Buffer High Level Output Voltage vs Temperature - RS485 and Profibus Mode

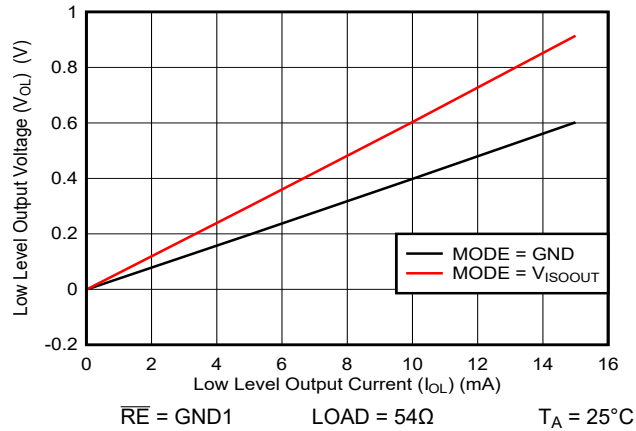


Figure 6-27. ISOW1412 Receiver Buffer Low Level Output Voltage vs Low Level Output Current - RS485 and Profibus Mode

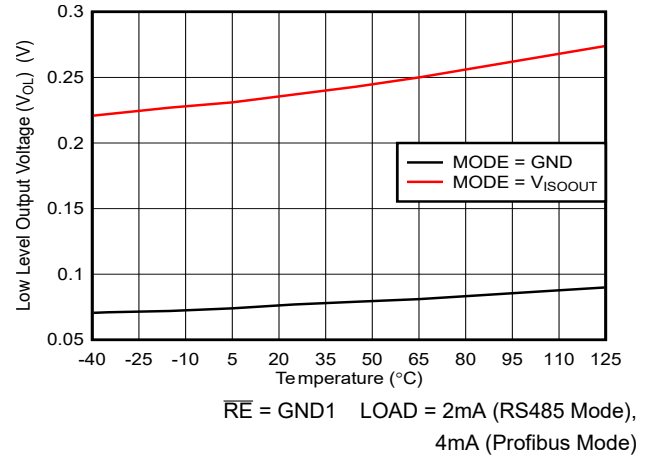


Figure 6-28. ISOW1412 Receiver Buffer Low Level Output Voltage vs Temperature - RS485 and Profibus Mode

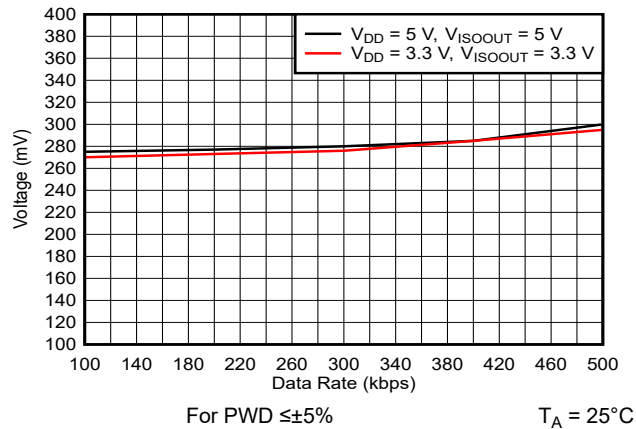


Figure 6-29. ISOW1412 Receiver V_{ID} vs Data Rate - RS485 and Profibus Mode

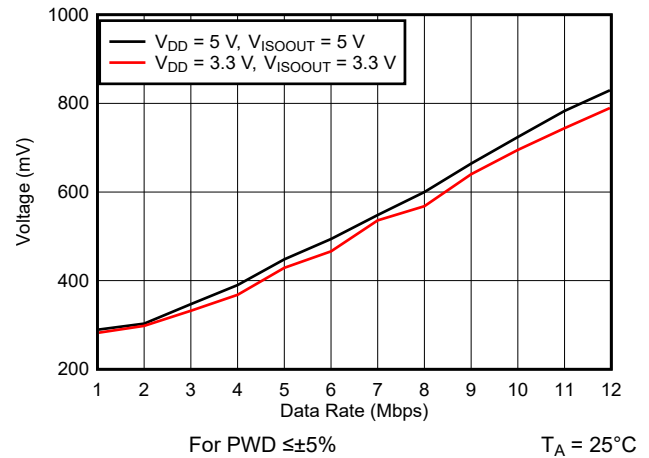
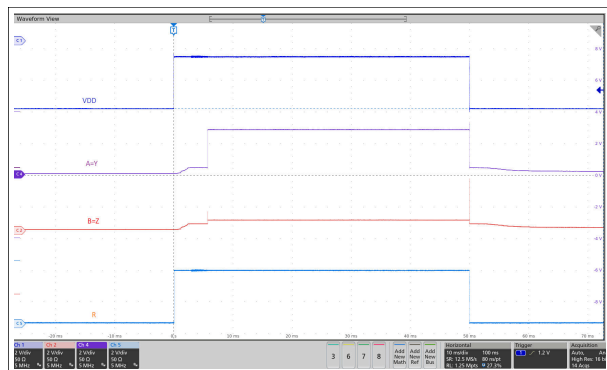
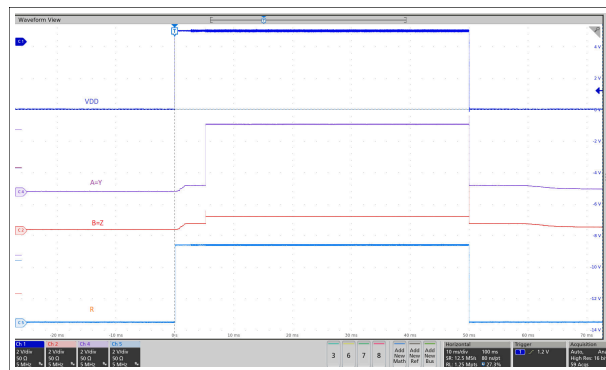


Figure 6-30. ISOW1432 Receiver V_{ID} vs Data Rate - RS485 and Profibus Mode



MODE = GND2 D = V_{IO} DE = V_{IO}
 $\overline{RE}$ = GND1 $T_A = 25^\circ\text{C}$ LOAD = $54\Omega \parallel 50\text{pF}$

Figure 6-31. Glitch-free Power Up/down- RS485 Mode



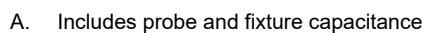
MODE = V_{ISOOUT} D = V_{IO} DE = V_{IO}
 $T_A = 25^\circ\text{C}$ LOAD = $54\Omega \parallel 50\text{pF}$

Figure 6-32. Glitch-free Power Up/down- Profibus Mode

In this section, GND1 = GNDIO, GND2 = GISOIN unless otherwise noted.

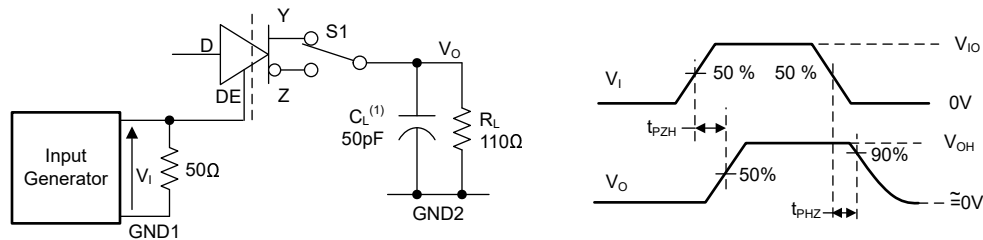


A. C_l includes fixture and instrumentation capacitance



- B. Pass-fail criteria: Device is tested in both half-duplex and full-duplex conditions. Both the signal path and power path must be in a specification compliant region during the application of CMTI pulse. This means no bit flips on R, and both V_{ISOOUT} and Driver V_{OD} must be within specifications mentioned in electrical characteristics table.

Figure 7-4. Common Mode Transient Immunity (CMTI)—Full Duplex



- A. C_L includes fixture and instrumentation capacitance

Figure 7-5. Driver Enable and Disable Times

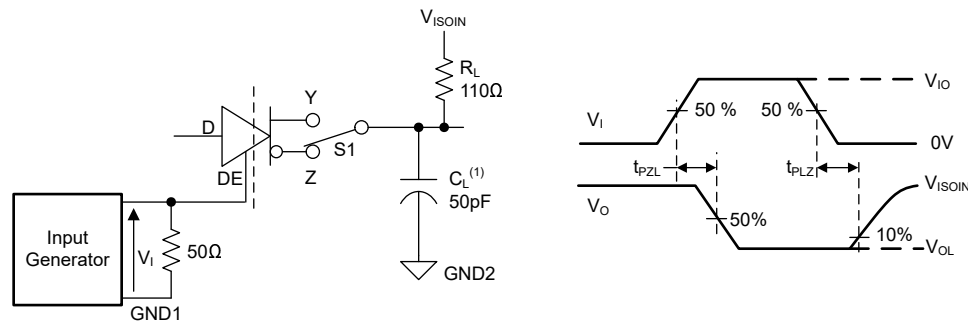
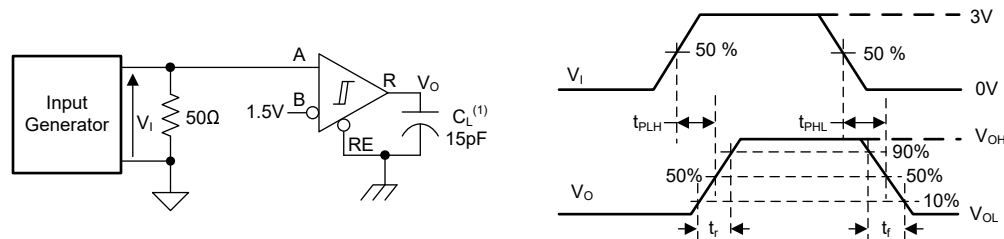


Figure 7-6. Driver Enable and Disable Times



- A. C_L includes fixture and instrumentation capacitance

Figure 7-7. Receiver Switching Specifications

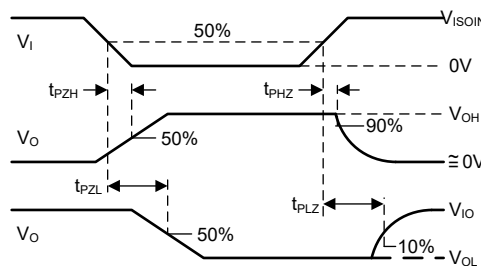


Figure 7-8. Receiver Enable and Disable Times

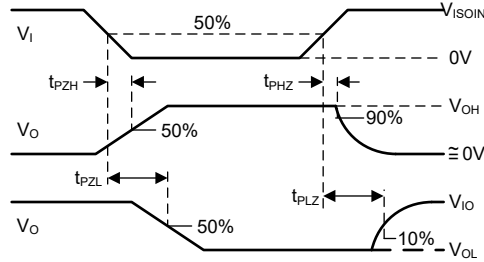
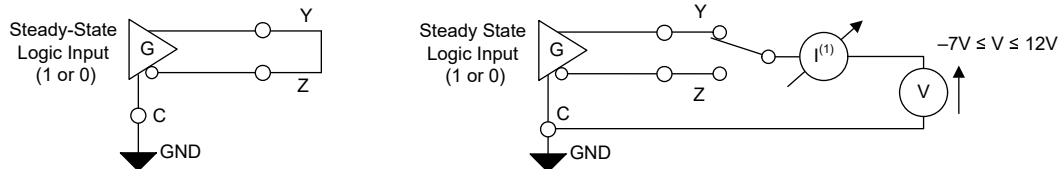
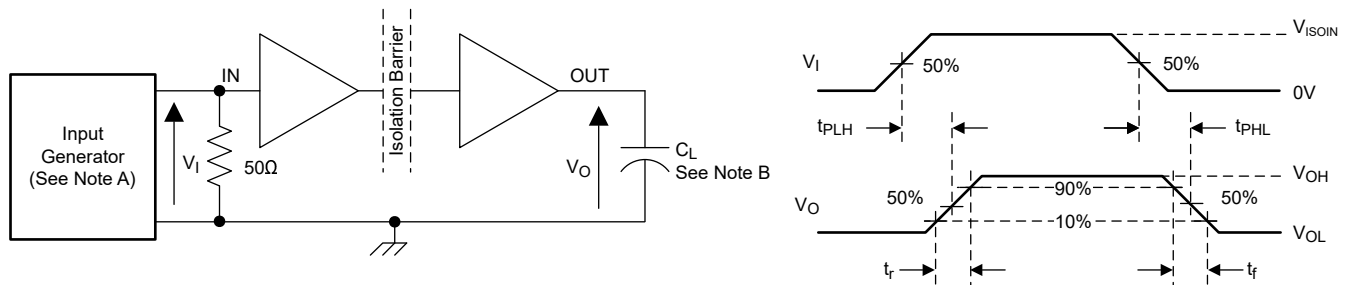


Figure 7-9. Receiver Enable and Disable Times



A. The driver must not sustain any damage with this configuration

Figure 7-10. Short-Circuit Current Limiting



The input pulse is supplied by a generator having the following characteristics: PRR $\leq$ 50kHz, 50% duty cycle, $t_r \leq$ 3ns, $t_f \leq$ 3ns, $Z_O = 50\Omega$. At the input, 50Ω resistor is required to terminate the input generator signal. The resistor is not required in the actual application. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 7-11. GPIO Channel: Switching Characteristics Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The ISOW14x2 family of devices has signal isolation channels, power isolation with integrated transformer and RS-485 transceiver all integrated in one package. ISOW1412 supports maximum signaling rate up to 500kbps, while ISOW1432 is designed for 12Mbps maximum data rate. [Figure 10-1](#) shows functional block diagram of ISOW14x2 family of devices.

8.2 Power Isolation

The integrated isolated DC-DC converter uses advanced circuit and on-chip layout techniques to reduce radiated emissions and achieve up to 46% typical efficiency. The integrated transformer uses thin film polymer as the insulation barrier. Output voltage of power converter can be controlled to 3.3V or 5V using MODE pin. In case bus communication is not needed, the DC-DC converter can be switched off using EN (enable) pin to save power. The output voltage, V_{ISOOUT} , is monitored and feedback information is conveyed to the primary side through a dedicated isolation channel. The duty cycle of the primary switching stage is adjusted accordingly. The fast feedback control loop of the power converter provides low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{IO} , V_{DD} and V_{ISOOUT} supplies which provides robust fails-safe system performance under noisy conditions. An integrated soft-start mechanism provides controlled inrush current and avoids any overshoot on the output during power up.

8.3 Signal Isolation

The integrated signal isolation channels employ an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one state and sends no signal to represent the other state. The receiver demodulates the signal after signal conditioning and produces the output through a buffer stage. The signal-isolation channels incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. [Figure 8-2](#) shows a functional block diagram of a typical signal isolation channel.

To keep any noise coupling from power converter away from signal path, power supplies on side1 for power converter (V_{DD}) and signal path(V_{IO}) are kept separate. Similarly on side2, power converter output (V_{ISOOUT}) needs to be connected to power supply for RS-485 (V_{ISOIN}) externally on PCB. For more details, refer to [Layout guidelines](#) section.

8.4 RS-485

In a typical RS-485 network, multiple nodes can be connected on the bus and the distance of communicating nodes can be as far as 4000-5000 feet. While communicating at such large distances, usual common mode of non-isolated RS-485 transceiver is not sufficient. ISOW14x2 has integrated isolation barrier with up to 1500Vpk working voltage rating. Isolation breaks the ground loop between the communicating nodes and allows for data transfer in the presence of large ground potential differences. These devices have a higher typical differential output voltage (V_{OD}) than traditional transceivers for better noise immunity. A minimum differential output voltage of 2.1V is specified when V_{ISOIN} is configured for 5V supply which meets the requirements for PROFIBUS applications.

The ISOW14x2 family of devices is designed for applications that have limited board space and require more integration. Only external bypass capacitors are needed to fully realize an isolated RS-485 port. This family of devices is also designed for very-high voltage applications, where power transformers for discrete isolated supply meeting the required isolation specifications are bulky and expensive. Though the device family is full-duplex, the device can also be used for half-duplex applications by connecting driver output (Y, Z) to receiver input (A, B) on PCB- this helps to reduce cabling costs. For more details, refer to [Application Information](#).

8.5 Functional Block Diagram

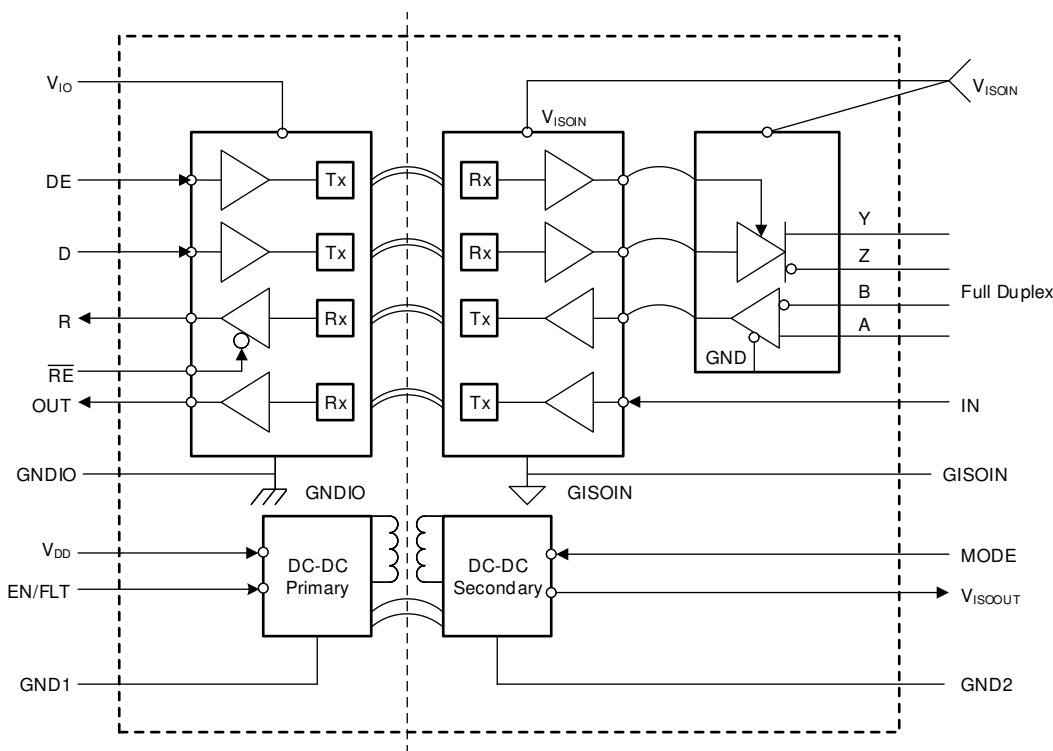


Figure 8-1. Block Diagram

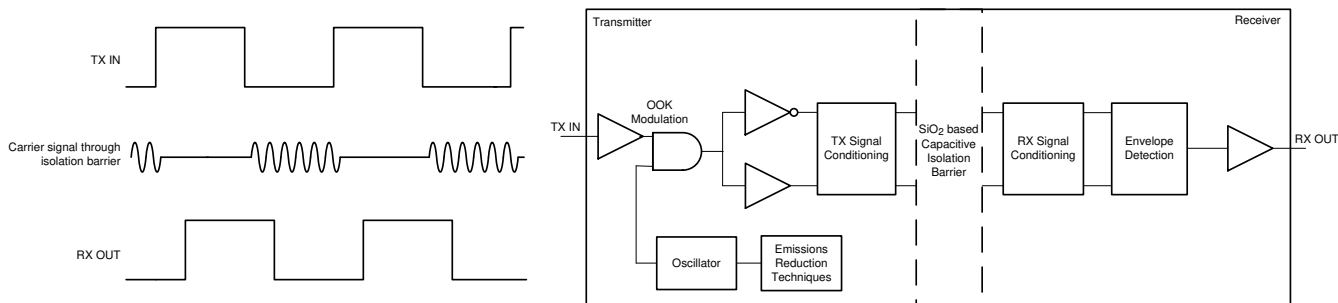


Figure 8-2. Signal Isolation channel

8.6 Feature Description

8.6.1 Power-Up and Power-Down Behavior

The ISOW14x2 family of devices has built-in under-voltage lockout (UVLO) on all supplies (V_{DD} , V_{IO} and V_{ISOOUT}) with positive-going and negative-going thresholds and hysteresis. Both the power converter supply (V_{DD}) and Logic supply (V_{IO}) need to be present for the device to work. If either of them is below UVLO, both the signal path and the power converter are disabled.

Assuming V_{IO} is above UVLO+, when the V_{DD} voltage crosses the positive-going UVLO threshold during power-up, the DC-DC converter initializes and the power converter duty cycle is increased in a controlled manner. This soft-start scheme limits primary peak currents drawn from the V_{DD} supply and charges the V_{ISOOUT} output in a controlled manner, avoiding overshoots. RS-485 driver output is in high impedance state in this duration. When the UVLO positive-going threshold is crossed on the secondary side V_{ISOOUT} pin, the feedback channel starts providing feedback to the primary controller. The regulation loop takes over and RS-485 drive output, Received data output (R) and general purpose logic output (OUT) take the respective states defined by the inputs to the

device, the Driver enable (DE), driver data to be transmitted (D), Receiver enable ($\overline{RE}$) and general purpose logic input (IN) respectively. Designers must consider a sufficient time margin (typically 5ms with 10 μ F load capacitance) to allow this power up sequence before any usable system functionality.

When either of V_{DD} or V_{IO} is lost, the primary side DC-DC controller turns off when the UVLO lower threshold is reached. The V_{ISOOUT} capacitor then discharges depending on the isolation channels and RS-485 load.

8.6.2 Protection Features

The ISOW14x2 family of devices has multiple protection features to create a robust system level design.

- The first feature is an Enable/Fault protection feature. This EN/FLT pin can be used as either an input pin to enable or disable the integrated DC-DC power converter or as an output pin which works as an alert signal if the power converter is not operating properly. In the /Fault use case, a fault is reported if $V_{DD} > 7V$, $V_{DD} < 2.5V$, or if the junction temperature $> 170^{\circ}C$. When a fault is detected, this pin goes low, disabling the DC-DC converter to prevent any damage.

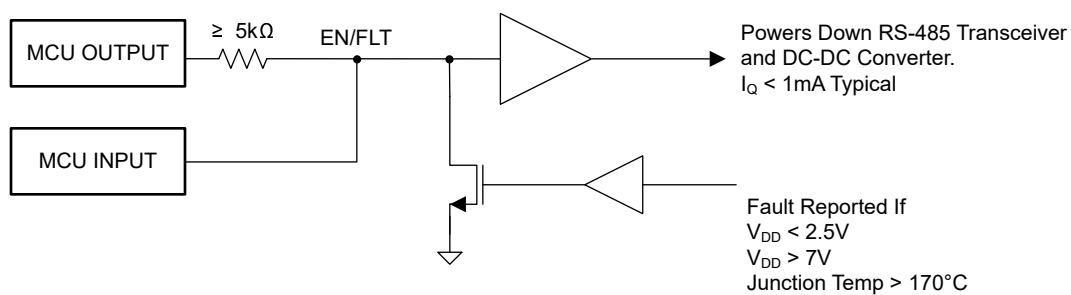


Figure 8-3. EN Fault Pin Diagram

- An over-voltage clamp feature is present on V_{ISOOUT} which clamps the voltage at 6V at Profibus mode ($MODE = V_{ISOOUT}$) or 4V at RS485 mode ($MODE = GND2$), if there is an increase in voltage seen. For device reliability, TI recommends that V_{ISOOUT} stays lower than the over-clamp voltage for device reliability.
- Over-Voltage Lock Out (OVLO) on V_{DD} occurs when a voltage higher than 7V on V_{DD} is seen. At OVLO, the device goes into a low power state and the EN/FLT pin goes low.
- These devices are protected against output overload and short circuit. In cases of overload or short on power converter output V_{ISOOUT} , maximum duty cycle of power converter is limited. In cases of driver bus short circuit due to the external power supply cable shorting to the bus cable, or due to bus contention, short circuit current protection on RS-485 chip restricts the bus current to $\pm 250mA$ maximum.
- Thermal protection is also integrated to help prevent the device from getting damaged under such scenarios. An increase in the die temperature is monitored and the device is disabled when the die temperature becomes $165^{\circ}C$ (typical), thus disabling the short condition. The device is re-enabled when the junction temperature becomes $155^{\circ}C$ (typical). If an overload or output short-circuit condition prevails, this protection cycle is repeated. Care must be taken in the system design to prevent repeated or prolonged exposure to bus shorts as this exposes the device to high junction temperatures for extreme amounts of time affecting device reliability.

8.6.3 Failsafe Receiver

The differential receiver of the ISOW14x2 devices has failsafe protection from invalid bus states caused by:

- Open bus conditions such as a broken cable or a disconnected connector
- Shorted bus conditions such as insulation breakdown of a cable that shorts the twisted-pair
- Idle bus conditions that occur when no driver on the bus is actively driving.

The differential input of the RS-485 receiver is 0 in any of these conditions for a terminated transmission line. The receiver outputs a failsafe logic-high state on R pin so that the output of the receiver is determinate. The receiver thresholds are offset in the receiver design so that the indeterminate range does not include a 0V differential. See [Receiver functional table](#) for more details.

8.6.4 Glitch-Free Power Up and Power Down

Communication on the bus that already exist between a controller node and target node in an RS-485 network must not be disturbed when a new node is swapped in or out of the network. No glitches on the bus must occur when the device is:

- Hot plugged into the network in an unpowered state
- Hot plugged into the network in a powered state and disabled state
- Powered up or powered down in a disabled state when already connected to the bus

The ISOW14x2 devices meet above criteria and do not cause any false data toggling on the bus when powered up or powered down in a disabled state with supply ramp rates $\geq 50\mu\text{s}$.

8.7 Device Functional Modes

Table 8-1 lists the supply configuration for these devices:

Table 8-1. Supply Configuration Function Table

INPUTS				OUTPUT
$V_{DD}^{(1)}$	V_{IO}	EN/FLT	MODE	$V_{ISOOUT}^{(3)}$
$< V_{DD(UVLO+)}$	$> V_{IO(UVLO+)}$	H or Open	X	OFF
$> V_{DD(UVLO+)}$	$< V_{IO(UVLO+)}$		X	Invalid Operation
5V	1.71V to 5.5V		High(shorted to V_{ISOOUT})	5V
5V or 3.3V	1.71V to 5.5V		Low(shorted to GND2) or floating ⁽²⁾	3.3V
3.3V	1.71V to 5.5V		High(shorted to V_{ISOOUT})	Invalid Operation
X	X	L	X	OFF

(1) $V_{DD} = 3.3\text{V}$, MODE shorted to V_{ISOOUT} (essentially $V_{ISOOUT} = 5\text{V}$) is an invalid operation

(2) The MODE pin has a weak pulldown internally. Therefore for $V_{ISOOUT} = 3.3\text{V}$, the MODE pin must be strongly connected to the GND2 pin in noisy system scenarios.

(3) V_{ISOOUT} shorted to V_{ISOIN} on PCB. GND2 and GISOIN pins are shorted to each other and EN=High

Table 8-2 shows the driver functional modes:

Table 8-2. Driver Functional Table

INPUTS					OUTPUTS ⁽³⁾	
$V_{DD}^{(1)}$	V_{IO}	EN/FLT	D	DE	Y	Z
PU	PU	H or Open	H	H	H	L
			L	H	L	H
			X	L	Hi-Z	Hi-Z
			X	Open	Hi-Z	Hi-Z
			Open	H	H	L
		L	X	X	Hi-Z	Hi-Z
PD	PU	X	X	X	Hi-Z	Hi-Z
PU	PD ⁽²⁾	X	X	X	Invalid Operation	

(1) PU=Powered up, PD=Powered down; H=high level; L=Low level; X=Irrelevant; Hi-Z=High impedance state

(2) A strongly driven input signal on D, DE or RE can weakly power the floating V_{IO} through an internal protection diode and cause an undetermined output.

(3) V_{ISOOUT} shorted to V_{ISOIN} on PCB and both GND2 pins are shorted to each other and EN=High

When the driver enable pin, DE, is logic high, the differential outputs, Y and Z, follow the logic states at data input, D. A logic high at the D input causes the Y output to go high and the Z output to go low. Therefore the differential output voltage defined by Equation 1 is positive.

$$V_{OD} = V_Y - V_Z \quad (1)$$

A logic low at the D input causes the Z output to go high and the Y output to go low. Therefore the differential output voltage defined by Equation 1 is negative. A logic low at the DE input causes both outputs to go to the high-impedance (Hi-Z) state. The logic state at the D pin is irrelevant when the DE input is logic low. The DE pin has an internal pulldown resistor to ground. The driver is disabled (bus outputs are in the Hi-Z) by default when the DE pin is left open. The D pin has an internal pullup resistor. The Y output goes high and the Z output goes low when the D pin is left open while the driver enabled.

Table 8-3 shows the receiver functional modes:

Table 8-3. Receiver Functional Table

INPUTS					OUTPUT
V _{DD} ⁽¹⁾	V _{IO}	EN/FLT	Differential Input V _{ID} = V _A - V _B	RE	R ⁽³⁾
PU	PU	H or Open	V _{ID} > V _{IT+}	L	H
			V _{IT-} < V _{ID} < V _{IT+}	L	Indeterminate
			V _{ID} < V _{IT-}	L	L
			X	H	Hi-Z
			X	Open	Hi-Z
			Open, Short, Idle	L	H
PD	PU	L	X	X	H
PD	PU	X	X	X	Hi-Z
PU	PD ⁽²⁾	H or Open	X	X	Invalid Operation
		L	X	X	

(1) PU=Powered up, PD=Powered down; H=high level; L=Low level; X=Irrelevant; Hi-Z=High impedance state

(2) A strongly driven input signal on D, DE or RE can weakly power the floating VIO through an internal protection diode and cause an undetermined output.

(3) V_{ISOOUT} shorted to V_{ISOIN} on PCB and both GND2 pins are shorted to each other and EN/FLT=High

The receiver is enabled when the receiver enable pin, RE, is logic low. The receiver output, R, goes high when the differential input voltage defined by Equation 2 is greater than the positive input threshold, V_{TH+}.

$$V_{ID} = V_A - V_B \quad (2)$$

The receiver output, R, goes low when the differential input voltage defined by Equation 2 is less than the negative input threshold, V_{TH-}. If the V_{ID} voltage is between the V_{TH+} and V_{TH-} thresholds, the output is indeterminate. The receiver output is in the Hi-Z state and the magnitude and polarity of V_{ID} are irrelevant when the RE pin is logic high or left open. The internal biasing of the receiver inputs causes the output to go to a failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Other device feature functional states in shown in Table 8-4 and Table 8-5 below:

Table 8-4. DC-DC Converter Enable/Disable

INPUTS			OUTPUT
V _{DD}	V _{IO}	EN/FLT	V _{ISOOUT}
PU	PU	H or Open	3.3V or 5V depending on MODE pin setting
PU	PU	L	OFF

Table 8-5. General Purpose Logic Input/Output

INPUTS				OUTPUT	Comments
V _{DD} ^{(1) (2)}	V _{IO}	EN/FLT	IN	OUT	
PU	PU	H or Open	H	H	Output channel assumes logic state governed by IN
			L	L	
			Open	L	Default state
		L	X	Hi-Z	Device is in disabled state when either of VDD or VIO is missing
PD	PU	X	X	Hi-Z	
PU	PD	X	X	Invalid Operation	

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L = Logic Low; X = Irrelevant, Hi-Z = High Impedance (OFF) state

(2) V_{ISOOUT} shorted to V_{ISOIN} on PCB. GISOIN and GND2 pins are shorted to each other and EN/FLT=High

8.8 Device I/O Schematics

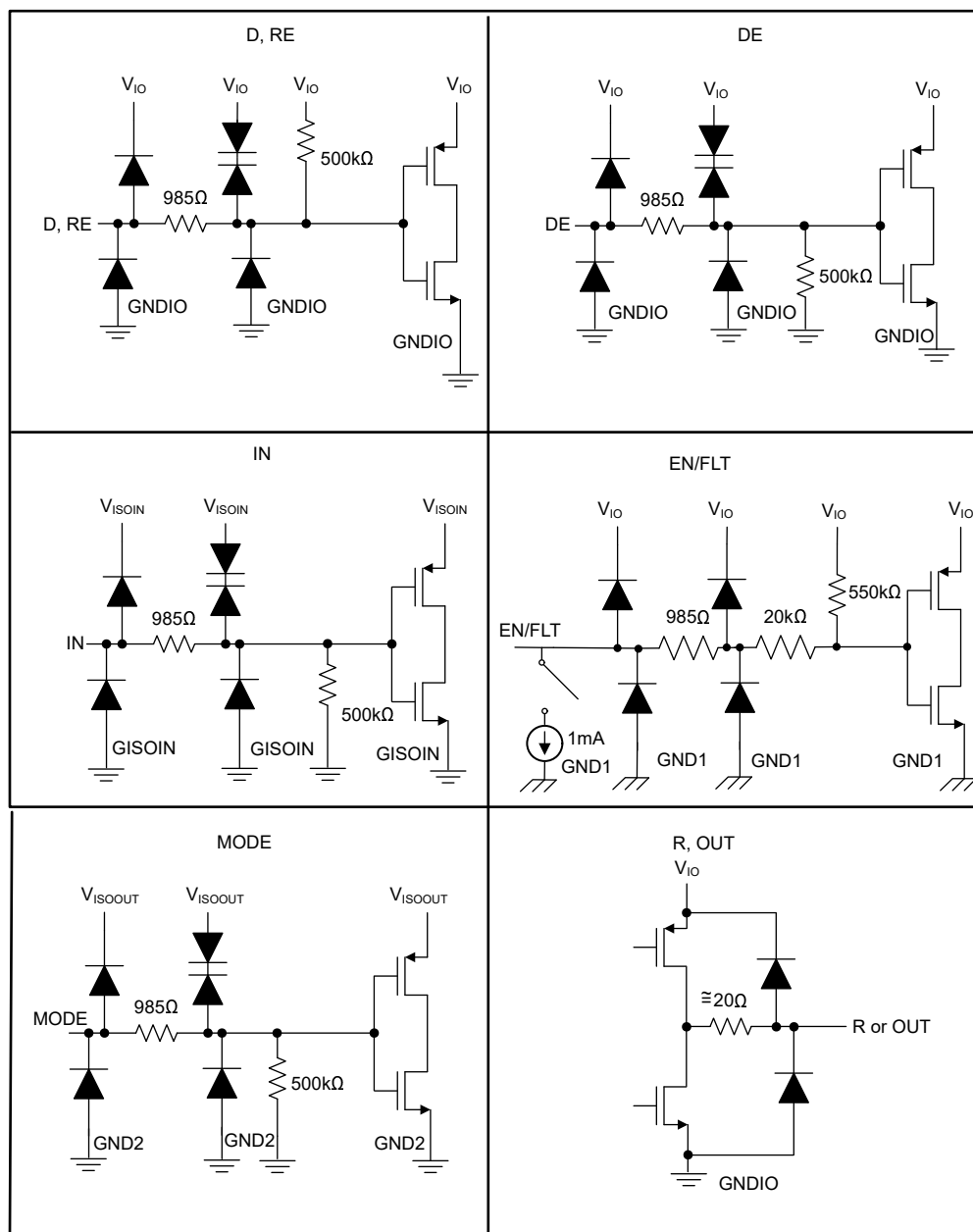


Figure 8-4. Device I/O schematics

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISOW14x2 devices are designed for bidirectional data transfer on multipoint RS-485 networks. An RS-485 bus has multiple transceivers that connect in parallel to a bus cable. Both cable ends are terminated with a termination resistor, R_T , to remove line reflections. The value of R_T matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, lets higher data rates be used over a longer cable length.

Full-duplex implementation shown in [Figure 9-1](#) requires two signal pairs (four wires). Full-duplex implementation lets each node to transmit data on one pair while simultaneously receiving data on the other pair.

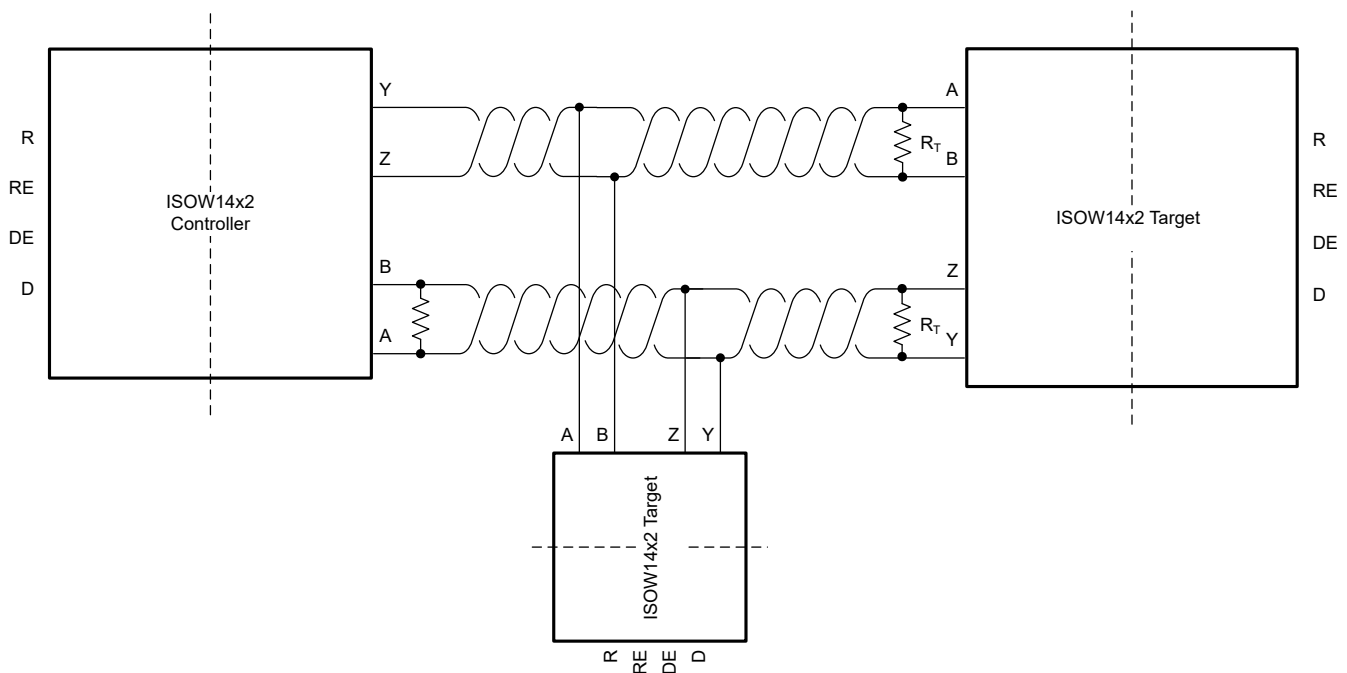


Figure 9-1. Typical RS-485 network with Full-duplex Isolated transceivers

[Figure 9-2](#) below, shows ISOW14x2 devices used in half duplex configuration. Driver outputs Y and Z are shorted to A and B respectively. This reduces overall cabling requirements. Also DE/RE are shorted to each other, and at a time, any node acts as either a driver or a receiver. Split termination is also shown in this configuration which helps to boost network immunity in noisy environments by providing common-mode noise filtering and also reduces radiated emissions by providing low impedance path to earth to the bus common mode excursions.

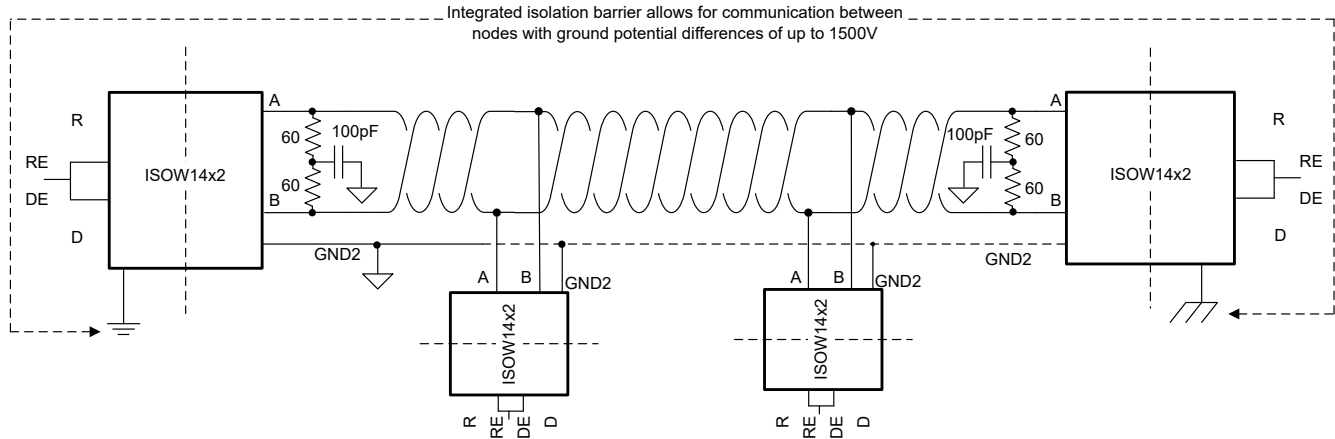
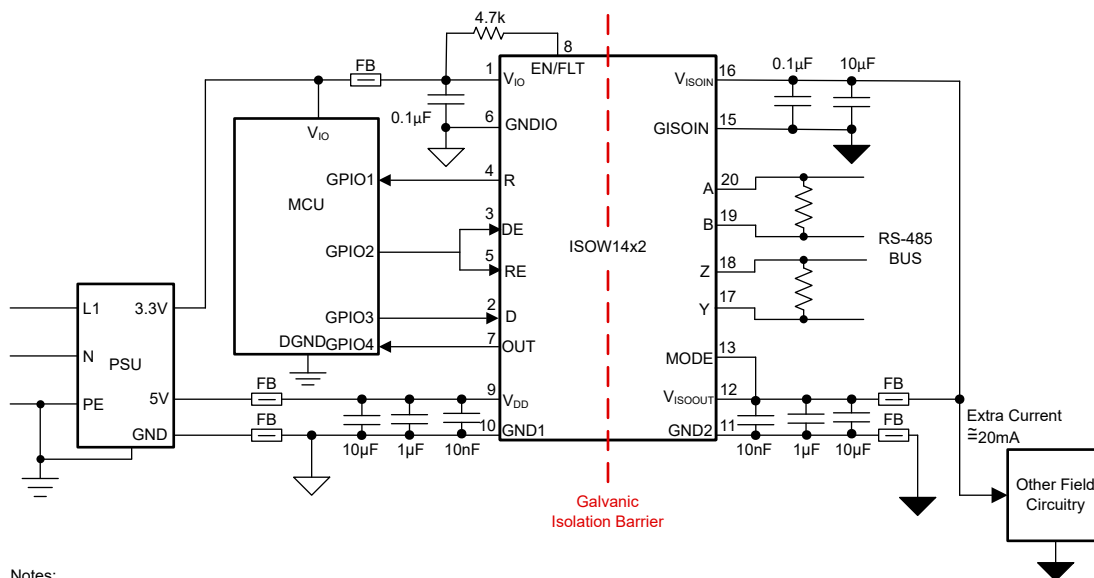


Figure 9-2. Typical RS-485 Network With Half-Duplex Isolated Transceivers

9.2 Typical Application



Notes:

1. Extra current is only available in $V_{DD} = 5V \pm 10\%$ mode.
2. Keep 10nF bypass capacitors close to V_{DD} and V_{ISOOUT} pins ($< 1\text{ mm}$) for optimum radiated emissions performance.
3. GND1 and GNDIO must be shorted directly. GND2 and GISOIN must be shorted directly, or through ferrite beads.

Figure 9-3. Application circuit for ISOW14x2

9.2.1 Design Requirements

Unlike an optocoupler-based design, which requires several external components to improve performance, provide bias, or limit current, the ISOW14x2 devices only require external bypass capacitors to operate as shown in above application diagram. Because of high peak currents flowing through V_{DD} and V_{ISOOUT} supplies, bulk capacitance of minimum 10µF is recommended on both pins. Higher values of bulk capacitors attenuates noise and ripple further, enhancing performance.

9.2.2 Detailed Design Procedure

The RS-485 bus is a robust electrical interface designed for long-distance communications. The RS-485 interface can be used in a wide range of applications with varying requirements of distance of communication, data rate, and number of nodes.

9.2.2.1 Data Rate, Bus Length and Bus Loading

The RS-485 standard has typical curves similar to those shown in Figure 11-4. These curves show the inverse relationship between signaling rate and cable length. If the data rate of the payload between two nodes is lower, the cable length between the nodes can be longer. Use below Figure as a guideline for cable selection, data rate, cable length and subsequent jitter budgeting.

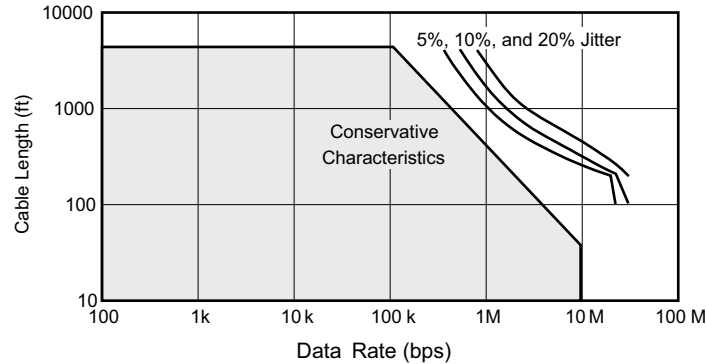


Figure 9-4. Cable Length vs Data Rate Characteristics

The current supplied by the driver must supply into a load because the output of the driver depends on this current. Add transceivers to the bus to increase the total bus loading. The RS-485 standard specifies a hypothetical term of a unit load (UL) to estimate the maximum number of possible bus loads. The UL represents a load impedance of approximately 12kΩ. Standard-compliant drivers must be able to drive 32 of these ULs. The ISOW14x2 devices have 1/8 UL impedance transceiver and can connect up to 256 nodes to the bus.

9.2.2.2 Stub Length

In an RS-485 network, the distance between the transceiver inputs and the cable trunk is known as the stub. The stub must be as short as possible when a node is connected to the bus. Stubs are a non-terminated piece of bus line that can introduce reflections of varying phase as the length of the stub increases. The electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver as a general guideline. Therefore, the maximum physical stub length (L(STUB)) is calculated as shown in Equation 3.

$$L(\text{STUB}) \leq 0.1 \times t_r \times v \times c \quad (3)$$

where:

- t_r is the 10/90 rise time of the driver.
- c is the speed of light ($3 \times 10^8 \text{m/s}$).
- v is the signal velocity of the cable or trace as a factor of c .

9.2.3 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides as shown in below TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that is 20% higher than the specified value.

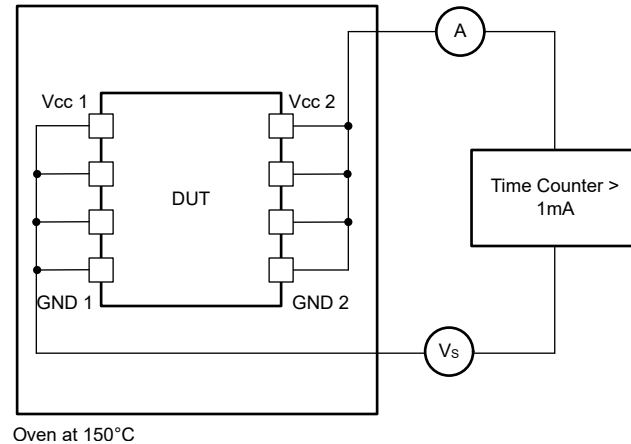


Figure 9-5. Test Setup for Insulation Lifetime Measurement

The insulation lifetime projection data shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDDB data, the intrinsic capability of the insulation is $1000V_{RMS}$ with a lifetime of 1184 years.

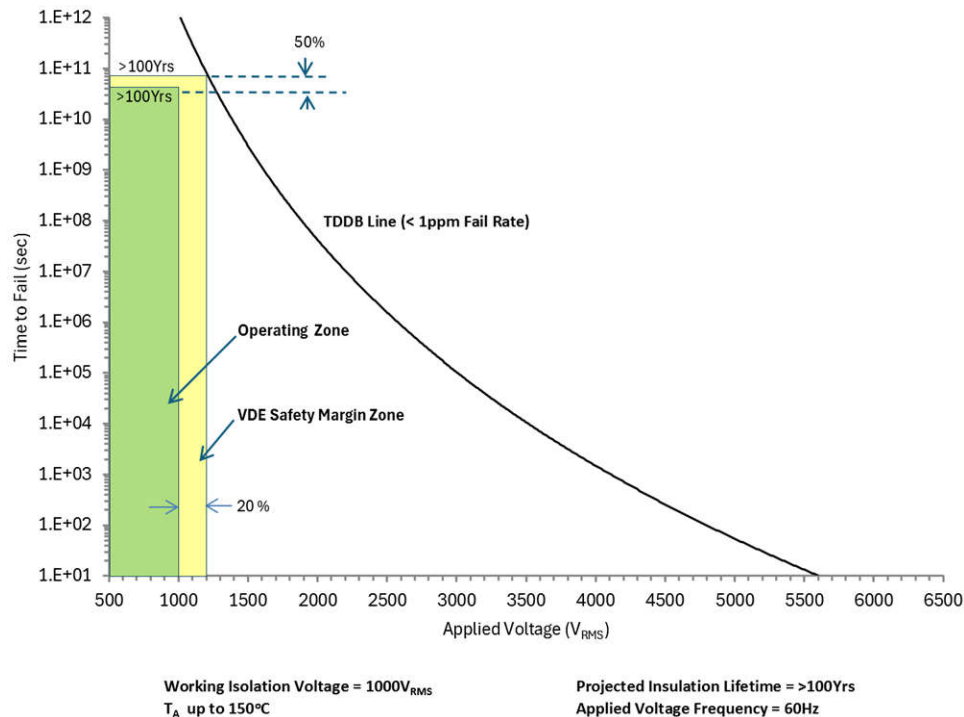


Figure 9-6. Insulation Lifetime Projection Data

9.3 Power Supply Recommendations

To make sure that operation is reliable at all data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible. Power converter input V_{DD} and output V_{ISOOUT} supply pins must have high frequency ceramic capacitors 10nF and bulk capacitors 10 μ F at least close to the pins. Signal path supply pins, V_{IO} and V_{ISOIN} , must have 100nF or higher value ceramic bypass capacitors close to device pins. ISOW1412 can consume typical peak pulse currents of up to 250mA under fully loaded conditions for short durations (10s of μ s) from the power source that is powering V_{DD} of ISOW1412. Please make sure the current limit of upstream power device is at least 300mA typical.

9.4 Layout

9.4.1 Layout Guidelines

Figure 11-1 shows the recommended placement and routing of device bypass capacitors. Below guidelines must be followed to achieve low emissions design:

1. High frequency bypass capacitors 10nF must be placed close to V_{DD} and V_{ISOOUT} pins, less than 1mm distance away from device pins. This is very essential for optimised radiated emissions performance. Verify that these capacitors are 0402 size so that the capacitors offer least inductance (ESL).
2. Bulk capacitors of at least 10 μ F must be placed on power converter input (V_{DD}) and output (V_{ISOOUT}) supply pins.
3. Traces on V_{DD} and GND1 must be symmetric until bypass capacitors. Similarly traces on V_{ISOOUT} and GND2 must be symmetric.
4. Place two 0402 size Ferrite beads (Part number: BLM15EX331SN1) on power supply pins, one between V_{ISOOUT} and V_{ISOIN} and the other between GND2(11) and GISOIN(15), as shown in example PCB layout, so that any high frequency noise from power converter output sees high impedance before reaching other components on PCB.
5. Do not have any metal traces or ground pour within 4mm of power converter output terminals V_{ISOOUT} (pin12) and GND2 (pin11). MODE pin is also in V_{ISOOUT} domain and must be shorted to either pin 11 or pin 12 for output voltage selection.
6. Common mode choke or ferrite beads on bus terminals (Y/Z/A/B) can minimise any high frequency noise that can couple of RS-485 bus cable which can act as antenna and amplify that noise. This improves radiated emissions performance on a system level.
7. Following the layout guidelines of EVM as much as possible is highly recommended for a low radiated emissions design. Reference to the EVM is available in [Related Documentation](#).

9.4.2 Layout Example

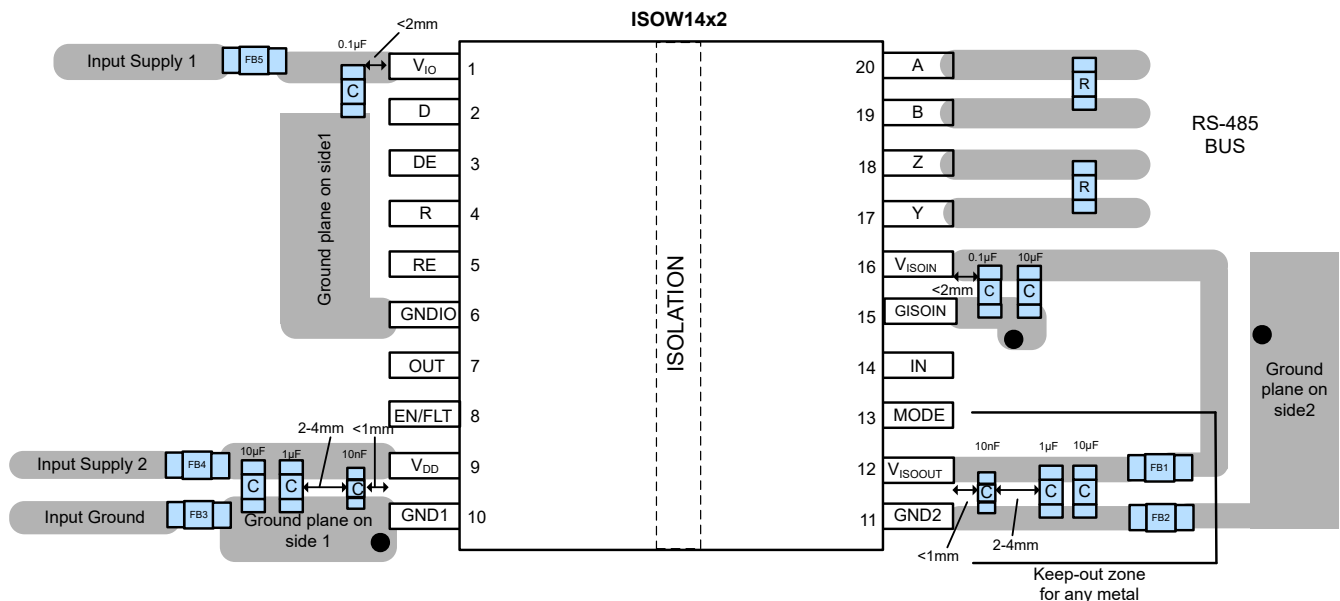


Figure 9-7. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Isolation Glossary application note](#)
- ISOW1412DFM [Evaluation board](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2022) to Revision D (August 2026)	Page
• Added <i>ESD Ratings</i> table.....	6
• Fixed typos in the <i>Power Ratings</i> table and changed ISOW1432 P _{D2} From: 610 mW To: 600 mW.....	8
• Updated <i>Insulation Specifications</i> section per DIN EN IEC 60747-17 (VDE 0884-17).....	9
• Updated the <i>Safety-Related Certifications</i> section to remove content that is found in the associated certificates.....	10
• Updated legacy terminology to "Controller" and "Target" throughout the document.....	33
• Updated the <i>Driver Functional Table</i> in the <i>Device Functional Modes</i> section.....	33
• Updated the <i>Insulation Lifetime</i> section and the <i>Insulation Lifetime Projection Data</i> graph.....	39

Changes from Revision B (October 2021) to Revision C (March 2022)	Page
• Changed ISOW1432 from Advanced Information to Production Data.....	2

Changes from Revision A (May 2021) to Revision B (October 2021)	Page
• Changed ISOW1412 from Advanced Information to Production Data.....	2

Changes from Revision * (May 2018) to Revision A (May 2021)	Page
• Updated datasheet to include ISOW1432 device.....	2

12 Mechanical, Packaging, and Orderable Information

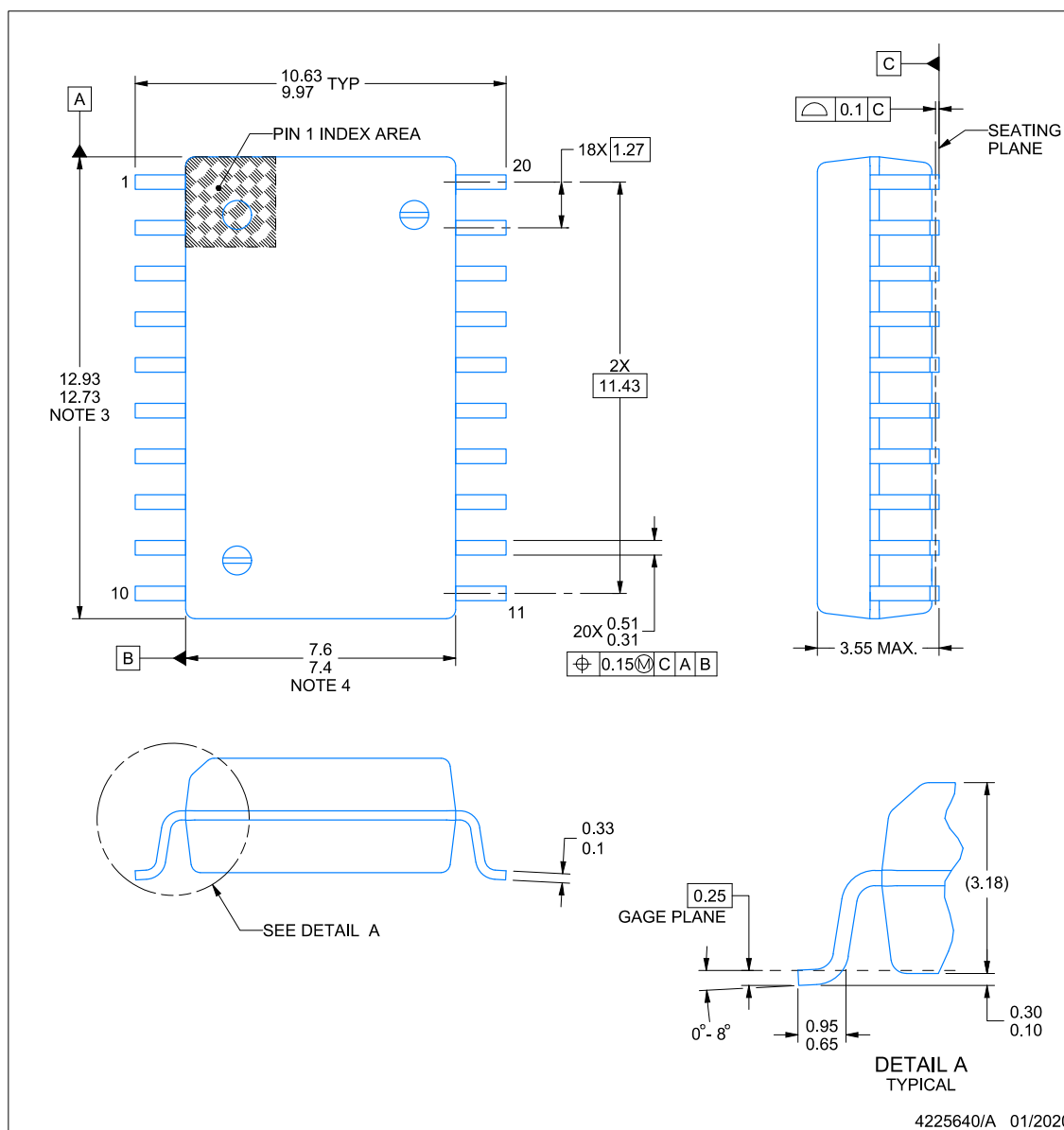
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



NOTES:

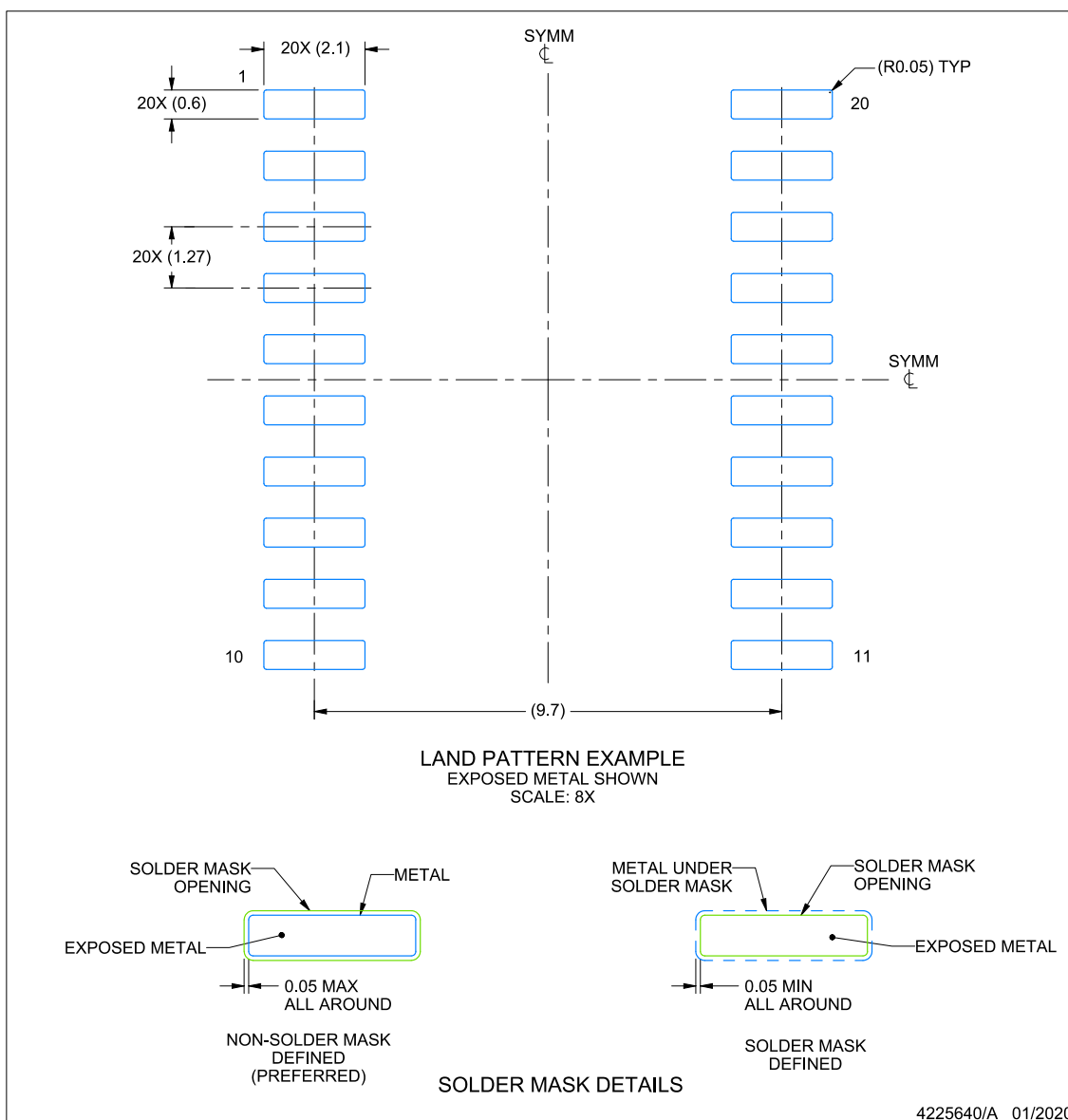
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013

EXAMPLE BOARD LAYOUT

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE

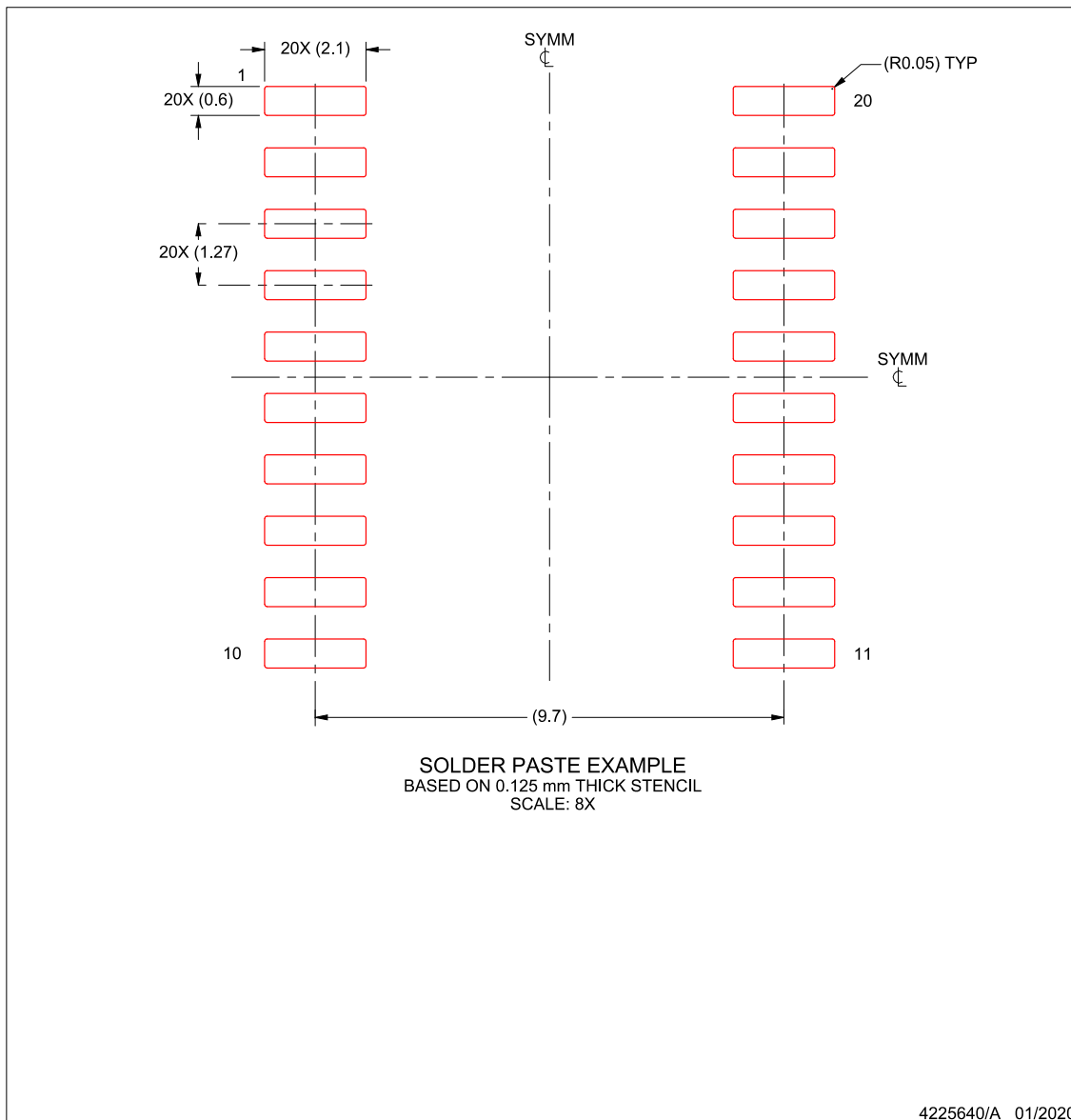


NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN**DFM0020A****SOIC - 3.55 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISOW1412BDFMR	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1412
ISOW1412BDFMR.A	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1412
ISOW1412DFMR	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1412
ISOW1412DFMR.A	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1412
ISOW1412DFMRG4	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1412
ISOW1412DFMRG4.A	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1412
ISOW1432BDFMR	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1432
ISOW1432BDFMR.A	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1432
ISOW1432DFMR	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1432
ISOW1432DFMR.A	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1432
ISOW1432DFMRG4	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1432
ISOW1432DFMRG4.A	Active	Production	SOIC (DFM) 20	850 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1432

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

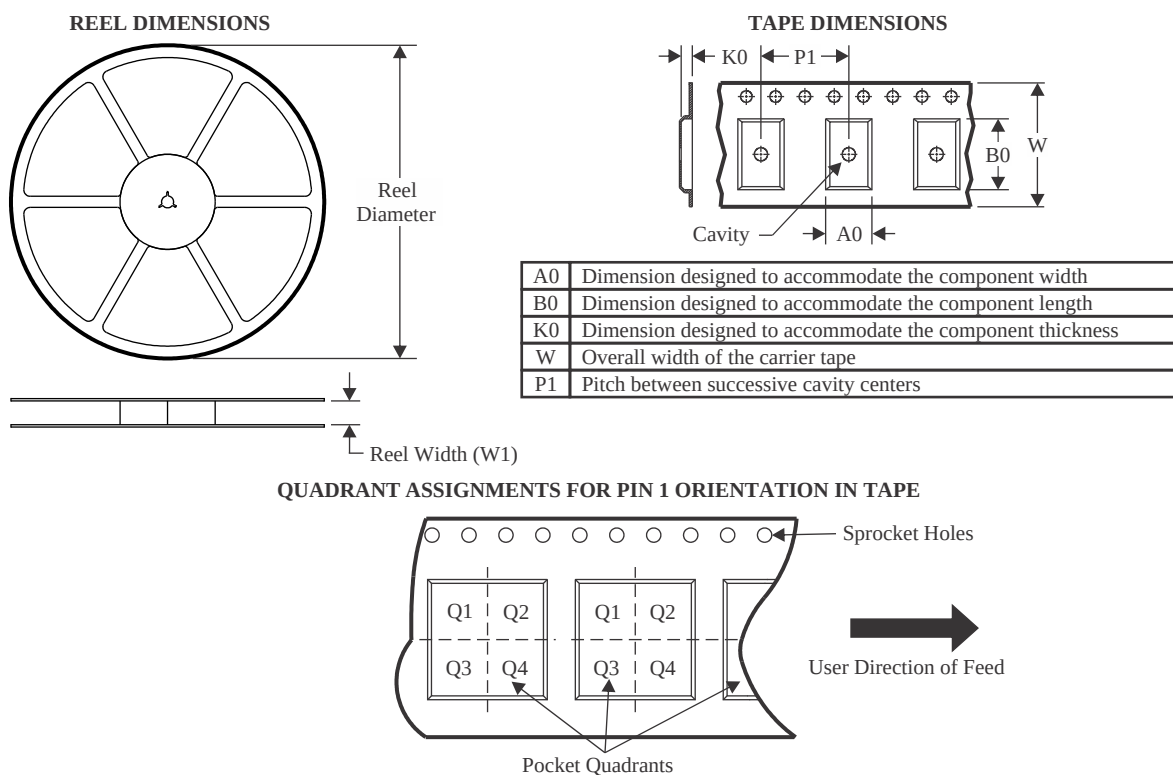
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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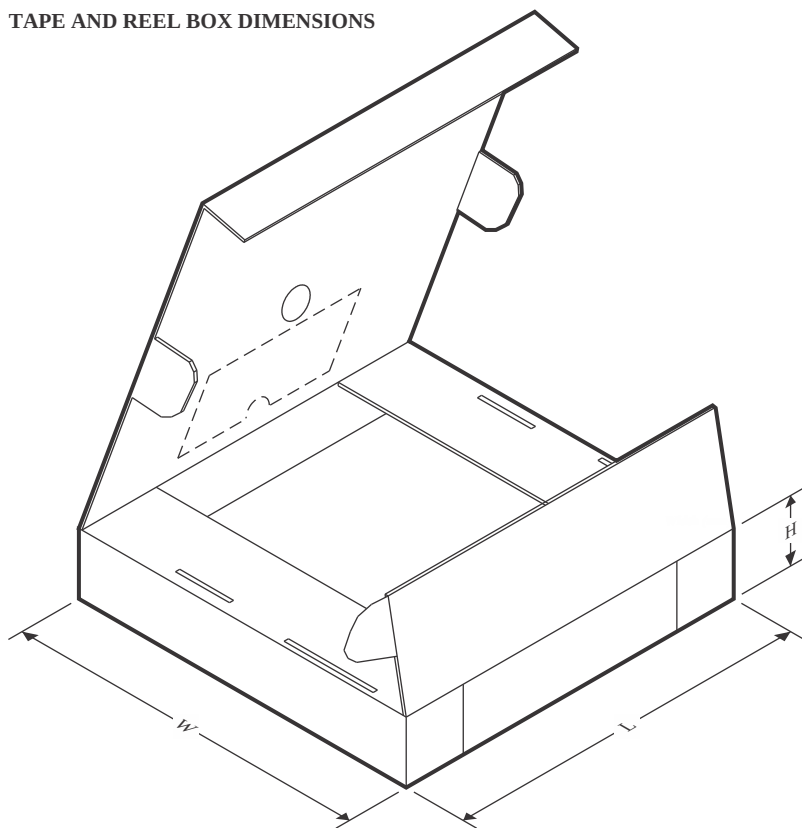
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOW1412BDFMR	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1
ISOW1412DFMR	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1
ISOW1412DFMRG4	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1
ISOW1432BDFMR	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1
ISOW1432DFMR	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1
ISOW1432DFMRG4	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

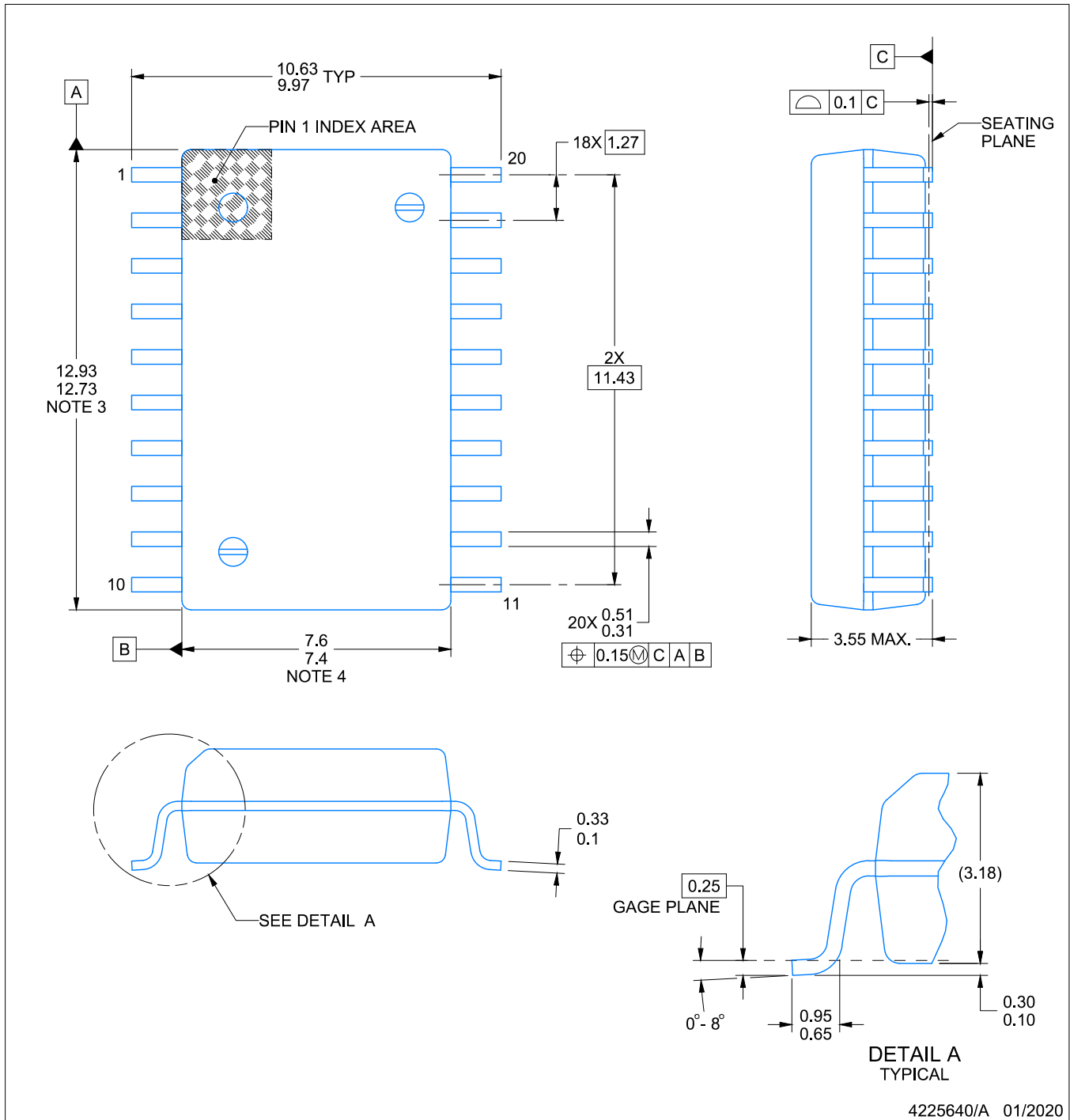
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOW1412BDFMR	SOIC	DFM	20	850	350.0	350.0	43.0
ISOW1412DFMR	SOIC	DFM	20	850	350.0	350.0	43.0
ISOW1412DFMRG4	SOIC	DFM	20	850	350.0	350.0	43.0
ISOW1432BDFMR	SOIC	DFM	20	850	350.0	350.0	43.0
ISOW1432DFMR	SOIC	DFM	20	850	350.0	350.0	43.0
ISOW1432DFMRG4	SOIC	DFM	20	850	350.0	350.0	43.0

PACKAGE OUTLINE

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



4225640/A 01/2020

NOTES:

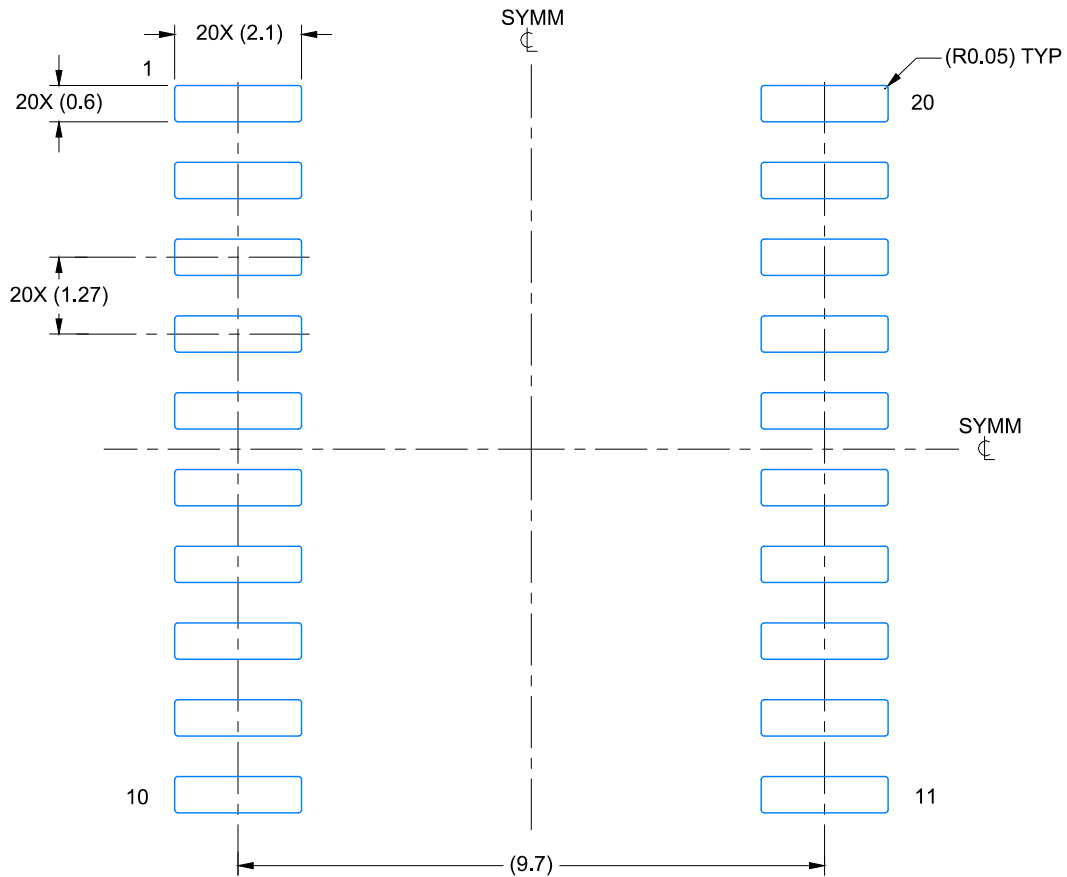
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013

EXAMPLE BOARD LAYOUT

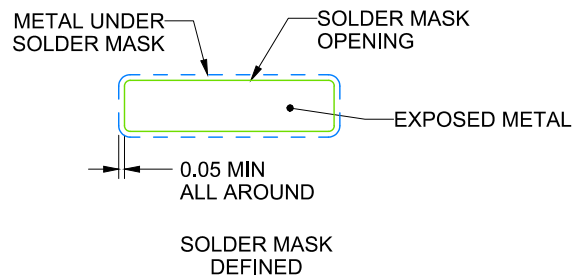
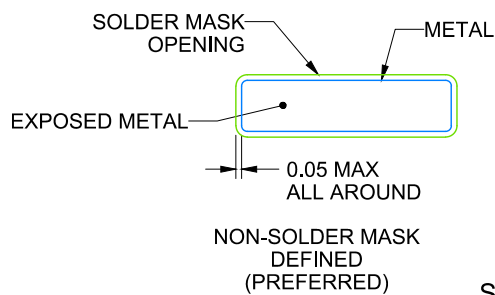
DFM0020A

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SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

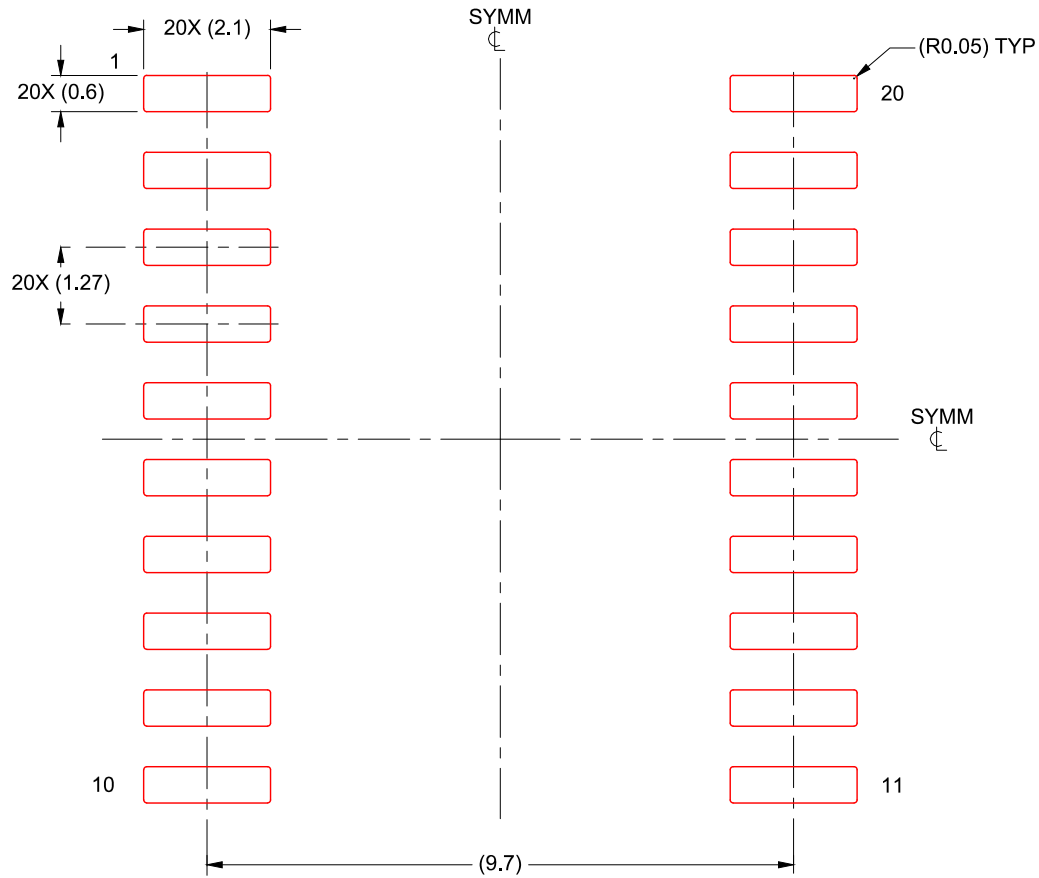
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225640/A 01/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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