

# ISO672x General Purpose Basic Dual-Channel Digital Isolators with Robust EMC

## 1 Features

- [Functional Safety-Capable](#)
  - Documentation available to aid functional safety system design: [ISO6720](#), [ISO6721](#)
- 50-Mbps data rate
- Robust isolation barrier:
  - High lifetime at 450 V<sub>RMS</sub> working voltage
  - Up to 3000 V<sub>RMS</sub> isolation rating
  - ±150 kV/μs typical CMTI
- Wide supply range: 1.71 V to 1.89 V and 2.25 V to 5.5 V
- 1.71-V to 5.5-V level translation
- Default output *High* (ISO672xB) and *Low* (ISO672xFB) Options
- Wide temperature range: –40°C to +125°C
- 1.8 mA per channel typical at 1 Mbps
- Low propagation delay: 11 ns typical
- Robust electromagnetic compatibility (EMC)
  - System-Level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Low emissions
- Narrow-SOIC (D-8) package
- [Safety-Related Certifications](#):
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1
  - GB 4943.1

## 2 Applications

- [Power supplies](#)
- [Grid, Electricity meter](#)
- [Motor drives](#)
- [Factory automation](#)
- [Building automation](#)
- [Lighting](#)
- [Appliances](#)

## 3 Description

The ISO672xB devices are high-performance, dual-channel digital isolators ideal for cost sensitive applications requiring up to 3000 V<sub>RMS</sub> (D package) isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

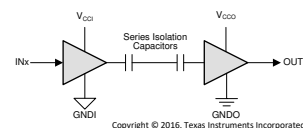
The ISO672xB devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO<sub>2</sub>) insulation barrier. The ISO6720B device has 2 isolation channels with both channels in the same direction. The ISO6721B device has 2 isolation channels with 1 channel in each direction. In the event of input power or signal loss, the default output is *high* for devices without suffix F and *low* for devices with suffix F. See [Device Functional Modes](#) section for further details.

Used in conjunction with isolated power supplies, these devices help prevent noise currents on data buses, such as UART, SPI, RS-485, RS-232, and CAN from damaging sensitive circuitry. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO672xB devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO672xB family of devices is available in a 8-pin SOIC narrow-body (D) package and is a pin-to-pin upgrade to the older generations. For reinforced isolation requirements, refer to the [ISO672x-Q1](#).

### Device Information

| PART NUMBER <sup>(1)</sup> | PACKAGE | BODY SIZE (NOM)   |
|----------------------------|---------|-------------------|
| ISO6720B, ISO6720FB        | D (8)   | 4.90 mm x 3.91 mm |
| ISO6721B, ISO6721FB        |         |                   |
| ISO6721RB, ISO6721RFB      |         |                   |

- (1) For all available packages, see the orderable addendum at the end of the datasheet.



V<sub>CCI</sub>=Input supply, V<sub>CCO</sub>=Output supply  
GNDI=Input ground, GNDO=Output ground

### Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

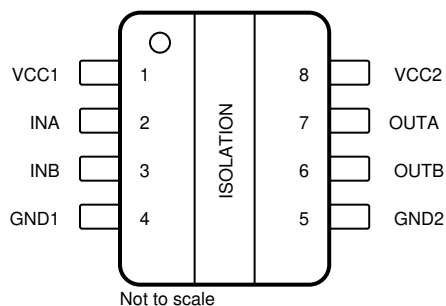
| Changes from Revision E (May 2022) to Revision F (February 2023)                                                                                | Page |
|-------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Changed standard name from: "DIN V VDE V 0884-11:2017-01" to: "DIN EN IEC 60747-17 (VDE 0884-17)" throughout the document.....                | 1    |
| • Removed references to standard IEC/EN/CSA 60950-1 throughout the document.....                                                                | 1    |
| • Updated standards marked as 'planned' to include certificate numbers throughout the document.....                                             | 1    |
| • Removed standard revision and year references from all standard names throughout the document.....                                            | 1    |
| • Added Maximum impulse voltage ( $V_{IMP}$ ) specification per DIN EN IEC 60747-17 (VDE 0884-17).....                                          | 8    |
| • Changed test conditions and values of Maximum surge isolation voltage ( $V_{IOSM}$ ) specification per DIN EN IEC 60747-17 (VDE 0884-17)..... | 8    |
| • Clarified method b test conditions of Apparent charge ( $q_{PD}$ ).....                                                                       | 8    |
| • Changed Maximum surge isolation voltage ( $V_{IOSM}$ ) from 5000 $V_{PK}$ to 6500 $V_{PK}$ .....                                              | 10   |
| • Changed working voltage lifetime margin from 30% to 20% and minimum required insulation lifetime from 26 years to 24 years.....               | 32   |
| • Changed <a href="#">Figure 9-8</a> per DIN EN IEC 60747-17 (VDE 0884-17).....                                                                 | 32   |

| Changes from Revision D (September 2021) to Revision E (May 2022)                                                                                                | Page |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Updated CMTI typical to 150 kV/us and minimum to 100 kV/us.....                                                                                                | 5    |
| • Switched the labels for $V_{CC1}$ falling and $V_{CC2}$ rising in the graph legend of <i>Power Supply Undervoltage Threshold vs Free-Air Temperature</i> ..... | 23   |

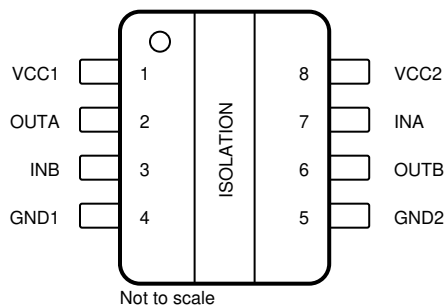
| Changes from Revision C (May 2021) to Revision D (September 2021) | Page |
|-------------------------------------------------------------------|------|
| • Added ISO6721RB device to the data sheet.....                   | 1    |

|                                                                                                                                                                  |                    |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| <b>Changes from Revision B (March 2021) to Revision C (May 2021)</b>                                                                                             | <b>Page</b>        |
| • Updated CISPR 22 to CISPR 32.....                                                                                                                              | <a href="#">27</a> |
| • Updated <i>Insulation Lifetime Projection Data</i> image.....                                                                                                  | <a href="#">32</a> |
| • Updated <i>Power Supply Recommendations</i> document references.....                                                                                           | <a href="#">34</a> |
| • Added the <i>Device Support</i> section.....                                                                                                                   | <a href="#">37</a> |
| <br><b>Changes from Revision A (December 2020) to Revision B (March 2021)</b>                                                                                    | <br><b>Page</b>    |
| • Switched the line colors for $V_{CC}$ at 2.5 V and $V_{CC}$ at 3.3 V in .....                                                                                  | <a href="#">23</a> |
| • Switched the labels for $V_{CC1}$ falling and $V_{CC2}$ rising in the graph legend of <i>Power Supply Undervoltage Threshold vs Free-Air Temperature</i> ..... | <a href="#">23</a> |
| <br><b>Changes from Revision * (July 2020) to Revision A (December 2020)</b>                                                                                     | <br><b>Page</b>    |
| • Changed device status to Production Data.....                                                                                                                  | <a href="#">1</a>  |

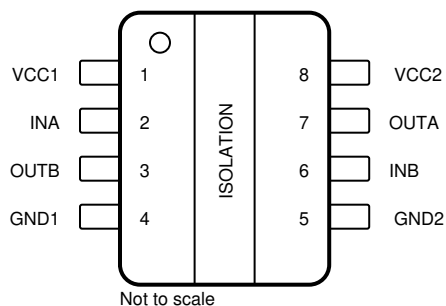
## 5 Pin Configuration and Functions



**Figure 5-1. ISO6720B D Package 8-Pin SOIC Top View**



**Figure 5-2. ISO6721B D Package 8-Pin SOIC Top View**



**Figure 5-3. ISO6721RB D Package 8-Pin SOIC Top View**

**Table 5-1. Pin Functions**

| PIN       |           |          |           | I/O | DESCRIPTION                     |
|-----------|-----------|----------|-----------|-----|---------------------------------|
| NAME      | D PACKAGE |          |           |     |                                 |
|           | ISO6720B  | ISO6721B | ISO6721RB |     |                                 |
| GND1      | 4         | 4        | 4         | —   | Ground connection for $V_{CC1}$ |
| GND2      | 5         | 5        | 5         | —   | Ground connection for $V_{CC2}$ |
| INA       | 2         | 7        | 2         | I   | Input, channel A                |
| INB       | 3         | 3        | 6         | I   | Input, channel B                |
| OUTA      | 7         | 2        | 7         | O   | Output, channel A               |
| OUTB      | 6         | 6        | 3         | O   | Output, channel B               |
| $V_{CC1}$ | 1         | 1        | 1         | —   | Power supply, $V_{CC1}$         |
| $V_{CC2}$ | 8         | 8        | 8         | —   | Power supply, $V_{CC2}$         |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

See<sup>(1)</sup>

|                               |                                                | MIN  | MAX                                   | UNIT |
|-------------------------------|------------------------------------------------|------|---------------------------------------|------|
| Supply Voltage <sup>(2)</sup> | V <sub>CC1</sub> to GND1                       | -0.5 | 6                                     | V    |
|                               | V <sub>CC2</sub> to GND2                       | -0.5 | 6                                     |      |
| Input/Output Voltage          | INx to GNDx                                    | -0.5 | V <sub>CCX</sub> + 0.5 <sup>(3)</sup> | V    |
|                               | OUTx to GNDx                                   | -0.5 | V <sub>CCX</sub> + 0.5 <sup>(3)</sup> |      |
| Output Current                | I <sub>o</sub>                                 | -15  | 15                                    | mA   |
| Temperature                   | Operating junction temperature, T <sub>J</sub> |      | 150                                   | °C   |
|                               | Storage temperature, T <sub>stg</sub>          | -65  | 150                                   | °C   |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values

(3) Maximum voltage must not exceed 6 V.

### 6.2 ESD Ratings

|                    |                         |                                                                                          | VALUE | UNIT |
|--------------------|-------------------------|------------------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±6000 | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±1500 |      |
|                    |                         | Contact discharge per IEC 61000-4-2; Isolation barrier withstand test <sup>(3) (4)</sup> | ±8000 |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.

(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

### 6.3 Recommended Operating Conditions

|                          |                                               |                                                         | MIN                                 | NOM                  | MAX       | UNIT |
|--------------------------|-----------------------------------------------|---------------------------------------------------------|-------------------------------------|----------------------|-----------|------|
| $V_{CC1}$ <sup>(1)</sup> | Supply Voltage Side 1                         | $V_{CC} = 1.8 \text{ V}$ <sup>(3)</sup>                 | 1.71                                |                      | 1.89      | V    |
| $V_{CC1}$ <sup>(1)</sup> | Supply Voltage Side 1                         | $V_{CC} = 2.5 \text{ V to } 5 \text{ V}$ <sup>(3)</sup> | 2.25                                |                      | 5.5       | V    |
| $V_{CC2}$ <sup>(1)</sup> | Supply Voltage Side 2                         | $V_{CC} = 1.8 \text{ V}$ <sup>(3)</sup>                 | 1.71                                |                      | 1.89      | V    |
| $V_{CC2}$ <sup>(1)</sup> | Supply Voltage Side 2                         | $V_{CC} = 2.5 \text{ V to } 5 \text{ V}$ <sup>(3)</sup> | 2.25                                |                      | 5.5       | V    |
| $V_{CC}$ (UVLO+)         | UVLO threshold when supply voltage is rising  |                                                         |                                     | 1.53                 | 1.71      | V    |
| $V_{CC}$ (UVLO-)         | UVLO threshold when supply voltage is falling |                                                         | 1.1                                 | 1.41                 |           | V    |
| $V_{hys}$ (UVLO)         | Supply voltage UVLO hysteresis                |                                                         | 0.08                                | 0.13                 |           | V    |
| $V_{IH}$                 | High level Input voltage                      |                                                         | $0.7 \times V_{CCI}$ <sup>(2)</sup> |                      | $V_{CCI}$ | V    |
| $V_{IL}$                 | Low level Input voltage                       |                                                         | 0                                   | $0.3 \times V_{CCI}$ |           | V    |
| $I_{OH}$                 | High level output current                     | $V_{CCO}$ <sup>(2)</sup> = 5 V                          | -4                                  |                      |           | mA   |
|                          |                                               | $V_{CCO} = 3.3 \text{ V}$                               | -2                                  |                      |           | mA   |
|                          |                                               | $V_{CCO} = 2.5 \text{ V}$                               | -1                                  |                      |           | mA   |
|                          |                                               | $V_{CCO} = 1.8 \text{ V}$                               | -1                                  |                      |           | mA   |
| $I_{OL}$                 | Low level output current                      | $V_{CCO} = 5 \text{ V}$                                 |                                     |                      | 4         | mA   |
|                          |                                               | $V_{CCO} = 3.3 \text{ V}$                               |                                     |                      | 2         | mA   |
|                          |                                               | $V_{CCO} = 2.5 \text{ V}$                               |                                     |                      | 1         | mA   |
|                          |                                               | $V_{CCO} = 1.8 \text{ V}$                               |                                     |                      | 1         | mA   |
| DR                       | Data Rate                                     |                                                         | 0                                   |                      | 50        | Mbps |
| $T_A$                    | Ambient temperature                           |                                                         | -40                                 | 25                   | 125       | °C   |

(1)  $V_{CC1}$  and  $V_{CC2}$  can be set independent of one another

(2)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$

(3) The channel outputs are in undetermined state when  $1.89 \text{ V} < V_{CC1}$ ,  $V_{CC2} < 2.25 \text{ V}$  and  $1.05 \text{ V} < V_{CC1}$ ,  $V_{CC2} < 1.71 \text{ V}$

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | ISO672xB | ISO6721RB | UNIT |
|-------------------------------|----------------------------------------------|----------|-----------|------|
|                               |                                              | D (SOIC) | D (SOIC)  |      |
|                               |                                              | 8 PINS   | 8 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 104.6    | 98.5      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 48.9     | 33.8      | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 52.9     | 47        | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 7.9      | 2.3       | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 52.1     | 46.2      | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | n/a      | n/a       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Power Ratings

| PARAMETER       |                                        | TEST CONDITIONS                                                                                                                        | MIN | TYP | MAX | UNIT |
|-----------------|----------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| ISO6720B        |                                        |                                                                                                                                        |     |     |     |      |
| P <sub>D</sub>  | Maximum power dissipation (both sides) | V <sub>CC1</sub> = V <sub>CC2</sub> = 5.5 V, T <sub>J</sub> = 150°C, C <sub>L</sub> = 15 pF, Input a 25-MHz 50% duty cycle square wave |     |     | 72  | mW   |
| P <sub>D1</sub> | Maximum power dissipation (side-1)     |                                                                                                                                        |     |     | 20  | mW   |
| P <sub>D2</sub> | Maximum power dissipation (side-2)     |                                                                                                                                        |     |     | 52  | mW   |
| ISO6721B        |                                        |                                                                                                                                        |     |     |     |      |
| P <sub>D</sub>  | Maximum power dissipation (both sides) | V <sub>CC1</sub> = V <sub>CC2</sub> = 5.5 V, T <sub>J</sub> = 150°C, C <sub>L</sub> = 15 pF, Input a 25-MHz 50% duty cycle square wave |     |     | 73  | mW   |
| P <sub>D1</sub> | Maximum power dissipation (side-1)     |                                                                                                                                        |     |     | 37  | mW   |
| P <sub>D2</sub> | Maximum power dissipation (side-2)     |                                                                                                                                        |     |     | 37  | mW   |
| ISO6721RB       |                                        |                                                                                                                                        |     |     |     |      |
| P <sub>D</sub>  | Maximum power dissipation (both sides) | V <sub>CC1</sub> = V <sub>CC2</sub> = 5.5 V, T <sub>J</sub> = 150°C, C <sub>L</sub> = 15 pF, Input a 25-MHz 50% duty cycle square wave |     |     | 86  | mW   |
| P <sub>D1</sub> | Maximum power dissipation (side-1)     |                                                                                                                                        |     |     | 43  | mW   |
| P <sub>D2</sub> | Maximum power dissipation (side-2)     |                                                                                                                                        |     |     | 43  | mW   |

## 6.6 Insulation Specifications

| PARAMETER                                        |                                                       | TEST CONDITIONS                                                                                                                                                                                                                                                                                                            | VALUE              | UNIT             |
|--------------------------------------------------|-------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------------------|
|                                                  |                                                       |                                                                                                                                                                                                                                                                                                                            | 8-D                |                  |
| IEC 60664-1                                      |                                                       |                                                                                                                                                                                                                                                                                                                            |                    |                  |
| CLR                                              | External clearance <sup>(1)</sup>                     | Side 1 to side 2 distance through air                                                                                                                                                                                                                                                                                      | >4                 | mm               |
| CPG                                              | External creepage <sup>(1)</sup>                      | Side 1 to side 2 distance across package surface                                                                                                                                                                                                                                                                           | >4                 | mm               |
| DTI                                              | Distance through the insulation                       | Minimum internal gap (internal clearance)                                                                                                                                                                                                                                                                                  | >17                | μm               |
| CTI                                              | Comparative tracking index                            | IEC 60112; UL 746A                                                                                                                                                                                                                                                                                                         | >400               | V                |
|                                                  | Material Group                                        | According to IEC 60664-1                                                                                                                                                                                                                                                                                                   | II                 |                  |
|                                                  | Overvoltage category                                  | Rated mains voltage ≤ 150 V <sub>RMS</sub>                                                                                                                                                                                                                                                                                 | I-IV               |                  |
|                                                  |                                                       | Rated mains voltage ≤ 300 V <sub>RMS</sub>                                                                                                                                                                                                                                                                                 | I-III              |                  |
| DIN EN IEC 60747-17 (VDE 0884-17) <sup>(2)</sup> |                                                       |                                                                                                                                                                                                                                                                                                                            |                    |                  |
| V <sub>IORM</sub>                                | Maximum repetitive peak isolation voltage             | AC voltage (bipolar)                                                                                                                                                                                                                                                                                                       | 637                | V <sub>PK</sub>  |
| V <sub>IOWM</sub>                                | Maximum isolation working voltage                     | AC voltage (sine wave); time-dependent dielectric breakdown (TDDb) test. See <a href="#">Figure 9-8</a>                                                                                                                                                                                                                    | 450                | V <sub>RMS</sub> |
|                                                  |                                                       | DC voltage                                                                                                                                                                                                                                                                                                                 | 637                | V <sub>DC</sub>  |
| V <sub>IOTM</sub>                                | Maximum transient isolation voltage                   | V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production)                                                                                                                                                                                  | 4242               | V <sub>PK</sub>  |
| V <sub>IMP</sub>                                 | Maximum impulse voltage <sup>(3)</sup>                | Tested in air, 1.2/50-us waveform per IEC 62368-1                                                                                                                                                                                                                                                                          | 5000               | V <sub>PK</sub>  |
| V <sub>IOSM</sub>                                | Maximum surge isolation voltage <sup>(4)</sup>        | V <sub>IOSM</sub> ≥ 1.3 x V <sub>IMP</sub> ; Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1                                                                                                                                                                                                        | 6500               | V <sub>PK</sub>  |
| q <sub>pd</sub>                                  | Apparent charge <sup>(5)</sup>                        | Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s                                                                                                                                         | ≤ 5                | pC               |
|                                                  |                                                       | Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.3 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s                                                                                                                                       | ≤ 5                |                  |
|                                                  |                                                       | Method b: At routine test (100% production) and preconditioning (type test); V <sub>ini</sub> = 1.2 x V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s; V <sub>pd(m)</sub> = 1.5 x V <sub>IORM</sub> , t <sub>m</sub> = 1 s (method b1) or V <sub>pd(m)</sub> = V <sub>ini</sub> , t <sub>m</sub> = t <sub>ini</sub> (method b2) | ≤ 5                |                  |
| C <sub>IO</sub>                                  | Barrier capacitance, input to output <sup>(6)</sup>   | V <sub>IO</sub> = 0.4 × sin (2 πft), f = 1 MHz                                                                                                                                                                                                                                                                             | ~0.5               | pF               |
| R <sub>IO</sub>                                  | Insulation resistance, input to output <sup>(6)</sup> | V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C                                                                                                                                                                                                                                                                             | > 10 <sup>12</sup> | Ω                |
|                                                  |                                                       | V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C                                                                                                                                                                                                                                                                    | > 10 <sup>11</sup> |                  |
|                                                  |                                                       | V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C                                                                                                                                                                                                                                                                          | > 10 <sup>9</sup>  |                  |
|                                                  | Pollution degree                                      |                                                                                                                                                                                                                                                                                                                            | 2                  |                  |
|                                                  | Climatic category                                     |                                                                                                                                                                                                                                                                                                                            | 40/125/21          |                  |
| UL 1577                                          |                                                       |                                                                                                                                                                                                                                                                                                                            |                    |                  |
| V <sub>ISO</sub>                                 | Withstand isolation voltage                           | V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1 s (100% production)                                                                                                                                                                                    | 3000               | V <sub>RMS</sub> |

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) ISO672x is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).

- (6) All pins on each side of the barrier tied together creating a two-pin device.

## 6.7 Safety-Related Certifications

| VDE                                                                                                                                                                                      | CSA                                                                                                                                                                                                                                                                                                           | UL                                                           | CQC                                                                                                 | TUV                                                                                                                                                                                                                                |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Certified according to DIN EN IEC 60747-17 (VDE 0884-17)                                                                                                                                 | Certified according to IEC 62368-1, IEC 61010-1 and IEC 60601                                                                                                                                                                                                                                                 | Certified according to UL 1577 Component Recognition Program | Certified according to GB 4943.1                                                                    | Certified according to EN 61010-1 and EN 62368-1                                                                                                                                                                                   |
| Maximum transient isolation voltage, 4242 V <sub>PK</sub> ;<br>Maximum repetitive peak isolation voltage, 637 V <sub>PK</sub> ;<br>Maximum surge isolation voltage, 6500 V <sub>PK</sub> | 400 V <sub>RMS</sub> basic insulation per CSA 62368-1 and IEC 62368-1; 300 V <sub>RMS</sub> basic insulation per CSA 61010-1 and IEC 61010-1 (pollution degree 2, material group III)<br>1 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V <sub>RMS</sub> (D-8) max working voltage | Single protection, 3000 V <sub>RMS</sub>                     | Basic insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V <sub>RMS</sub> maximum working voltage | 3000 V <sub>RMS</sub> (D-8) Basic insulation per EN 61010-1 up to working voltage of 300 V <sub>RMS</sub> (D-8)<br>3000 V <sub>RMS</sub> (D-8) basic insulation per EN 62368-1 up to working voltage of 400 V <sub>RMS</sub> (D-8) |
| Certificate number: 40047657                                                                                                                                                             | Master contract number: 220991                                                                                                                                                                                                                                                                                | File number: E181974                                         | Certificate number: CQC21001305151                                                                  | Client ID number: 077311                                                                                                                                                                                                           |

## 6.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER                     |                                                        | TEST CONDITIONS                                                                                                                        | MIN | TYP | MAX   | UNIT |
|-------------------------------|--------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-------|------|
| <b>D-8 PACKAGE - ISO672xB</b> |                                                        |                                                                                                                                        |     |     |       |      |
| I <sub>S</sub>                | Safety input, output, or supply current <sup>(1)</sup> | R <sub>θJA</sub> = 104.6°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C<br>See <a href="#">Figure 6-1</a>  |     |     | 217.2 | mA   |
|                               |                                                        | R <sub>θJA</sub> = 104.6°C/W, V <sub>I</sub> = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C<br>See <a href="#">Figure 6-1</a>  |     |     | 332   | mA   |
|                               |                                                        | R <sub>θJA</sub> = 104.6°C/W, V <sub>I</sub> = 2.75 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C<br>See <a href="#">Figure 6-1</a> |     |     | 434.5 | mA   |
|                               |                                                        | R <sub>θJA</sub> = 104.6°C/W, V <sub>I</sub> = 1.89 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C<br>See <a href="#">Figure 6-1</a> |     |     | 628.9 | mA   |
| P <sub>S</sub>                | Safety input, output, or total power <sup>(1)</sup>    | R <sub>θJA</sub> = 104.6°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C<br>See <a href="#">Figure 6-2</a>                          |     |     | 1195  | mW   |
| T <sub>S</sub>                | Maximum safety temperature <sup>(1)</sup>              |                                                                                                                                        |     |     | 150   | °C   |

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER                      |                                                        | TEST CONDITIONS                                                                                                                       | MIN | TYP | MAX   | UNIT |
|--------------------------------|--------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-------|------|
| <b>D-8 PACKAGE - ISO6721RB</b> |                                                        |                                                                                                                                       |     |     |       |      |
| I <sub>S</sub>                 | Safety input, output, or supply current <sup>(1)</sup> | R <sub>θJA</sub> = 98.5°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C<br>See <a href="#">Figure 6-3</a>  |     |     | 230.7 | mA   |
|                                |                                                        | R <sub>θJA</sub> = 98.5°C/W, V <sub>I</sub> = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C<br>See <a href="#">Figure 6-3</a>  |     |     | 352.5 | mA   |
|                                |                                                        | R <sub>θJA</sub> = 98.5°C/W, V <sub>I</sub> = 2.75 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C<br>See <a href="#">Figure 6-3</a> |     |     | 461.5 | mA   |
|                                |                                                        | R <sub>θJA</sub> = 98.5°C/W, V <sub>I</sub> = 1.89 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C<br>See <a href="#">Figure 6-3</a> |     |     | 671.4 | mA   |
| P <sub>S</sub>                 | Safety input, output, or total power <sup>(1)</sup>    | R <sub>θJA</sub> = 98.5°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C<br>See <a href="#">Figure 6-4</a>                          |     |     | 1269  | mW   |
| T <sub>S</sub>                 | Maximum safety temperature <sup>(1)</sup>              |                                                                                                                                       |     |     | 150   | °C   |

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T<sub>J</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P, where P is the power dissipated in the device.

T<sub>J(max)</sub> = T<sub>S</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P<sub>S</sub>, where T<sub>J(max)</sub> is the maximum allowed junction temperature.

P<sub>S</sub> = I<sub>S</sub> × V<sub>I</sub>, where V<sub>I</sub> is the maximum input voltage.

## 6.9 Electrical Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER     | TEST CONDITIONS                                                                                                                                               | MIN                  | TYP                        | MAX | UNIT          |
|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------------|-----|---------------|
| $V_{OH}$      | High-level output voltage<br>$I_{OH} = -4\text{ mA}$ ; See <a href="#">Figure 7-1</a>                                                                         | $V_{CCO} - 0.4$      |                            |     | V             |
| $V_{OL}$      | Low-level output voltage<br>$I_{OL} = 4\text{ mA}$ ; See <a href="#">Figure 7-1</a>                                                                           |                      |                            | 0.4 | V             |
| $V_{IT+(IN)}$ | Rising input switching threshold                                                                                                                              |                      | $0.7 \times V_{CCI}^{(1)}$ |     | V             |
| $V_{IT-(IN)}$ | Falling input switching threshold                                                                                                                             | $0.3 \times V_{CCI}$ |                            |     | V             |
| $V_{I(HYS)}$  | Input threshold voltage hysteresis                                                                                                                            | $0.1 \times V_{CCI}$ |                            |     | V             |
| $I_{IH}$      | High-level input current<br>$V_{IH} = V_{CCI}^{(1)}$ at INx                                                                                                   |                      |                            | 10  | $\mu\text{A}$ |
| $I_{IL}$      | Low-level input current<br>$V_{IL} = 0\text{ V}$ at INx                                                                                                       | -10                  |                            |     | $\mu\text{A}$ |
| CMTI          | Common mode transient immunity<br>$V_I = V_{CC}$ or 0 V, $V_{CM} = 1200\text{ V}$                                                                             | 100                  | 150                        |     | kV/us         |
| $C_i$         | Input Capacitance <sup>(2)</sup><br>$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 2\text{ MHz}$ , $V_{CC} = 5\text{ V}$ ; See <a href="#">Figure 7-3</a> |                      | 2.8                        |     | pF            |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$

(2) Measured from input pin to same side ground.

## 6.10 Supply Current Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                                                                 |         | SUPPLY CURRENT     | MIN | TYP | MAX | UNIT |
|-------------------------------------------|---------------------------------------------------------------------------------|---------|--------------------|-----|-----|-----|------|
| ISO6720B                                  |                                                                                 |         |                    |     |     |     |      |
| Supply current - DC signal <sup>(2)</sup> | $V_I = V_{CCI}$ <sup>(1)</sup> (ISO6720B), $V_I = 0$ V (ISO6720B with F suffix) |         | $I_{CC1}$          |     | 1.1 | 1.7 | mA   |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 1.3 | 2.1 |      |
|                                           | $V_I = 0$ V (ISO6720B), $V_I = V_{CC1}$ (ISO6720B with F suffix)                |         | $I_{CC1}$          |     | 3.2 | 4.6 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 1.4 | 2.3 |      |
| Supply current - AC signal <sup>(3)</sup> | All channels switching with square wave clock input; $C_L = 15$ pF              | 1 Mbps  | $I_{CC1}$          |     | 2.1 | 3.1 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 1.5 | 2.3 |      |
|                                           |                                                                                 | 10 Mbps | $I_{CC1}$          |     | 2.2 | 3.2 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 2.7 | 3.6 |      |
|                                           |                                                                                 | 50 Mbps | $I_{CC1}$          |     | 2.5 | 3.6 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 7.9 | 9.5 |      |
| ISO6721B                                  |                                                                                 |         |                    |     |     |     |      |
| Supply current - DC signal <sup>(2)</sup> | $V_I = V_{CCI}$ <sup>(1)</sup> (ISO6721B); $V_I = 0$ V (ISO6721B with F suffix) |         | $I_{CC1}, I_{CC2}$ |     | 1.2 | 2.1 | mA   |
|                                           | $V_I = 0$ V (ISO6721B); $V_I = V_{CCI}$ (ISO6721B with F suffix)                |         | $I_{CC1}, I_{CC2}$ |     | 2.3 | 3.5 |      |
| Supply current - AC signal <sup>(3)</sup> | All channels switching with square wave clock input; $C_L = 15$ pF              | 1 Mbps  | $I_{CC1}, I_{CC2}$ |     | 1.9 | 2.9 |      |
|                                           |                                                                                 | 10 Mbps | $I_{CC1}, I_{CC2}$ |     | 2.5 | 3.6 |      |
|                                           |                                                                                 | 50 Mbps | $I_{CC1}, I_{CC2}$ |     | 5.2 | 6.7 |      |

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER                         | TEST CONDITIONS                                                            | SUPPLY CURRENT     | MIN | TYP | MAX | UNIT |
|-----------------------------------|----------------------------------------------------------------------------|--------------------|-----|-----|-----|------|
| <b>ISO6721RB</b>                  |                                                                            |                    |     |     |     |      |
| Supply current - DC signal<br>(2) | $V_I = V_{CCI}$ (1)(ISO6721R); $V_I = 0\text{ V}$ (ISO6721R with F suffix) | $I_{CC1}, I_{CC2}$ |     | 2.1 | 3.3 | mA   |
|                                   | $V_I = 0\text{ V}$ (ISO6721R); $V_I = V_{CCI}$ (ISO6721R with F suffix)    | $I_{CC1}, I_{CC2}$ |     | 3.2 | 4.7 |      |
| Supply current - AC signal<br>(3) | All channels switching with square wave clock input; $C_L = 15\text{ pF}$  | 1 Mbps             |     | 2.7 | 4.1 |      |
|                                   |                                                                            | 10 Mbps            |     | 3.3 | 4.7 |      |
|                                   |                                                                            | 50 Mbps            |     | 6.0 | 7.7 |      |

(1)  $V_{CCI} = \text{Input-side } V_{CC}$ 

(2) Supply current valid for  $ENx = V_{CCx}$  and  $ENx = 0\text{ V}$ 

(3) Supply current valid for  $ENx = V_{CCx}$

## 6.11 Electrical Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER     |                                    | TEST CONDITIONS                                                                                                                | MIN                        | TYP | MAX | UNIT          |
|---------------|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|----------------------------|-----|-----|---------------|
| $V_{OH}$      | High-level output voltage          | $I_{OH} = -2\text{mA}$ ; See <a href="#">Figure 7-1</a>                                                                        | $V_{CCO} - 0.2$            |     |     | V             |
| $V_{OL}$      | Low-level output voltage           | $I_{OL} = 2\text{mA}$ ; See <a href="#">Figure 7-1</a>                                                                         | 0.2                        |     |     | V             |
| $V_{IT+(IN)}$ | Rising input switching threshold   |                                                                                                                                | $0.7 \times V_{CCI}^{(1)}$ |     |     | V             |
| $V_{IT-(IN)}$ | Falling input switching threshold  |                                                                                                                                | $0.3 \times V_{CCI}$       |     |     | V             |
| $V_{I(HYS)}$  | Input threshold voltage hysteresis |                                                                                                                                | $0.1 \times V_{CCI}$       |     |     | V             |
| $I_{IH}$      | High-level input current           | $V_{IH} = V_{CCI}^{(1)}$ at INx                                                                                                | 10                         |     |     | $\mu\text{A}$ |
| $I_{IL}$      | Low-level input current            | $V_{IL} = 0 \text{ V}$ at INx                                                                                                  | -10                        |     |     | $\mu\text{A}$ |
| CMTI          | Common mode transient immunity     | $V_I = V_{CC}$ or $0 \text{ V}$ , $V_{CM} = 1200 \text{ V}$                                                                    | 100                        | 150 |     | kV/us         |
| $C_i$         | Input Capacitance <sup>(2)</sup>   | $V_I = V_{CC}/2 + 0.4 \times \sin(2\pi f t)$ , $f = 2 \text{ MHz}$ , $V_{CC} = 3.3 \text{ V}$ ; See <a href="#">Figure 7-3</a> |                            | 2.8 |     | pF            |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$

(2) Measured from input pin to same side ground.

## 6.12 Supply Current Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                                                                                                                                                                                              |         | SUPPLY CURRENT                      | MIN | TYP | MAX | UNIT |
|-------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-------------------------------------|-----|-----|-----|------|
| ISO6720B                                  |                                                                                                                                                                                                              |         |                                     |     |     |     |      |
| Supply current - DC signal <sup>(2)</sup> | V <sub>I</sub> = V <sub>CC1</sub> <sup>(1)</sup> (ISO6720B), V <sub>I</sub> = 0 V (ISO6720B with F suffix)                                                                                                   |         | I <sub>CC1</sub>                    |     | 1.1 | 1.6 | mA   |
|                                           |                                                                                                                                                                                                              |         | I <sub>CC2</sub>                    |     | 1.3 | 2   |      |
|                                           | V <sub>I</sub> = 0V (ISO6720B), V <sub>I</sub> = V <sub>CC1</sub> (ISO6720B with F suffix)                                                                                                                   |         | I <sub>CC1</sub>                    |     | 3.2 | 4.5 |      |
|                                           |                                                                                                                                                                                                              |         | I <sub>CC2</sub>                    |     | 1.4 | 2.2 |      |
| Supply current - AC signal <sup>(3)</sup> | All channels switching with square wave clock input; C <sub>L</sub> = 15 pF                                                                                                                                  | 1 Mbps  | I <sub>CC1</sub>                    |     | 2.1 | 3.1 |      |
|                                           |                                                                                                                                                                                                              |         | I <sub>CC2</sub>                    |     | 1.4 | 2.2 |      |
|                                           |                                                                                                                                                                                                              | 10 Mbps | I <sub>CC1</sub>                    |     | 2.2 | 3.1 |      |
|                                           |                                                                                                                                                                                                              |         | I <sub>CC2</sub>                    |     | 2.3 | 3.2 |      |
|                                           |                                                                                                                                                                                                              | 50 Mbps | I <sub>CC1</sub>                    |     | 2.4 | 3.4 |      |
|                                           |                                                                                                                                                                                                              |         | I <sub>CC2</sub>                    |     | 6   | 7.3 |      |
| ISO6721B                                  |                                                                                                                                                                                                              |         |                                     |     |     |     |      |
| Supply current - DC signal <sup>(2)</sup> | V <sub>I</sub> = V <sub>CC1</sub> <sup>(1)</sup> (ISO6721B); V <sub>I</sub> = 0 V (ISO6721B with F suffix)<br>V <sub>I</sub> = 0 V (ISO6721B);<br>V <sub>I</sub> = V <sub>CC1</sub> (ISO6721B with F suffix) |         | I <sub>CC1</sub> , I <sub>CC2</sub> |     | 1.2 | 2.1 | mA   |
|                                           |                                                                                                                                                                                                              |         | I <sub>CC1</sub> , I <sub>CC2</sub> |     | 2.3 | 3.5 |      |
| Supply current - AC signal <sup>(3)</sup> | All channels switching with square wave clock input; C <sub>L</sub> = 15 pF                                                                                                                                  | 1 Mbps  | I <sub>CC1</sub> , I <sub>CC2</sub> |     | 1.8 | 2.8 |      |
|                                           |                                                                                                                                                                                                              | 10 Mbps | I <sub>CC1</sub> , I <sub>CC2</sub> |     | 2.3 | 3.3 |      |
|                                           |                                                                                                                                                                                                              | 50 Mbps | I <sub>CC1</sub> , I <sub>CC2</sub> |     | 4.2 | 5.5 |      |

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER                         | TEST CONDITIONS                                                             | SUPPLY CURRENT     | MIN | TYP | MAX | UNIT |
|-----------------------------------|-----------------------------------------------------------------------------|--------------------|-----|-----|-----|------|
| <b>ISO6721RB</b>                  |                                                                             |                    |     |     |     |      |
| Supply current - DC signal<br>(2) | $V_I = V_{CCI}$ (1) (ISO6721R); $V_I = 0\text{ V}$ (ISO6721R with F suffix) | $I_{CC1}, I_{CC2}$ |     | 2.1 | 3.3 | mA   |
|                                   | $V_I = 0\text{ V}$ (ISO6721R); $V_I = V_{CCI}$ (ISO6721R with F suffix)     | $I_{CC1}, I_{CC2}$ |     | 3.2 | 4.7 | mA   |
| Supply current - AC signal<br>(3) | All channels switching with square wave clock input; $C_L = 15\text{ pF}$   | 1 Mbps             |     | 2.7 | 4.0 | mA   |
|                                   |                                                                             | 10 Mbps            |     | 3.1 | 4.5 | mA   |
|                                   |                                                                             | 50 Mbps            |     | 5.0 | 6.7 | mA   |

(1)  $V_{CCI} = \text{Input-side } V_{CC}$ 

(2) Supply current valid for  $ENx = V_{CCx}$  and  $ENx = 0\text{ V}$ 

(3) Supply current valid for  $ENx = V_{CCx}$

### 6.13 Electrical Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER     | TEST CONDITIONS                                                                                                                                                    | MIN                  | TYP                        | MAX | UNIT          |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------------|-----|---------------|
| $V_{OH}$      | High-level output voltage<br>$I_{OH} = -1 \text{ mA}$ ; See <a href="#">Figure 7-1</a>                                                                             | $V_{CCO} - 0.1$      |                            |     | V             |
| $V_{OL}$      | Low-level output voltage<br>$I_{OL} = 1 \text{ mA}$ ; See <a href="#">Figure 7-1</a>                                                                               |                      |                            | 0.1 | V             |
| $V_{IT+(IN)}$ | Rising input switching threshold                                                                                                                                   |                      | $0.7 \times V_{CCI}^{(1)}$ |     | V             |
| $V_{IT-(IN)}$ | Falling input switching threshold                                                                                                                                  | $0.3 \times V_{CCI}$ |                            |     | V             |
| $V_{I(HYS)}$  | Input threshold voltage hysteresis                                                                                                                                 | $0.1 \times V_{CCI}$ |                            |     | V             |
| $I_{IH}$      | High-level input current<br>$V_{IH} = V_{CCI}^{(1)}$ at INx                                                                                                        |                      |                            | 10  | $\mu\text{A}$ |
| $I_{IL}$      | Low-level input current<br>$V_{IL} = 0 \text{ V}$ at INx                                                                                                           | -10                  |                            |     | $\mu\text{A}$ |
| CMTI          | Common mode transient immunity<br>$V_I = V_{CC}$ or $0 \text{ V}$ , $V_{CM} = 1200 \text{ V}$                                                                      | 100                  | 150                        |     | kV/us         |
| $C_i$         | Input Capacitance <sup>(2)</sup><br>$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi f t)$ , $f = 2 \text{ MHz}$ , $V_{CC} = 2.5 \text{ V}$ ; See <a href="#">Figure 7-3</a> |                      | 2.8                        |     | pF            |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$

(2) Measured from input pin to same side ground.

### 6.14 Supply Current Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                                                                 |         | SUPPLY CURRENT     | MIN | TYP | MAX | UNIT |
|-------------------------------------------|---------------------------------------------------------------------------------|---------|--------------------|-----|-----|-----|------|
| ISO6720B                                  |                                                                                 |         |                    |     |     |     |      |
| Supply current - DC signal <sup>(2)</sup> | $V_I = V_{CC1}$ <sup>(1)</sup> (ISO6720B), $V_I = 0$ V (ISO6720B with F suffix) |         | $I_{CC1}$          |     | 1.1 | 1.6 | mA   |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 1.3 | 2   |      |
|                                           | $V_I = 0$ V (ISO6720B), $V_I = V_{CC1}$ (ISO6720B with F suffix)                |         | $I_{CC1}$          |     | 3.1 | 4.5 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 1.4 | 2.2 |      |
| Supply current - AC signal <sup>(3)</sup> | All channels switching with square wave clock input; $C_L = 15$ pF              | 1 Mbps  | $I_{CC1}$          |     | 2.1 | 3.1 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 1.4 | 2.2 |      |
|                                           |                                                                                 | 10 Mbps | $I_{CC1}$          |     | 2.1 | 3.1 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 2   | 2.9 |      |
|                                           |                                                                                 | 50 Mbps | $I_{CC1}$          |     | 2.3 | 3.3 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 4.8 | 6   |      |
| ISO6721B                                  |                                                                                 |         |                    |     |     |     |      |
| Supply current - DC signal <sup>(2)</sup> | $V_I = V_{CC1}$ <sup>(1)</sup> (ISO6721B); $V_I = 0$ V (ISO6721B with F suffix) |         | $I_{CC1}, I_{CC2}$ |     | 1.2 | 2.1 | mA   |
|                                           | $V_I = 0$ V (ISO6721B); $V_I = V_{CC1}$ (ISO6721B with F suffix)                |         | $I_{CC1}, I_{CC2}$ |     | 2.3 | 3.5 |      |
| Supply current - AC signal <sup>(3)</sup> | All channels switching with square wave clock input; $C_L = 15$ pF              | 1 Mbps  | $I_{CC1}, I_{CC2}$ |     | 1.8 | 2.8 |      |
|                                           |                                                                                 | 10 Mbps | $I_{CC1}, I_{CC2}$ |     | 2.1 | 3.2 |      |
|                                           |                                                                                 | 50 Mbps | $I_{CC1}, I_{CC2}$ |     | 3.6 | 4.9 |      |

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER                         | TEST CONDITIONS                                                            | SUPPLY CURRENT     | MIN | TYP | MAX | UNIT |
|-----------------------------------|----------------------------------------------------------------------------|--------------------|-----|-----|-----|------|
| <b>ISO6721RB</b>                  |                                                                            |                    |     |     |     |      |
| Supply current - DC signal<br>(2) | $V_I = V_{CCI}$ (1)(ISO6721R); $V_I = 0\text{ V}$ (ISO6721R with F suffix) | $I_{CC1}, I_{CC2}$ |     | 2.1 | 3.3 | mA   |
|                                   | $V_I = 0\text{ V}$ (ISO6721R); $V_I = V_{CCI}$ (ISO6721R with F suffix)    | $I_{CC1}, I_{CC2}$ |     | 3.2 | 4.7 | mA   |
| Supply current - AC signal<br>(3) | All channels switching with square wave clock input; $C_L = 15\text{ pF}$  | 1 Mbps             |     | 2.7 | 4.0 | mA   |
|                                   |                                                                            | 10 Mbps            |     | 3.0 | 4.4 | mA   |
|                                   |                                                                            | 50 Mbps            |     | 4.4 | 6   | mA   |

(1)  $V_{CCI} = \text{Input-side } V_{CC}$ 

(2) Supply current valid for  $ENx = V_{CCx}$  and  $ENx = 0\text{ V}$ 

(3) Supply current valid for  $ENx = V_{CCx}$

## 6.15 Electrical Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8 \text{ V} \pm 5\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER     | TEST CONDITIONS                    | MIN                                                                                                                            | TYP                        | MAX | UNIT          |
|---------------|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|----------------------------|-----|---------------|
| $V_{OH}$      | High-level output voltage          | $I_{OH} = -1 \text{ mA}$ ; See <a href="#">Figure 7-1</a>                                                                      | $V_{CCO} - 0.1$            |     | V             |
| $V_{OL}$      | Low-level output voltage           | $I_{OL} = 1 \text{ mA}$ ; See <a href="#">Figure 7-1</a>                                                                       |                            | 0.1 | V             |
| $V_{IT+(IN)}$ | Rising input switching threshold   |                                                                                                                                | $0.7 \times V_{CCI}^{(1)}$ |     | V             |
| $V_{IT-(IN)}$ | Falling input switching threshold  |                                                                                                                                | $0.3 \times V_{CCI}$       |     | V             |
| $V_{I(HYS)}$  | Input threshold voltage hysteresis |                                                                                                                                | $0.1 \times V_{CCI}$       |     | V             |
| $I_{IH}$      | High-level input current           | $V_{IH} = V_{CCI}^{(1)}$ at $INx$                                                                                              |                            | 10  | $\mu\text{A}$ |
| $I_{IL}$      | Low-level input current            | $V_{IL} = 0 \text{ V}$ at $INx$                                                                                                | -10                        |     | $\mu\text{A}$ |
| CMTI          | Common mode transient immunity     | $V_I = V_{CC}$ or $0 \text{ V}$ , $V_{CM} = 1200 \text{ V}$                                                                    | 100                        | 150 | kV/us         |
| $C_i$         | Input Capacitance <sup>(2)</sup>   | $V_I = V_{CC}/2 + 0.4 \times \sin(2\pi f t)$ , $f = 2 \text{ MHz}$ , $V_{CC} = 1.8 \text{ V}$ ; See <a href="#">Figure 7-3</a> | 2.8                        |     | pF            |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$

(2) Measured from input pin to same side ground.

## 6.16 Supply Current Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8 \text{ V} \pm 5\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                                                                 |         | SUPPLY CURRENT     | MIN | TYP | MAX | UNIT |
|-------------------------------------------|---------------------------------------------------------------------------------|---------|--------------------|-----|-----|-----|------|
| ISO6720B                                  |                                                                                 |         |                    |     |     |     |      |
| Supply current - DC signal <sup>(2)</sup> | $V_I = V_{CC1}$ <sup>(1)</sup> (ISO6720B), $V_I = 0$ V (ISO6720B with F suffix) |         | $I_{CC1}$          |     | 0.8 | 1.5 | mA   |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 1.2 | 2.1 |      |
|                                           | $V_I = 0$ V (ISO6720B), $V_I = V_{CC1}$ (ISO6720B with F suffix)                |         | $I_{CC1}$          |     | 2.8 | 4.3 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 1.3 | 2.2 |      |
| Supply current - AC signal <sup>(3)</sup> | All channels switching with square wave clock input; $C_L = 15$ pF              | 1 Mbps  | $I_{CC1}$          |     | 1.8 | 2.9 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 1.3 | 2.2 |      |
|                                           |                                                                                 | 10 Mbps | $I_{CC1}$          |     | 1.8 | 2.9 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 1.8 | 2.7 |      |
|                                           |                                                                                 | 50 Mbps | $I_{CC1}$          |     | 2   | 3.1 |      |
|                                           |                                                                                 |         | $I_{CC2}$          |     | 3.8 | 4.9 |      |
| ISO6721B                                  |                                                                                 |         |                    |     |     |     |      |
| Supply current - DC signal <sup>(2)</sup> | $V_I = V_{CC1}$ <sup>(1)</sup> (ISO6721B); $V_I = 0$ V (ISO6721B with F suffix) |         | $I_{CC1}, I_{CC2}$ |     | 1.1 | 2   | mA   |
|                                           | $V_I = 0$ V (ISO6721B); $V_I = V_{CC1}$ (ISO6721B with F suffix)                |         | $I_{CC1}, I_{CC2}$ |     | 2.1 | 3.4 |      |
| Supply current - AC signal <sup>(3)</sup> | All channels switching with square wave clock input; $C_L = 15$ pF              | 1 Mbps  | $I_{CC1}, I_{CC2}$ |     | 1.6 | 2.7 |      |
|                                           |                                                                                 | 10 Mbps | $I_{CC1}, I_{CC2}$ |     | 1.9 | 3   |      |
|                                           |                                                                                 | 50 Mbps | $I_{CC1}, I_{CC2}$ |     | 3   | 4.2 |      |
|                                           |                                                                                 |         |                    |     |     |     |      |

$V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 5\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                                                                        | SUPPLY CURRENT     | MIN | TYP | MAX | UNIT |
|-------------------------------------------|----------------------------------------------------------------------------------------|--------------------|-----|-----|-----|------|
| <b>ISO6721RB</b>                          |                                                                                        |                    |     |     |     |      |
| Supply current - DC signal <sup>(2)</sup> | $V_I = V_{CCI}$ <sup>(1)</sup> (ISO6721R); $V_I = 0\text{ V}$ (ISO6721R with F suffix) | $I_{CC1}, I_{CC2}$ |     | 1.8 | 3.1 | mA   |
|                                           | $V_I = 0\text{ V}$ (ISO6721R); $V_I = V_{CCI}$ (ISO6721R with F suffix)                | $I_{CC1}, I_{CC2}$ |     | 2.9 | 4.5 | mA   |
| Supply current - AC signal <sup>(3)</sup> | All channels switching with square wave clock input; $C_L = 15\text{ pF}$              | 1 Mbps             |     | 2.4 | 3.8 | mA   |
|                                           |                                                                                        | 10 Mbps            |     | 2.6 | 4.1 | mA   |
|                                           |                                                                                        | 50 Mbps            |     | 3.7 | 5.3 | mA   |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ 

(2) Supply current valid for  $ENx = V_{CCx}$  and  $ENx = 0\text{ V}$ 

(3) Supply current valid for  $ENx = V_{CCx}$

## 6.17 Switching Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER             |                                                             | TEST CONDITIONS                                                                 | MIN | TYP | MAX | UNIT  |
|-----------------------|-------------------------------------------------------------|---------------------------------------------------------------------------------|-----|-----|-----|-------|
| $t_{PLH}$ , $t_{PHL}$ | Propagation delay time                                      | See <a href="#">Figure 7-1</a>                                                  |     | 11  | 18  | ns    |
| $t_{P(dft)}$          | Propagation delay drift                                     |                                                                                 |     | 8   |     | ps/°C |
| $t_{UI}$              | Minimum pulse width                                         | See <a href="#">Figure 7-1</a>                                                  | 20  |     |     | ns    |
| PWD                   | Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ | See <a href="#">Figure 7-1</a>                                                  |     | 0.2 | 7   | ns    |
| $t_{sk(o)}$           | Channel-to-channel output skew time <sup>(2)</sup>          | Same direction channels                                                         |     |     | 6   | ns    |
| $t_{sk(p-p)}$         | Part-to-part skew time <sup>(3)</sup>                       |                                                                                 |     |     | 6   | ns    |
| $t_r$                 | Output signal rise time                                     | See <a href="#">Figure 7-1</a>                                                  |     | 2.6 | 4.5 | ns    |
| $t_f$                 | Output signal fall time                                     |                                                                                 |     | 2.6 | 4.5 | ns    |
| $t_{PU}$              | Time from UVLO to valid output data                         |                                                                                 |     |     | 300 | us    |
| $t_{DO}$              | Default output delay time from input power loss             | Measured from the time $V_{CC}$ goes below 1.2V. See <a href="#">Figure 7-2</a> |     | 0.1 | 0.3 | us    |
| $t_{ie}$              | Time interval error                                         | $2^{16} - 1$ PRBS data at 50 Mbps                                               |     | 1   |     | ns    |

(1) Also known as pulse skew.

(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 6.18 Switching Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER             |                                                             | TEST CONDITIONS                                                                 | MIN | TYP | MAX | UNIT  |
|-----------------------|-------------------------------------------------------------|---------------------------------------------------------------------------------|-----|-----|-----|-------|
| $t_{PLH}$ , $t_{PHL}$ | Propagation delay time                                      | See <a href="#">Figure 7-1</a>                                                  |     | 11  | 18  | ns    |
| $t_{P(dft)}$          | Propagation delay drift                                     |                                                                                 |     | 9.2 |     | ps/°C |
| $t_{UI}$              | Minimum pulse width                                         | See <a href="#">Figure 7-1</a>                                                  | 20  |     |     | ns    |
| PWD                   | Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ | See <a href="#">Figure 7-1</a>                                                  |     | 0.5 | 7   | ns    |
| $t_{sk(o)}$           | Channel-to-channel output skew time <sup>(2)</sup>          | Same direction channels                                                         |     |     | 6   | ns    |
| $t_{sk(p-p)}$         | Part-to-part skew time <sup>(3)</sup>                       |                                                                                 |     |     | 6   | ns    |
| $t_r$                 | Output signal rise time                                     | See <a href="#">Figure 7-1</a>                                                  |     | 1.6 | 3.2 | ns    |
| $t_f$                 | Output signal fall time                                     |                                                                                 |     | 1.6 | 3.2 | ns    |
| $t_{PU}$              | Time from UVLO to valid output data                         |                                                                                 |     |     | 300 | us    |
| $t_{DO}$              | Default output delay time from input power loss             | Measured from the time $V_{CC}$ goes below 1.2V. See <a href="#">Figure 7-2</a> |     | 0.1 | 0.3 | us    |
| $t_{ie}$              | Time interval error                                         | $2^{16} - 1$ PRBS data at 50 Mbps                                               |     | 1   |     | ns    |

(1) Also known as pulse skew.

(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 6.19 Switching Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER          |                                                             | TEST CONDITIONS                                                                 | MIN | TYP  | MAX  | UNIT  |
|--------------------|-------------------------------------------------------------|---------------------------------------------------------------------------------|-----|------|------|-------|
| $t_{PLH}, t_{PHL}$ | Propagation delay time                                      | See <a href="#">Figure 7-1</a>                                                  |     | 12   | 20.5 | ns    |
| $t_{P(dft)}$       | Propagation delay drift                                     |                                                                                 |     | 14.3 |      | ps/°C |
| $t_{UI}$           | Minimum pulse width                                         | See <a href="#">Figure 7-1</a>                                                  | 20  |      |      | ns    |
| PWD                | Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ | See <a href="#">Figure 7-1</a>                                                  |     | 0.6  | 7.1  | ns    |
| $t_{sk(o)}$        | Channel-to-channel output skew time <sup>(2)</sup>          | Same direction channels                                                         |     |      | 6    | ns    |
| $t_{sk(p-p)}$      | Part-to-part skew time <sup>(3)</sup>                       |                                                                                 |     |      | 6.1  | ns    |
| $t_r$              | Output signal rise time                                     | See <a href="#">Figure 7-1</a>                                                  |     | 2    | 4    | ns    |
| $t_f$              | Output signal fall time                                     |                                                                                 |     | 2    | 4    | ns    |
| $t_{PU}$           | Time from UVLO to valid output data                         |                                                                                 |     |      | 300  | us    |
| $t_{DO}$           | Default output delay time from input power loss             | Measured from the time $V_{CC}$ goes below 1.2V. See <a href="#">Figure 7-2</a> |     | 0.1  | 0.3  | us    |
| $t_{ie}$           | Time interval error                                         | $2^{16} - 1$ PRBS data at 50 Mbps                                               |     | 1    |      | ns    |

- (1) Also known as pulse skew.  
 (2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.  
 (3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

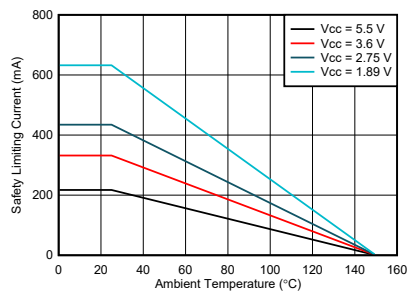
## 6.20 Switching Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8 \text{ V} \pm 5\%$  (over recommended operating conditions unless otherwise noted)

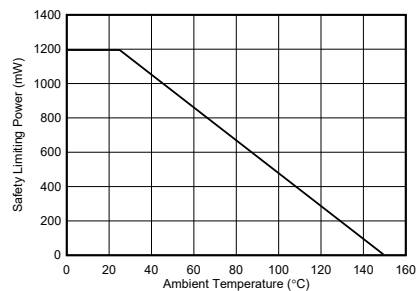
| PARAMETER          |                                                             | TEST CONDITIONS                                                                 | MIN | TYP  | MAX | UNIT  |
|--------------------|-------------------------------------------------------------|---------------------------------------------------------------------------------|-----|------|-----|-------|
| $t_{PLH}, t_{PHL}$ | Propagation delay time                                      | See <a href="#">Figure 7-1</a>                                                  |     | 15   | 24  | ns    |
| $t_{P(dft)}$       | Propagation delay drift                                     |                                                                                 |     | 15.2 |     | ps/°C |
| $t_{UI}$           | Minimum pulse width                                         | See <a href="#">Figure 7-1</a>                                                  | 20  |      |     | ns    |
| PWD                | Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ | See <a href="#">Figure 7-1</a>                                                  |     | 0.7  | 8.2 | ns    |
| $t_{sk(o)}$        | Channel-to-channel output skew time <sup>(2)</sup>          | Same direction channels                                                         |     |      | 6   | ns    |
| $t_{sk(p-p)}$      | Part-to-part skew time <sup>(3)</sup>                       |                                                                                 |     |      | 8.8 | ns    |
| $t_r$              | Output signal rise time                                     | See <a href="#">Figure 7-1</a>                                                  |     | 2.7  | 5.3 | ns    |
| $t_f$              | Output signal fall time                                     |                                                                                 |     | 2.7  | 5.3 | ns    |
| $t_{PU}$           | Time from UVLO to valid output data                         |                                                                                 |     |      | 300 | us    |
| $t_{DO}$           | Default output delay time from input power loss             | Measured from the time $V_{CC}$ goes below 1.2V. See <a href="#">Figure 7-2</a> |     | 0.1  | 0.3 | us    |
| $t_{ie}$           | Time interval error                                         | $2^{16} - 1$ PRBS data at 50 Mbps                                               |     | 1    |     | ns    |

- (1) Also known as pulse skew.  
 (2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.  
 (3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

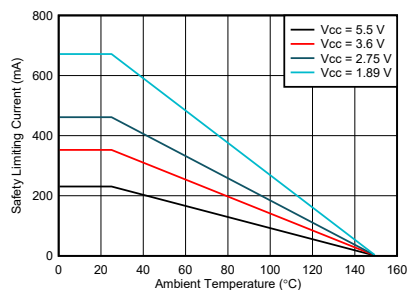
## 6.21 Insulation Characteristics Curves



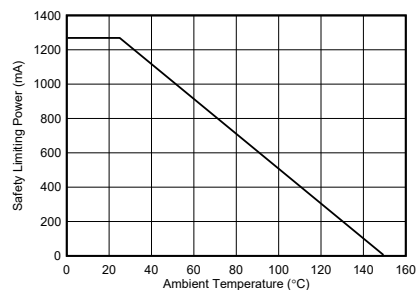
**Figure 6-1. Thermal Derating Curve for Safety Limiting Current for D-8 Package - ISO672x**



**Figure 6-2. Thermal Derating Curve for Safety Limiting Power for D-8 Package - ISO672x**

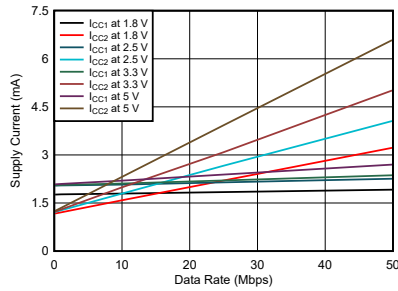


**Figure 6-3. Thermal Derating Curve for Safety Limiting Current for D-8 Package - ISO6721R**



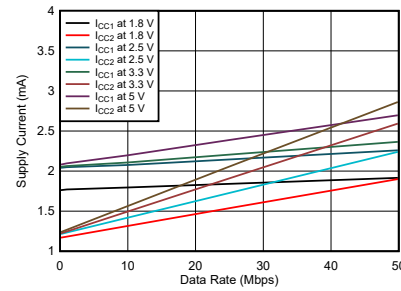
**Figure 6-4. Thermal Derating Curve for Safety Limiting Power for D-8 Package - ISO6721R**

## 6.22 Typical Characteristics



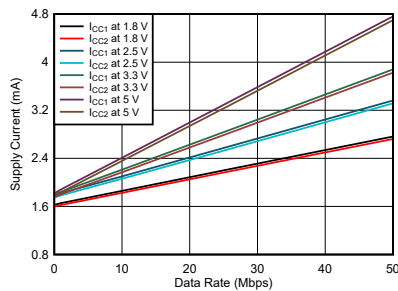
$T_A = 25^\circ\text{C}$   $C_L = 15\text{ pF}$

**Figure 6-5. ISO6720B Supply Current vs Data Rate (With 15-pF Load)**



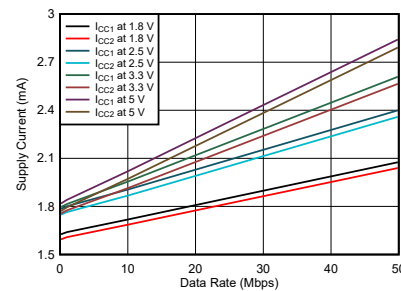
$T_A = 25^\circ\text{C}$   $C_L = \text{No Load}$

**Figure 6-6. ISO6720B Supply Current vs Data Rate (With No Load)**



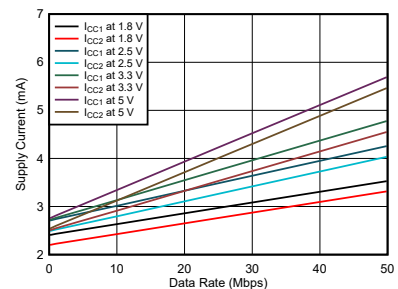
$T_A = 25^\circ\text{C}$   $C_L = 15\text{ pF}$

**Figure 6-7. ISO6721B Supply Current vs Data Rate (With 15-pF Load)**



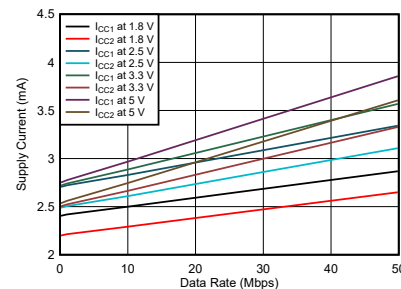
$T_A = 25^\circ\text{C}$   $C_L = \text{No Load}$

**Figure 6-8. ISO6721B Supply Current vs Data Rate (With No Load)**



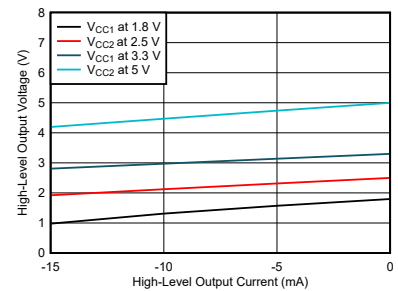
$T_A = 25^\circ\text{C}$   $C_L = 15\text{ pF}$

**Figure 6-9. ISO6721RB Supply Current vs Data Rate (With 15-pF Load)**



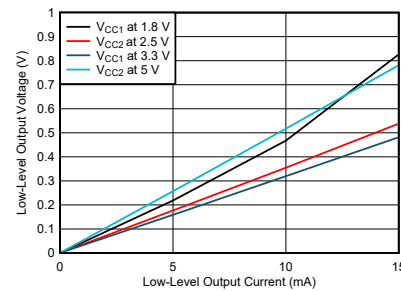
$T_A = 25^\circ\text{C}$   $C_L = \text{No Load}$

**Figure 6-10. ISO6721RB Supply Current vs Data Rate (With No Load)**



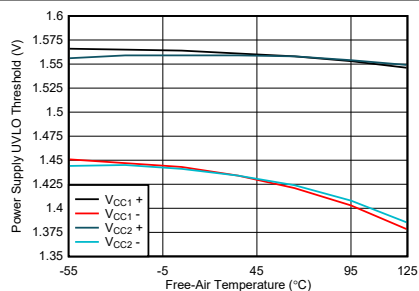
$T_A = 25^\circ\text{C}$

**Figure 6-11. High-Level Output Voltage vs High-level Output Current**

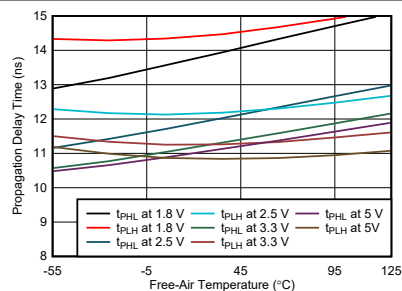


$T_A = 25^\circ\text{C}$

**Figure 6-12. Low-Level Output Voltage vs Low-Level Output Current**

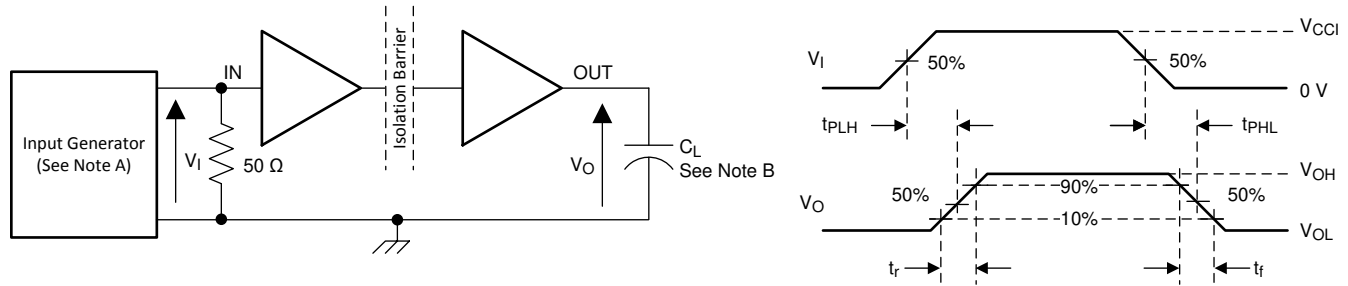


**Figure 6-13. Power Supply Undervoltage Threshold vs Free-Air Temperature**



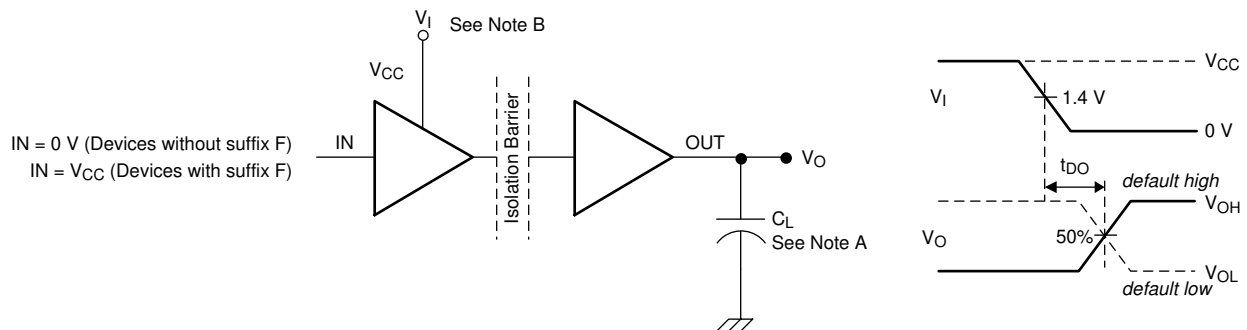
**Figure 6-14. Propagation Delay Time vs Free-Air Temperature**

## 7 Parameter Measurement Information



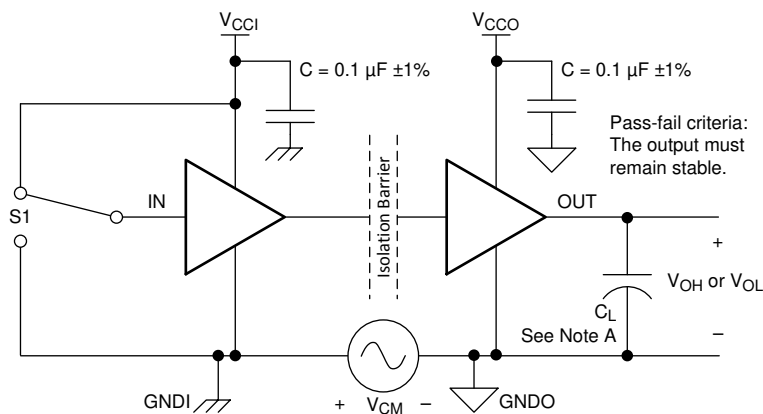
- A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 50$  kHz, 50% duty cycle,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns,  $Z_O = 50 \Omega$ . At the input, 50  $\Omega$  resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 7-1. Switching Characteristics Test Circuit and Voltage Waveforms**



- A.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .
- B. Power Supply Ramp Rate = 10 mV/ns

**Figure 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms**



- A.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

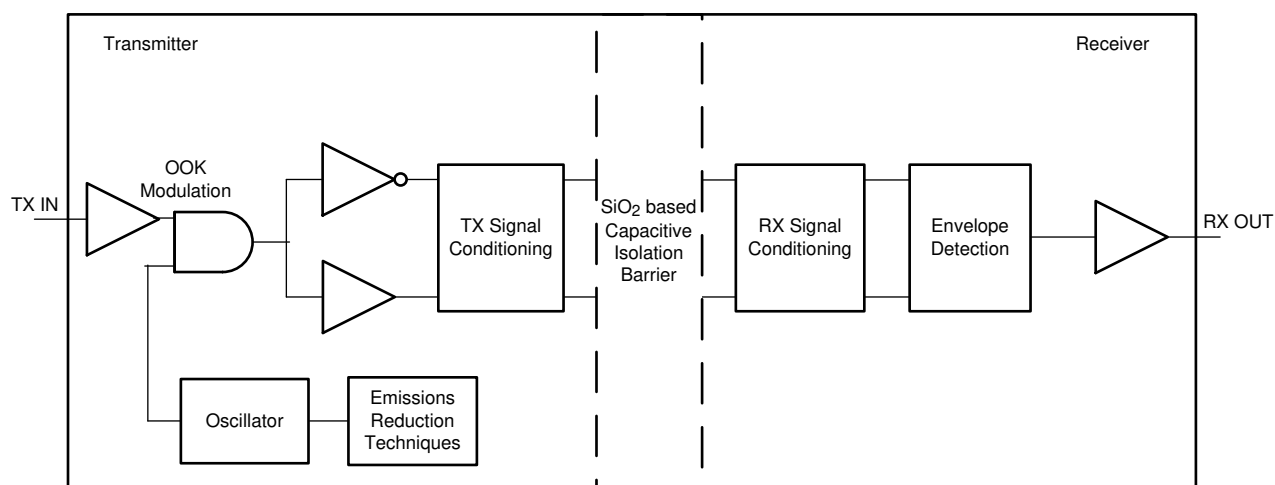
**Figure 7-3. Common-Mode Transient Immunity Test Circuit**

## 8 Detailed Description

### 8.1 Overview

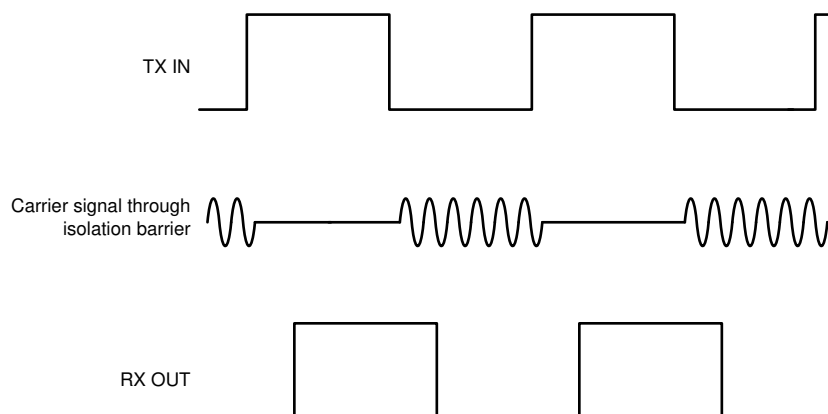
The ISO672xB family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 8-1](#), shows a functional block diagram of a typical channel.

### 8.2 Functional Block Diagram



**Figure 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator**

[Figure 8-2](#) shows a conceptual detail of how the OOK scheme works.



**Figure 8-2. On-Off Keying (OOK) Based Modulation Scheme**

## 8.3 Feature Description

The ISO672xB family of devices is available in two channel configurations and default output state options to enable a variety of application uses. [Table 8-1](#) lists the device features of the ISO672xB devices.

**Table 8-1. Device Features**

| PART NUMBER | MAXIMUM DATA RATE | CHANNEL DIRECTION    | DEFAULT OUTPUT STATE | PACKAGE | RATED ISOLATION <sup>(1)</sup>               |
|-------------|-------------------|----------------------|----------------------|---------|----------------------------------------------|
| ISO6720B    | 50 Mbps           | 2 Forward, 0 Reverse | High                 | D-8     | 3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub> |
| ISO6720FB   | 50 Mbps           | 2 Forward, 0 Reverse | Low                  | D-8     | 3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub> |
| ISO6721B    | 50 Mbps           | 1 Forward, 1 Reverse | High                 | D-8     | 3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub> |
| ISO6721FB   | 50 Mbps           | 1 Forward, 1 Reverse | Low                  | D-8     | 3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub> |
| ISO6721RB   | 50 Mbps           | 1 Forward, 1 Reverse | High                 | D-8     | 3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub> |
| ISO6721RFB  | 50 Mbps           | 1 Forward, 1 Reverse | Low                  | D-8     | 3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub> |

(1) See [Safety-Related Certifications](#) for detailed isolation ratings.

### 8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 32. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO672xB family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

## 8.4 Device Functional Modes

Table 8-2 lists the functional modes for the ISO672xB devices.

**Table 8-2. Function Table**

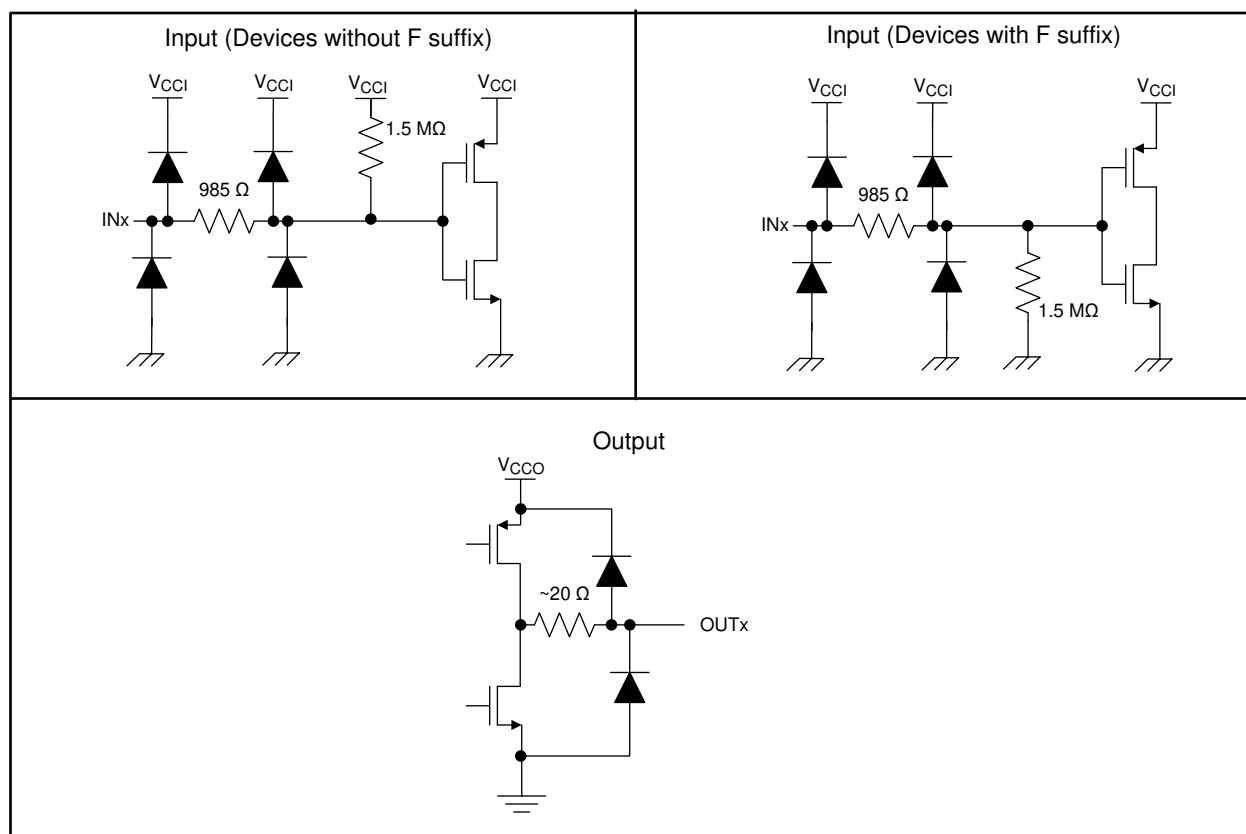
| $V_{CCI}^{(1)}$ | $V_{CCO}$ | INPUT (INx) <sup>(2)</sup> | OUTPUT (OUTx) | COMMENTS                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----------------|-----------|----------------------------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PU              | PU        | H                          | H             | Normal Operation: A channel output assumes the logic state of the input.                                                                                                                                                                                                                                                                                                                                                                 |
|                 |           | L                          | L             |                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|                 |           | Open                       | Default       | Default mode: When INx is open, the corresponding channel output goes to the default logic state. The default is <i>High</i> for ISO672xB and <i>Low</i> for ISO672xB with F suffix.                                                                                                                                                                                                                                                     |
| PD              | PU        | X                          | Default       | Default mode: When $V_{CCI}$ is unpowered, a channel output assumes the logic state based on the selected default option. The default is <i>High</i> for ISO672xB and <i>Low</i> for ISO672xB with F suffix. When $V_{CCI}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When $V_{CCI}$ transitions from powered-up to unpowered, channel output assumes the selected default state. |
| X               | PD        | X                          | Undetermined  | When $V_{CCO}$ is unpowered, a channel output is undetermined <sup>(3)</sup> . When $V_{CCO}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input.                                                                                                                                                                                                                                           |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ ; PU = Powered up ( $V_{CC} \geq 1.71V$ ); PD = Powered down ( $V_{CC} \leq 1.05V$ ); X = Irrelevant; H = High level; L = Low level

(2) A strongly driven input signal can weakly power the floating  $V_{CC}$  via an internal protection diode and cause undetermined output.

(3) The outputs are in undetermined state when  $1.89V < V_{CCI}$ ,  $V_{CCO} < 2.25V$  and  $1.05V < V_{CCI}$ ,  $V_{CCO} < 1.71V$

### 8.4.1 Device I/O Schematics



**Figure 8-3. Device I/O Schematics**

## 9 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant the accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

---

### 9.1 Application Information

The ISO672xB devices are high-performance, dual-channel digital isolators. The devices use single-ended CMOS-logic switching technology. The supply voltage range is from 1.71 V to 5.5 V for both supplies,  $V_{CC1}$  and  $V_{CC2}$ . Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within recommended operating conditions. As an example, it is possible to supply ISO672xB  $V_{CC1}$  with 3.3 V (which is within 1.71 V to 1.89 V and 2.25 V to 5 V) and  $V_{CC2}$  with 5 V (which is also within 1.71 V to 1.89 V and 2.25 V to 5 V). You can use the digital isolator as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

## 9.2 Typical Application

For industrial applications, the ISO672xB device can be used with Texas Instruments' mixed signal microcontroller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4-mA to 20-mA current loop.

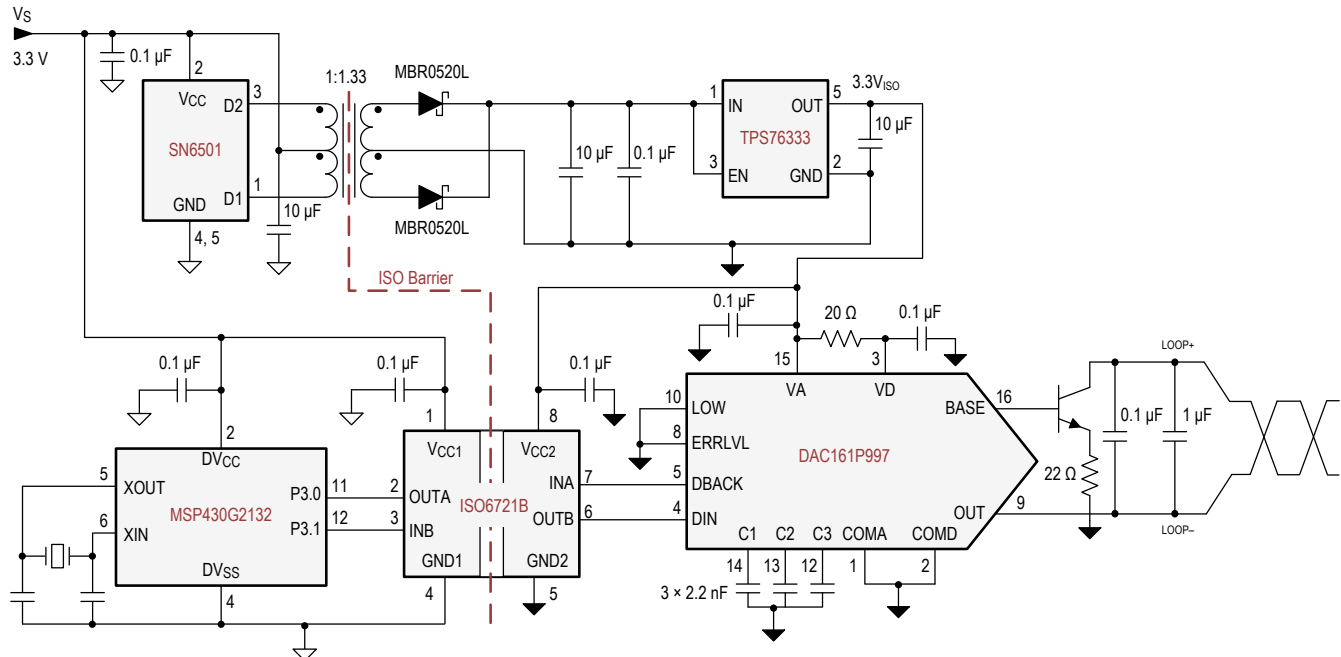


Figure 9-1. Isolated 4-mA to 20-mA Current Loop

## 9.2.1 Design Requirements

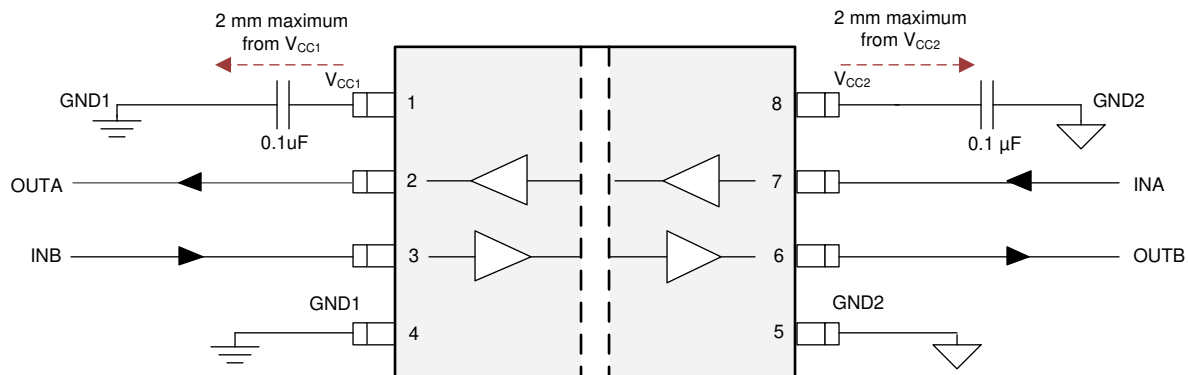
To design with these devices, use the parameters listed in [Table 9-1](#).

**Table 9-1. Design Parameters**

| PARAMETER                                       | VALUE                                |
|-------------------------------------------------|--------------------------------------|
| Supply voltage, $V_{CC1}$ and $V_{CC2}$         | 1.71 V to 1.89 V and 2.25 V to 5.5 V |
| Decoupling capacitor between $V_{CC1}$ and GND1 | 0.1 $\mu$ F                          |
| Decoupling capacitor from $V_{CC2}$ and GND2    | 0.1 $\mu$ F                          |

## 9.2.2 Detailed Design Procedure

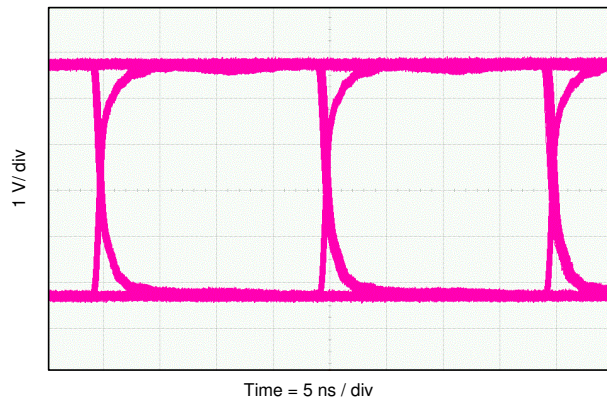
Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO672xB devices only require two external bypass capacitors to operate.



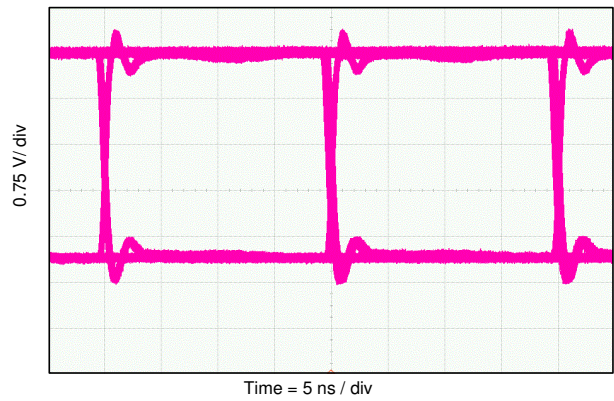
**Figure 9-2. Typical ISO672xB Circuit Hook-up**

### 9.2.3 Application Curve

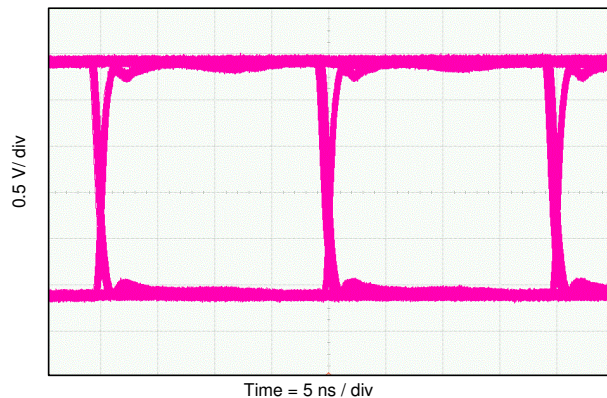
The following typical eye diagrams of the ISO672xB family of devices indicate low jitter and wide open eye at the maximum data rate of 50 Mbps.



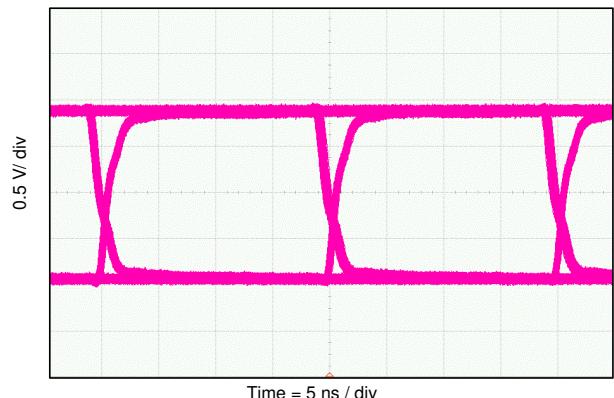
**Figure 9-3. Eye Diagram at 50 Mbps PRBS  $2^{16} - 1$ , 5 V and 25°C**



**Figure 9-4. Eye Diagram at 50 Mbps PRBS  $2^{16} - 1$ , 3.3 V and 25°C**



**Figure 9-5. Eye Diagram at 50 Mbps PRBS  $2^{16} - 1$ , 2.5 V and 25°C**



**Figure 9-6. Eye Diagram at 50 Mbps PRBS  $2^{16} - 1$ , 1.8 V and 25°C**

### 9.3 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See [Figure 9-7](#) for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For basic insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1000 part per million (ppm). For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm).

Even though the expected minimum insulation lifetime is 20 years, at the specified working isolation voltage, VDE basic and reinforced certifications require additional safety margin of 20% for working voltage. For basic certification, device lifetime requires a safety margin of 20% translating to a minimum required insulation lifetime of 24 years at a working voltage that is 20% higher than the specified value.

[Figure 9-8](#) shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 450 V<sub>RMS</sub> with a lifetime of >100 years in the 8D package. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. At the lower working voltages, the corresponding insulation lifetime is much longer than 100 years in the 8-D package.

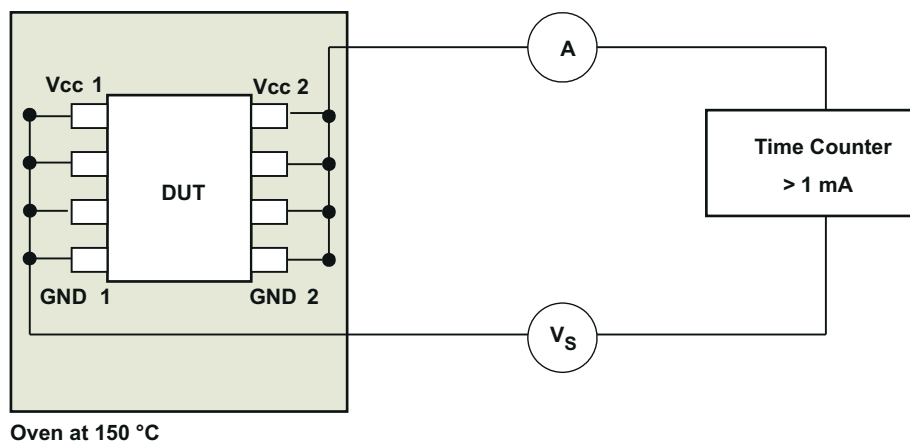


Figure 9-7. Test Setup for Insulation Lifetime Measurement

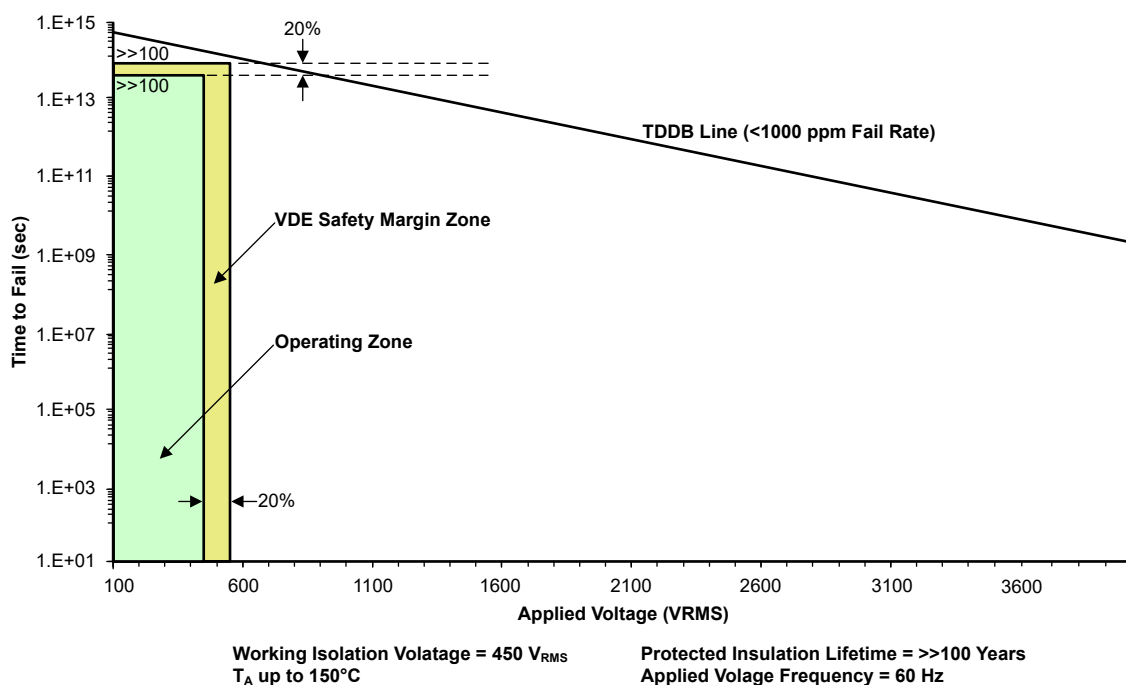


Figure 9-8. Insulation Lifetime Projection Data for 8-D Package

## 10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1- $\mu$ F bypass capacitor is recommended at the input and output supply pins ( $V_{CC1}$  and  $V_{CC2}$ ). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For industrial applications, please use Texas Instruments' [SN6501](#) or [SN6505B](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Drivers for Isolated Power Supplies](#) or [SN6505B-Q1 Low-noise, 1-A Transformer Drivers for Isolated Power Supplies](#).

## 11 Layout

### 11.1 Layout Guidelines

A minimum of two layers is required to accomplish a cost optimized and low EMI PCB design. To further improve EMI, a four layer board can be used (see [Section 11.2](#)). Layer stacking for a four layer board should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

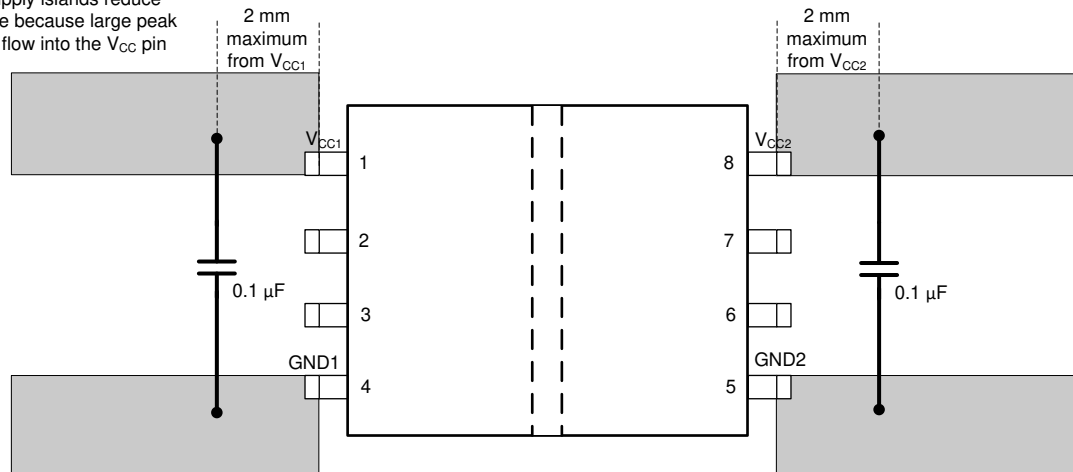
For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

#### 11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

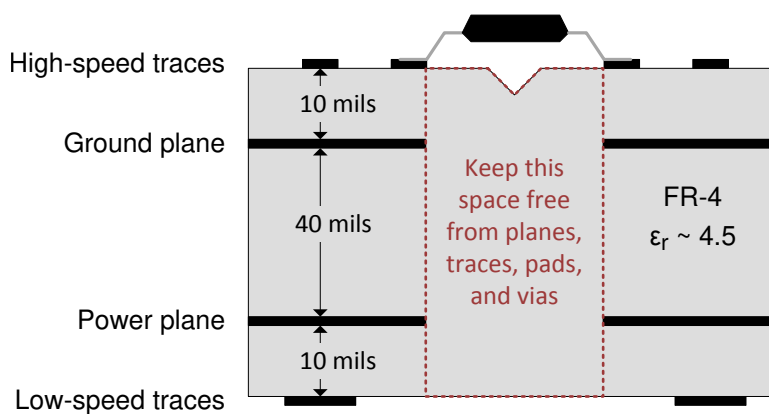
## 11.2 Layout Example

Solid supply islands reduce inductance because large peak currents flow into the  $V_{CC}$  pin



Solid ground islands help dissipate heat through PCB

**Figure 11-1. Layout Example**



**Figure 11-2. Four Layer Board Layout Example**

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

For development support, refer to:

- [Isolated CAN Flexible Data \(FD\) Rate Repeater Reference Design](#)
- [Isolated 16-Channel AC Analog Input Module Reference Design Using Dual Simultaneously Sampled ADCs](#)
- [Polyphase Shunt Metrology with Isolated AFE Reference Design](#)
- [Reference Design for Power-Isolated Ultra-Compact Analog Output Module](#)

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [How to use isolation to improve ESD, EFT and Surge immunity in industrial systems application report](#)
- Texas Instruments, [Isolation Glossary](#)
- Texas Instruments, [Enabling high voltage signal isolation quality and reliability](#)
- Texas Instruments, [DAC161P997 Single-Wire 16-bit DAC for 4- to 20-mA Loops data sheet](#)
- Texas Instruments, [MSP430G2132 Mixed Signal Microcontroller data sheet](#)
- Texas Instruments, [SN6501 Transformer Driver for Isolated Power Supplies data sheet](#)
- Texas Instruments, [TPS76333 Low-Power 150-mA Low-Dropout Linear Regulators data sheet](#)

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

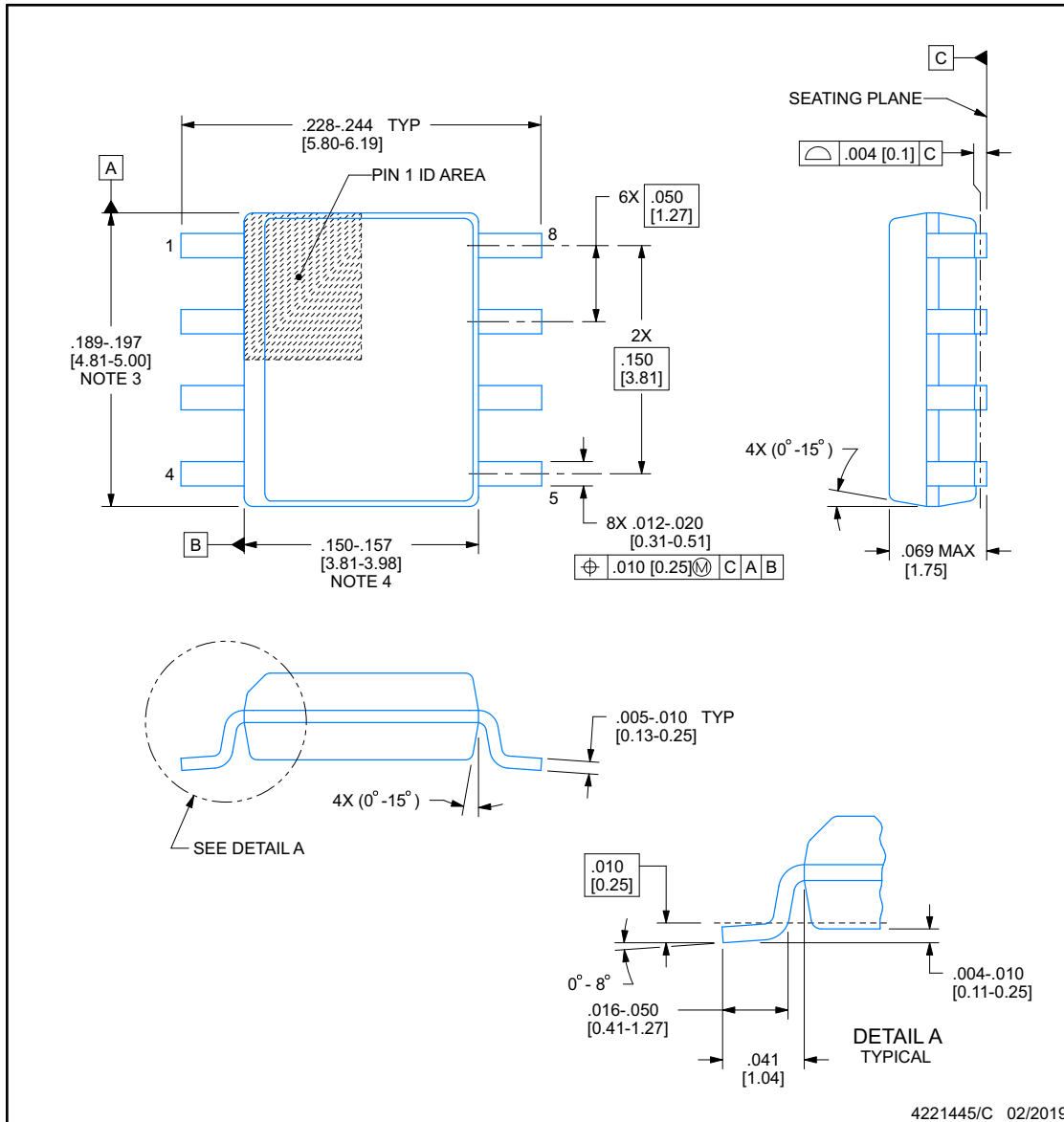
[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**D0008B**
**PACKAGE OUTLINE**  
**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

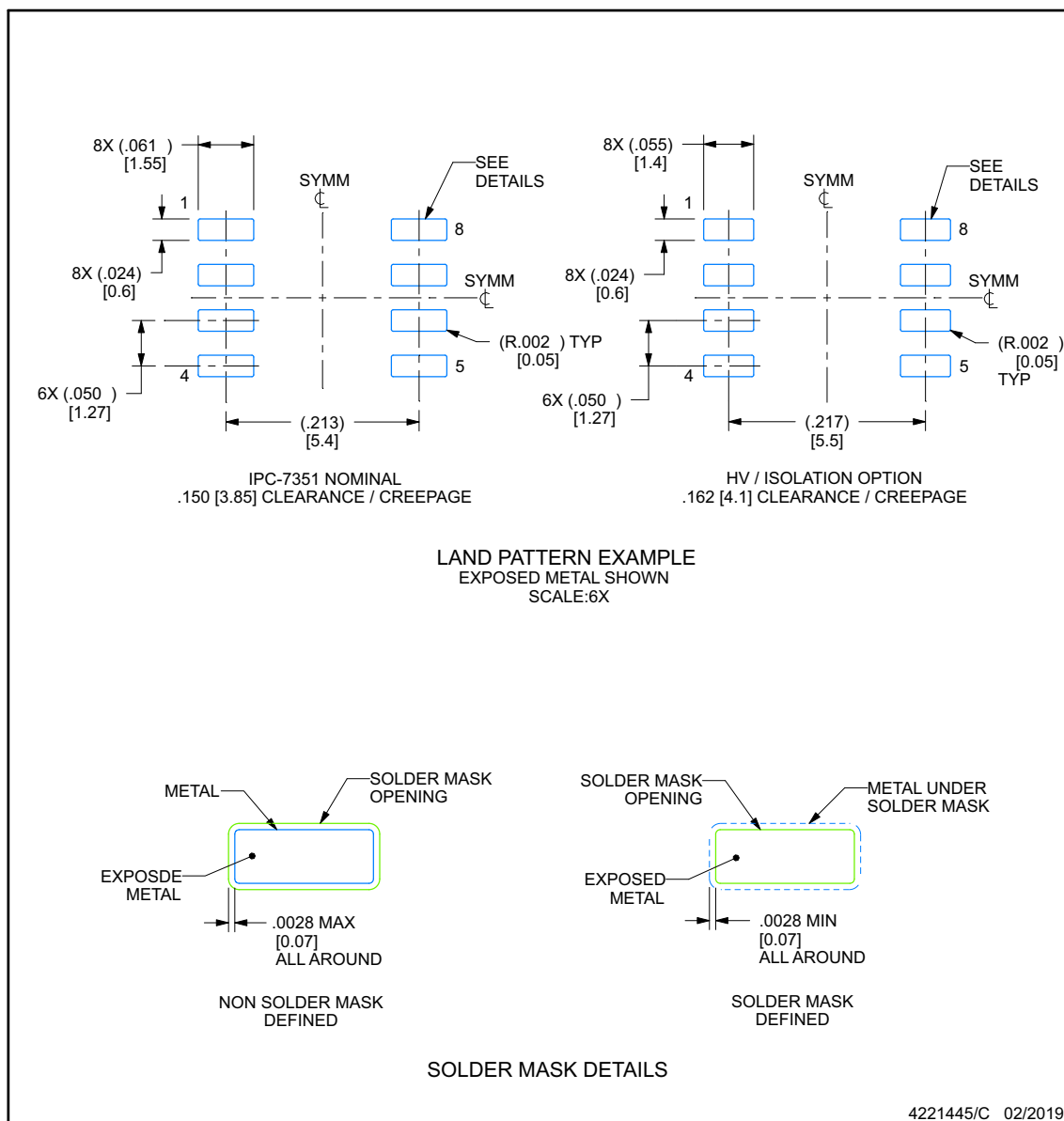
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

## EXAMPLE BOARD LAYOUT

**D0008B**

### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

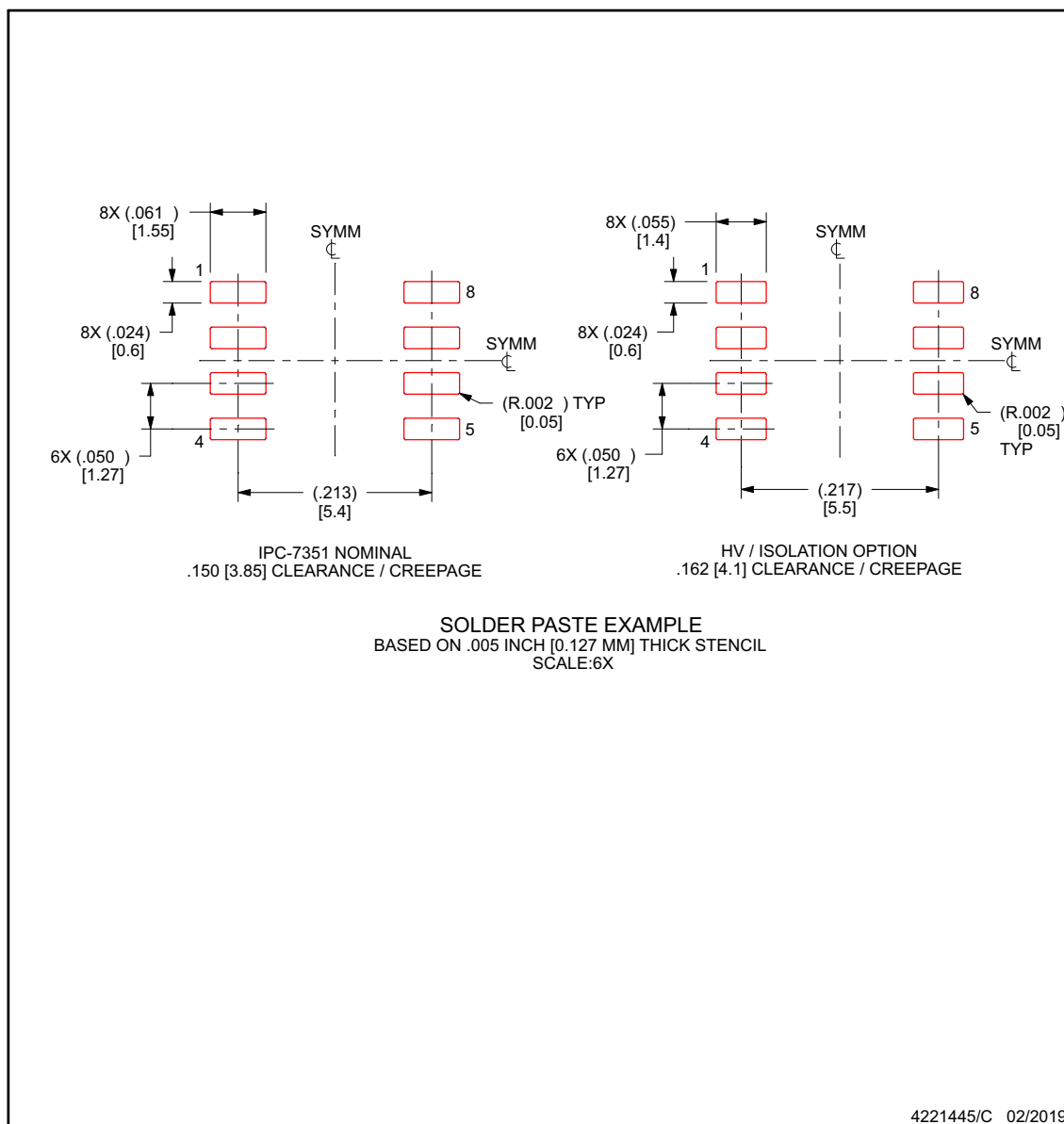


NOTES: (continued)

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN****D0008B****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">ISO6720BDR</a>   | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 6720B               |
| ISO6720BDR.A                 | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 6720B               |
| <a href="#">ISO6720FBDR</a>  | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 6720FB              |
| ISO6720FBDR.A                | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 6720FB              |
| <a href="#">ISO6721BDR</a>   | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 6721B               |
| ISO6721BDR.A                 | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 6721B               |
| <a href="#">ISO6721FBDR</a>  | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 6721FB              |
| ISO6721FBDR.A                | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 6721FB              |
| <a href="#">ISO6721RBDR</a>  | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 21RB                |
| ISO6721RBDR.A                | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 21RB                |
| <a href="#">ISO6721RFBDR</a> | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 21RFB               |
| ISO6721RFBDR.A               | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 21RFB               |
| ISO6721RFBDRG4               | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 21RFB               |
| ISO6721RFBDRG4.A             | Active        | Production           | SOIC (D)   8   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | 21RFB               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

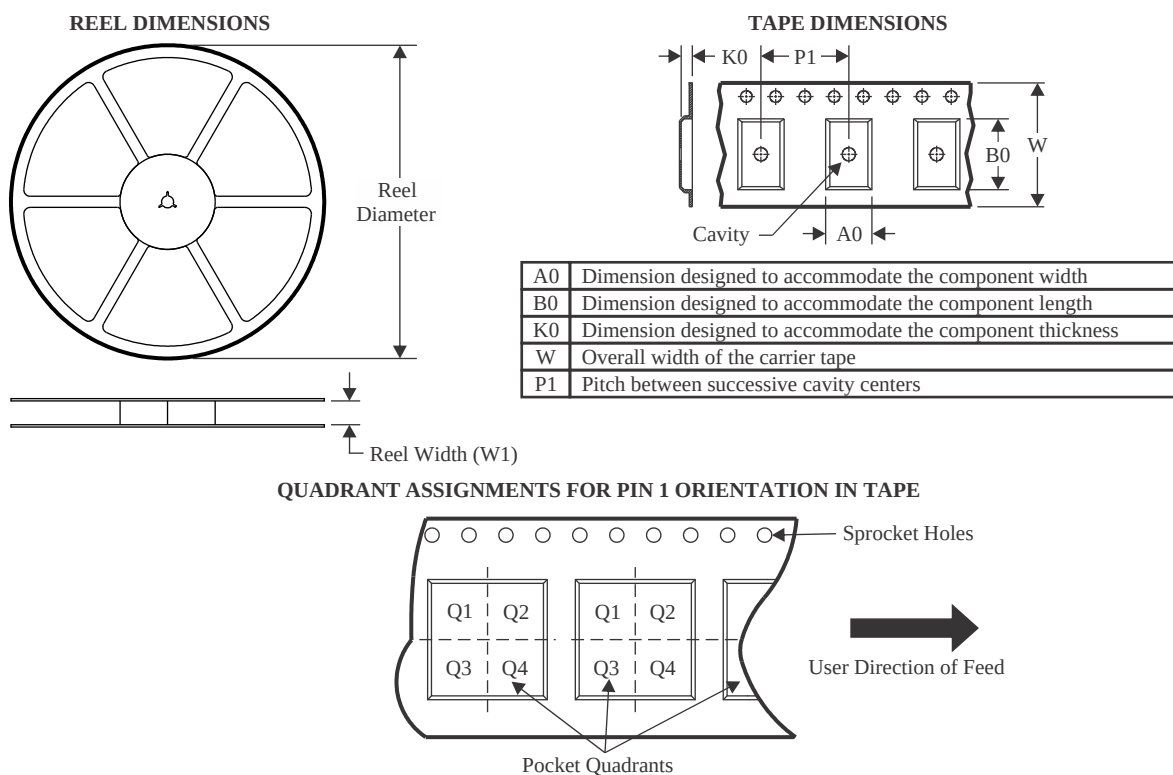
**OTHER QUALIFIED VERSIONS OF ISO6720, ISO6721, ISO6721R :**

- Automotive : [ISO6720-Q1](#), [ISO6721-Q1](#), [ISO6721R-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

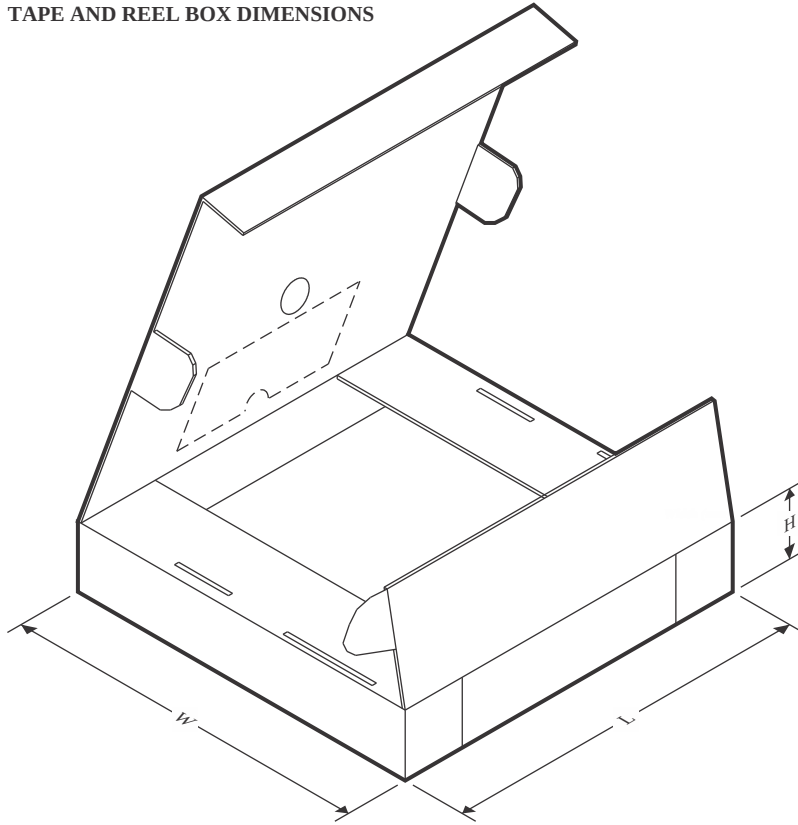
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISO6720BDR     | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |
| ISO6720FBDR    | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |
| ISO6721BDR     | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |
| ISO6721BDR     | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| ISO6721FBDR    | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |
| ISO6721RBDR    | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| ISO6721RBDR    | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |
| ISO6721RFBDR   | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |
| ISO6721RFBDRG4 | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| ISO6721RFBDRG4 | SOIC         | D               | 8    | 3000 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ISO6720BDR     | SOIC         | D               | 8    | 3000 | 356.0       | 356.0      | 36.0        |
| ISO6720FBDR    | SOIC         | D               | 8    | 3000 | 356.0       | 356.0      | 36.0        |
| ISO6721BDR     | SOIC         | D               | 8    | 3000 | 356.0       | 356.0      | 36.0        |
| ISO6721BDR     | SOIC         | D               | 8    | 3000 | 353.0       | 353.0      | 32.0        |
| ISO6721FBDR    | SOIC         | D               | 8    | 3000 | 356.0       | 356.0      | 36.0        |
| ISO6721RBDR    | SOIC         | D               | 8    | 3000 | 353.0       | 353.0      | 32.0        |
| ISO6721RBDR    | SOIC         | D               | 8    | 3000 | 356.0       | 356.0      | 36.0        |
| ISO6721RFBDR   | SOIC         | D               | 8    | 3000 | 356.0       | 356.0      | 36.0        |
| ISO6721RFBDRG4 | SOIC         | D               | 8    | 3000 | 353.0       | 353.0      | 32.0        |
| ISO6721RFBDRG4 | SOIC         | D               | 8    | 3000 | 356.0       | 356.0      | 36.0        |



## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



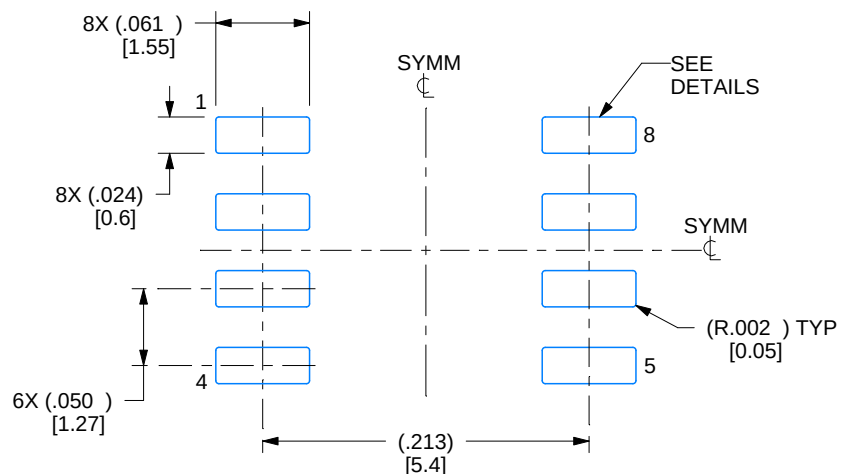
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

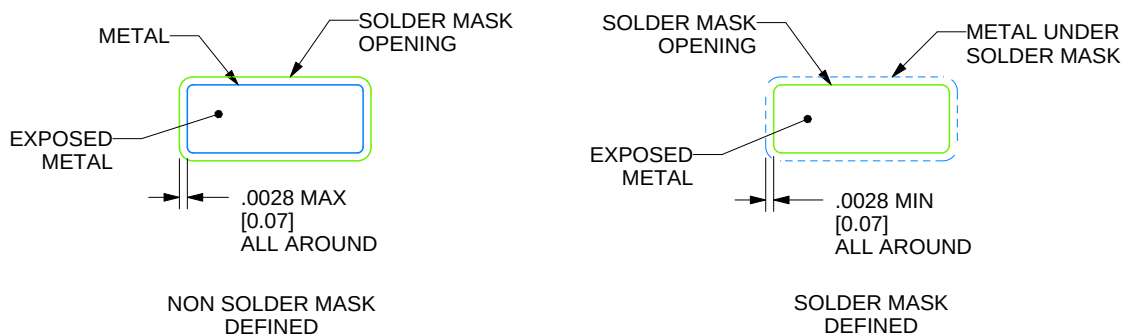
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

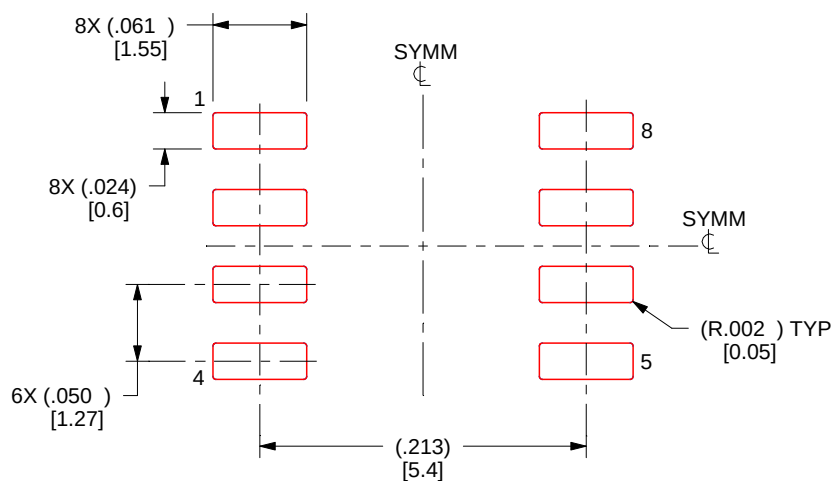
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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