ISO644x General-Purpose, Basic and Reinforced, Quad-Channel Digital Isolators

1 Features

- Functional Safety-Capable
  - Documentation available to aid IEC 61508 system design
- Up to 150Mbps data rate
- Robust SiO_2 isolation barrier:
  - High lifetime at up to $1061V_{RMS}$ and $1500V_{DC}$ working voltage
  - Up to $5000V_{RMS}$ isolation rating
  - Up to 10.4kV surge capability
  - Up to ±200kV/µs minimum CMTI
  - Wide temperature range: –40°C to 125°C ambient operating
- Supply range: 2.25V to 5.5V
- Overvoltage Tolerant Inputs
- Default output *high* (ISO644x) and *low* (ISO644xF) options
- Low propagation delay: 10ns maximum at 5V, 12ns maximum at 3.3V
- Supports SPI up to: 25MHz at 5V, 20.8MHz at 3.3V
- Low pulse width distortion: 1.8ns maximum at 5V, 2.2ns maximum at 3.3V
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - Low emissions
- Small Footprint Packages:
  - Wide-SSOP (DFP-16) Package
  - SSOP (DBQ-16) Package
- Safety-Related Certifications (Planned):
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 and CSA CAS Notice No. 5A
  - IEC 62368-1, IEC 61010-1 and GB 4943.1 certifications

2 Applications

- Power supplies
- Grid, Electricity meter
- Motor drives
- Factory automation
- Building automation
- Lighting
- Appliances

3 Description

The ISO644x devices are general purpose digital isolators designed for applications requiring up to $5000V_{RMS}$ isolation rating per UL 1577. The devices are also certified by VDE, TUV, and CQC.

The ISO644x devices provide high EMC performance while isolating CMOS or LVCMOS digital I/Os. ISO644x uses SiO_2 as the isolation barrier. Each isolation channel has a logic input and output buffer separated by the insulation barrier. These devices come with enable pins that can be used to put the respective outputs in high impedance.

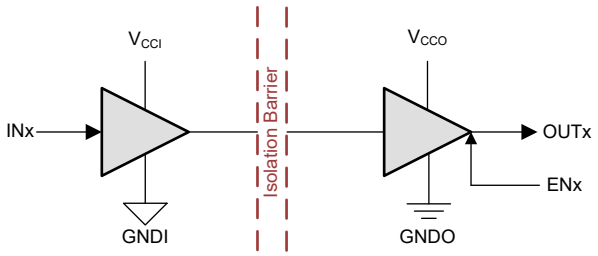
The ISO6440 and ISO6440F devices have all channels in the forward direction. The ISO6441 and ISO6441F devices have one reverse-direction channel. The ISO6442 and ISO6442F devices have two reverse-direction channels.

In the event of input power or signal loss, the default output is *high* for devices without the suffix F and *low* for devices with the suffix F. See the *Device Functional Modes* section for further details.

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE(2)
ISO6440 , ISO6440F	Wide-SOIC (DW-16) (3)	10.3mm × 10.3mm
ISO6441 , ISO6441F	Wide-SSOP (DFP-16) (3)	10.3mm × 4.65mm
ISO6442 , ISO6442F	SSOP (DBQ-16) (3)	6mm × 4.9mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Please refer to Packaging Information table on the Package Option Addendum page in the Mechanical, Packaging, and Orderable Information section for Production or Preproduction status for specific device and package.



V_{CCI}=Input supply, V_{CCO}=Output supply
GNDI=Input ground, GNDO=Output ground

Simplified Schematic

Table of Contents

4 Device Comparison

Table 4-1. Device Comparison Table

DEVICE NAME	TOTAL CHANNELS	REVERSE CHANNELS	DEFAULT OUTPUT	PACKAGE	CREEPAGE & CLEARANCE	VDE RATING	UL V_{ISO}	CMTI
ISO6440DWR	4	0	HIGH	Wide-SOIC (DW-16)	>8.15mm	Reinforced	5000V_{RMS}	±250kV/µs typical, ±200kV/µs minimum
ISO6440FDWR			LOW					
ISO6441DWR		1	HIGH					
ISO6441FDWR			LOW					
ISO6442DWR		2	HIGH					
ISO6442FDWR			LOW					
ISO6440DFPR	4	0	HIGH	Wide-SSOP (DFP-16)	>8mm	Reinforced	5000V_{RMS}	±250kV/µs typical, ±200kV/µs minimum
ISO6440FDFPR			LOW					
ISO6441DFPR		1	HIGH					
ISO6441FDFPR			LOW					
ISO6442DFPR		2	HIGH					
ISO6442FDFPR			LOW					
ISO6440DBQR	4	0	HIGH	SSOP (DBQ-16)	>3.7mm	Basic	3000V_{RMS}	±180kV/µs typical, ±150kV/µs minimum
ISO6440FDBQR			LOW					
ISO6441DBQR		1	HIGH					
ISO6441FDBQR			LOW					
ISO6442DBQR		2	HIGH					
ISO6442FDBQR			LOW					

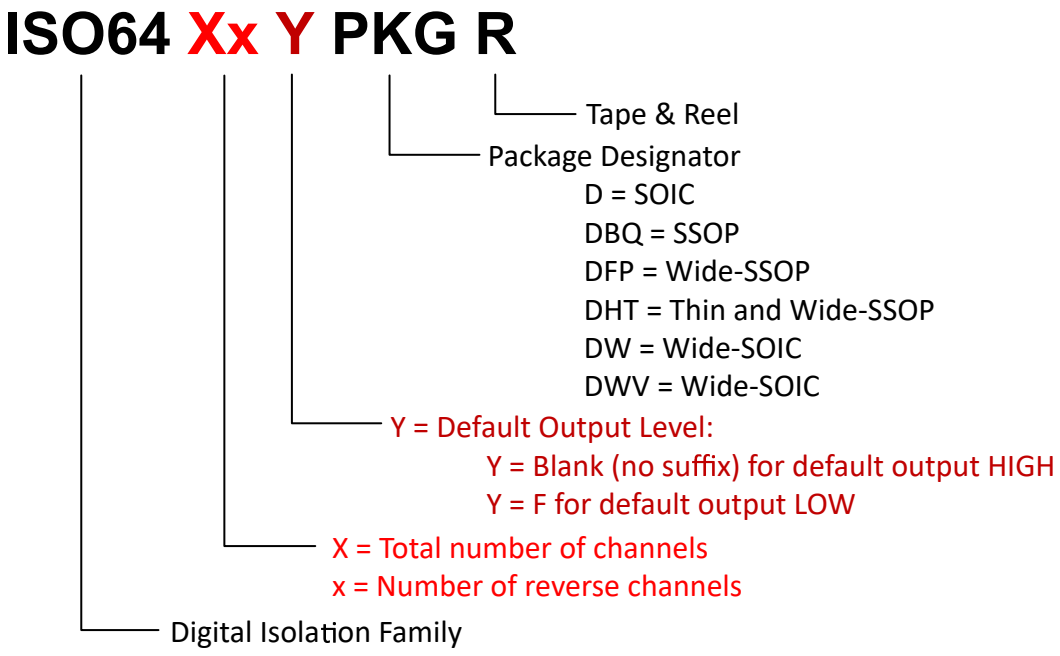


Figure 4-1. Device Nomenclature

5 Pin Configuration and Functions

Pin Configuration for Wide-SOIC (DW-16) , Wide-SSOP (DFP-16) and SSOP (DBQ-16)

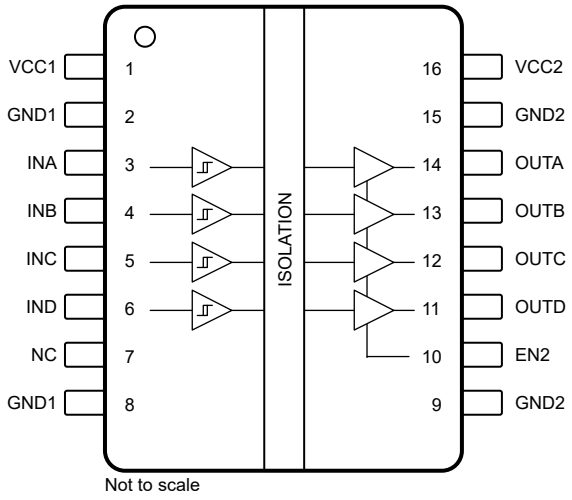


Figure 5-1. ISO6440 and ISO6440F Top View

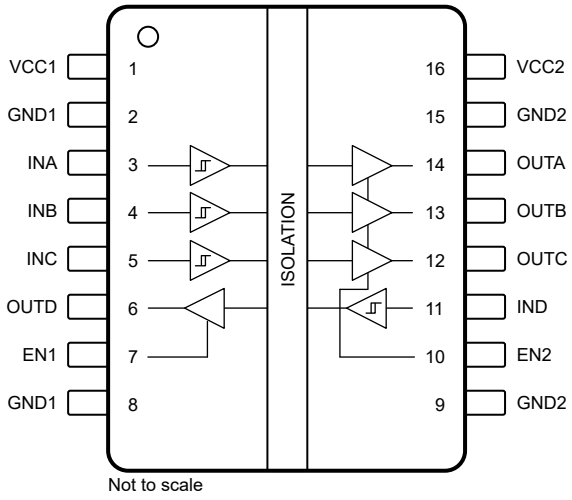


Figure 5-2. ISO6441 and ISO6441F Top View

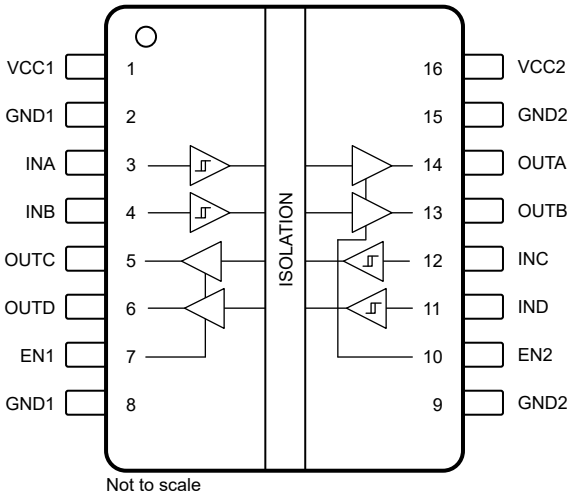


Figure 5-3. ISO6442 and ISO6442F Top View

Table 5-1. Pin Functions

PIN				Type[1]	DESCRIPTION
NAME	ISO6440 , ISO6440F	ISO6441 , ISO6441F	ISO6442 , ISO6442F		
EN1	-	7	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	10	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2, 8	2,8	2,8	—	Ground connection for V_{CC1}
GND2	9, 15	9,15	9,15	—	Ground connection for V_{CC2}
INA	3	3	3	I	Input, channel A
INB	4	4	4	I	Input, channel B
INC	5	5	12	I	Input, channel C
IND	6	11	11	I	Input, channel D
NC	7	-	-		Not connected
OUTA	14	14	14	O	Output, channel A
OUTB	13	13	13	O	Output, channel B
OUTC	12	12	5	O	Output, channel C
OUTD	11	6	6	O	Output, channel D
V_{CC1}	1	1	1	—	Power supply, side 1
V_{CC2}	16	16	16	—	Power supply, side 2

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
Supply voltage (2)	V_{CC1} to GND1	-0.5	6	V
	V_{CC2} to GND2	-0.5	6	
Digital Input Voltage	INx to GNDx	-0.5	6	V
Digital Input Voltage	ENx to GNDx	-0.5	6	V
Digital Output Voltage	OUTx to GNDx	-0.5	V_{CCX} + 0.5 (3)	V
Digital Output current	I_O	-15	15	mA
Temperature	Operating junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC_RO} (1)	Supply Voltage Side 1 (Recommended Operating Range)	V_{CC1} = 2.5V to 5V (3)	2.25		5.5	V
	Supply Voltage Side 2 (Recommended Operating Range)	V_{CC2} = 2.5V to 5V (3)	2.25		5.5	V
V_{CC_UVLO+}	V_{CC} UVLO threshold when supply voltage is rising				2.24	V
V_{CC_UVLO-}	V_{CC} UVLO threshold when supply voltage is falling		1.6			V
$V_{CC\_UVLO\_HYS}$	V_{CC} Supply voltage UVLO hysteresis		0.1			V
$V_{IH(ENx)}$	Enable: High level Input voltage	Enable: High level Input voltage	0.7 × V_{CCI} (2)		V_{CCI}	V
$V_{IL(ENx)}$	Enable: Low level Input voltage	Enable: Low level Input voltage	0		0.3 × V_{CCI}	V
$V_{IH(INx)}$	Input: High level Input voltage		0.7 × V_{CCI} (2)		V_{CCI}	V
$V_{IL(INx)}$	Input: Low level Input voltage		0		0.3 × V_{CCI}	V
I_{OH}	Output: High level output current	V_{CCO} = 5V (2)	-4			mA
		V_{CCO} = 3.3V (2)	-2			mA
		V_{CCO} = 2.5V (2)	-1			mA
I_{OL}	Output: Low level output current	V_{CCO} = 5V (2)			4	mA
		V_{CCO} = 3.3V (2)			2	mA
		V_{CCO} = 2.5V (2)			1	mA
DR	Data Rate	3.0V ≤ V_{CCx} ≤ 5.5V and C_L≤ 15pF(4)	0		150	Mbps
		2.25V ≤ V_{CCx} < 3V and C_L≤ 10pF(4)	0		150	Mbps
		2.25V ≤ V_{CCx} < 3V and 10pF < C_L≤ 15pF(4)	0		100	Mbps
T_A	Ambient temperature		-40	25	125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(3) The channel outputs are in undetermined state when $V_{CC\_UVLO-} \le V_{CC1}, V_{CC2} < V_{CC\_RO(MIN)}$.
(4) See Section 7 .

6.4 Thermal Information

		THERMAL METRIC(1)						UNIT
PACKAGE	PINS	$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DW (Wide-SOIC)	16	83	48.5	49	28	48.4	NA	°C/W
DFP (Wide-SSOP)	16	113.3	63.6	75.6	32.5	74.4	NA	°C/W
DBQ (SSOP)	16	117.8	60	69.8	29.9	69	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6440 (default high) and ISO6440F (default low, with F suffix)						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 75MHz 50% duty cycle square wave			268.2	mW
P_{D1}	Maximum power dissipation (side-1)				58.1	mW
P_{D2}	Maximum power dissipation (side-2)				210.1	mW
ISO6441 (default high) and ISO6441F (default low, with F suffix)						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L =15pF, Input a 75MHz 50% duty cycle square wave			262.2	mW
P_{D1}	Maximum power dissipation (side-1)				94.1	mW
P_{D2}	Maximum power dissipation (side-2)				168.1	mW
ISO6442 (default high) and ISO6442F (default low, with F suffix)						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, Input a 75MHz 50% duty cycle square wave			268	mW
P_{D1}	Maximum power dissipation (side-1)				134	mW
P_{D2}	Maximum power dissipation (side-2)				134	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	PACKAGE			UNIT
			16-DW	16-DFP	16-DBQ	
IEC 60664-1						
CLR	External clearance(1)	Side 1 to side 2 distance through air	>8.15	>8.0	>3.7	mm
CPG	External creepage(1)	Side 1 to side 2 distance across package surface	>8.15	>8.0	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	>17	>9	µm
CTI	Comparative tracking index	IEC 60112	>600	>600	>600	V
	Material Group	According to IEC 60664-1	I	I	I	
	Overvoltage category	Rated mains voltage ≤ 150V_{RMS}	I-IV	I-IV	I-IV	
		Rated mains voltage ≤ 300V_{RMS}	I-IV	I-IV	I-III	
		Rated mains voltage ≤ 600V_{RMS}	I-IV	I-IV	n/a	
		Rated mains voltage ≤ 1000V_{RMS}	I-III	I-III	n/a	
DIN EN IEC 60747-17 (VDE 0884-17)						
	Suitability	DIN EN IEC 60747-17 (VDE 0884-17) suitability(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	1500	707	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test.	1061	1061	500	V_{RMS}
		DC voltage	1500	1500	707	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	7071	7071	4243	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	8000	8000	4000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10400	10400	5200	V_{PK}
q_{pd}	Apparent charge(5)	Method a, After Input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤5	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM}$ (for reinforced devices) or $1.2 \times V_{IORM}$ (for basic devices) for t_m = 10s	≤5	≤5	≤5	
		Method b: At routine test (100% production); $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$ (for reinforced devices) or $1.5 \times V_{IORM}$ (for basic devices), t_m = 1s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	≤5	≤5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2 πft), f = 1MHz	≅1.6	≅1.3	≅1.9	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$>10^9$	$>10^9$	$>10^9$	
	Pollution degree		2	2	2	
	Climatic category		40/125/21	40/125/21	40/125/21	
UL 1577						
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5000	5000	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal

in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.

(2) This digital isolator is suitable for *safe electrical insulation* (reinforced device) or *basic electrical insulation* (basic device) only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air to determine the surge immunity of the package.

(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.

(5) Apparent charge is electrical discharge caused by a partial discharge (pd).

(6) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to UL 1577 and CSA CAS Notice No. 5A	Plan to certify according to GB4943.1	Plan to certify according to EN 61010-1 and EN 62368-1
Certificate planned	Certificate planned	Certificate planned	Certificate planned

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 Package						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 83°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			273.8	mA
		$R_{\theta JA}$ = 83°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			418.3	mA
		$R_{\theta JA}$ = 83°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C			547.6	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 83°C/W, T_J = 150°C, T_A = 25°C			1506	mW
T_S	Maximum safety temperature				150	°C
DFP-16 Package						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 113.3°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			200.6	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 113.3°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			306.5	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 113.3°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C			401.2	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 113.3°C/W, T_J = 150°C, T_A = 25°C			1103.3	mW
T_S	Maximum safety temperature				150	°C
DBQ-16 Package						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 117.8°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			192.9	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 117.8°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			294.8	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 117.8°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C			385.9	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 117.8°C/W, T_J = 150°C, T_A = 25°C			1061.1	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(OUTx)}$	OUTx (output) high-level output voltage	I_{OH} = -4mA; See Section 7	V_{CCO} - 0.4 (1)			V
$V_{OL(OUTx)}$	OUTx (output) low-level output voltage	I_{OL} = 4mA; See Section 7			0.4	V
$V_{IT+(INx)}$	INx (input) switching threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IT-(INx)}$	INx (input) switching threshold voltage, falling		0.3 × V_{CCI} (1)			V
$V_{I\_HYS(INx)}$	INx (input) switching threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
$I_{I(INx)}$	INx (input) input current (default high device)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at INx (leakage and current through default high pull-up resistance)	-10			µA
	INx (input) input current (default low device, with F suffix)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage and current through default low pull-down resistance)			10	µA
		LOW Input Current: V_{IL} = 0V at INx (leakage current)	-1			µA
$V_{IH(ENx)}$	ENx (enable) threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IL(ENx)}$	ENx (enable) threshold voltage, falling		0.3 × V_{CCI} (1)			V
$V_{I\_HYS(ENx)}$	ENx (enable) threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
$I_{I(ENx)}$	ENx (enable) input current (integrated pull-up)	HIGH Input Current: V_{IH} = V_{CCI} (1) at ENx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at ENx (leakage and current through default high pull-up resistance)	-10			µA
CMTI_R	Common mode transient immunity, device rated for reinforced isolation (DW Package , DFP Package)	V_I = V_{CC} or 0V, V_{CM} = 1200V, V_{ENx} = V_{CC} ; See Section 7	200	250		kV/µs
CMTI_B	Common mode transient immunity, device rated for basic isolation (DBQ Package)	V_I = V_{CC} or 0V, V_{CM} = 500V, V_{ENx} = V_{CC} ; See Section 7	150	180		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 5V		1.5		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.10 Supply Current Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6440 (default high) and ISO6440F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0V (default low, with F suffix)		I_{CC1}		3.4	4.7	mA
			I_{CC2}		1.3	1.5	
	V_I = 0V (default high); V_I = V_{CC1} (default low, with F suffix)		I_{CC1}		11.3	13.1	
			I_{CC2}		1.1	1.3	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		7.25	8.9	
			I_{CC2}		1.4	1.6	
		10Mbps	I_{CC1}		7.35	8.9	
			I_{CC2}		3.2	3.9	
		100Mbps	I_{CC1}		7.8	10.0	
			I_{CC2}		22	26	
ISO6441 (default high) and ISO6441F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0V (default low, with F suffix)		I_{CC1}		3.2	4.6	mA
			I_{CC2}		2.2	3	
	V_I = 0V (default high); V_I = V_{CC1} (default low, with F suffix)		I_{CC1}		8.5	10.5	
			I_{CC2}		3.9	4.8	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		5.9	7.5	
			I_{CC2}		3.2	4	
		10Mbps	I_{CC1}		6.5	8.1	
			I_{CC2}		4.7	5.6	
		100Mbps	I_{CC1}		11.5	13.9	
			I_{CC2}		18.4	21.7	
ISO6442 (default high) and ISO6442F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0V (default low, with F suffix)		I_{CC1} , I_{CC2}		2.2	3.15	mA
	V_I = 0V (default high); V_I = V_{CC1} (default low, with F suffix)		I_{CC1} , I_{CC2}		5.6	7.4	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}, I_{CC2}		4.1	5.3	
		10Mbps	I_{CC1}, I_{CC2}		5.5	6.5	
		100Mbps	I_{CC1}, I_{CC2}		15.2	18.0	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx}
(3) Supply current valid for ENx = V_{CCx}

6.11 Electrical Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(OUTx)}$	OUTx (output) high-level output voltage	I_{OH} = -2mA; See Section 7	V_{CCO} - 0.2(1)			V
$V_{OL(OUTx)}$	OUTx (output) low-level output voltage	I_{OL} = 2mA; See Section 7			0.2	V
$V_{IT+(INx)}$	INx (input) switching threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IT-(INx)}$	INx (input) switching threshold voltage, falling		0.3 × V_{CCI} (1)			V
$V_{I\_HYS(INx)}$	INx (input) switching threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
$I_{I(INx)}$	INx (input) input current (default high device)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at INx (leakage and current through default high pull-up resistance)	-10			µA
	INx (input) input current (default low device, with F suffix)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage and current through default low pull-down resistance)			10	µA
		LOW Input Current: V_{IL} = 0V at INx (leakage current)	-1			µA
$V_{IH(ENx)}$	ENx (enable) threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IL(ENx)}$	ENx (enable) threshold voltage, falling		0.3 × V_{CCI} (1)			V
$V_{I\_HYS(ENx)}$	ENx (enable) threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
$I_{I(ENx)}$	ENx (enable) input current (integrated pull-up)	HIGH Input Current: V_{IH} = V_{CCI} (1) at ENx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at ENx (leakage and current through default high pull-up resistance)	-10			µA
CMTI_R	Common mode transient immunity, device rated for reinforced isolation (DW Package , DFP Package)	V_I = V_{CC} or 0V, V_{CM} = 1200V, V_{ENx} = V_{CC} ; See Section 7	200	250		kV/µs
CMTI_B	Common mode transient immunity, device rated for basic isolation (DBQ Package)	V_I = V_{CC} or 0V, V_{CM} = 500V, V_{ENx} = V_{CC} ; See Section 7	150	180		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 3.3V		1.5		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.12 Supply Current Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6440 (default high) and ISO6440F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0V (default low, with F suffix)		I_{CC1}		3.3	4.7	mA
			I_{CC2}		1.2	1.5	
	V_I = 0V (default high); V_I = V_{CC1} (default low, with F suffix)		I_{CC1}		10.3	13.1	
			I_{CC2}		1.1	1.3	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		7.5	8.8	
			I_{CC2}		1.3	1.5	
		10Mbps	I_{CC1}		7.5	8.9	
			I_{CC2}		2.5	2.9	
		100Mbps	I_{CC1}		8.0	9.5	
			I_{CC2}		14.9	17.0	
ISO6441 (default high) and ISO6441F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0V (default low, with F suffix)		I_{CC1}		3.2	4.5	mA
			I_{CC2}		2.2	2.9	
	V_I = 0V (default high); V_I = V_{CC1} (default low, with F suffix)		I_{CC1}		8.5	10.4	
			I_{CC2}		3.8	4.8	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		5.9	7.4	
			I_{CC2}		3.1	3.9	
		10Mbps	I_{CC1}		6.2	7.8	
			I_{CC2}		4.1	5	
		100Mbps	I_{CC1}		9.5	11.6	
			I_{CC2}		13.2	15.5	
ISO6442 (default high) and ISO6442F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0V (default low, with F suffix)		I_{CC1} , I_{CC2}		2.4	3.1	mA
	V_I = V_{CC1} (1)(default high); V_I = 0V (default low, with F suffix)		I_{CC1} , I_{CC2}		5.6	7.3	
Supply current - AC signal (3)	V_I = 0V (default high); V_I = V_{CC1} (default low, with F suffix)	1Mbps	I_{CC1}, I_{CC2}		4.4	5.2	
		10Mbps	I_{CC1}, I_{CC2}		5.1	6.0	
		100Mbps	I_{CC1}, I_{CC2}		11.5	13.1	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx}
(3) Supply current valid for ENx = V_{CCx}

6.13 Electrical Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH(OUTx)}$	OUTx (output) high-level output voltage	I_{OH} = -1mA; See Section 7	V_{CCO} - 0.1 (1)			V
$V_{OL(OUTx)}$	OUTx (output) low-level output voltage	I_{OL} = 1mA; See Section 7			0.1	V
$V_{IT+(INx)}$	INx (input) switching threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IT-(INx)}$	INx (input) switching threshold voltage, falling		0.3 × V_{CCI} (1)			V
$V_{I\_HYS(INx)}$	INx (input) switching threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
$I_{I(INx)}$	INx (input) input current (default high device)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at INx (leakage and current through default high pull-up resistance)	-10			µA
	INx (input) input current (default low device, with F suffix)	HIGH Input Current: V_{IH} = V_{CCI} (1) at INx (leakage and current through default low pull-down resistance)			10	µA
		LOW Input Current: V_{IL} = 0V at INx (leakage current)	-1			µA
$V_{IH(ENx)}$	ENx (enable) threshold voltage, rising				0.7 × V_{CCI} (1)	V
$V_{IL(ENx)}$	ENx (enable) threshold voltage, falling		0.3 × V_{CCI} (1)			V
$V_{I\_HYS(ENx)}$	ENx (enable) threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
$I_{I(ENx)}$	ENx (enable) input current (integrated pull-up)	HIGH Input Current: V_{IH} = V_{CCI} (1) at ENx (leakage current)			1	µA
		LOW Input Current: V_{IL} = 0V at ENx (leakage and current through default high pull-up resistance)	-10			µA
CMTI_R	Common mode transient immunity, device rated for reinforced isolation (DW Package , DFP Package)	V_I = V_{CC} or 0V, V_{CM} = 1200V, V_{ENx} = V_{CC} ; See Section 7	200	250		kV/µs
CMTI_B	Common mode transient immunity, device rated for basic isolation (DBQ Package)	V_I = V_{CC} or 0V, V_{CM} = 500V, V_{ENx} = V_{CC} ; See Section 7	150	180		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2MHz, V_{CC} = 2.5V		1.5		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

6.14 Supply Current Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6440 (default high) and ISO6440F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0V (default low, with F suffix)		I_{CC1}		3.3	4.6	mA
			I_{CC2}		1.2	1.4	
	V_I = 0V (default high); V_I = V_{CC1} (default low, with F suffix)		I_{CC1}		11.2	13.0	
			I_{CC2}		1.0	1.21	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		7.3	8.8	
			I_{CC2}		1.2	1.5	
		10Mbps	I_{CC1}		7.4	8.8	
			I_{CC2}		2.2	2.5	
		100Mbps	I_{CC1}		7.6	9.3	
			I_{CC2}		11.5	13.3	
ISO6441 (default high) and ISO6441F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0V (default low, with F suffix)		I_{CC1}		3.1	4.5	mA
			I_{CC2}		2.1	2.9	
	V_I = 0V (default high); V_I = V_{CC1} (default low, with F suffix)		I_{CC1}		8.5	10.4	
			I_{CC2}		3.8	4.7	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		5.8	7.4	
			I_{CC2}		3.1	3.9	
		10Mbps	I_{CC1}		6.1	7.7	
			I_{CC2}		3.8	4.7	
		100Mbps	I_{CC1}		8.6	10.6	
			I_{CC2}		10.7	12.7	
ISO6442 (default high) and ISO6442F (default low, with F suffix)							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(default high); V_I = 0V (default low, with F suffix)		I_{CC1} , I_{CC2}		2.1	3.1	mA
	V_I = 0V (default high); V_I = V_{CC1} (default low, with F suffix)		I_{CC1} , I_{CC2}		5.6	7.2	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}, I_{CC2}		3.9	5.2	
		10Mbps	I_{CC1}, I_{CC2}		4.6	5.8	
		100Mbps	I_{CC1}, I_{CC2}		9.3	11.5	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx}
(3) Supply current valid for ENx = V_{CCx}

6.15 Switching Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Section 7	3.85	6.2	10	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.07	1.8	
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.5	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				3	
t_r	Output signal rise time	See Section 7			3	ns
t_f	Output signal fall time				3	
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Section 7			9	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output				8	
t_{PZH}	Enable propagation delay, high impedance-to-high output for device with EN	See Section 7			7	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for device with EN				8	
t_{PU}	Time from V_{CC} UVLO to valid output data	V_{CC} ramp < 1µs			90	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below $V_{CC\_UVLO-(MIN)}$. See Section 7		0.045	0.1	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.23		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Section 7	4	7	12	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.35	2.2	
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.5	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				3	
t_r	Output signal rise time	See Section 7			4	ns
t_f	Output signal fall time				4	
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Section 7			14	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output				12	
t_{PZH}	Enable propagation delay, high impedance-to-high output for device with EN	See Section 7			11	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for device with EN				10	
t_{PU}	Time from V_{CC} UVLO to valid output data	V_{CC} ramp < 1µs			70	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below $V_{CC\_UVLO-(MIN)}$. See Section 7		0.045	0.1	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.2		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Section 7	4.75	8.4	14.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.55	2.6	
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			1.5	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				3	
t_r	Output signal rise time	See Section 7			5	ns
t_f	Output signal fall time				5	
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Section 7			19	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output				17	
t_{PZH}	Enable propagation delay, high impedance-to-high output for device with EN	See Section 7			17	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for device with EN				12	
t_{PU}	Time from V_{CC} UVLO to valid output data	V_{CC} ramp < 1µs			80	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below $V_{CC\_UVLO-(MIN)}$. See Section 7		0.047	0.1	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.22		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Insulation Characteristics Curves

Insulation Characteristics Curves for Wide-SOIC (DW-16) Package

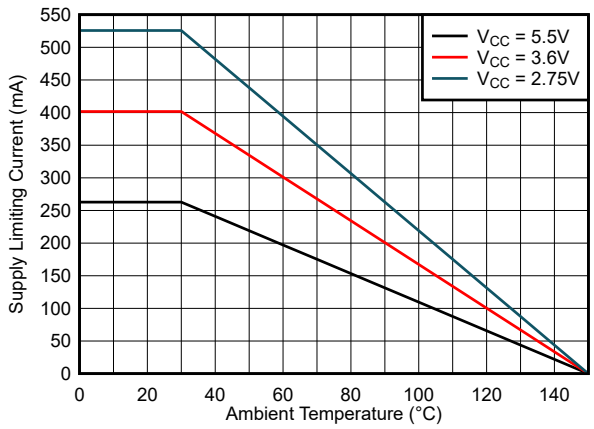


Figure 6-1. Thermal Derating Curve for Safety Limiting Current for Wide-SOIC (DW-16) Package

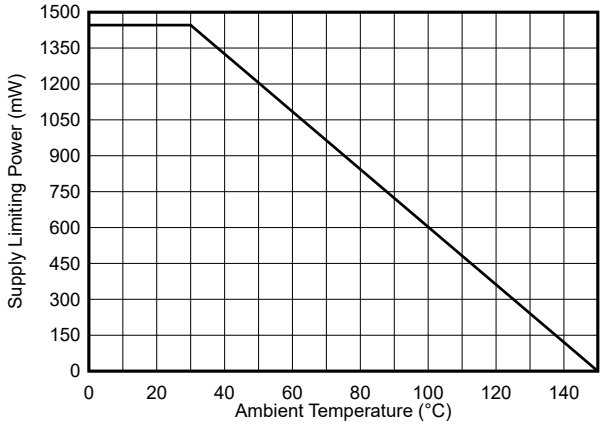


Figure 6-2. Thermal Derating Curve for Safety Limiting Power for Wide-SOIC (DW-16) Package

Insulation Characteristics Curves for Wide-SSOP (DFP-16) Package

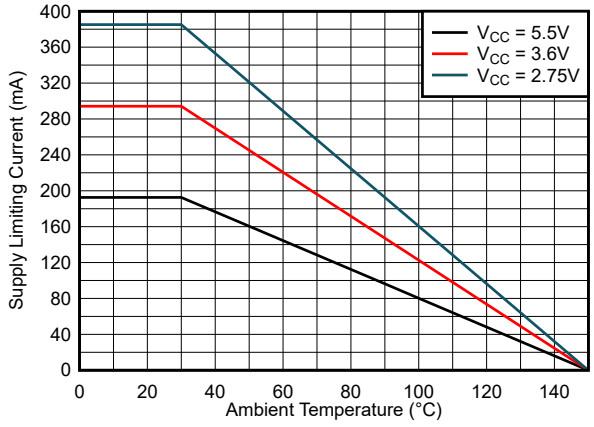


Figure 6-3. Thermal Derating Curve for Safety Limiting Current for Wide-SSOP (DFP-16) Package

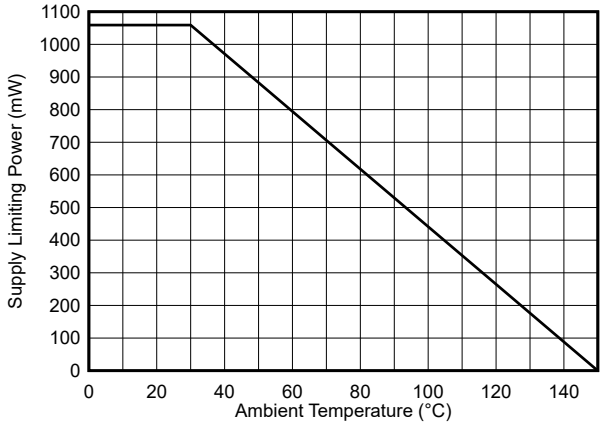


Figure 6-4. Thermal Derating Curve for Safety Limiting Power for Wide-SSOP (DFP-16) Package

Insulation Characteristics Curves for SSOP (DBQ-16) Package

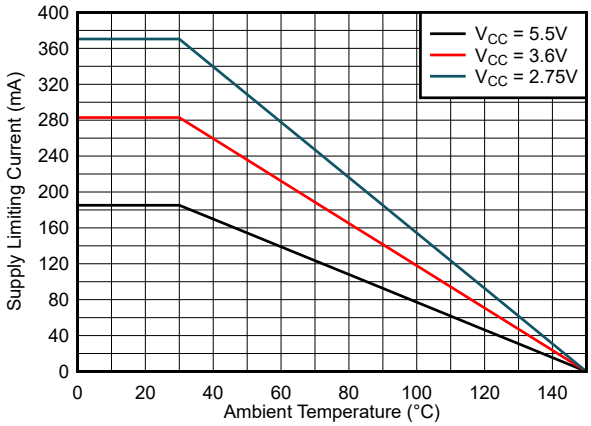


Figure 6-5. Thermal Derating Curve for Safety Limiting Current for SSOP (DBQ-16) Package

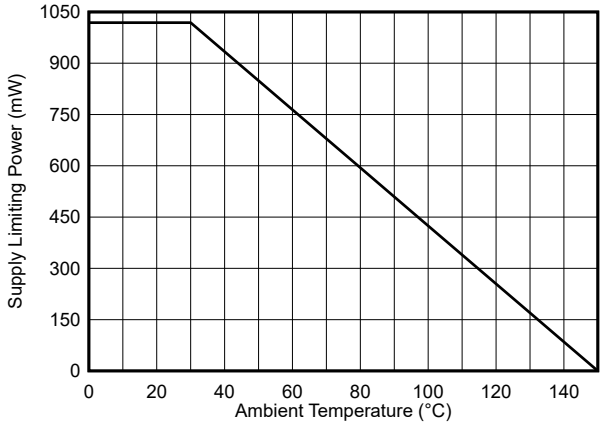


Figure 6-6. Thermal Derating Curve for Safety Limiting Power for SSOP (DBQ-16) Package

6.19 Typical Characteristics

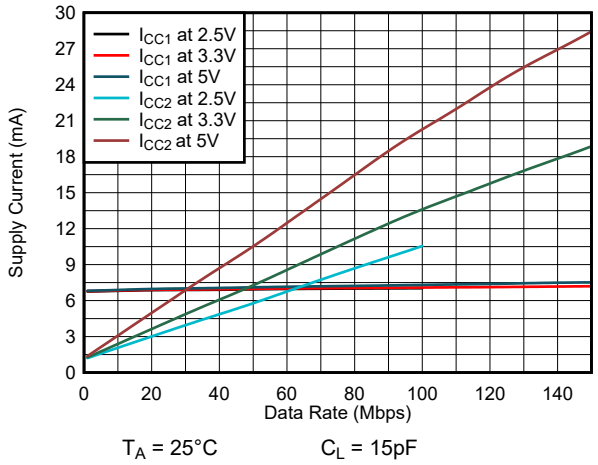


Figure 6-7. ISO6440 or ISO6440F Supply Current vs Data Rate (With 15pF Load)

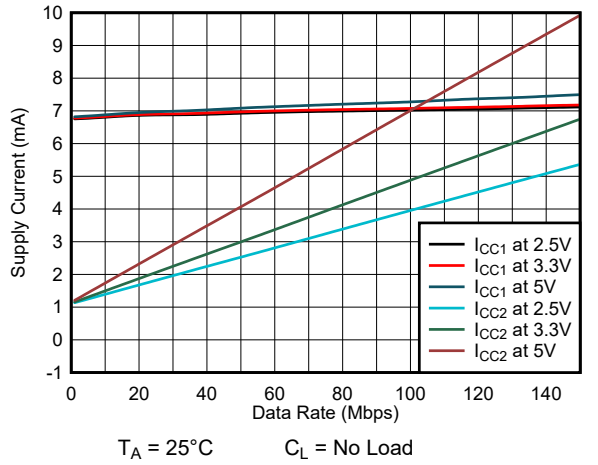


Figure 6-8. ISO6440 or ISO6440F Supply Current vs Data Rate (With No Load)

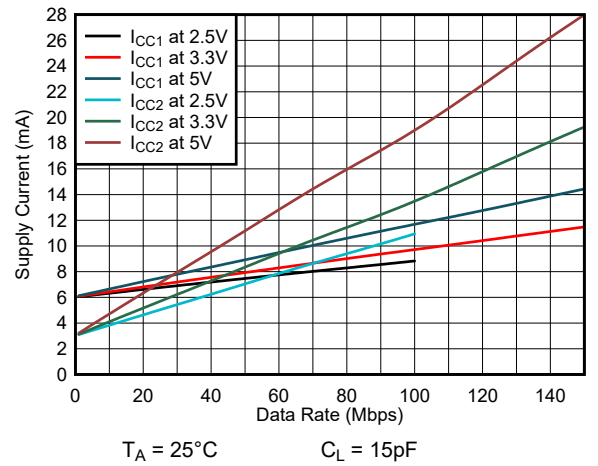


Figure 6-9. ISO6441 or ISO6441F Supply Current vs Data Rate (With 15pF Load)

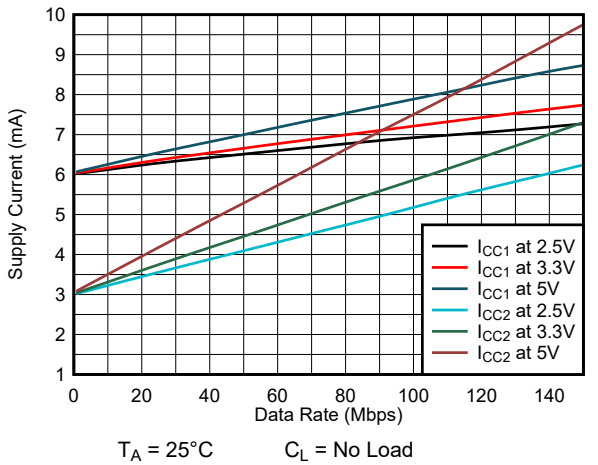


Figure 6-10. ISO6441 or ISO6441F Supply Current vs Data Rate (With No Load)

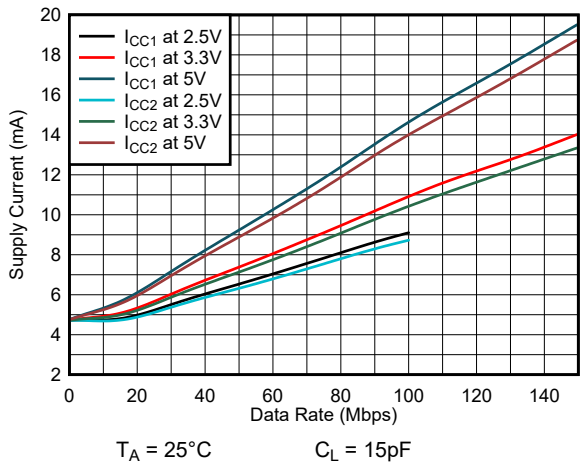


Figure 6-11. ISO6442 or ISO6442F Supply Current vs Data Rate (With 15pF Load)

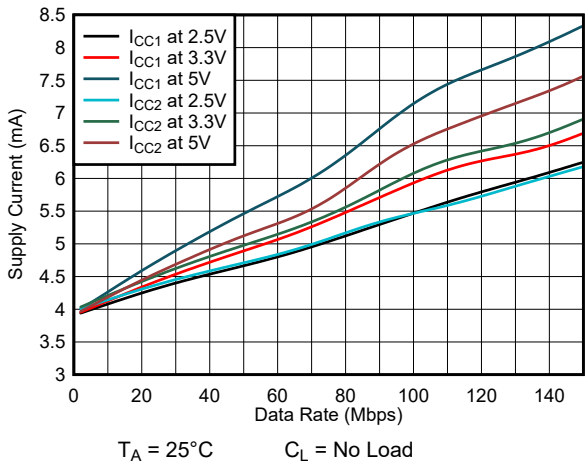


Figure 6-12. ISO6442 or ISO6442F Supply Current vs Data Rate (With No Load)

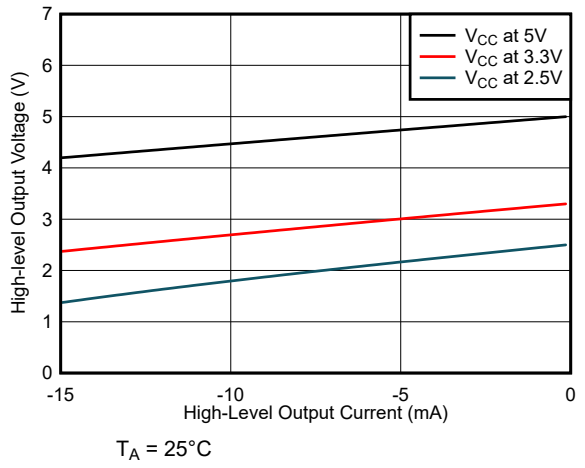


Figure 6-13. High-Level Output Voltage vs High-level Output Current

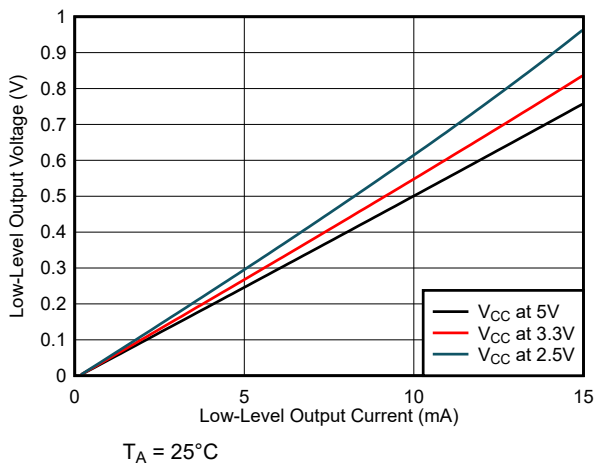


Figure 6-14. Low-Level Output Voltage vs Low-Level Output Current

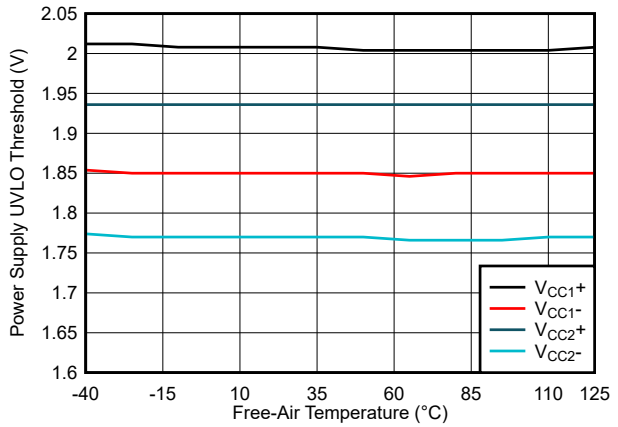


Figure 6-15. Power Supply Undervoltage Threshold vs Free-Air Temperature

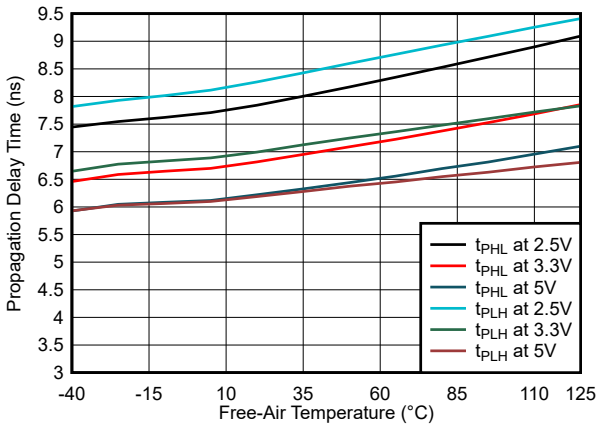
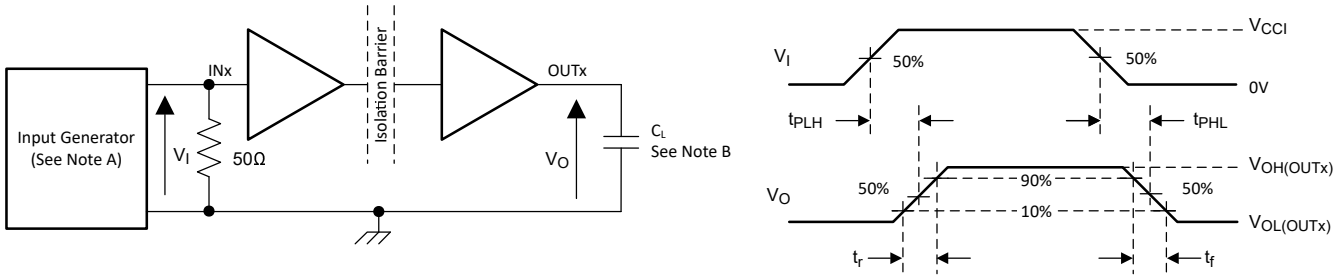


Figure 6-16. Propagation Delay Time vs Free-Air Temperature

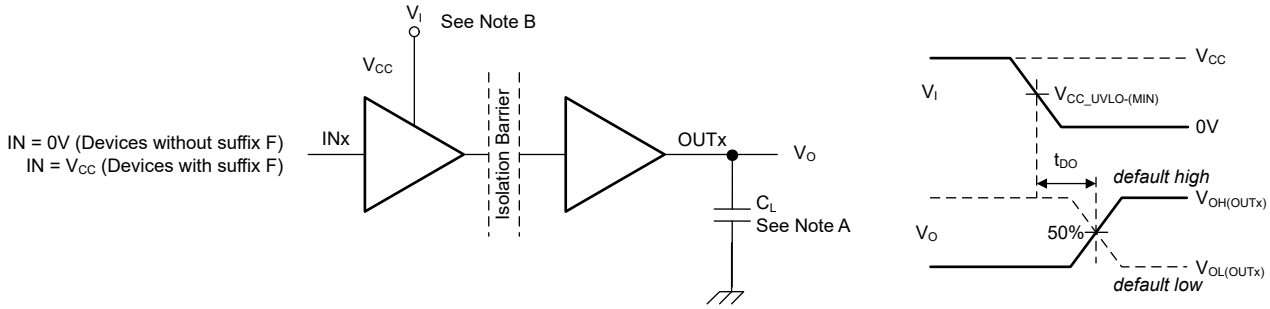
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 1ns, t_f ≤ 1ns, Z_O = 50Ω. At the input, 50Ω resistor is required to terminate INx (input) generator signal. The 50Ω resistor is not needed in the actual application.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

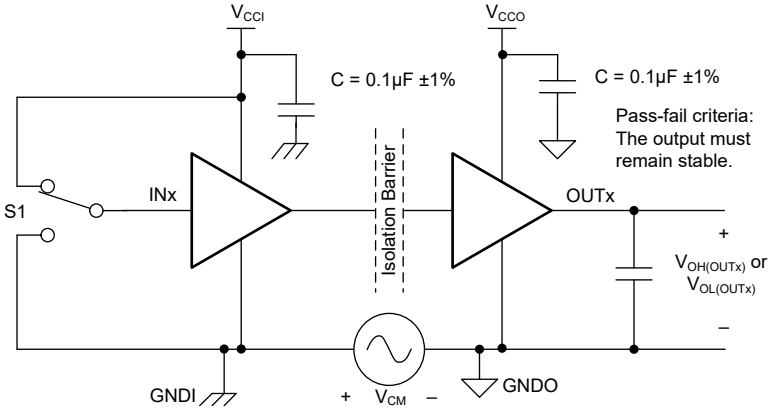
Figure 7-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10mV/ns

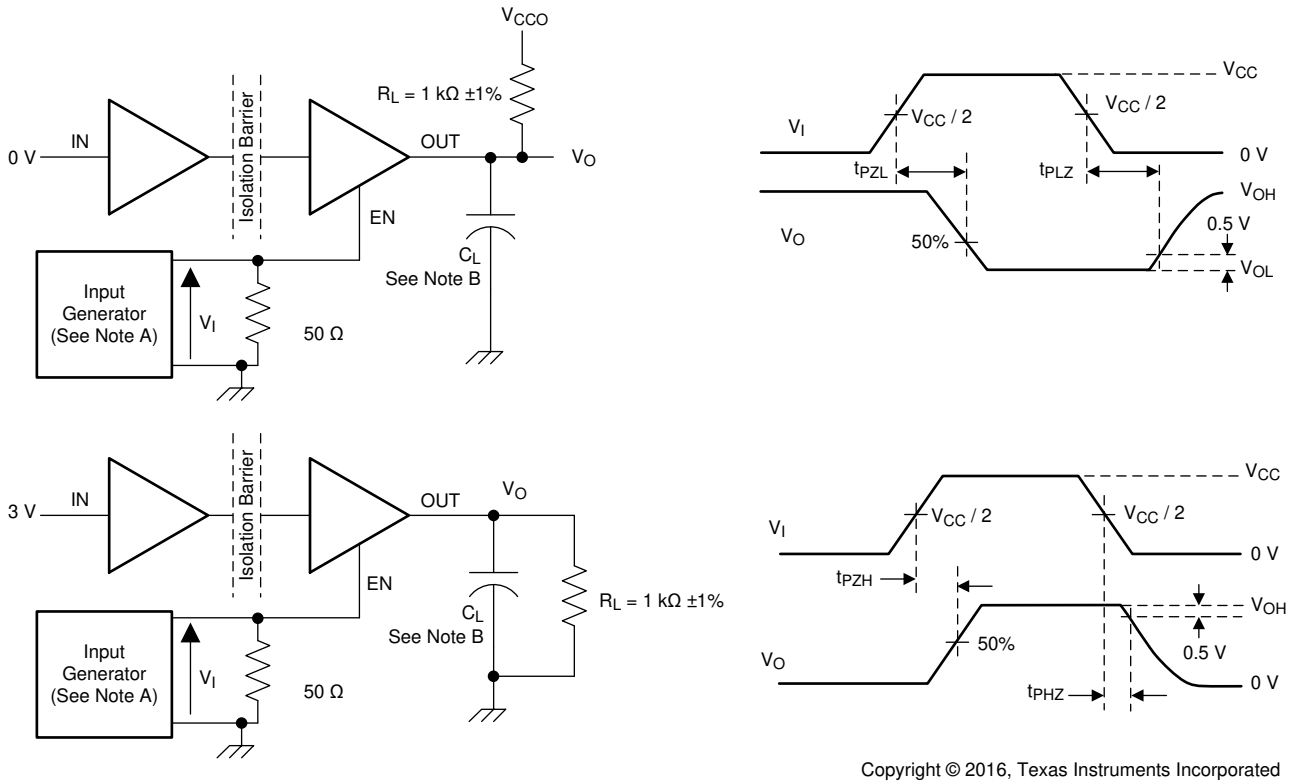
Figure 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

B. ENx = V_{CC}, channels are enabled during CMTI test.

Figure 7-3. Common-Mode Transient Immunity Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 7-4. Enable Propagation Delay Time Test Circuit and Waveform

8 Detailed Description

8.1 Overview

The ISO644x family of devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier.

The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The ISO644x devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching.

8.2 Functional Block Diagram

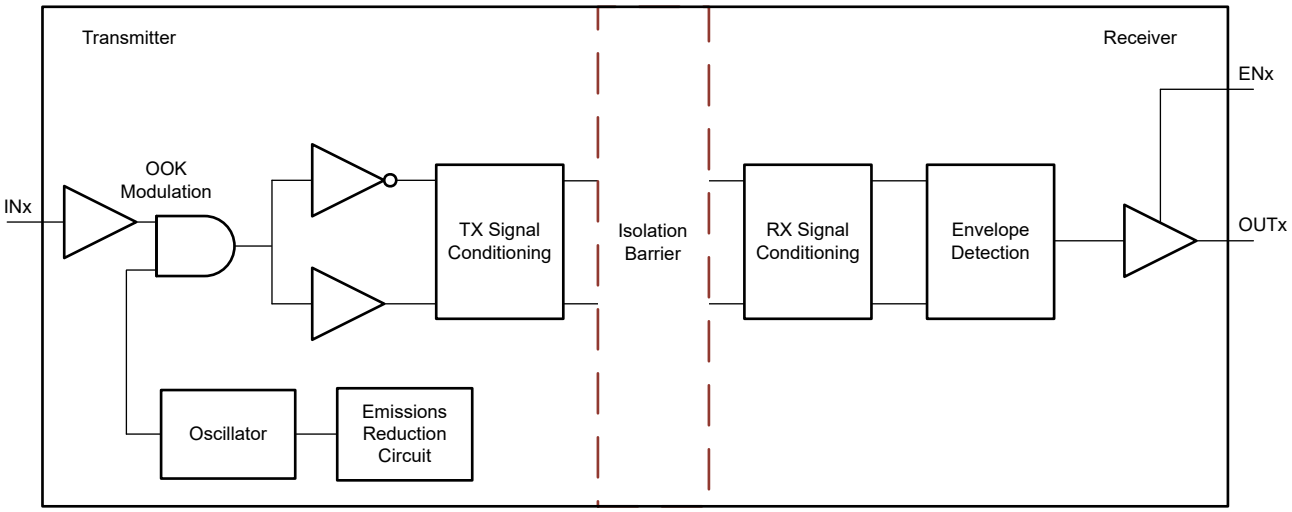


Figure 8-1. Conceptual Block Diagram of an OOK Based Digital Isolator

Figure 8-2 shows a conceptual detail of how the ON-OFF keying scheme works.

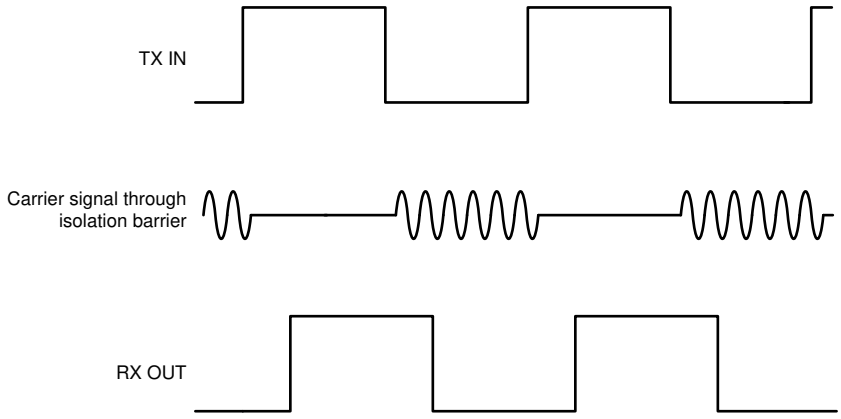


Figure 8-2. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

Table 8-1 provides an overview of the device features.

Table 8-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE
ISO6440	4 Forward 0 Reverse	150Mbps	High	DW-16 , DFP-16 , DBQ-16
ISO6440F	4 Forward 0 Reverse	150Mbps	Low	DW-16 , DFP-16 , DBQ-16
ISO6441	3 Forward 1 Reverse	150Mbps	High	DW-16 , DFP-16 , DBQ-16
ISO6441F	3 Forward 1 Reverse	150Mbps	Low	DW-16 , DFP-16 , DBQ-16
ISO6442	2 Forward 2 Reverse	150Mbps	High	DW-16 , DFP-16 , DBQ-16
ISO6442F	2 Forward 2 Reverse	150Mbps	Low	DW-16 , DFP-16 , DBQ-16

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are defined and tested by international standards such as IEC 61000-4-x and CISPR 32. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO644x family of devices incorporates many chip-level design techniques to help overall system robustness.

8.4 Device Functional Modes

The following table lists the functional modes for the ISO644x devices.

Table 8-2. Function Table

V_{CCI}(1)	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default is *High* for ISO644x and *Low* for ISO644xF (with F suffix).
X	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO644x and *Low* for ISO644xF (with F suffix). When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(2). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up ($V_{CC} \geq V_{CC\_RO(MIN)}$); PD = Powered down ($V_{CC} \leq V_{CC\_UVLO-}$); X = Irrelevant; H = High level; L = Low level; Z = High Impedance

(2) The outputs are in undetermined state when $V_{CC\_UVLO-} \leq V_{CCI}$ or $V_{CCO} < V_{CC} \geq V_{CC\_RO(MIN)}$.

8.5 Device I/O Schematics

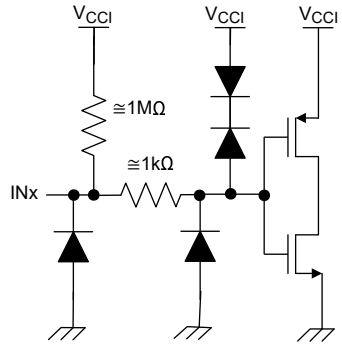


Figure 8-3. Input (INx) Default High (Device Without F Suffix Device) Schematics

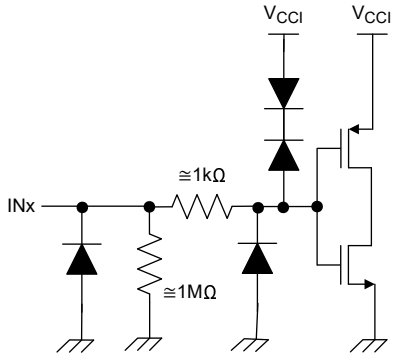


Figure 8-4. Input (INx) Default Low (Device With F Suffix Device) Schematics

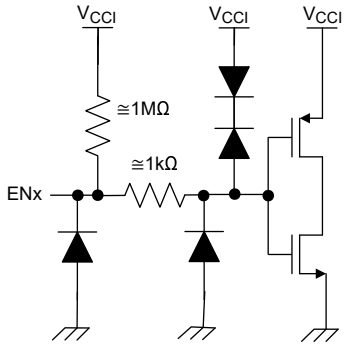


Figure 8-5. Enable (ENx) Schematics

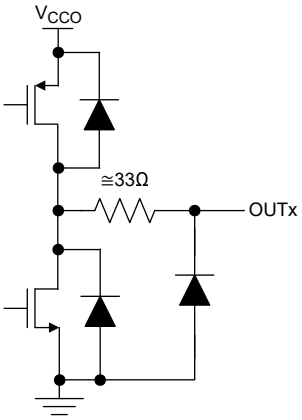


Figure 8-6. Output (OUTx) Schematics

8.6 Overvoltage Tolerant Input

The input pins of this device, INx and ENx, support input signal voltage in excess of the supply voltage (V_{CCI}) on the input side of the device as long as the voltage on the inputs remains below the voltages listed in the Recommended Operating Conditions , and Absolute Maximum Ratings .

This allows the device to support input signal voltages on the inputs when the input supply, V_{CCI}, is unpowered. In this use case, the outputs transition to the default output state when the input side no longer has a valid supply.

These inputs also provide the capability of the inputs to down translate input signal voltages up to the V_{IMAX} in the Recommended Operating Conditions . For example, an input signal 5V high-level can be used while V_{CCI} is operating a 3.3V.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO644x devices are high-performance, low power, quad-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for parallel (multiple) driver applications. The ISO644x devices use single-ended CMOS-logic switching technology.

The supply voltage range is from 2.25V to 5.5V for both supplies, V_{CC1} and V_{CC2}. Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within the Recommended Operating Conditions section. As an example, supplying ISO644x V_{CC1} with 3.3V (which is within 2.25V to 5.5V) and V_{CC2} with 5V (which is also within 2.25V to 5.5V) is possible. You can use the digital isolator as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

Figure 9-1 shows the isolated serial peripheral interface (SPI).

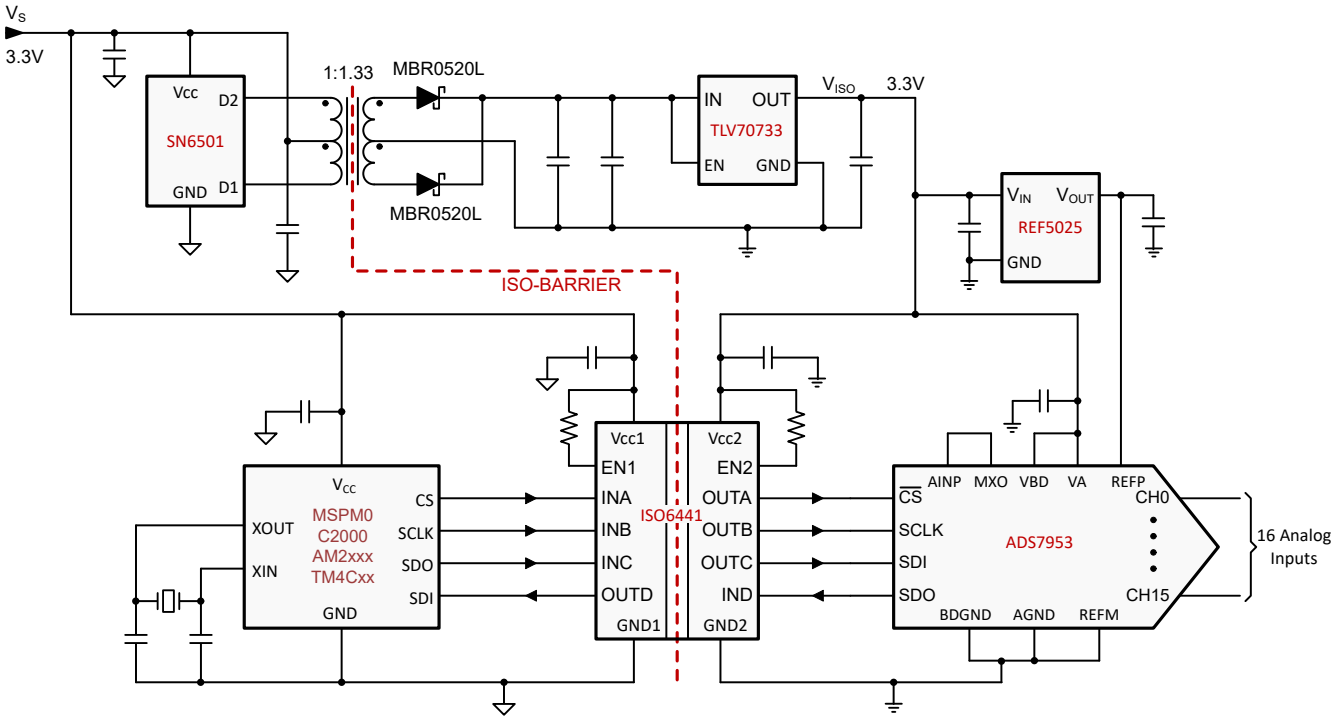


Figure 9-1. Isolated SPI for an Analog Input Module With 16 Inputs

9.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25V to 5.5V
Decoupling capacitor between V_{CC1} and GND1	0.1µF
Decoupling capacitor from V_{CC2} and GND2	0.1µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO644x family of devices only require two external bypass capacitors to operate.

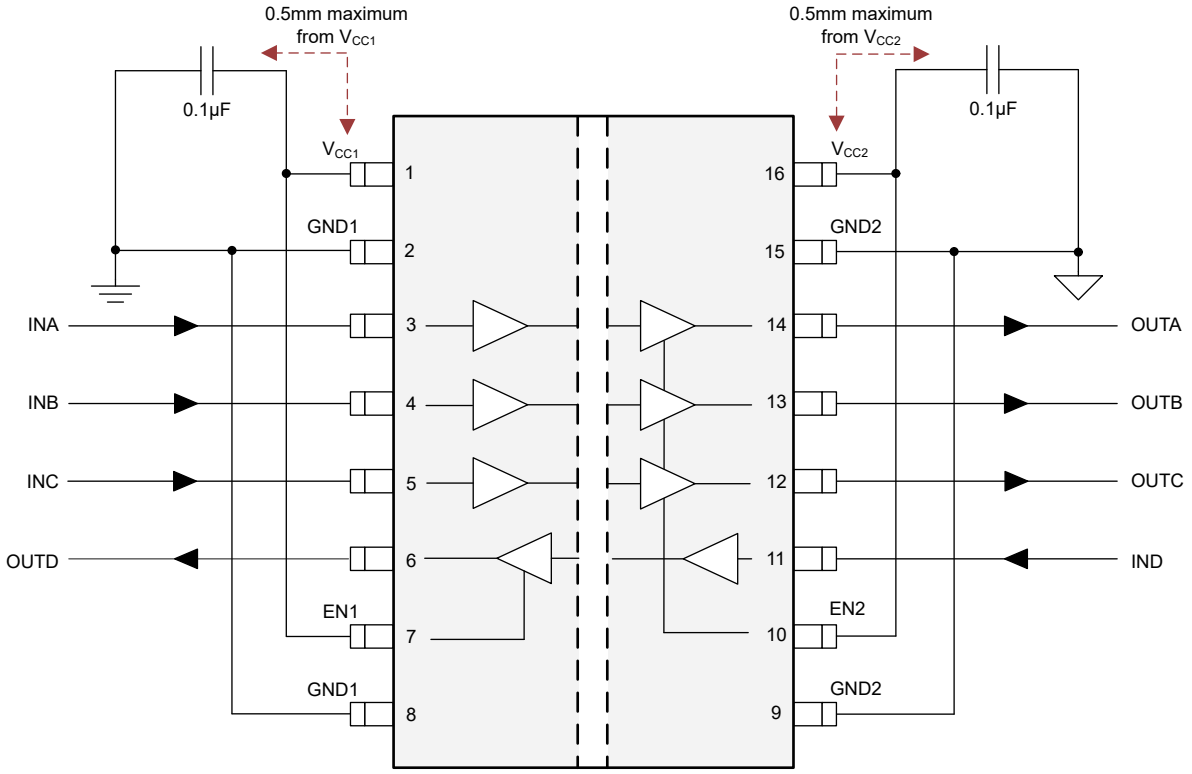
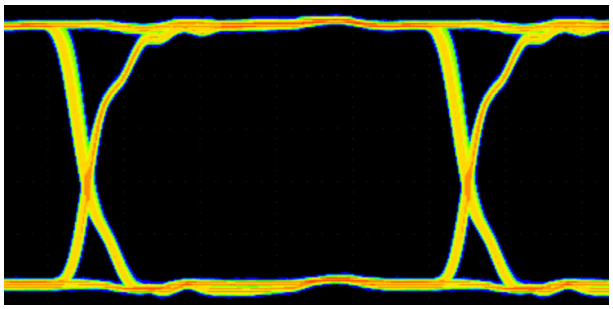


Figure 9-2. Typical ISO644x Circuit

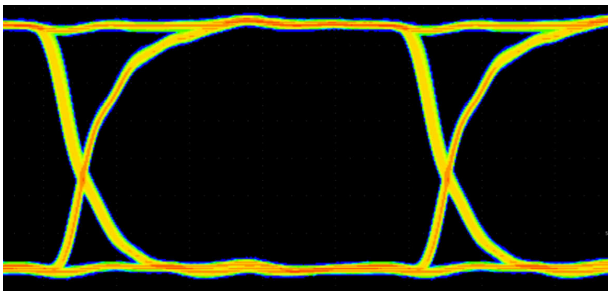
9.2.3 Application Curve

The following typical eye diagrams of the ISO644x family of devices indicates low jitter and wide open eye at 100Mbps.



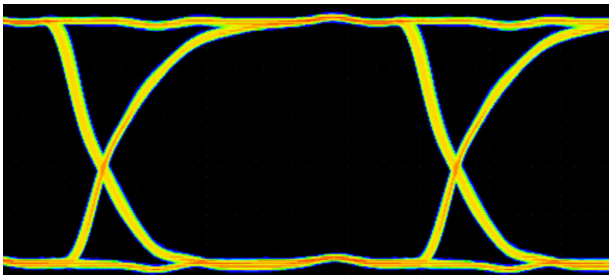
Horizontal 2ns / division, Vertical 1V / division.

Figure 9-3. ISO644x Eye Diagram at 100Mbps PRBS 2^{16} – 1, 5V and 25°C



Horizontal 2ns / division, Vertical 500mV / division.

Figure 9-4. ISO644x Eye Diagram at 100Mbps PRBS 2^{16} – 1, 3.3V and 25°C



Horizontal 2ns / division, Vertical 500mV / division.

Figure 9-5. ISO644x Eye Diagram at 100Mbps PRBS 2^{16} – 1, 2.5V and 25°C

9.3 Power Supply Recommendations

To provide reliable operation at data rates and supply voltages, a 0.1µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For industrial applications, please use Texas Instruments' SN6501 or SN6505B. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* or *SN6505B Low-noise, 1A Transformer Drivers for Isolated Power Supplies* .

9.4 Layout

9.4.1 Layout Guidelines

A minimum of two layers is required to accomplish a cost optimized and low EMI PCB design. To further improve EMI, a four layer board can be used (see Layout Example Schematic). Layer stacking for a four layer board must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This design makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide* application note.

9.4.2 Layout Example

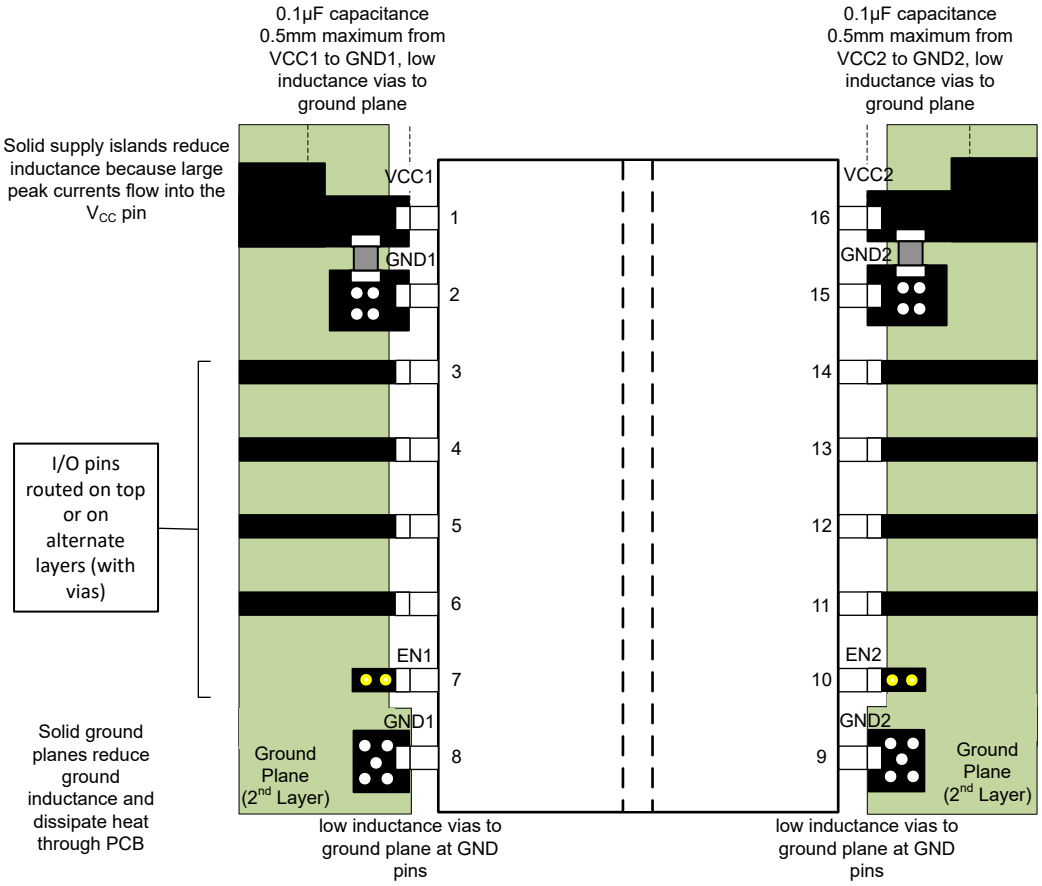


Figure 9-6. Layout Example

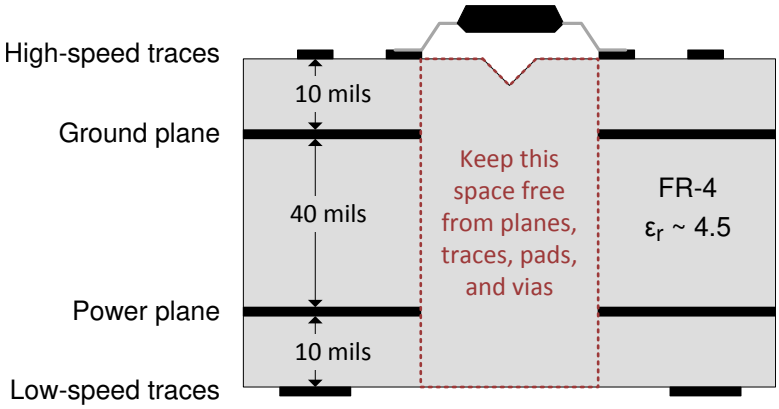


Figure 9-7. Layout Example PCB Cross Section

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ISO6440 Technical Documents*
- Texas Instruments, *ISO6441 Technical Documents*
- Texas Instruments, *ISO6442 Technical Documents*
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies,* data sheet

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Device Nomenclature

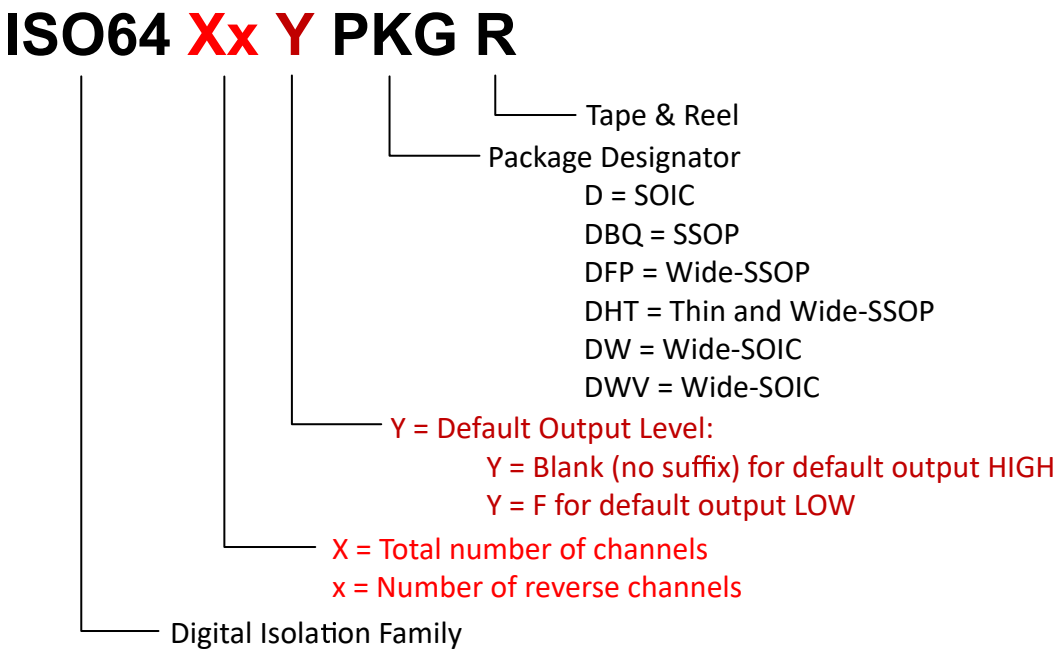


Figure 10-1. Device Nomenclature

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2025) to Revision C (May 2026) — **Page**

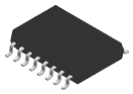
- Deleted planned CSA certification and added planned UL 1577 and CSA CAS Notice No. 5A certification throughout the document. Removed IEC 60601-1 from planned certifications. 1
- Updated the packages highlighted in the Features section for small footprint packages instead of all packages. 1
- Updated the nominal width of the DFP package in the Description Section Package Information Table. 1
- Updated the CMTI minimum and typical values throughout the document for CMTI_B (devices with basic insulation). 1
- Added ISO6440 and ISO6442 to the Pin Functions Table in the Pin Configurations and Functions section..... 4
- Added 16-DFP and 16-DBQ packages to the Insulation Specifications sub-section of the *Specifications* section and added test conditions for basic devices (16-DBQ package)..... 6
- Updated the Safety-Related Certifications sub-section of the *Specifications* section..... 6
- Updated the C_i typical value and CMTI_B minimum and typical value in all Electrical Characteristics for all supply voltages sub-sections of the *Specifications* section..... 6

Changes from Revision A (October 2024) to Revision B (November 2025) — **Page**

- Updated status of the data sheet to mixed status for both production and advanced information devices. Added ISO6440, ISO6440F, ISO6441F, ISO6442 and ISO6442F devices to the data sheet. Added Wide-SSOP (DFP-16) and SSOP (DBQ-16) packages to the data sheet. 1
- Added Device Comparison section to the data sheet. 3
- Updated the minimum propagation delay time, t_{PLH} and t_{PHL}, in the 5V Switching Characteristics and 2.5V Switching Characteristics sub-sections of the *Specifications* section covering the entire family of devices with ISO6440 and ISO6442 added to the data sheet. 6
- Added Enable Propagation Delay Time Test Circuit and Waveform in Section 7. 24

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

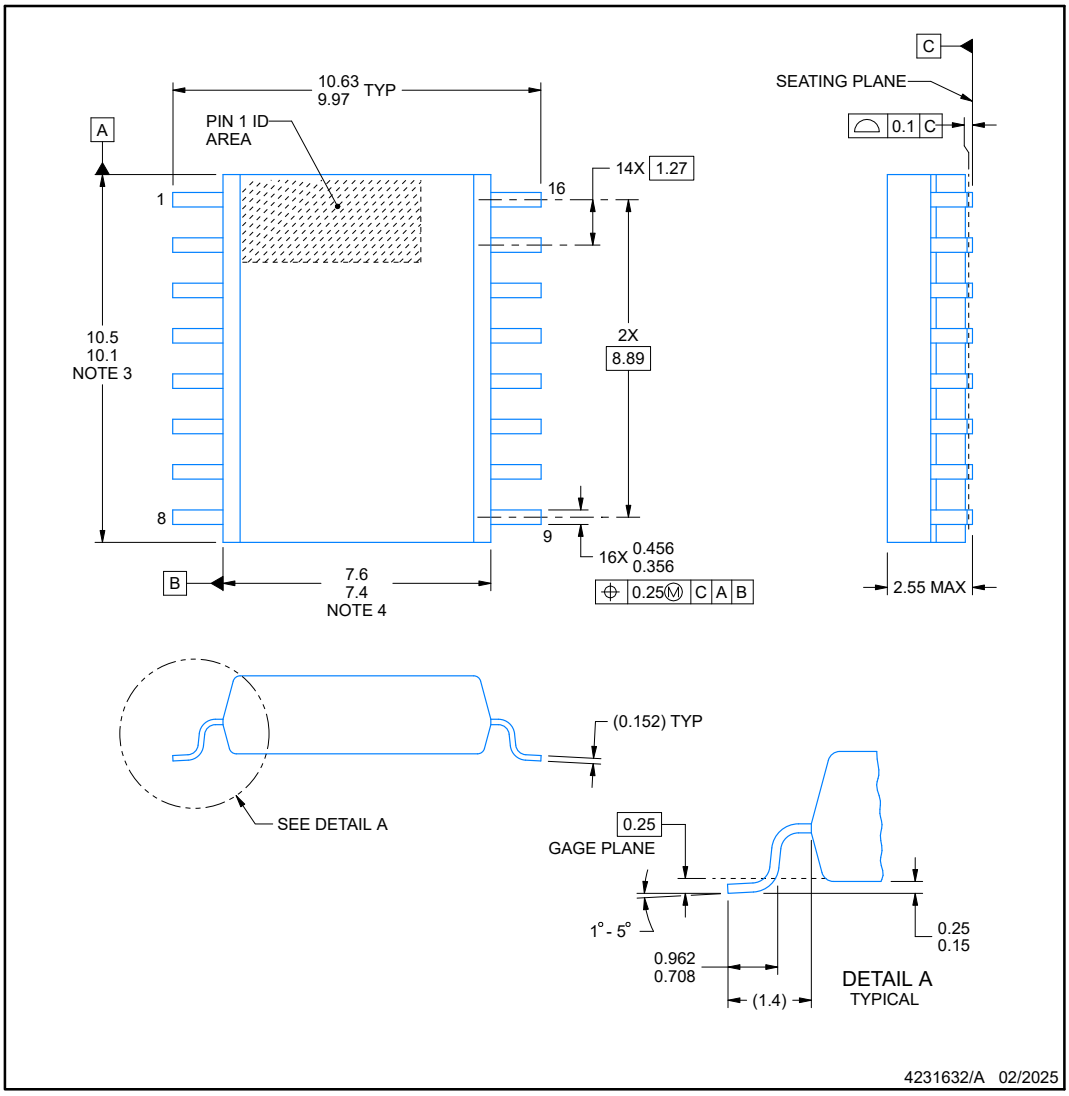


PACKAGE OUTLINE

DW0016C-C01

SOIC - 2.55 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

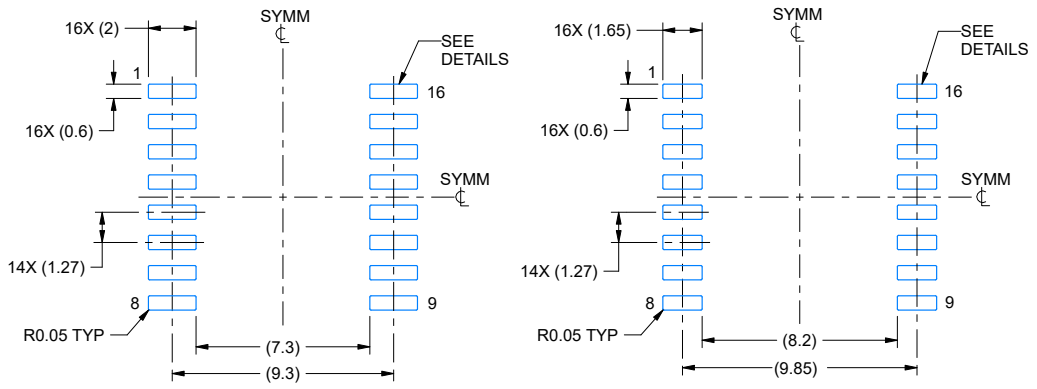
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

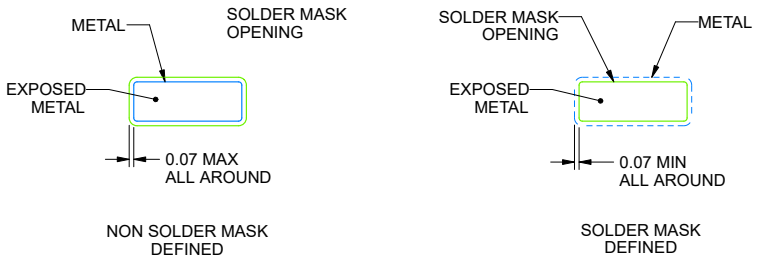
DW0016C-C01

SOIC - 2.55 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X



SOLDER MASK DETAILS

4231632/A 02/2025

NOTES: (continued)

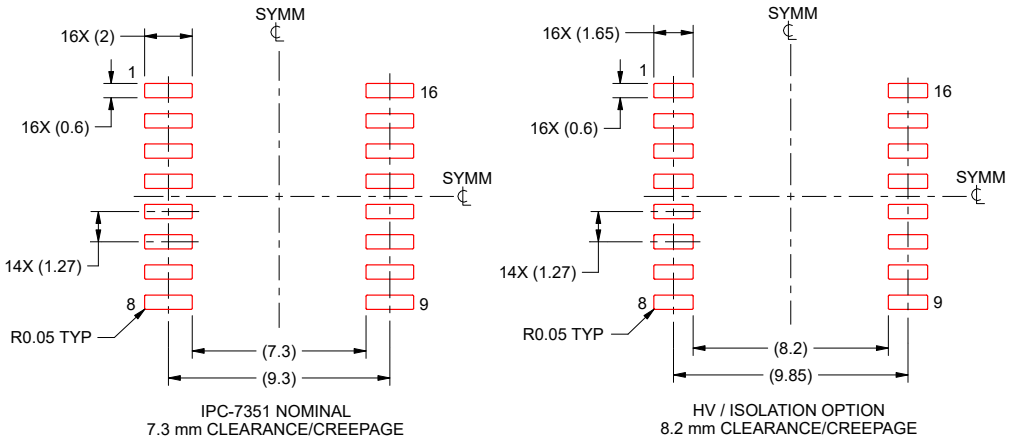
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016C-C01

SOIC - 2.55 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4231632/A 02/2025

NOTES: (continued)

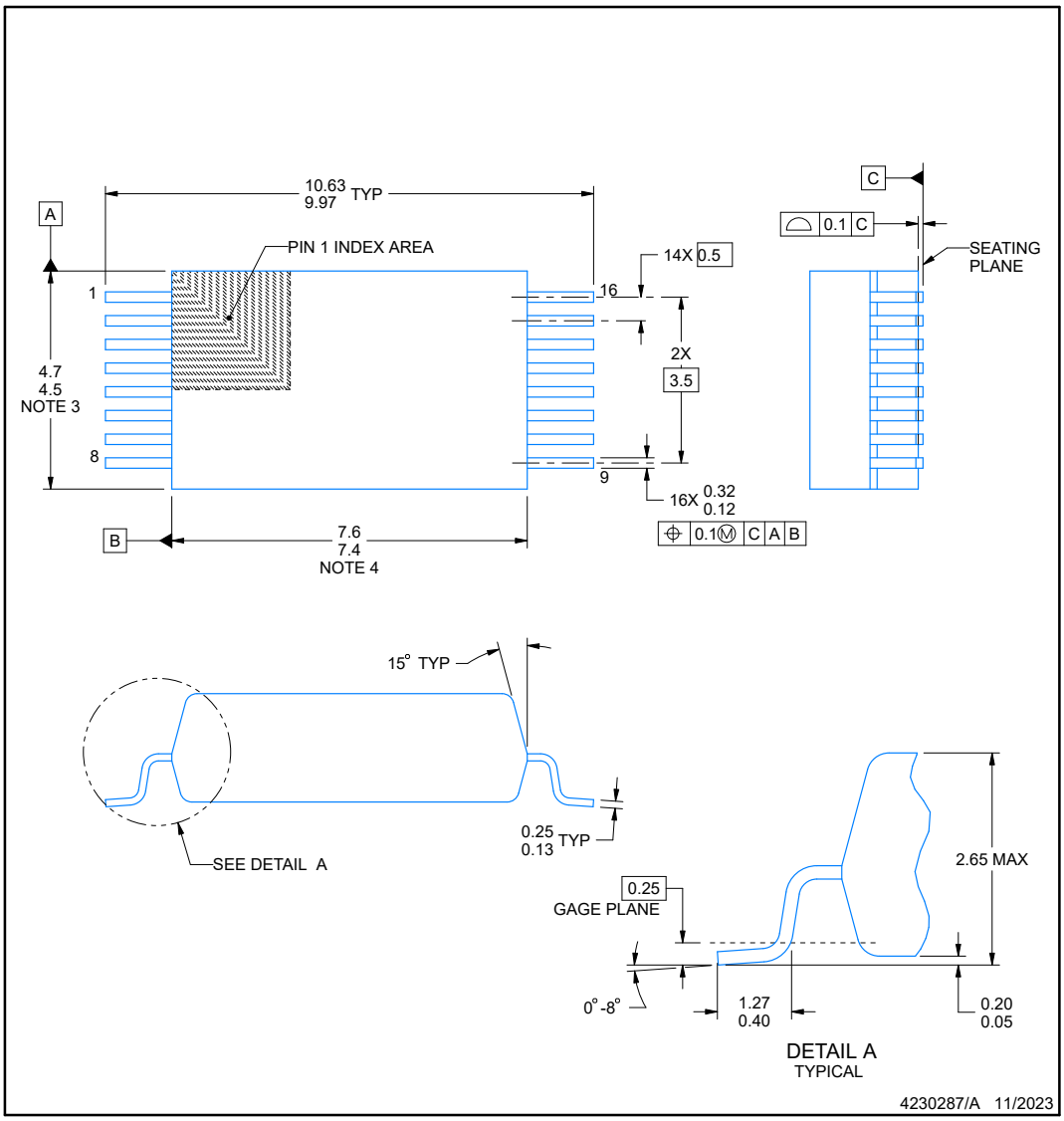
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DFP0016A

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



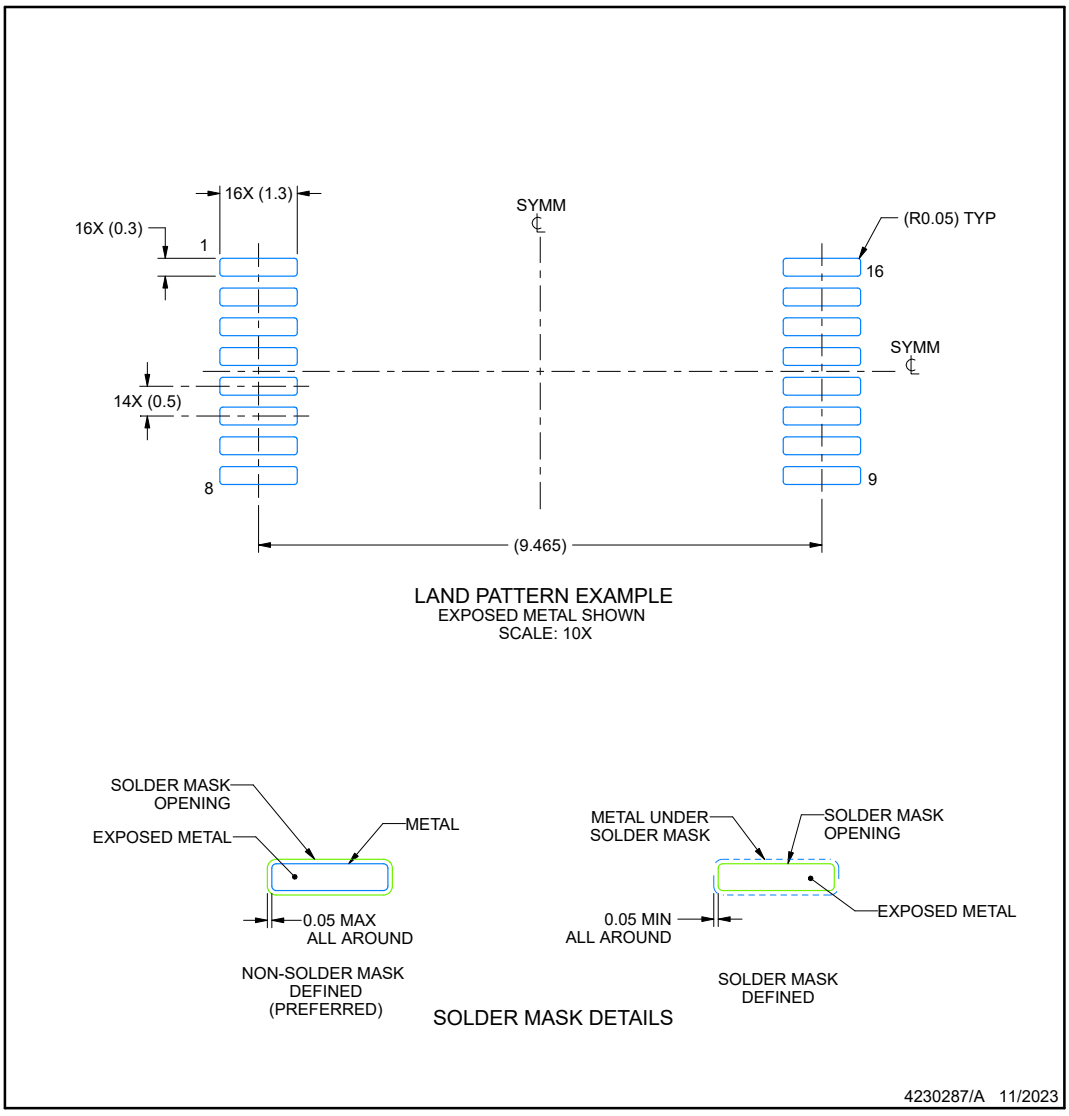
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

DFP0016A — **SSOP - 2.65 mm max height**

SMALL OUTLINE PACKAGE



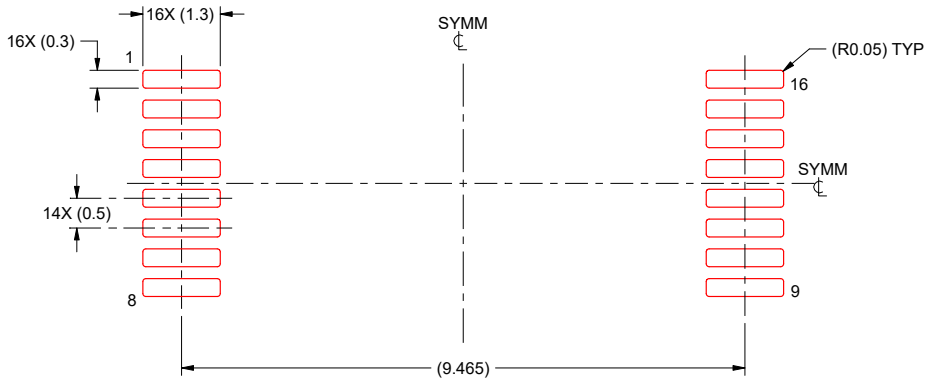
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DFP0016A — **SSOP - 2.65 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4230287/A 11/2023

NOTES: (continued)

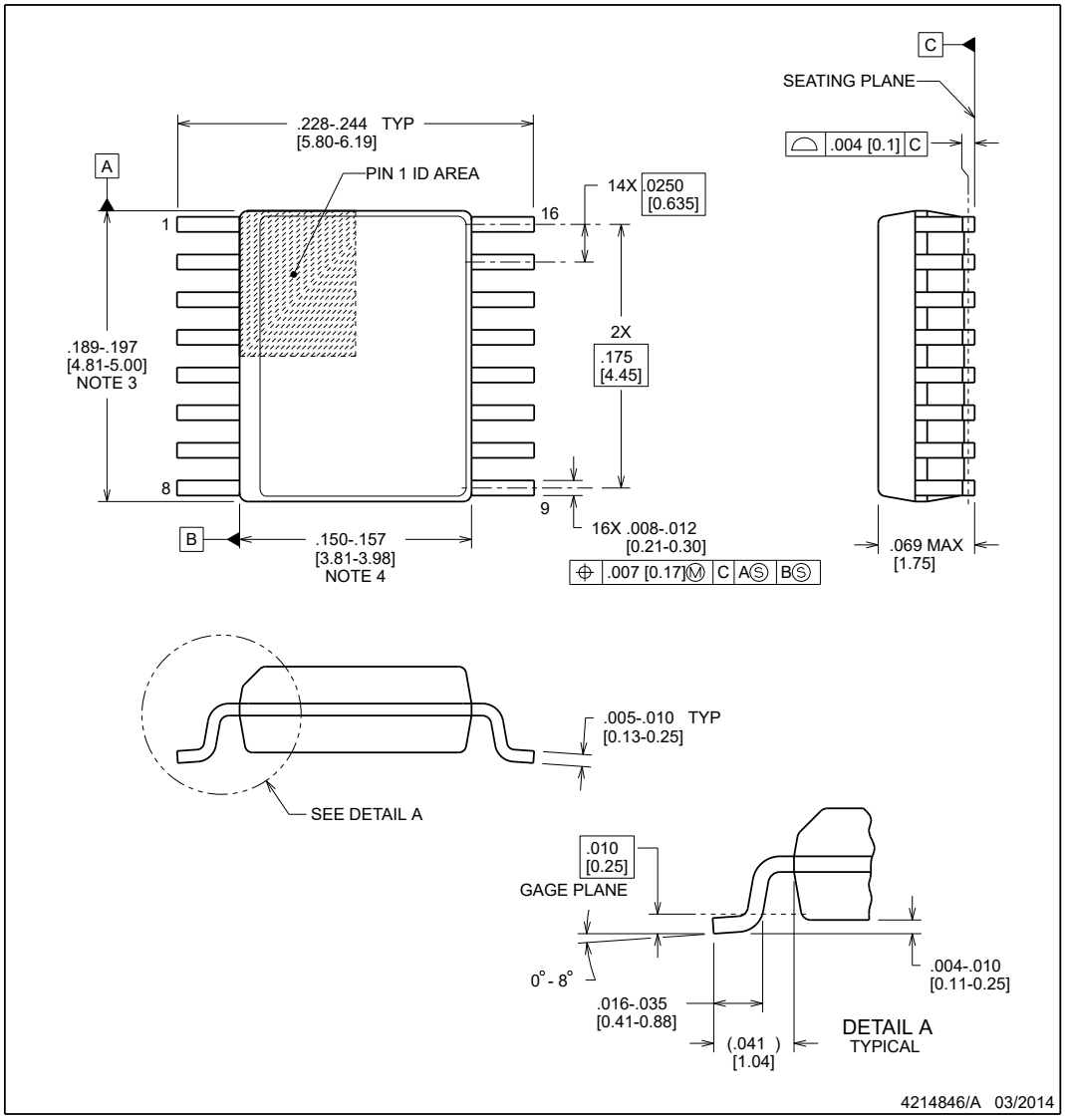
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



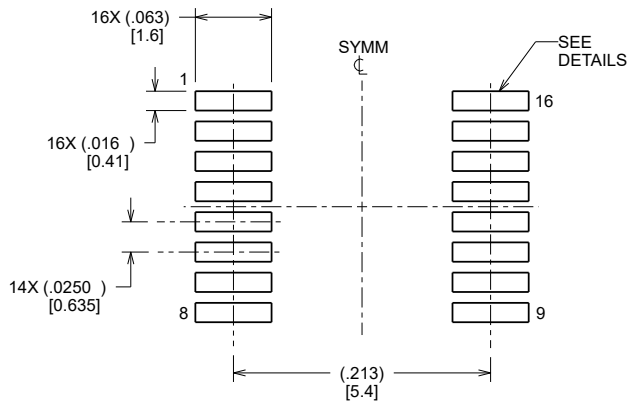
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

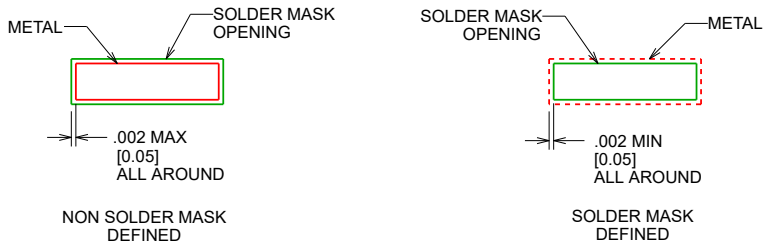
EXAMPLE BOARD LAYOUT

DBQ0016A — **SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

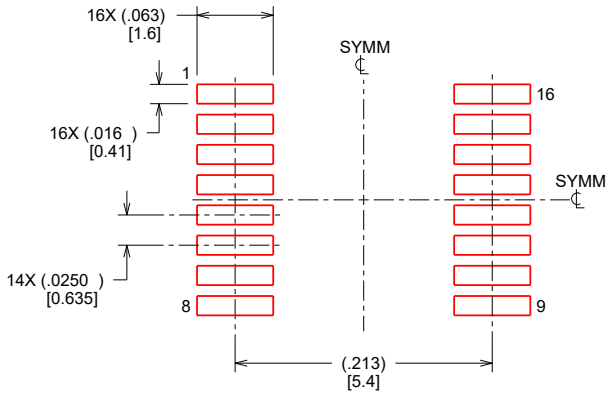
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A — **SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO6440DBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6440
ISO6440DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6440
ISO6440FDBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6440F
ISO6440FDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6440F
ISO6441DBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6441
ISO6441DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6441
ISO6441FDBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6441F
ISO6441FDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6441F
ISO6442DBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6442
ISO6442DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6442
ISO6442FDBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6442F
ISO6442FDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6442F
XISO6440DFPR	Active	Preproduction	SSOP (DFP) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XISO6440FDFPR	Active	Preproduction	SSOP (DFP) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XISO6441DFPR	Active	Preproduction	SSOP (DFP) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XISO6441FDFPR	Active	Preproduction	SSOP (DFP) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XISO6442DFPR	Active	Preproduction	null (null) |	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XISO6442FDFPR	Active	Preproduction	SSOP (DFP) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO6440, ISO6441, ISO6442 :

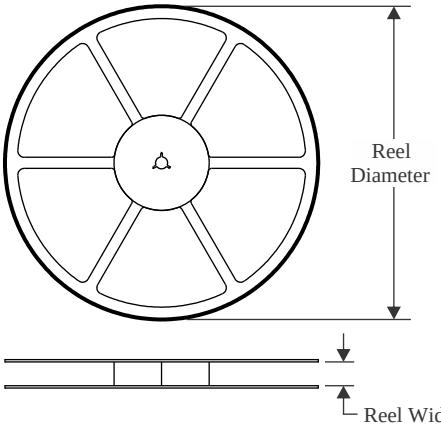
- Automotive : ISO6440-Q1, ISO6441-Q1, ISO6442-Q1

NOTE: Qualified Version Definitions:

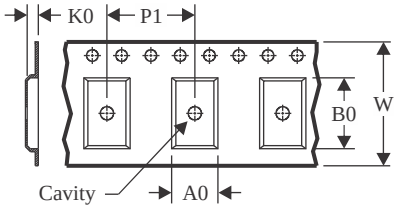
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

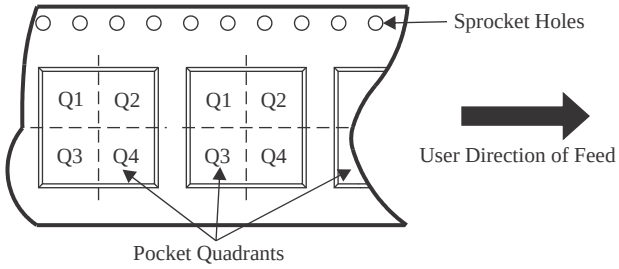


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

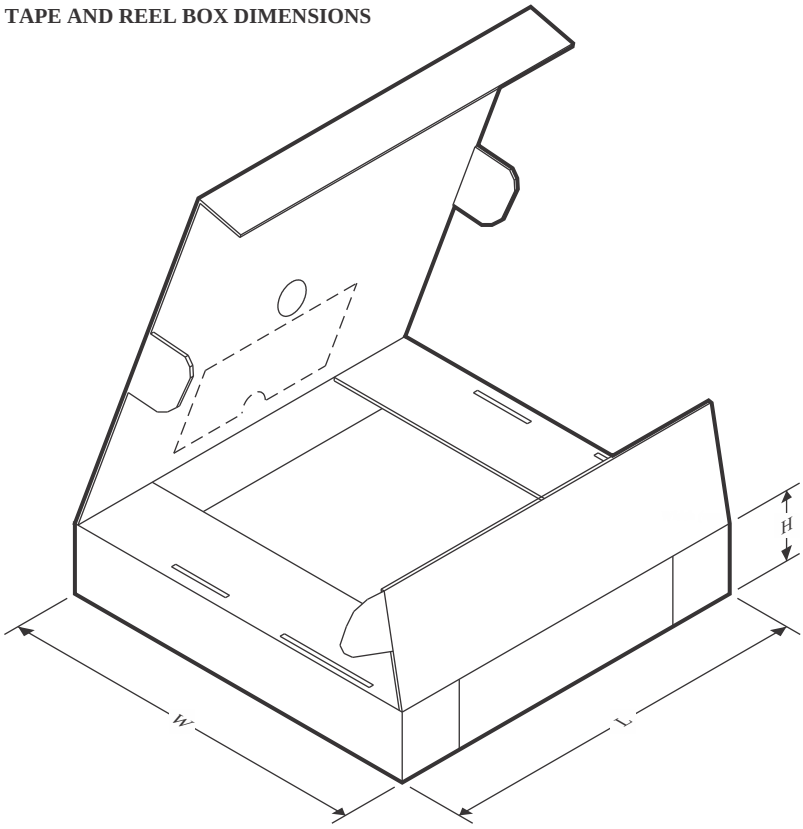
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO6440DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6440DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6440FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6440FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6441DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6441FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6442DBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6442DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6442FDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6442FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO6440DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO6440DWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6440FDBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO6440FDWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6441DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO6441FDBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO6442DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO6442DWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6442FDBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
ISO6442FDWR	SOIC	DW	16	2000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

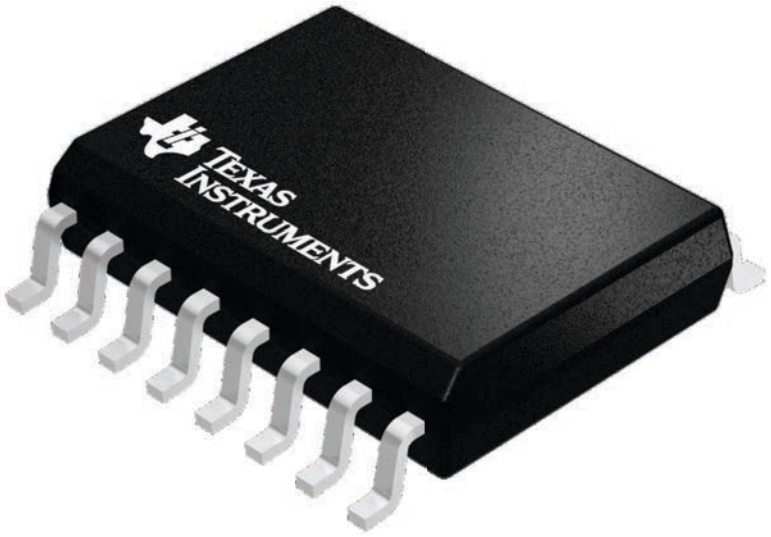
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

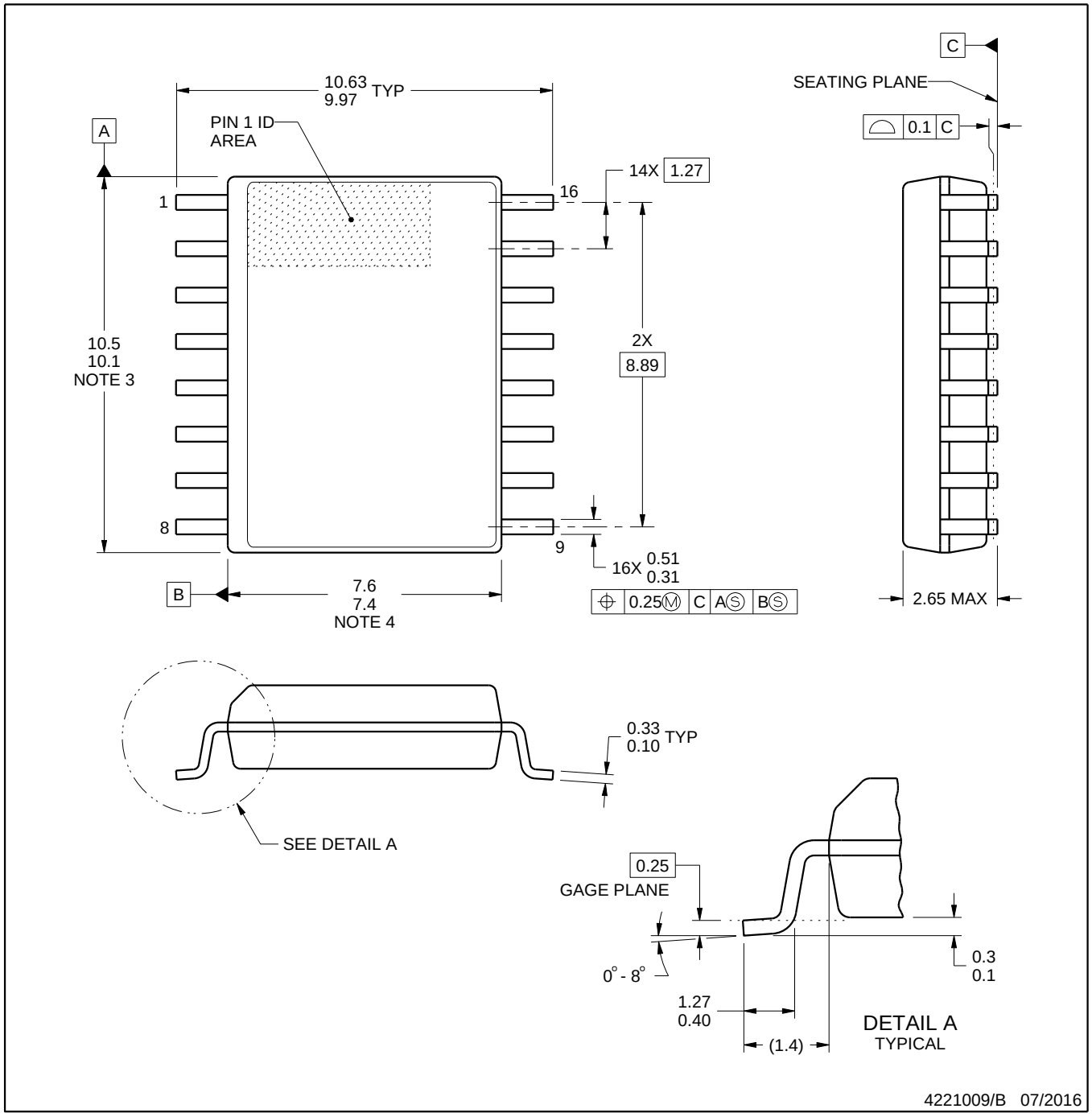
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



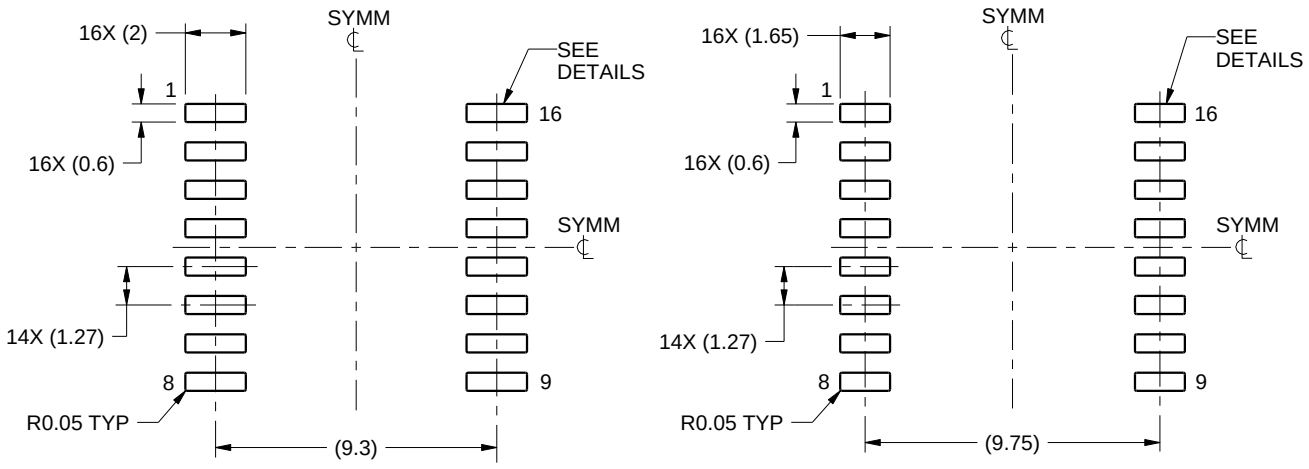
4224780/A

SOIC



NOTES:

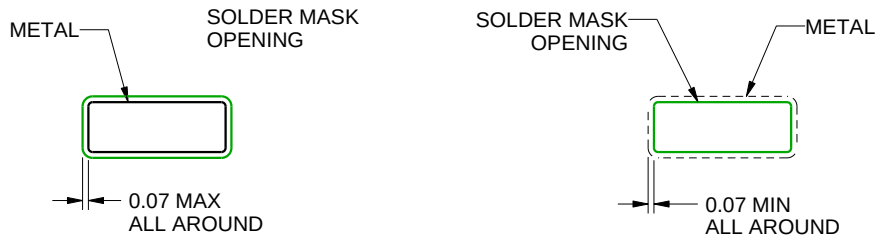
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

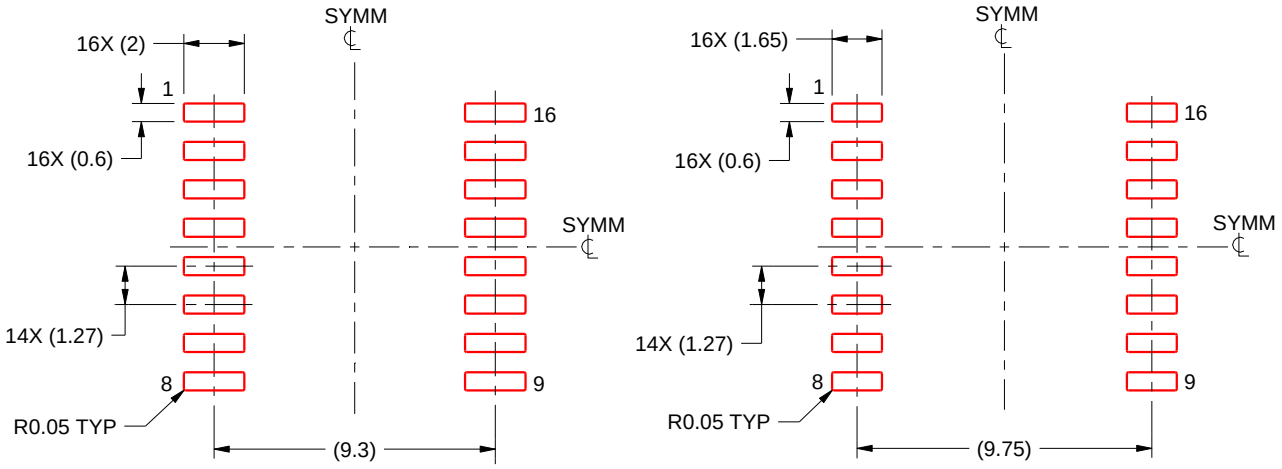
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

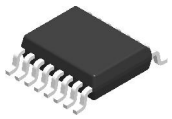
HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

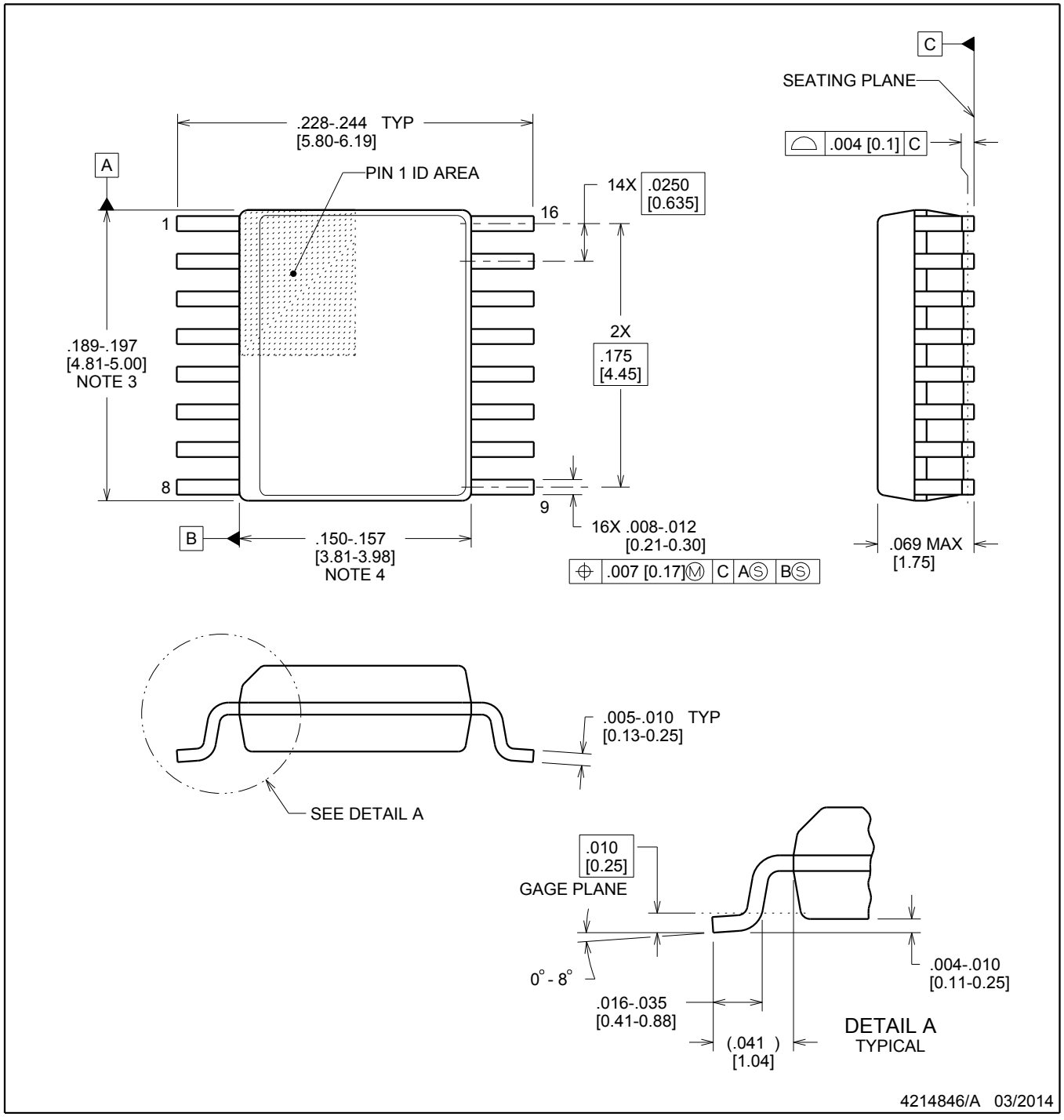


PACKAGE OUTLINE

DBQ0016A

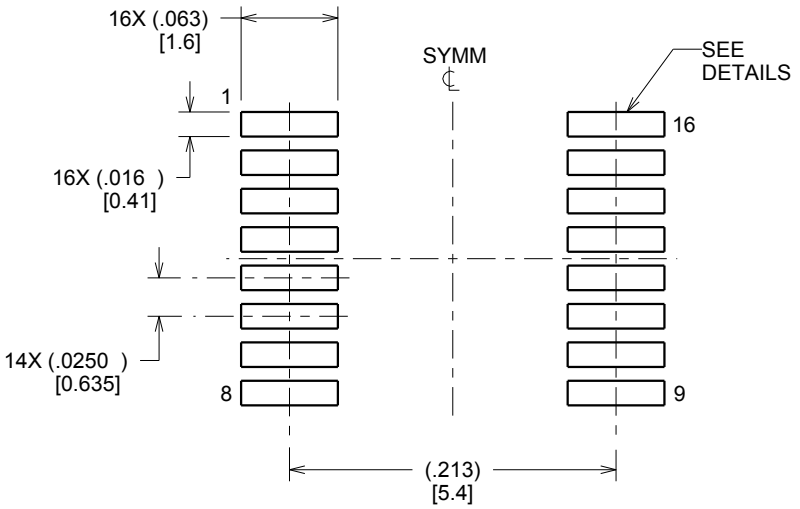
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

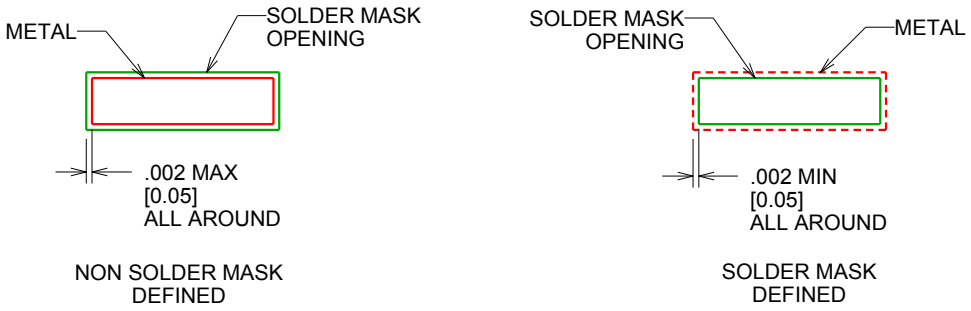


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

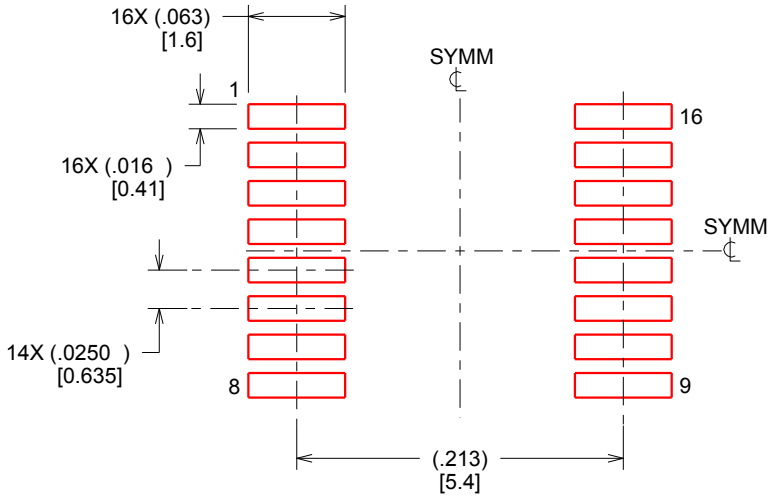
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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