

# ISO5852S-Q1 High-CMTI 2.5-A and 5-A Reinforced Isolated IGBT, MOSFET Gate Driver With Split Outputs and Active Protection Features

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM Classification Level 3A
  - Device CDM Classification Level C6
- 100-kV/ $\mu\text{s}$  Minimum Common-Mode Transient Immunity (CMTI) at  $V_{\text{CM}} = 1500$  V
- Split Outputs to Provide 2.5-A Peak Source and 5-A Peak Sink Currents
- Short Propagation Delay: 76 ns (Typ), 110 ns (Max)
- 2-A Active Miller Clamp
- Output Short-Circuit Clamp
- Soft Turn-Off (STO) during Short Circuit
- Fault Alarm upon Desaturation Detection is Signaled on **FLT** and Reset Through **RST**
- Input and Output Undervoltage Lockout (UVLO) with Ready (RDY) Pin Indication
- Active Output Pulldown and Default Low Outputs with Low Supply or Floating Inputs
- 2.25-V to 5.5-V Input Supply Voltage
- 15-V to 30-V Output Driver Supply Voltage
- CMOS Compatible Inputs
- Rejects Input Pulses and Noise Transients Shorter Than 20 ns
- Isolation Surge Withstand Voltage 12800-V<sub>PK</sub>
- Safety-Related Certifications:
  - 8000-V<sub>PK</sub>  $V_{\text{IOTM}}$  and 2121-V<sub>PK</sub>  $V_{\text{IORM}}$  Reinforced Isolation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - 5700-V<sub>RMS</sub> Isolation for 1 Minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 End Equipment Standards
  - TUV Certification per EN 61010-1 and EN 60950-1
  - GB4943.1-2011 CQC Certification
  - All Certifications Complete per UL, VDE, CQC, TUV and Planned for CSA

## 2 Applications

- Isolated IGBT and MOSFET Drives in:
  - HEV and EV Power Modules
  - Industrial Motor Control Drives
  - Industrial Power Supplies
  - Solar Inverters
  - Induction Heating

## 3 Description

The ISO5852S-Q1 device is a 5.7-kV<sub>RMS</sub>, reinforced isolated gate driver for IGBTs and MOSFETs with split outputs, **OUTH** and **OUTL**, providing 2.5-A source and 5-A sink current. The input side operates from a single 2.25-V to 5.5-V supply. The output side allows for a supply range from minimum 15 V to maximum 30 V. Two complementary CMOS inputs control the output state of the gate driver. The short propagation time of 76 ns provides accurate control of the output stage.

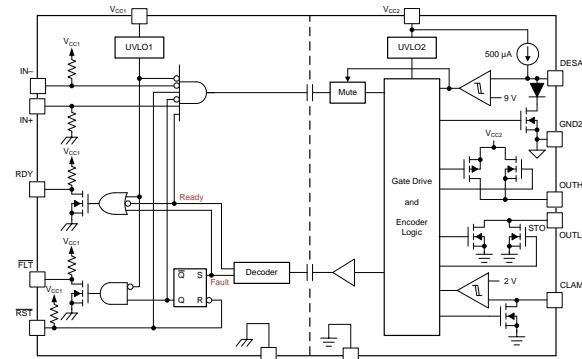
An internal desaturation (DESAT) fault detection recognizes when the IGBT is in an overcurrent condition. Upon a DESAT detect, a mute logic immediately blocks the output of the isolator and initiates a soft-turnoff procedure which disables the **OUTH** pin and pulls the **OUTL** pin to low over a time span of 2  $\mu\text{s}$ . When the **OUTL** pin reaches 2 V with respect to the most-negative supply potential,  $V_{\text{EE2}}$ , the gate-driver output is pulled hard to the  $V_{\text{EE2}}$  potential, turning the IGBT immediately off.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO5852S-Q1	SOIC (16)	10.30 mm $\times$ 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Functional Block Diagram



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2016) to Revision A	Page
• Changed the title of the data sheet from <i>Active Safety Features</i> to <i>Active Protection Features</i>	1
• Changed the <i>Electrostatic Discharge Caution</i>	32

## 5 Description (continued)

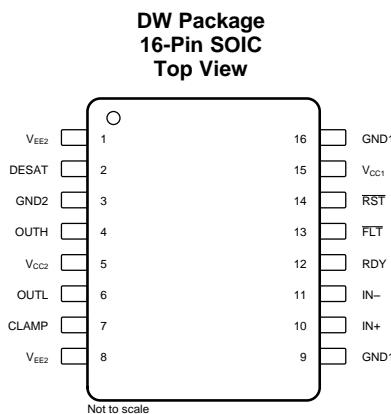
When desaturation is active, a fault signal is sent across the isolation barrier, pulling the **FLT** output at the input side low and blocking the isolator input. Mute logic is activated through the soft-turnoff period. The **FLT** output condition is latched and can be reset only after the **RDY** pin goes high, through a low-active pulse at the **RST** input.

When the IGBT is turned off during normal operation with a bipolar output supply, the output is hard clamp to  $V_{EE2}$ . If the output supply is unipolar, an active Miller clamp can be used, allowing Miller current to sink across a low-impedance path which prevents the IGBT from dynamic turnon during high-voltage transient conditions.

The readiness for the gate driver to be operated is under the control of two undervoltage-lockout circuits monitoring the input-side and output-side supplies. If either side has insufficient supply, the **RDY** output goes low, otherwise this output is high.

The ISO5852S-Q1 device is available in a 16-pin SOIC package. Device operation is specified over a temperature range from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ambient.

## 6 Pin Configuration and Function



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLAMP	7	O	Miller clamp output
DESAT	2	I	Desaturation voltage input
FLT	13	O	Fault output, active-low during DESAT condition
GND1	9	—	Input ground
	16		
GND2	3	—	Gate drive common. Connect to IGBT emitter.
IN+	10	I	Non-inverting gate drive voltage control input
IN-	11	I	Inverting gate drive voltage control input
OUTH	4	O	Positive gate drive voltage output
OUTL	6	O	Negative gate drive voltage output
RDY	12	O	Power-good output, active high when both supplies are good.
RST	14	I	Reset input, apply a low pulse to reset fault latch.
VCC1	15	—	Positive input supply (2.25-V to 5.5-V)
VCC2	5	—	Most positive output supply potential.
VEE2	1	—	Output negative supply. Connect to GND2 for unipolar supply application.
	8		

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC1}$	Supply-voltage input side		GND1 – 0.3	6	V
$V_{CC2}$	Positive supply-voltage output side	$(V_{CC2} - GND2)$	–0.3	35	V
$V_{EE2}$	Negative supply-voltage output side	$(V_{EE2} - GND2)$	–17.5	0.3	V
$V_{(SUP2)}$	Total-supply output voltage	$(V_{CC2} - V_{EE2})$	–0.3	35	V
$V_{(OUTH)}$	Positive gate-driver output voltage		$V_{EE2} - 0.3$	$V_{CC2} + 0.3$	V
$V_{(OUTL)}$	Negative gate-driver output voltage		$V_{EE2} - 0.3$	$V_{CC2} + 0.3$	V
$I_{(OUTH)}$	Gate-driver high output current	Maximum pulse width = 10 $\mu$ s, Maximum duty cycle = 0.2%		2.7	A
$I_{(OUTL)}$	Gate-driver low output current	Maximum pulse width = 10 $\mu$ s, Maximum duty cycle = 0.2%		5.5	A
$V_{(LIP)}$	Voltage at IN+, IN–, $\overline{FLT}$ , RDY, $\overline{RST}$		GND1 – 0.3	$V_{CC1} + 0.3$	V
$I_{(LOP)}$	Output current of $\overline{FLT}$ , RDY			10	mA
$V_{(DESAT)}$	Voltage at DESAT		GND2 – 0.3	$V_{CC2} + 0.3$	V
$V_{(CLAMP)}$	Clamp voltage		$V_{EE2} - 0.3$	$V_{CC2} + 0.3$	V
$T_J$	Junction temperature		–40	150	°C
$T_{STG}$	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	V
		Charged-device model (CDM), per AEC Q100-011	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC1}$	Supply-voltage input side		2.25	5.5	V
$V_{CC2}$	Positive supply-voltage output side ( $V_{CC2} - GND2$ )		15	30	V
$V_{(EE2)}$	Negative supply-voltage output side ( $V_{EE2} - GND2$ )		–15	0	V
$V_{(SUP2)}$	Total supply-voltage output side ( $V_{CC2} - V_{EE2}$ )		15	30	V
$V_{(IH)}$	High-level input voltage (IN+, IN–, $\overline{RST}$ )	$0.7 \times V_{CC1}$		$V_{CC1}$	V
$V_{(IL)}$	Low-level input voltage (IN+, IN–, $\overline{RST}$ )	0	$0.3 \times V_{CC1}$		V
$t_{UI}$	Pulse width at IN+, IN– for full output ( $C_{LOAD} = 1$ nF)		40		ns
$t_{RST}$	Pulse width at $\overline{RST}$ for resetting fault latch		800		ns
$T_A$	Ambient temperature		–40	125	°C

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ISO5852S-Q1	UNIT
		DW (SOIC)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	99.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	48.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	56.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	29.2	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	56.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).

## 7.5 Power Ratings

Full-chip power dissipation is derated 10.04 mW/°C beyond 25°C ambient temperature. At 125°C ambient temperature, a maximum of 251 mW total power dissipation is allowed. Power dissipation can be optimized depending on ambient temperature and board design, while ensuring that the junction temperature does not exceed 150°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>D</sub>	V <sub>CC1</sub> = 5.5 V, V <sub>CC2</sub> = 30 V, T <sub>A</sub> = 25°C			1255	mW
P <sub>ID</sub>	V <sub>CC1</sub> = 5.5 V, V <sub>CC2</sub> = 30 V, T <sub>A</sub> = 25°C			175	mW
P <sub>OD</sub>	V <sub>CC1</sub> = 5.5 V, V <sub>CC2</sub> = 30 V, T <sub>A</sub> = 25°C			1080	mW

## 7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT	
<b>GENERAL</b>					
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	8	mm	
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	8	mm	
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	μm	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; Material Group I according to IEC 60664-1; UL 746A	>600	V	
	Material group		I		
Overvoltage Category		Rated mains voltage $\leq$ 600 V <sub>RMS</sub>	I-IV		
		Rated mains voltage $\leq$ 1000 V <sub>RMS</sub>	I-III		
<b>DIN V VDE V 0884-10 (VDE V 0884-10):2006-12<sup>(2)</sup></b>					
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V <sub>PK</sub>	
V <sub>IOWM</sub>	Maximum isolation working voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test, see <a href="#">Figure 1</a>	1500	V <sub>RMS</sub>	
		DC voltage	2121	V <sub>DC</sub>	
V <sub>IOTM</sub>	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ ; t = 60 s (qualification); t = 1 s (100% production)	8000	V <sub>PK</sub>	
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 60065, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800$ V <sub>PK</sub> (qualification)	8000		
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60$ s; $V_{pd(m)} = 1.2 \times V_{IORM} = 2545$ V <sub>PK</sub> , $t_m = 10$ s	≤5	pC	
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60$ s; $V_{pd(m)} = 1.6 \times V_{IORM} = 3394$ V <sub>PK</sub> , $t_m = 10$ s	≤5		
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$ , $t_{ini} = 60$ s; $V_{pd(m)} = 1.875 \times V_{IORM} = 3977$ V <sub>PK</sub> , $t_m = 10$ s	≤5		
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	$V_{IO} = 0.4 \sin(2\pi ft)$ , f = 1 MHz	1	pF	
R <sub>IO</sub>	Isolation resistance, input to output <sup>(5)</sup>	$V_{IO} = 500$ V, $T_A = 25^\circ\text{C}$	$> 10^{12}$	Ω	
		$V_{IO} = 500$ V, $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	$> 10^{11}$		
		$V_{IO} = 500$ V at $T_S = 150^\circ\text{C}$	$> 10^9$		
Pollution degree			2		
<b>UL 1577</b>					
V <sub>ISO</sub>	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5700$ V <sub>RMS</sub> , t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 6840$ V <sub>RMS</sub> , t = 1 s (100% production)	5700	VRMS	

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device

## 7.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Plan to certify under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Reinforced Insulation Maximum Transient isolation voltage, 8000 $V_{PK}$ ; Maximum surge isolation voltage, 8000 $V_{PK}$ ; Maximum repetitive peak isolation voltage, 2121 $V_{PK}$	Isolation Rating of 5700 $V_{RMS}$ ; Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 (2nd Ed.), 800 $V_{RMS}$ max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 $V_{RMS}$ (354 $V_{PK}$ ) max working voltage	Single Protection, 5700 $V_{RMS}$ <sup>(1)</sup>	Reinforced Insulation, Altitude $\leq$ 5000m, Tropical climate, 400 $V_{RMS}$ maximum working voltage	5700 $V_{RMS}$ Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 $V_{RMS}$ 5700 $V_{RMS}$ Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 $V_{RMS}$
Certification completed Certificate number: 40040142	Certificate planned	Certification completed File number: E181974	Certification completed Certificate number: CQC16001141761	Certification completed Client ID number: 77311

(1) Production tested  $\geq$  6840 VRMS for 1 second in accordance with UL 1577.

## 7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_S$ Safety input, output, or supply current	$R_{0JA} = 99.6^\circ\text{C}/\text{W}$ , $V_I = 2.75 \text{ V}$ , $T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$ , see <a href="#">Figure 2</a>			456	mA
	$R_{0JA} = 99.6^\circ\text{C}/\text{W}$ , $V_I = 3.6 \text{ V}$ , $T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$ , see <a href="#">Figure 2</a>			346	
	$R_{0JA} = 99.6^\circ\text{C}/\text{W}$ , $V_I = 5.5 \text{ V}$ , $T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$ , see <a href="#">Figure 2</a>			228	
	$R_{0JA} = 99.6^\circ\text{C}/\text{W}$ , $V_I = 15 \text{ V}$ , $T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$ , see <a href="#">Figure 2</a>			84	
	$R_{0JA} = 99.6^\circ\text{C}/\text{W}$ , $V_I = 30 \text{ V}$ , $T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$ , see <a href="#">Figure 2</a>			42	
$P_S$ Safety input, output, or total power	$R_{0JA} = 99.6^\circ\text{C}/\text{W}$ , $T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$ , see <a href="#">Figure 3</a>			255 <sup>(1)</sup>	mW
$T_S$ Maximum ambient safety temperature				150	°C

(1) Input, output, or the sum of input and output power should not exceed this value

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

## 7.9 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} = 5\text{ V}$ ,  $V_{CC2} - GND2 = 15\text{ V}$ ,  $GND2 - V_{EE2} = 8\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>VOLTAGE SUPPLY</b>						
$V_{IT+(UVLO1)}$	Positive-going UVLO1 threshold-voltage input side ( $V_{CC1} - GND1$ )			2.25	V	
$V_{IT-(UVLO1)}$	Negative-going UVLO1 threshold-voltage input side ( $V_{CC1} - GND1$ )		1.7		V	
$V_{HYS(UVLO1)}$	UVLO1 Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) input side		0.2		V	
$V_{IT+(UVLO2)}$	Positive-going UVLO2 threshold-voltage output side ( $V_{CC2} - GND2$ )		12	13	V	
$V_{IT-(UVLO2)}$	Negative-going UVLO2 threshold-voltage output side ( $V_{CC2} - GND2$ )	9.5	11		V	
$V_{HYS(UVLO2)}$	UVLO2 hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) output side		1		V	
$I_{Q1}$	Input-supply quiescent current		2.8	4.5	mA	
$I_{Q2}$	Output-supply quiescent current		3.6	6	mA	
<b>LOGIC I/O</b>						
$V_{IT+(IN,RST)}$	Positive-going input-threshold voltage ( $IN+, IN-, RST$ )			$0.7 \times V_{CC1}$	V	
$V_{IT-(IN,RST)}$	Negative-going input-threshold voltage ( $IN+, IN-, RST$ )		0.3 $\times V_{CC1}$		V	
$V_{HYS(IN,RST)}$	Input hysteresis voltage ( $IN+, IN-, RST$ )		0.15 $\times V_{CC1}$		V	
$I_{IH}$	High-level input leakage at ( $IN+$ ) <sup>(1)</sup>	$IN+ = V_{CC1}$		100	$\mu\text{A}$	
$I_{IL}$	Low-level input leakage at ( $IN-, \overline{RST}$ ) <sup>(2)</sup>	$IN- = GND1$ , $\overline{RST} = GND1$		-100	$\mu\text{A}$	
$I_{PU}$	Pullup current of $\overline{FLT}$ , RDY	$V_{(RDY)} = GND1$ , $V_{(FLT)} = GND1$		100	$\mu\text{A}$	
$V_{(OL)}$	Low-level output voltage at $\overline{FLT}$ , RDY	$I_{(FLT)} = 5\text{ mA}$		0.2	V	
<b>GATE DRIVER STAGE</b>						
$V_{(OUTPD)}$	Active output pulldown voltage	$I_{(OUTH/L)} = 200\text{ mA}$ , $V_{CC2} = \text{open}$		2	V	
$V_{OUTH}$	High-level output voltage	$I_{(OUTH)} = -20\text{ mA}$	$V_{CC2} - 0.5$	$V_{CC2} - 0.24$	V	
$V_{OUTL}$	Low-level output voltage	$I_{(OUTL)} = 20\text{ mA}$		$V_{EE2} + 13$	$V_{EE2} + 50$ mV	
$I_{(OUTH)}$	High-level output peak current	$IN+ = \text{high}$ , $IN- = \text{low}$ , $V_{(OUTH)} = V_{CC2} - 15\text{ V}$	1.5	2.5	A	
$I_{(OUTL)}$	Low-level output peak current	$IN+ = \text{low}$ , $IN- = \text{high}$ , $V_{(OUTL)} = V_{EE2} + 15\text{ V}$	3.4	5	A	
$I_{(OLF)}$	Low-level output current during fault condition			130	mA	
<b>ACTIVE MILLER CLAMP</b>						
$V_{(CLP)}$	Low-level clamp voltage	$I_{(CLP)} = 20\text{ mA}$		$V_{EE2} + 0.015$	$V_{EE2} + 0.08$	V
$I_{(CLP)}$	Low-level clamp current	$V_{(CLAMP)} = V_{EE2} + 2.5\text{ V}$	1.6	2.5	3.3	A
$V_{(CLTH)}$	Clamp threshold voltage		1.6	2.1	2.5	V
<b>SHORT CIRCUIT CLAMPING</b>						
$V_{(CLP-OUTH)}$	Clamping voltage ( $V_{(OUTH)} - V_{CC2}$ )	$IN+ = \text{high}$ , $IN- = \text{low}$ , $t_{CLP} = 10\text{ }\mu\text{s}$ , $I_{(OUTH)} = 500\text{ mA}$		1.1	1.3	V
$V_{(CLP-OUTL)}$	Clamping voltage ( $V_{(OUTL)} - V_{CC2}$ )	$IN+ = \text{high}$ , $IN- = \text{low}$ , $t_{CLP} = 10\text{ }\mu\text{s}$ , $I_{(OUTL)} = 500\text{ mA}$		1.3	1.5	V
$V_{(CLP-CLP)}$	Clamping voltage ( $V_{CLP} - V_{CC2}$ )	$IN+ = \text{high}$ , $IN- = \text{low}$ , $t_{CLP} = 10\text{ }\mu\text{s}$ , $I_{(CLP)} = 500\text{ mA}$		1.3		V
$V_{(CLP-CLAMP)}$	Clamping voltage at CLAMP	$IN+ = \text{High}$ , $IN- = \text{Low}$ , $I_{(CLP)} = 20\text{ mA}$		0.7	1.1	V
$V_{(CLP-OUTL)}$	Clamping voltage at OUTL ( $V_{CLP} - V_{CC2}$ )	$IN+ = \text{High}$ , $IN- = \text{Low}$ , $I_{(OUTL)} = 20\text{ mA}$		0.7	1.1	V
<b>DESAT PROTECTION</b>						
$I_{(CHG)}$	Blanking-capacitor charge current	$V_{(DESAT)} - GND2 = 2\text{ V}$	0.42	0.5	0.58	mA
$I_{(DCHG)}$	Blanking-capacitor discharge current	$V_{(DESAT)} - GND2 = 6\text{ V}$	9	14		mA

(1)  $I_{IH}$  for  $IN-, \overline{RST}$  pin is zero as they are pulled high internally

(2)  $I_{IL}$  for  $IN+$  is zero, as it is pulled low internally

## Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} = 5\text{ V}$ ,  $V_{CC2} - GND2 = 15\text{ V}$ ,  $GND2 - V_{EE2} = 8\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DSTH)}$	DESAT threshold voltage with respect to GND2	8.3	9	9.5	V
$V_{(DSL)}$	DESAT voltage with respect to GND2, when OUTH or OUTL is driven low	0.4		1	V

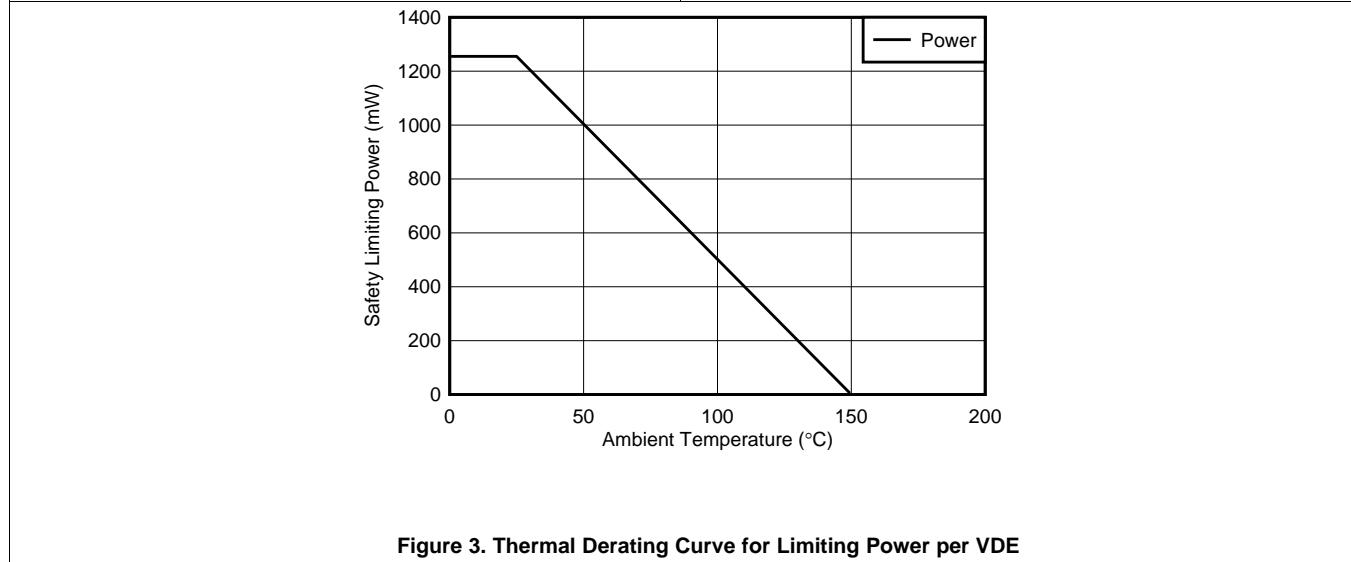
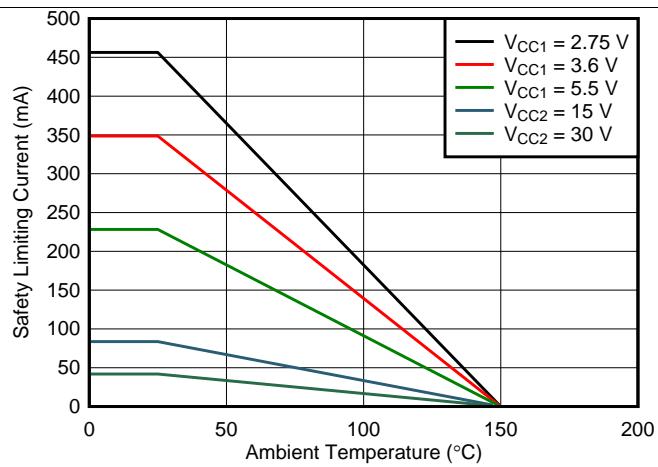
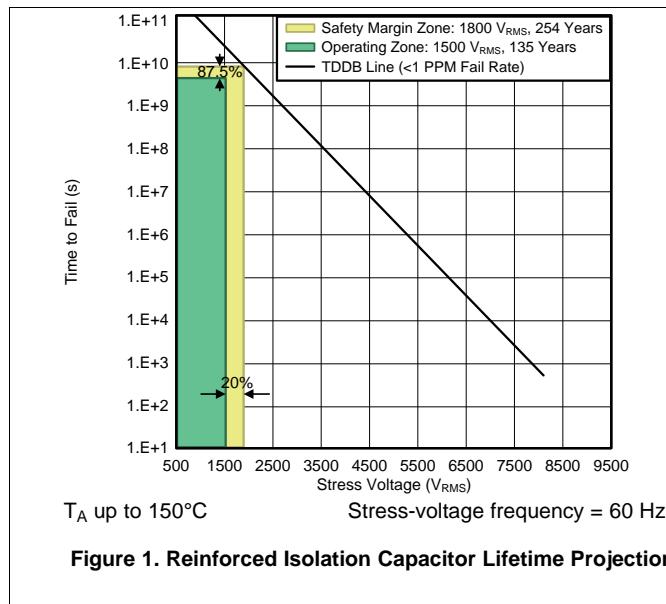
## 7.10 Switching Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC1} = 5\text{ V}$ ,  $V_{CC2} - GND2 = 15\text{ V}$ ,  $GND2 - V_{EE2} = 8\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	$C_{LOAD} = 1\text{ nF}$	See Figure 44, Figure 45, and Figure 46	12	18	35
$t_f$	$C_{LOAD} = 1\text{ nF}$		12	20	37
$t_{PLH}, t_{PHL}$	$C_{LOAD} = 1\text{ nF}$		76	110	ns
$t_{sk-p}$	$C_{LOAD} = 1\text{ nF}$		20		ns
$t_{sk-pp}$	$C_{LOAD} = 1\text{ nF}$		30 <sup>(1)</sup>		ns
$t_{GF}(\text{IN}, \text{RST})$	$C_{LOAD} = 1\text{ nF}$		20	30	40
$t_{DS}(90\%)$	DESAT sense to 90% $V_{OUTH/L}$ delay		553	760	ns
$t_{DS}(10\%)$	DESAT sense to 10% $V_{OUTH/L}$ delay		2	3.5	$\mu\text{s}$
$t_{DS}(\text{GF})$	DESAT-glitch filter delay		330		ns
$t_{DS}(\text{FLT})$	DESAT sense to $\overline{\text{FLT}}$ -low delay			1.4	$\mu\text{s}$
$t_{LEB}$	Leading-edge blanking time	See Figure 44 and Figure 45	310	400	480
$t_{GF(RSTFLT)}$	Glitch filter on $\overline{\text{RST}}$ for resetting $\overline{\text{FLT}}$		300	800	ns
$C_I$	Input capacitance <sup>(2)</sup>	$V_I = V_{CC1} / 2 + 0.4 \times \sin(2\pi ft)$ , $f = 1\text{ MHz}$ , $V_{CC1} = 5\text{ V}$	2		pF
CMTI	Common-mode transient immunity	$V_{CM} = 1500\text{ V}$ , see Figure 47	100	120	$\text{kV}/\mu\text{s}$

(1) Measured at same supply voltage and temperature condition  
(2) Measured from input pin to ground.

## 7.11 Insulation Characteristics Curves



## 7.12 Typical Characteristics

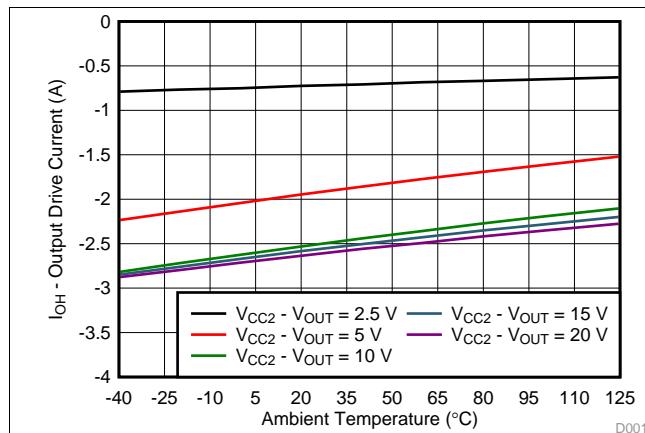


Figure 4. Output High Drive Current vs Temperature

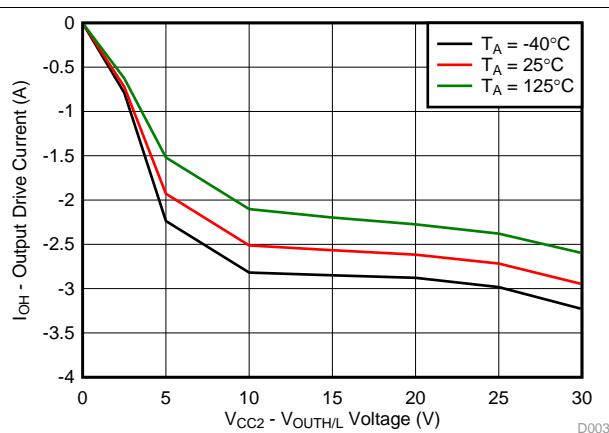


Figure 5. Output High Drive Current vs Output Voltage

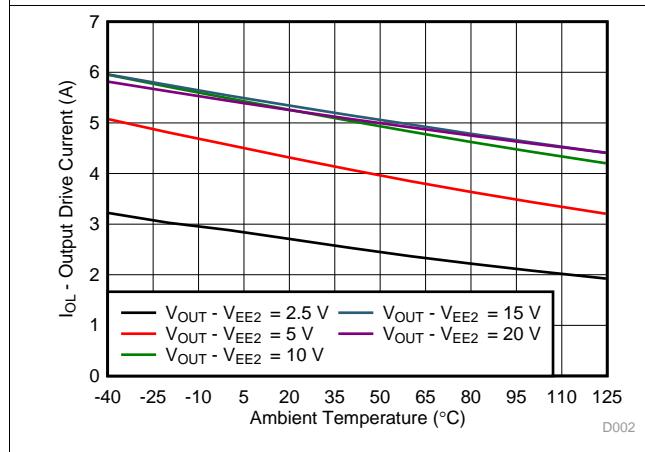


Figure 6. Output Low Drive Current vs Temperature

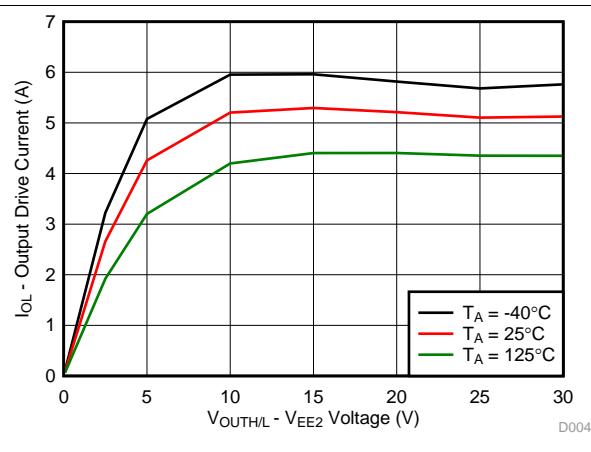


Figure 7. Output Low Drive Current vs Output Voltage

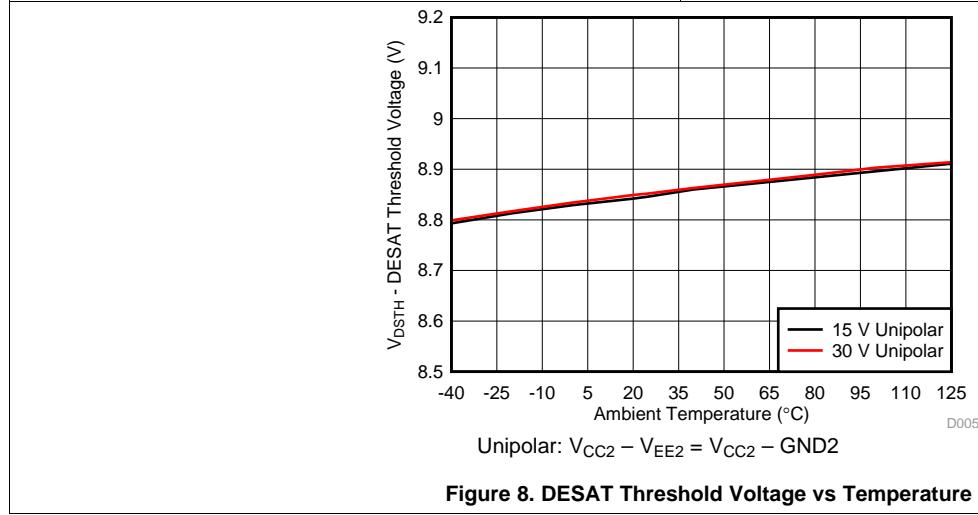
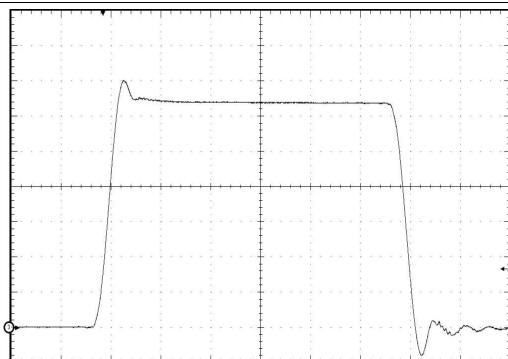


Figure 8. DESAT Threshold Voltage vs Temperature

**Typical Characteristics (continued)**

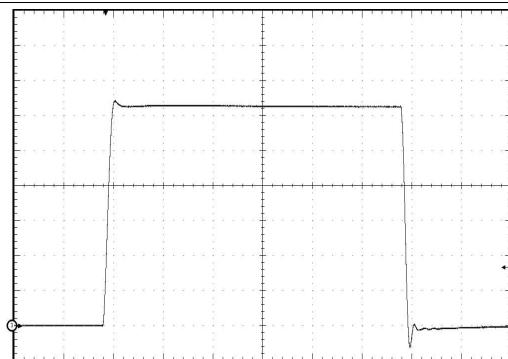
CH 3: 3 V/Div



$C_L = 1 \text{ nF}$        $R_{GH} = 0 \Omega$        $R_{GL} = 0 \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - GND2 = 20 \text{ V}$

**Figure 9. Output Transient Waveform**

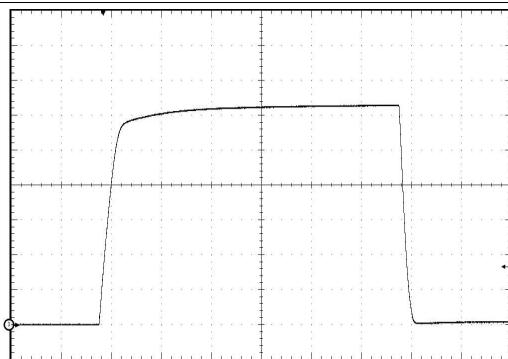
CH 3: 3 V/Div



$C_L = 10 \text{ nF}$        $R_{GH} = 0 \Omega$        $R_{GL} = 0 \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - GND2 = 20 \text{ V}$

**Figure 10. Output Transient Waveform**

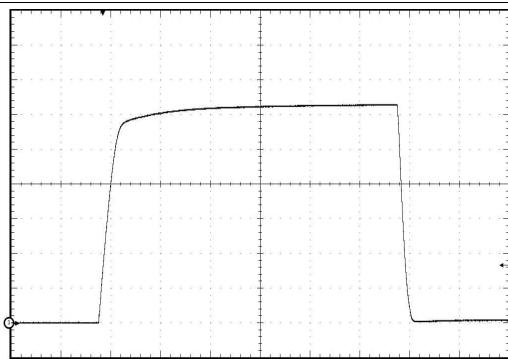
CH 3: 3 V/Div



$C_L = 100 \text{ nF}$        $R_{GH} = 0 \Omega$        $R_{GL} = 0 \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - GND2 = 20 \text{ V}$

**Figure 11. Output Transient Waveform**

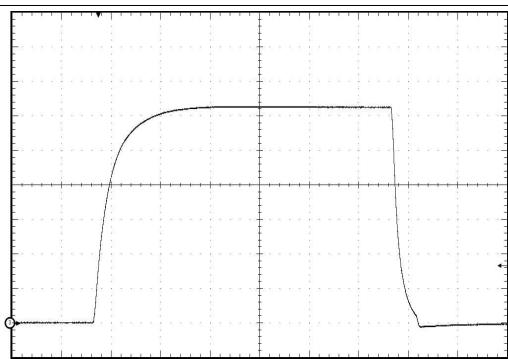
CH 3: 3 V/Div



$C_L = 1 \text{ nF}$        $R_{GH} = 10 \Omega$        $R_{GL} = 5 \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - GND2 = 20 \text{ V}$

**Figure 12. Output Transient Waveform**

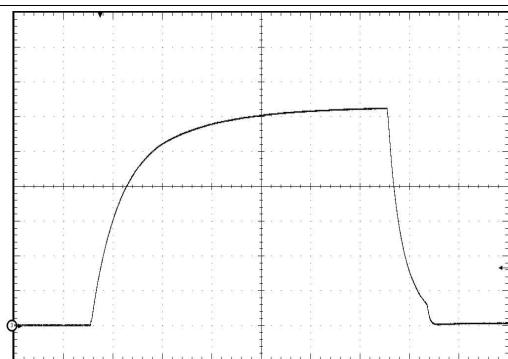
CH 3: 3 V/Div



$C_L = 10 \text{ nF}$        $R_{GH} = 10 \Omega$        $R_{GL} = 5 \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - GND2 = 20 \text{ V}$

**Figure 13. Output Transient Waveform**

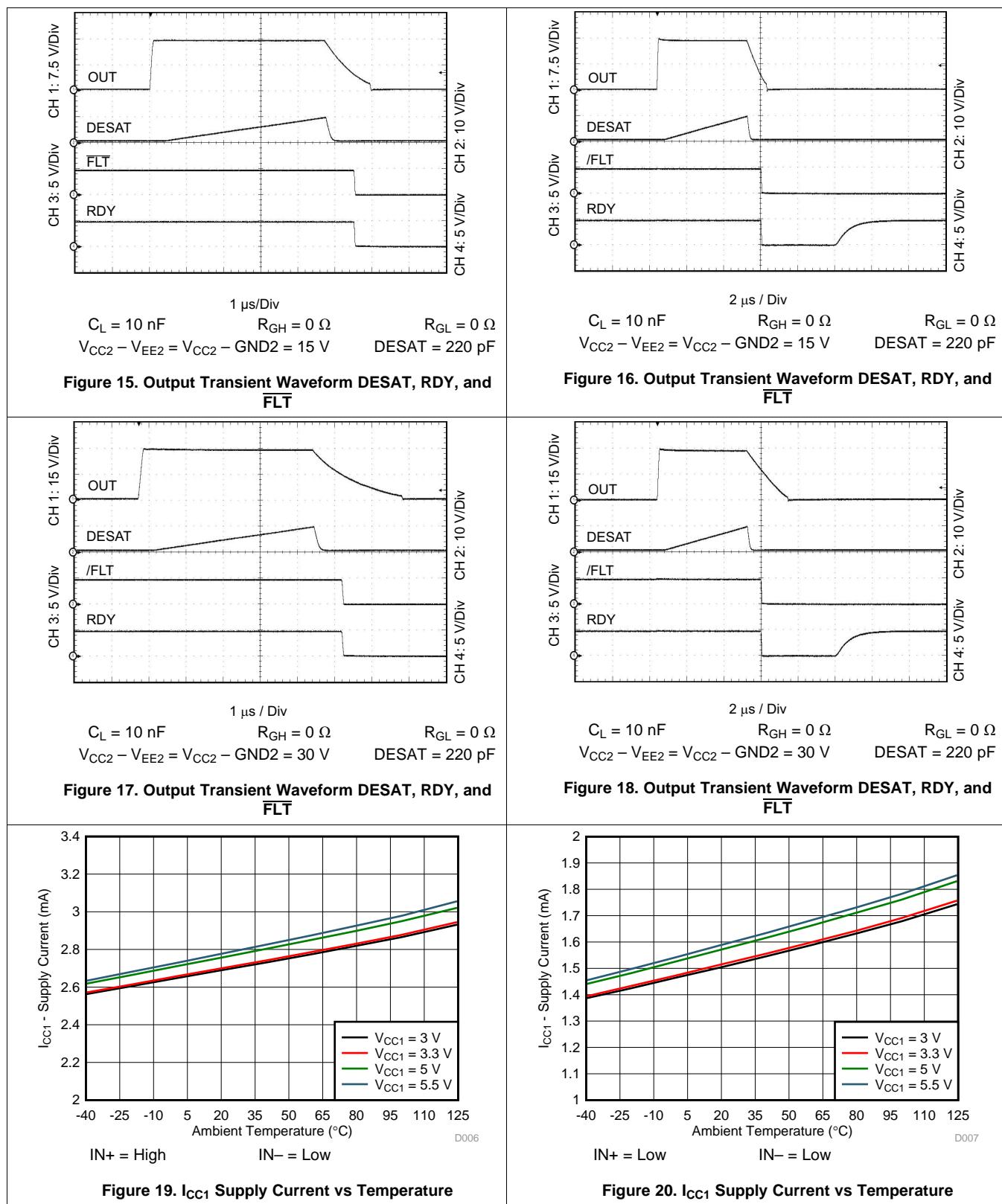
CH 3: 3 V/Div



$C_L = 100 \text{ nF}$        $R_{GH} = 10 \Omega$        $R_{GL} = 5 \Omega$   
 $V_{CC2} - V_{EE2} = V_{CC2} - GND2 = 20 \text{ V}$

**Figure 14. Output Transient Waveform**

## Typical Characteristics (continued)



## Typical Characteristics (continued)

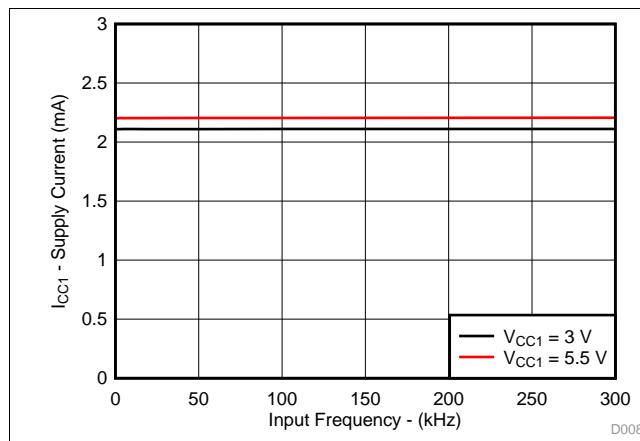
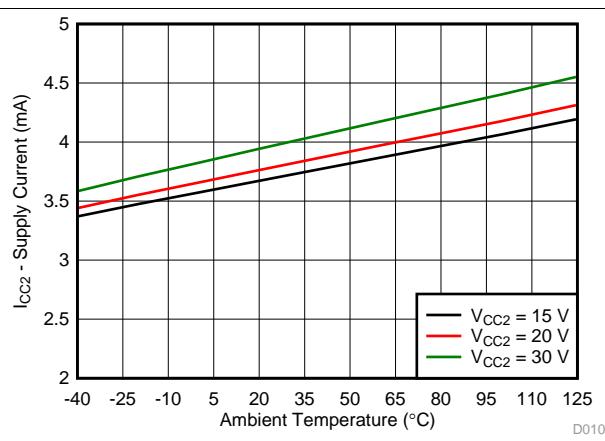
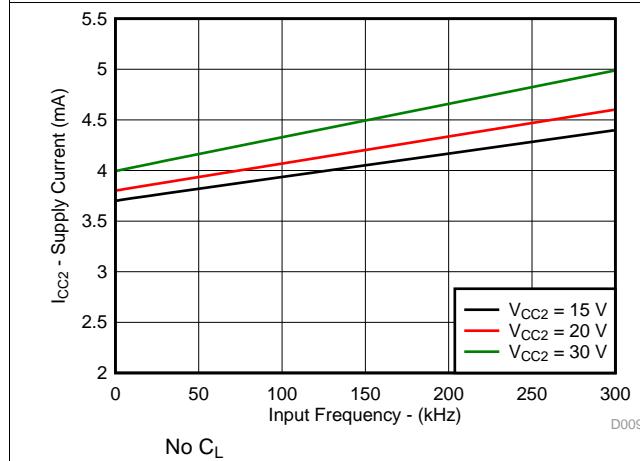
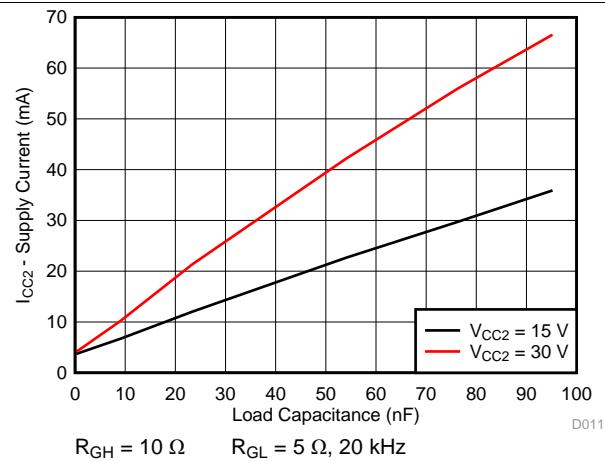
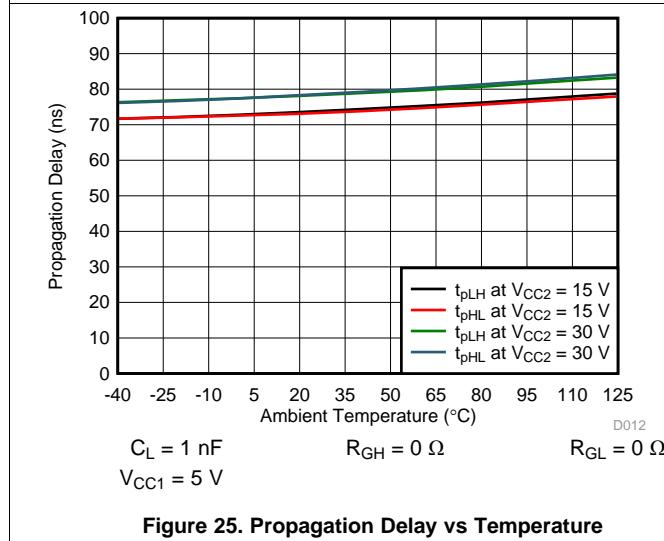
Figure 21.  $I_{CC1}$  Supply Current vs Input FrequencyFigure 22.  $I_{CC2}$  Supply Current vs TemperatureFigure 23.  $I_{CC2}$  Supply Current vs Input FrequencyFigure 24.  $I_{CC2}$  Supply Current vs Load Capacitance

Figure 25. Propagation Delay vs Temperature

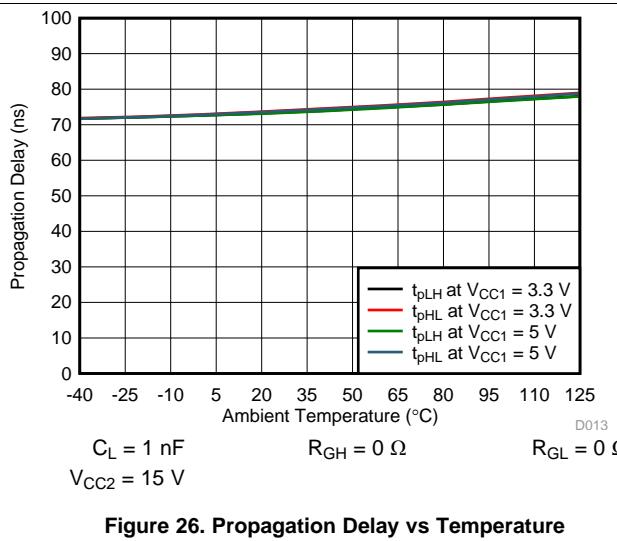
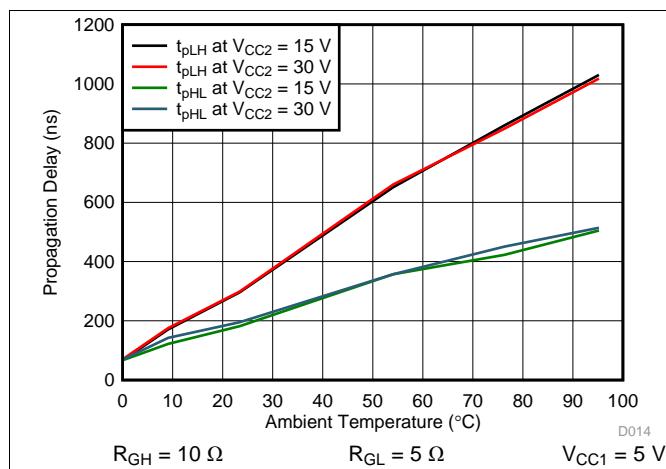
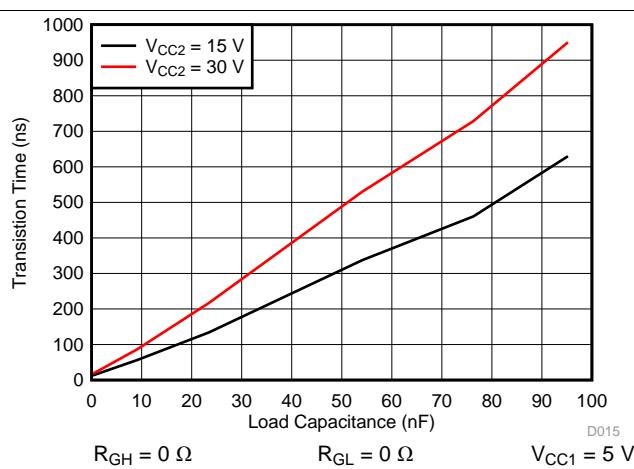


Figure 26. Propagation Delay vs Temperature

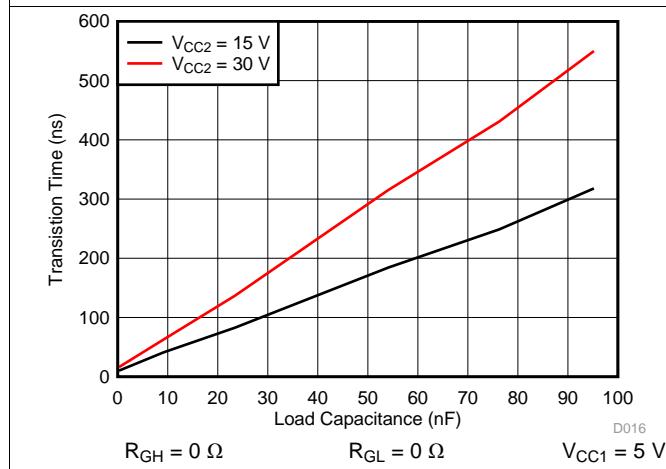
## Typical Characteristics (continued)



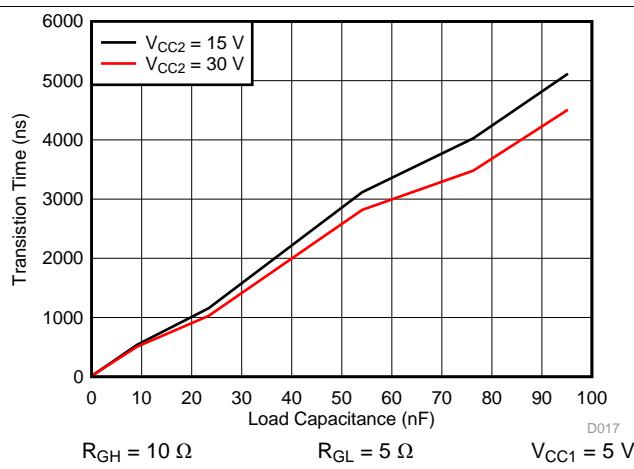
**Figure 27. Propagation Delay vs Load Capacitance**



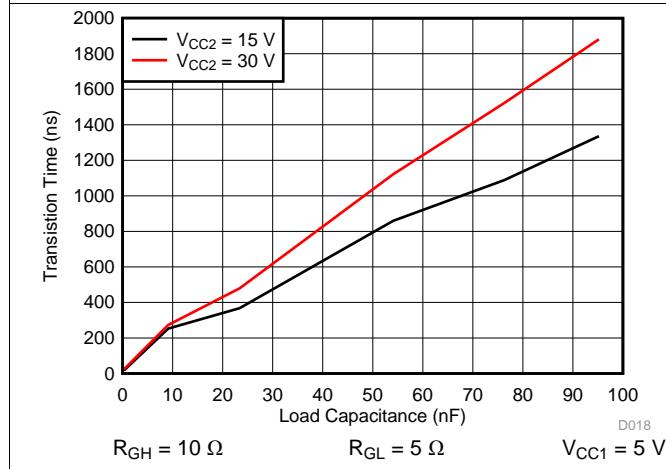
**Figure 28.  $t_r$  Rise Time vs Load Capacitance**



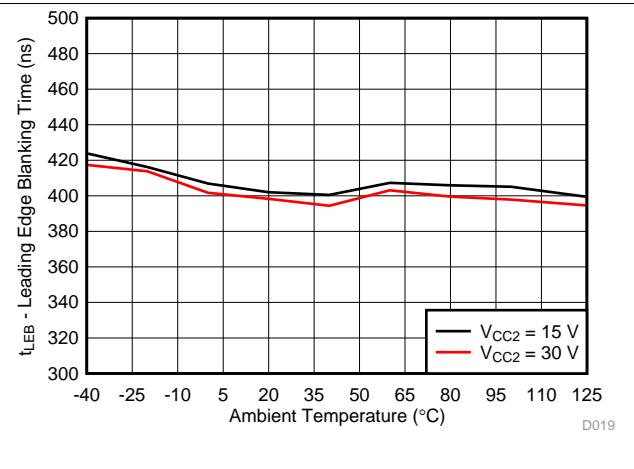
**Figure 29.  $t_f$  Fall Time v. Load Capacitance**



**Figure 30.  $t_r$  Rise Time vs Load Capacitance**

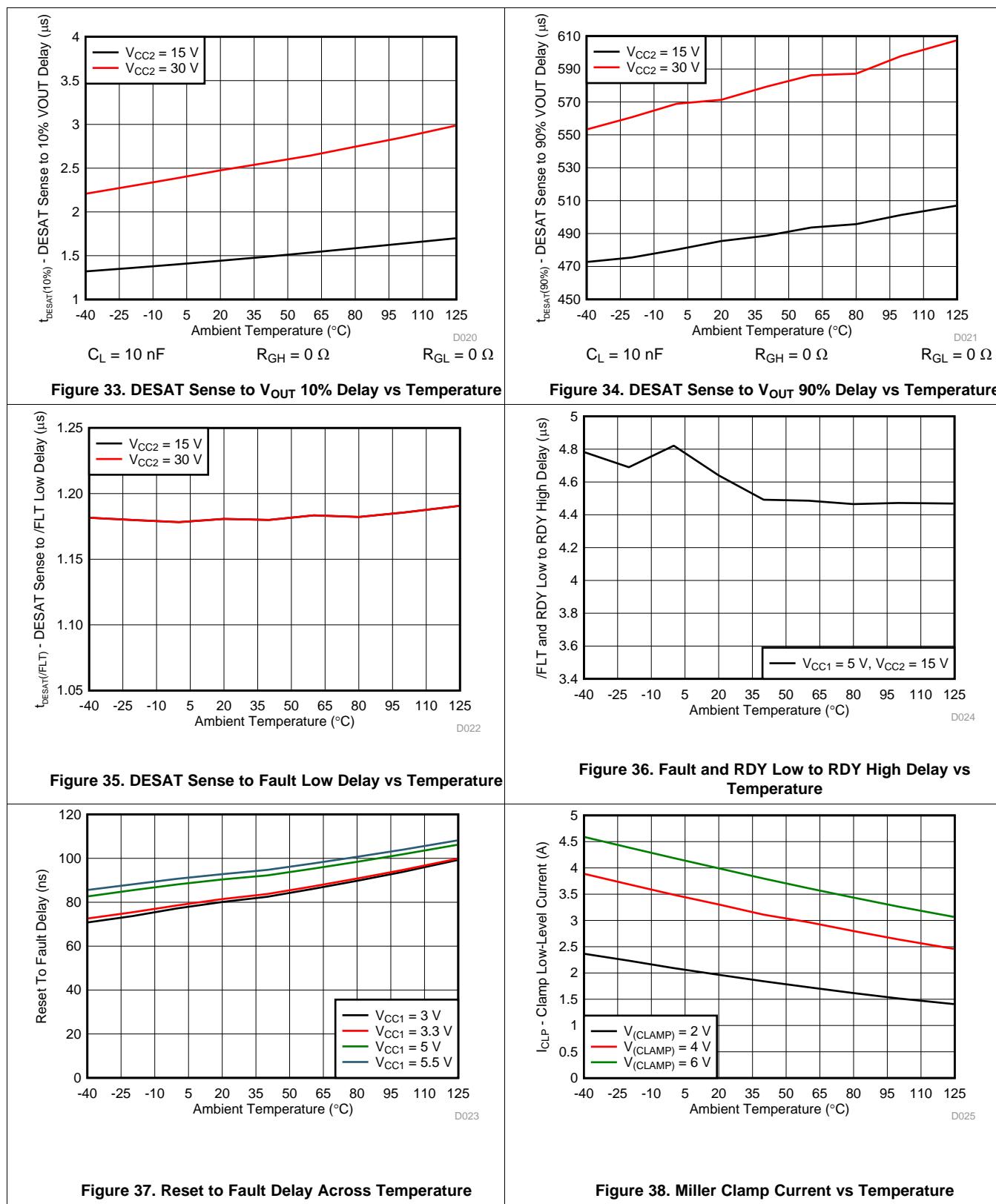


**Figure 31.  $t_f$  Fall Time vs Load Capacitance**

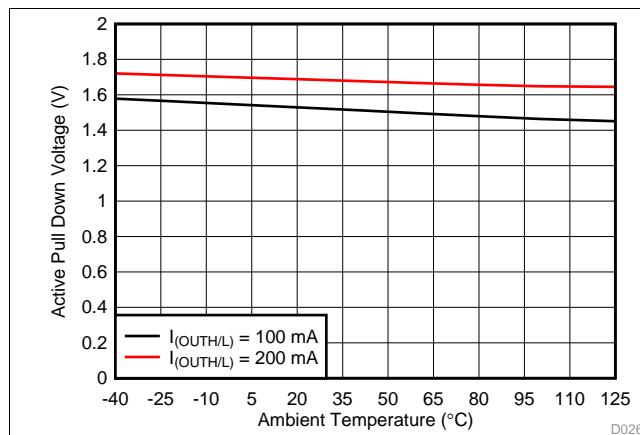


**Figure 32. Leading Edge Blanking Time With Temperature**

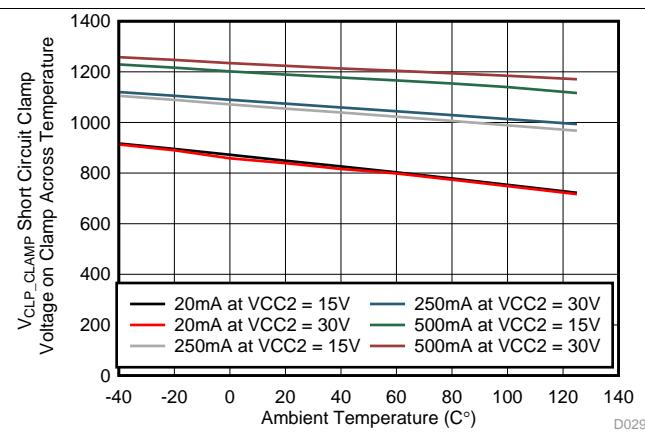
## Typical Characteristics (continued)



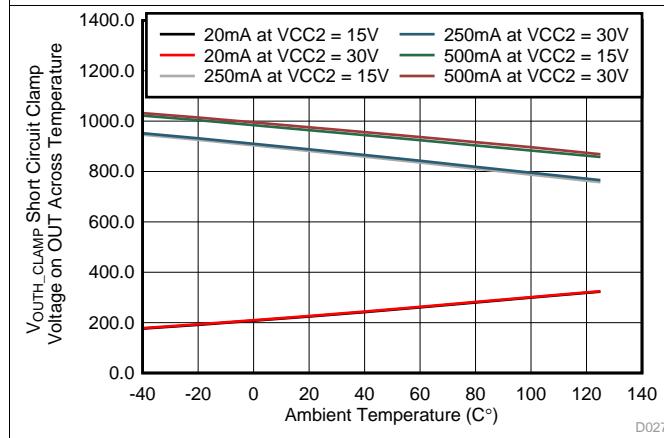
## Typical Characteristics (continued)



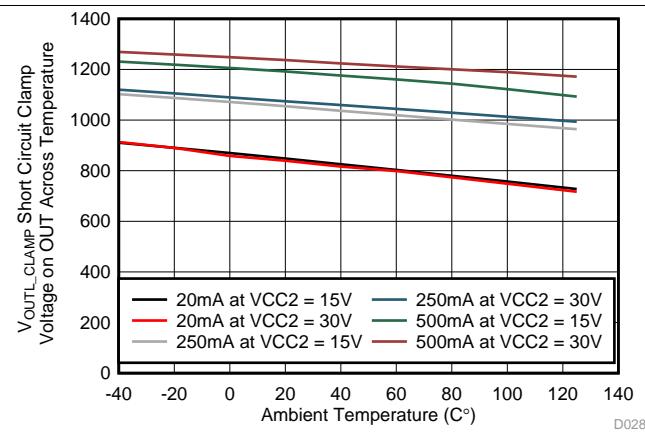
**Figure 39. Active Pulldown Voltage vs Temperature**



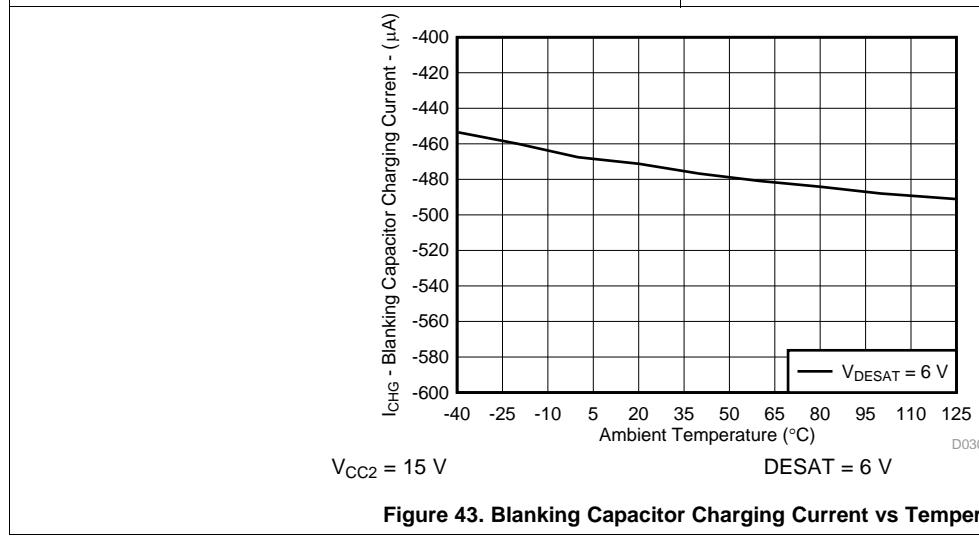
**Figure 40.  $V_{CLP\_CLAMP}$  - Short-Circuit Clamp Voltage on Clamp Across Temperature**



**Figure 41.  $V_{OUTH\_CLAMP}$  - Short-Circuit Clamp Voltage on OUTH Across Temperature**

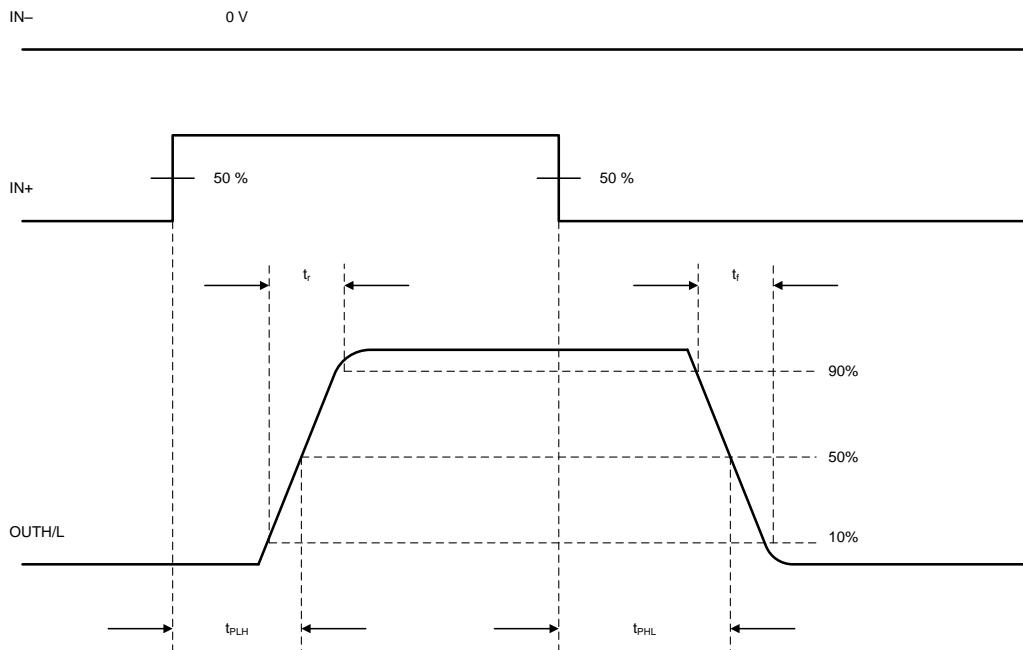


**Figure 42.  $V_{OUTL\_CLAMP}$  - Short-Circuit Clamp Voltage on OUTL Across Temperature**

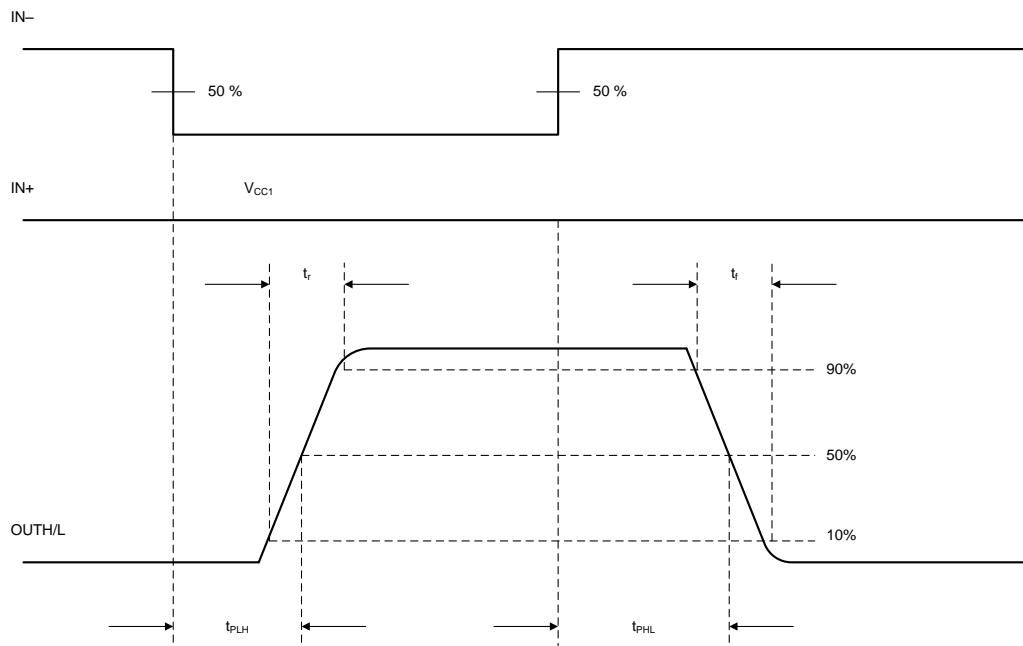


**Figure 43. Blanking Capacitor Charging Current vs Temperature**

## 8 Parameter Measurement Information

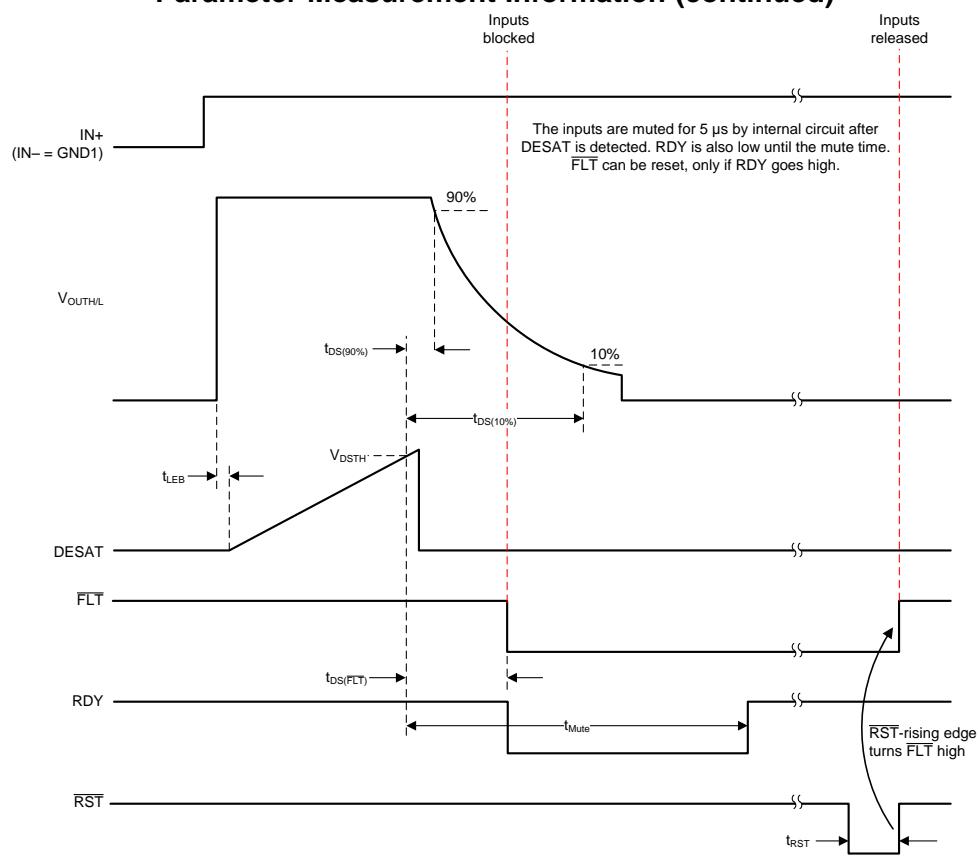


**Figure 44. OUTH and OUTL Propagation Delay, Non-Inverting Configuration**

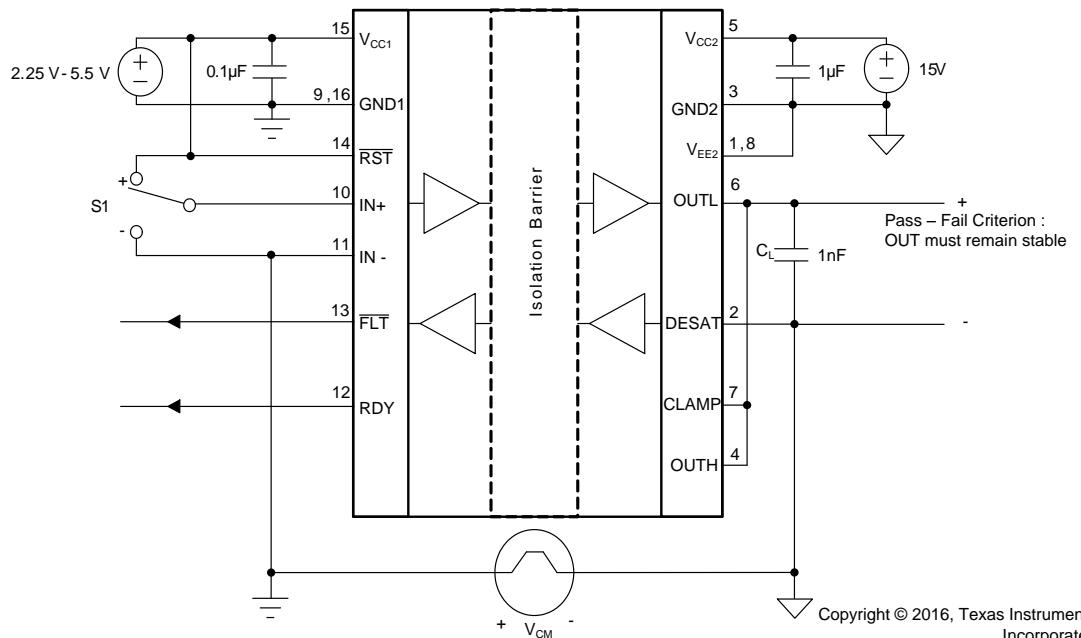


**Figure 45. OUTH and OUTL Propagation Delay, Inverting Configuration**

### Parameter Measurement Information (continued)



**Figure 46. DESAT, OUTH/L,  $\overline{FLT}$ ,  $\overline{RST}$  Delay**



**Figure 47. Common-Mode Transient Immunity Test Circuit**

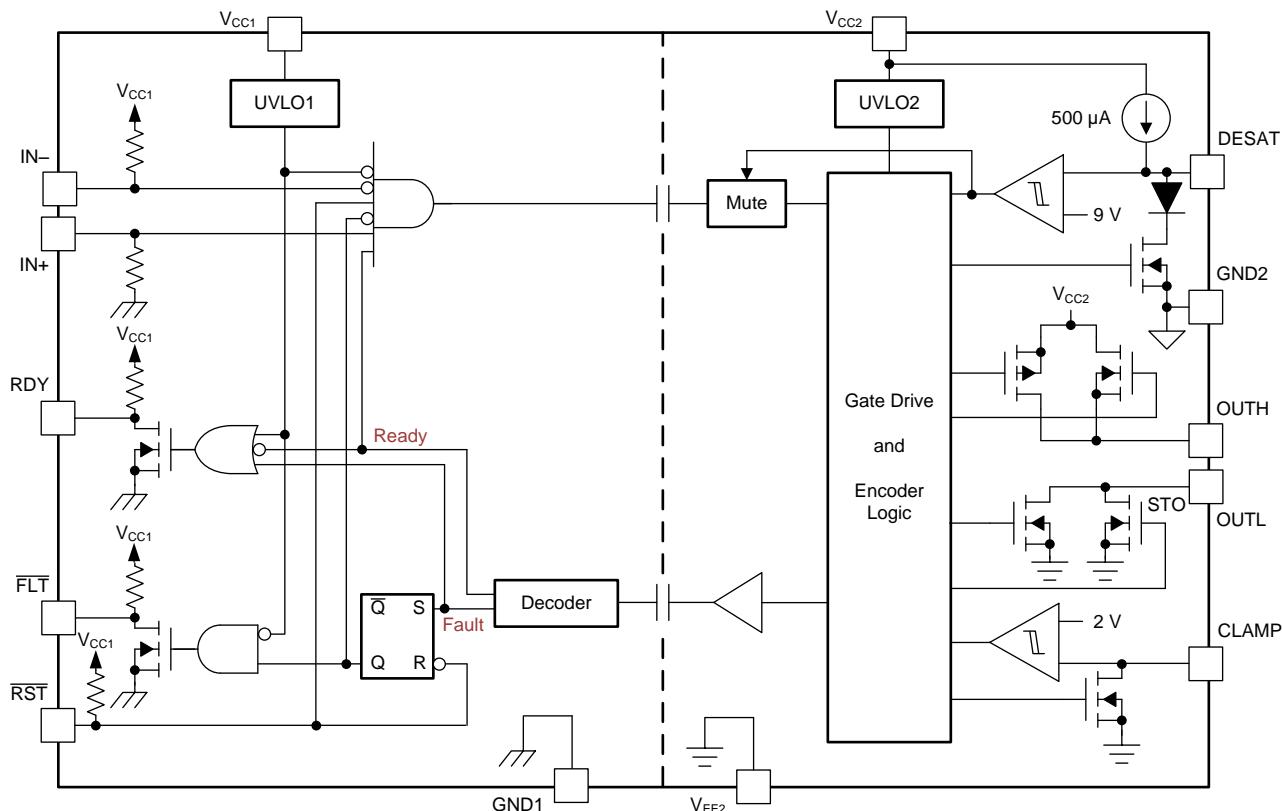
## 9 Detailed Description

### 9.1 Overview

The ISO5852S-Q1 is an isolated gate driver for IGBTs and MOSFETs. Input CMOS logic and output power stage are separated by a Silicon dioxide ( $\text{SiO}_2$ ) capacitive isolation.

The IO circuitry on the input side interfaces with a micro controller and consists of gate drive control and RESET (RST) inputs, READY (RDY) and FAULT (FLT) alarm outputs. The power stage consists of power transistors to supply 2.5-A pullup and 5-A pulldown currents to drive the capacitive load of the external power transistors, as well as DESAT detection circuitry to monitor IGBT collector-emitter overvoltage under short circuit events. The capacitive isolation core consists of transmit circuitry to couple signals across the capacitive isolation barrier, and receive circuitry to convert the resulting low-swing signals into CMOS levels. The ISO5852S-Q1 also contains under voltage lockout circuitry to prevent insufficient gate drive to the external IGBT, and active output pulldown feature which ensures that the gate-driver output is held low, if the output supply voltage is absent. The ISO5852S-Q1 also has an active Miller clamp function which can be used to prevent parasitic turn-on of the external power transistor, due to Miller effect, for unipolar supply operation.

### 9.2 Functional Block Diagram



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## 9.3 Feature Description

### 9.3.1 Supply and Active Miller Clamp

The ISO5852S-Q1 supports both bipolar and unipolar power supply with active Miller clamp.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage on its gate with respect to its emitter. This prevents the IGBT from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. In this condition it is not necessary to connect CLAMP output of the gate driver to the IGBT gate, but connecting CLAMP output of the gate driver to the IGBT gate is also not an issue. Typical values of  $V_{CC2}$  and  $V_{EE2}$  for bipolar operation are 15-V and -8-V with respect to GND2.

For operation with unipolar supply, typically,  $V_{CC2}$  is connected to 15-V with respect to GND2, and  $V_{EE2}$  is connected to GND2. In this use case, the IGBT can turn on due to additional charge from IGBT Miller capacitance caused by a high voltage slew rate transition on the IGBT collector. To prevent IGBT to turn on, the CLAMP pin is connected to IGBT gate and Miller current is sunked through a low impedance CLAMP transistor.

Miller CLAMP is designed for Miller current up to 2-A. When the IGBT is turned-off and the gate voltage transitions below 2-V the CLAMP current output is activated.

### 9.3.2 Active Output Pulldown

The Active output pulldown feature ensures that the IGBT gate OUTH/L is clamped to  $V_{EE2}$  to ensure safe IGBT off-state, when the output side is not connected to the power supply.

### 9.3.3 Undervoltage Lockout (UVLO) With Ready (RDY) Pin Indication Output

Undervoltage Lockout (UVLO) ensures correct switching of IGBT. The IGBT is turned-off, if the supply  $V_{CC1}$  drops below  $V_{IT-}(UVLO1)$ , irrespective of IN+, IN- and RST input till  $V_{CC1}$  goes above  $V_{IT+}(UVLO1)$ .

In similar manner, the IGBT is turned-off, if the supply  $V_{CC2}$  drops below  $V_{IT-}(UVLO2)$ , irrespective of IN+, IN- and RST input till  $V_{CC2}$  goes above  $V_{IT+}(UVLO2)$ .

Ready (RDY) pin indicates status of input and output side Under Voltage Lock-Out (UVLO) internal protection feature. If either side of device have insufficient supply ( $V_{CC1}$  or  $V_{CC2}$ ), the RDY pin output goes low; otherwise, RDY pin output is high. RDY pin also serves as an indication to the micro-controller that the device is ready for operation.

### 9.3.4 Soft Turnoff, Fault ( $\overline{FLT}$ ) and Reset ( $\overline{RST}$ )

During IGBT overcurrent condition, a mute logic initiates a soft-turn-off procedure which disables, OUTH, and pulls OUTL to low over a time span of 2  $\mu$ s. When desaturation is active, a fault signal is sent across the isolation barrier pulling the  $\overline{FLT}$  output at the input side low and blocking the isolator input. mute logic is activated through the soft-turn-off period. The  $\overline{FLT}$  output condition is latched and can be reset only after RDY goes high, through a active-low pulse at the  $\overline{RST}$  input.  $\overline{RST}$  has an internal filter to reject noise and glitches. By asserting  $\overline{RST}$  for at-least the specified minimum duration (800 ns), device input logic can be enabled or disabled.

### 9.3.5 Short Circuit Clamp

Under short circuit events it is possible that currents are induced back into the gate-driver OUTH/L and CLAMP pins due to parasitic Miller capacitance between the IGBT collector and gate terminals. Internal protection diodes on OUTH/L and CLAMP help to sink these currents while clamping the voltages on these pins to values slightly higher than the output side supply.

## 9.4 Device Functional Modes

In ISO5852S-Q1 OUTH/L to follow IN+ in normal functional mode,  $\overline{FLT}$  pin must be in the high state. [Table 1](#) lists the device functions.

**Table 1. Function Table<sup>(1)</sup>**

$V_{CC1}$	$V_{CC2}$	IN+	IN-	$\overline{RST}$	RDY	OUTH/L
PU	PD	X	X	X	Low	Low
PD	PU	X	X	X	Low	Low
PU	PU	X	X	Low	High	Low
PU	Open	X	X	X	Low	Low
PU	PU	Low	X	X	High	Low
PU	PU	X	High	X	High	Low
PU	PU	High	Low	High	High	High

(1) PU: Power Up ( $V_{CC1} \geq 2.25$  V,  $V_{CC2} \geq 13$  V), PD: Power Down ( $V_{CC1} \leq 1.7$  V,  $V_{CC2} \leq 9.5$  V), X: Irrelevant

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The ISO5852S-Q1 device is an isolated gate driver for power semiconductor devices such as IGBTs and MOSFETs. It is intended for use in applications such as motor control, industrial inverters and switched mode power supplies. In these applications, sophisticated PWM control signals are required to turn the power devices on and off, which at the system level eventually may determine, for example, the speed, position, and torque of the motor or the output voltage, frequency and phase of the inverter. These control signals are usually the outputs of a microcontroller, and are at low voltage levels such as 2.5 V, 3.3 V or 5 V. The gate controls required by the MOSFETs and IGBTs, however, are in the range of 30-V (using unipolar output supply) to 15-V (using bipolar output supply), and require high-current capability to drive the large capacitive loads offered by those power transistors. The gate drive must also be applied with reference to the emitter of the IGBT (source for MOSFET), and by construction, the emitter node in a gate-drive system may swing between 0 to the DC-bus voltage, which can be several 100s of volts in magnitude.

The ISO5852S-Q1 device is therefore used to level shift the incoming 2.5-V, 3.3-V, and 5-V control signals from the microcontroller to the 30-V (using unipolar output supply) to 15-V (using bipolar output supply) drive required by the power transistors while ensuring high-voltage isolation between the driver side and the microcontroller side.

### 10.2 Typical Applications

Figure 48 shows the typical application of a three-phase inverter using six ISO5852S-Q1 isolated gate drivers. Three-phase inverters are used for variable-frequency drives to control the operating speed and torque of AC motors and for high-power applications such as high-voltage DC (HVDC) power transmission.

The basic three-phase inverter consists of six power switches, and each switch is driven by one ISO5852S-Q1. The switches are driven on and off at high switching frequency with specific patterns that convert dc bus voltage to three-phase AC voltages.

## Typical Applications (continued)

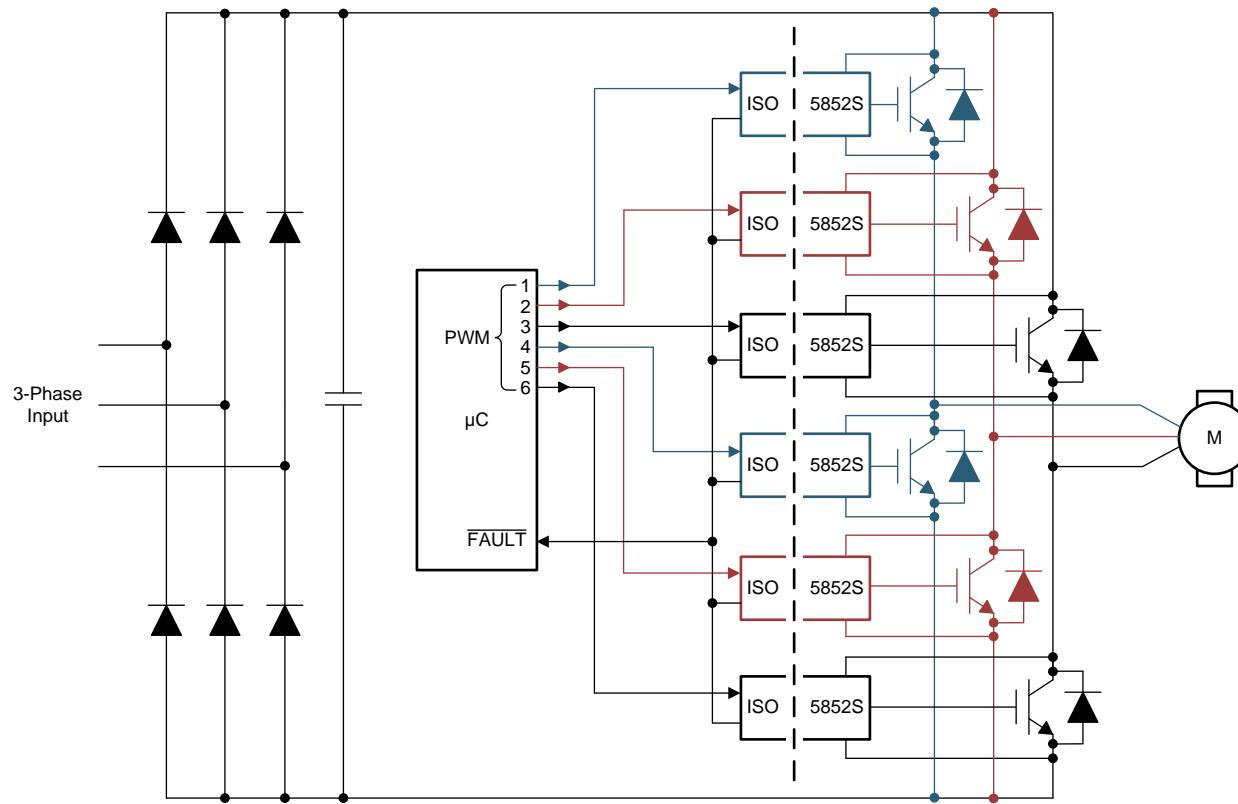


Figure 48. Typical Motor-Drive Application

### 10.2.1 Design Requirements

Unlike optocoupler-based gate drivers which required external current drivers and biasing circuitry to provide the input control signals, the input control to the device is CMOS and can be directly driven by the microcontroller. Other design requirements include decoupling capacitors on the input and output supplies, a pullup resistor on the common-drain FLT output signal and RST input signal, and a high-voltage protection diode between the IGBT collector and the DESAT input. Further details are explained in the subsequent sections. [Table 2](#) lists the allowed range for input and output supply voltage, and the typical current output available from the gate-driver.

Table 2. Design Parameters

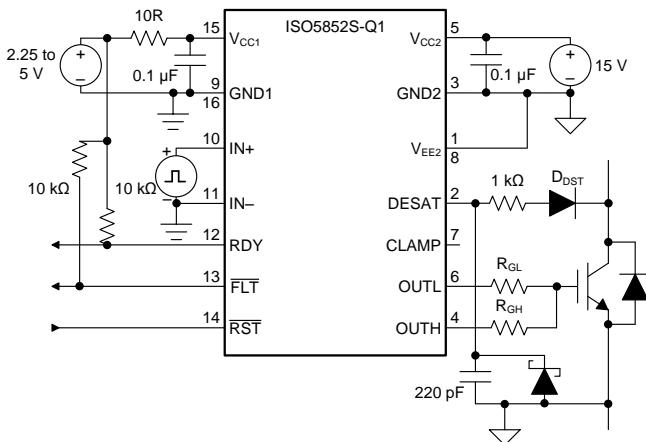
PARAMETER	VALUE
Input supply voltage	2.25 V to 5.5 V
Unipolar output-supply voltage ( $V_{CC2} - GND2 = V_{CC2} - V_{EE2}$ )	15 V to 30 V
Bipolar output-supply voltage ( $V_{CC2} - V_{EE2}$ )	15 V to 30 V
Bipolar output-supply voltage ( $GND2 - V_{EE2}$ )	0 V to 15 V
Output current	2.5 A

### 10.2.2 Detailed Design Procedure

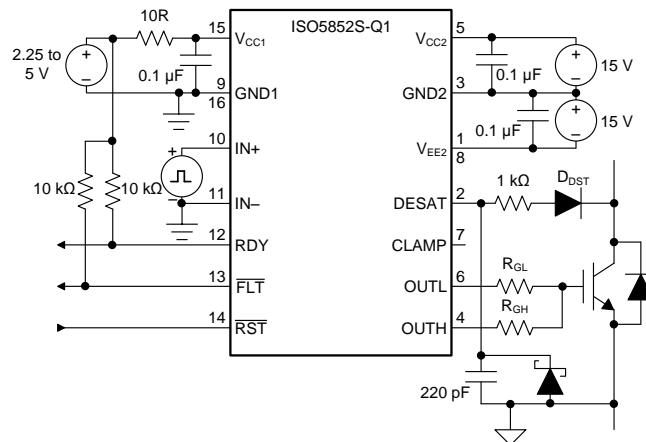
#### 10.2.2.1 Recommended ISO5852S-Q1 Application Circuit

The ISO5852S-Q1 device has both, inverting and noninverting gate-control inputs, an active-low reset input, and an open-drain fault output suitable for wired-OR applications. The recommended application circuit in [Figure 49](#) shows a typical gate-driver implementation with unipolar output supply. [Figure 50](#) shows a typical gate-driver implementation with bipolar output supply using the ISO5852S-Q1 device.

A 0.1- $\mu$ F bypass capacitor, recommended at the input supply pin  $V_{CC1}$ , and 1- $\mu$ F bypass capacitor, recommended at the  $V_{CC2}$  output supply pin, provide the large transient currents required during a switching transition to ensure reliable operation. The 220-pF blanking capacitor disables DESAT detection during the off-to-on transition of the power device. The DESAT diode ( $D_{DST}$ ) and the 1-k $\Omega$  series resistor on the DESAT pin are external protection components. The  $R_G$  gate resistor limits the gate-charge current and indirectly controls the rise and fall times of the IGBT collector voltage. The open-drain  $FLT$  output and  $RDY$  output have a passive 10-k $\Omega$  pullup resistor. In this application, the IGBT gate driver is disabled when a fault is detected and does not resume switching until the microcontroller applies a reset signal.



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**Figure 49. Unipolar Output Supply**

**Figure 50. Bipolar Output Supply**

### 10.2.2.2 FLT and RDY Pin Circuitry

A 50-k $\Omega$  pullup resistor exists internally on  $\overline{\text{FLT}}$  and  $\text{RDY}$  pins. The  $\overline{\text{FLT}}$  and  $\text{RDY}$  pins are an open-drain output. A 10-k $\Omega$  pullup resistor can be used to make it faster rise and to provide logic high when  $\overline{\text{FLT}}$  and  $\text{RDY}$  is inactive, as shown in [Figure 51](#).

Fast common-mode transients can inject noise and glitches on FLT and RDY pins because of parasitic coupling. The injection of noise and glitches is dependent on board layout. If required, additional capacitance (100 pF to 300 pF) can be included on the FLT and RDY pins.

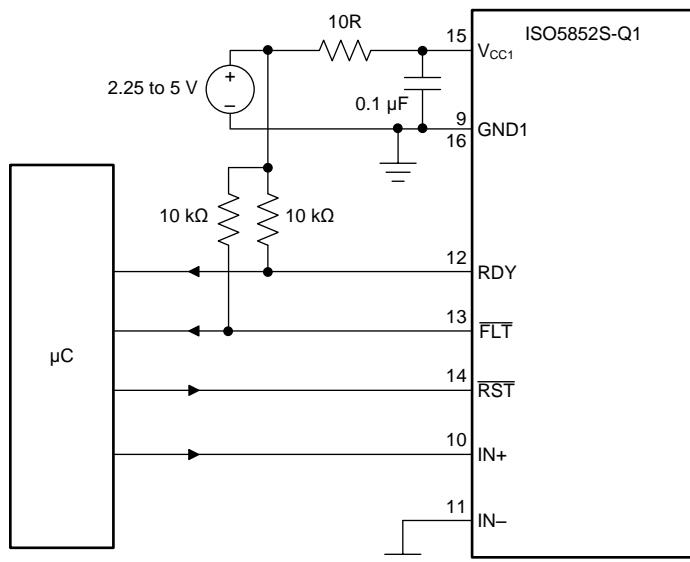


Figure 51 FLT and RDY Pin Circuitry for High CMTR

### 10.2.2.3 Driving the Control Inputs

The amount of common-mode transient immunity (CMTI) can be curtailed by the capacitive coupling from the high-voltage output circuit to the low-voltage input side of the ISO5852S-Q1 device. For maximum CMTI performance, the digital control inputs, IN+ and IN-, must be actively driven by standard CMOS, push-pull drive circuits. This type of low-impedance signal source provides active drive signals that prevent unwanted switching of the ISO5852S-Q1 output under extreme common-mode transient conditions. Passive drive circuits, such as open-drain configurations using pullup resistors, must be avoided. A 20-ns glitch filter exists that can filter a glitch up to 20 ns on IN+ or IN-.

### 10.2.2.4 Local Shutdown and Reset

In applications with local shutdown and reset, the  $\overline{\text{FLT}}$  output of each gate driver is polled separately, and the individual reset lines are independently asserted low to reset the motor controller after a fault condition.

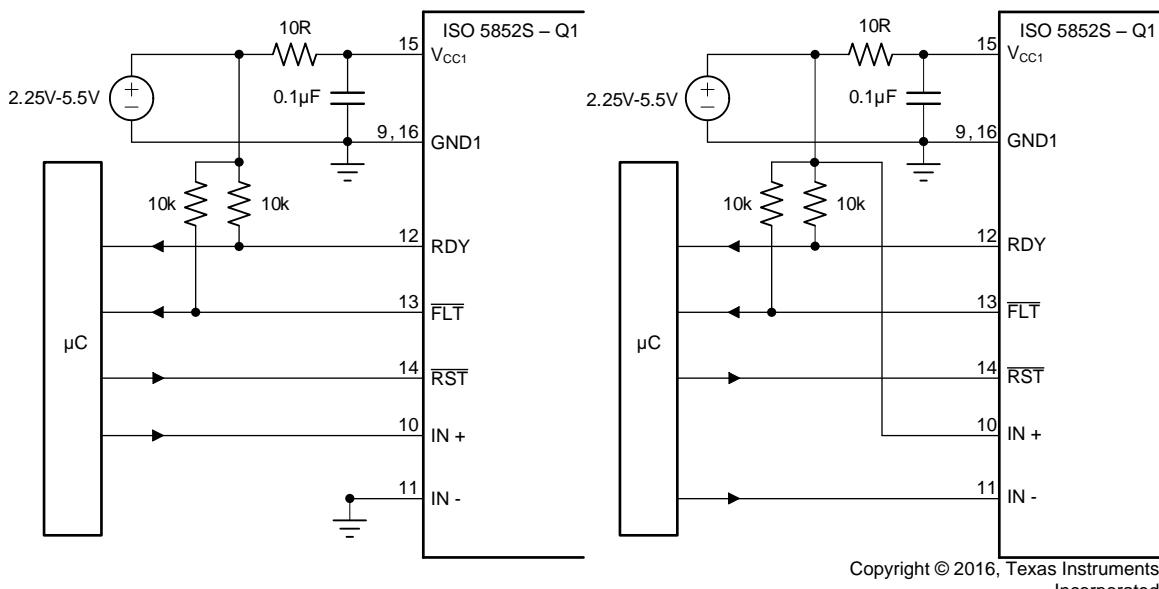
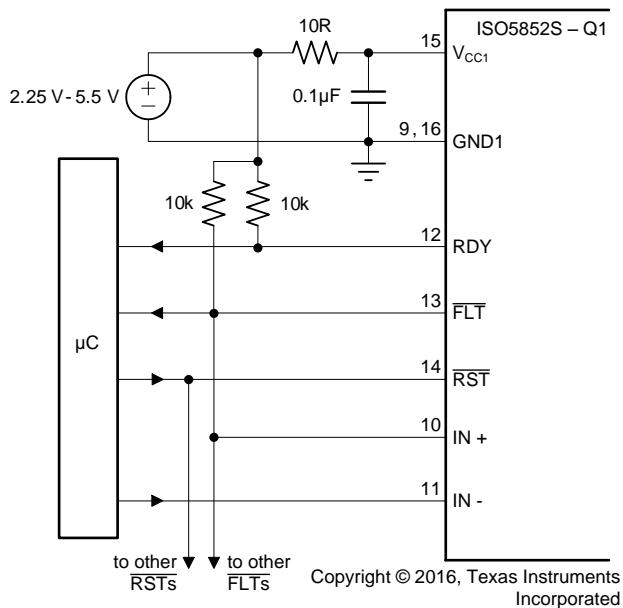


Figure 52. Local Shutdown and Reset for Noninverting (left) and Inverting Input Configuration (right)

### 10.2.2.5 Global-Shutdown and Reset

When configured for inverting operation, the ISO5852S-Q1 device can be configured to shutdown automatically in the event of a fault condition by tying the  $\overline{\text{FLT}}$  output to IN+. For high reliability drives, the open drain  $\overline{\text{FLT}}$  outputs of multiple ISO5852S-Q1 devices can be wired together forming a single, common fault bus for interfacing directly to the microcontroller. When any of the six gate drivers of a three-phase inverter detects a fault, the active-low  $\overline{\text{FLT}}$  output disables all six gate drivers simultaneously.

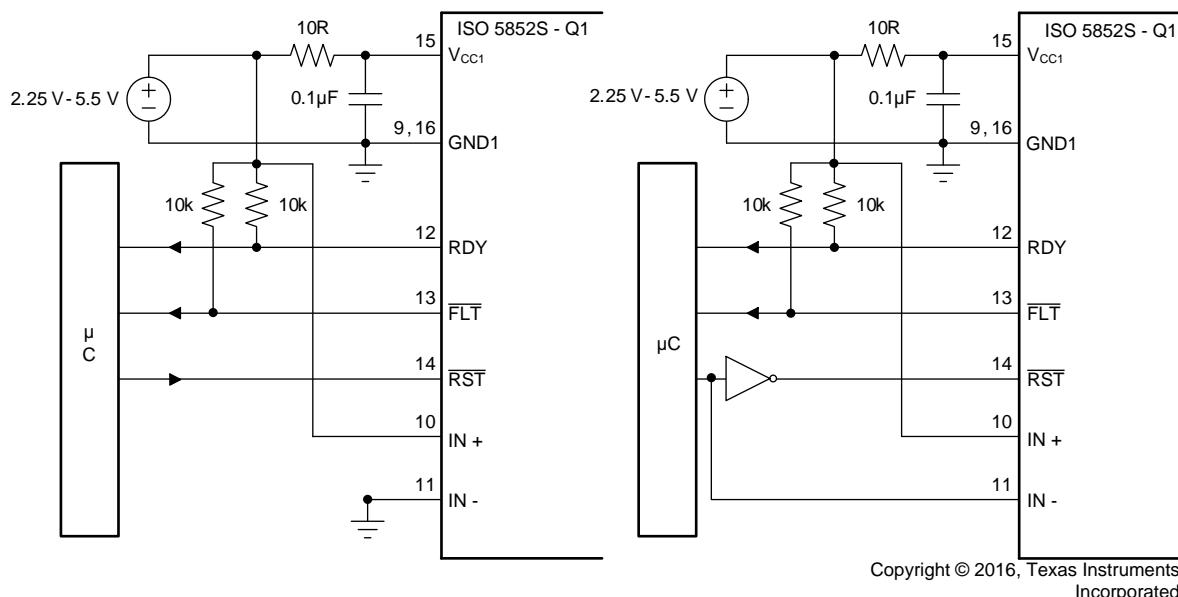


**Figure 53. Global Shutdown With Inverting Input Configuration**

### 10.2.2.6 Auto-Reset

In this case, the gate control signal at IN+ is also applied to the  $\overline{RST}$  input to reset the fault latch every switching cycle. Incorrect  $\overline{RST}$  makes output go low. A fault condition, however, the gate driver remains in the latched fault state until the gate control signal changes to the *gate-low* state and resets the fault latch.

If the gate control signal is a continuous PWM signal, the fault latch is always reset before IN+ goes high again. This configuration protects the IGBT on a cycle-by-cycle basis and automatically resets before the next on cycle.

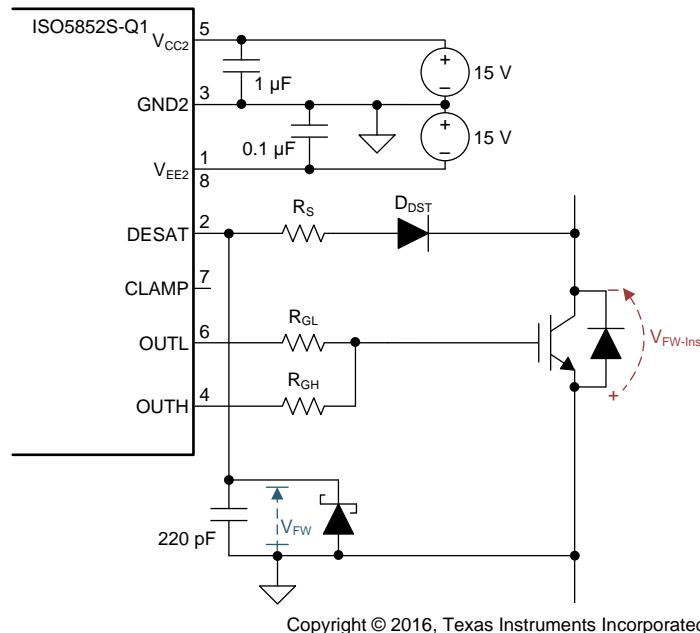


**Figure 54. Auto Reset for Noninverting and Inverting Input Configuration**

### 10.2.2.7 DESAT Pin Protection

Switching inductive loads causes large, instantaneous forward-voltage transients across the freewheeling diodes of the IGBTs. These transients result in large negative-voltage spikes on the DESAT pin which draw substantial current out of the device. To limit this current below damaging levels, a  $100\text{-}\Omega$  to  $1\text{-k}\Omega$  resistor is connected in series with the DESAT diode.

Further protection is possible through an optional Schottky diode, whose low-forward voltage assures clamping of the DESAT input to GND2 potential at low-voltage levels.



**Figure 55. DESAT Pin Protection With Series Resistor and Schottky Diode**

### 10.2.2.8 DESAT Diode and DESAT Threshold

The function of the DESAT diode is to conduct forward current, allowing sensing of the saturated collector-to-emitter voltage of the IGBT,  $V_{(DESAT)}$ , (when the IGBT is *on*), and to block high voltages (when the IGBT is *off*). During the short transition time when the IGBT is switching, a commonly high  $dV_{CE}/dt$  voltage ramp rate occurs across the IGBT. This ramp rate results in a charging current  $I_{(CHARGE)} = C_{(D-DESAT)} \times dV_{CE}/dt$ , charging the blanking capacitor.  $C_{(D-DESAT)}$  is the diode capacitance at DESAT.

To minimize this current and avoid false DESAT triggering, fast switching diodes with low capacitance are recommended. As the diode capacitance builds a voltage divider with the blanking capacitor, large collector voltage transients appear at DESAT attenuated by the ratio of  $1 + C_{\text{BLANK}} / C_{\text{D-DESAT}}$ .

Because the sum of the DESAT diode forward-voltage and the IGBT collector-emitter voltage make up the voltage at the DESAT-pin,  $V_F + V_{CE} = V_{(DESAT)}$ , the  $V_{CE}$  level, which triggers a fault condition, can be modified by adding multiple DESAT diodes in series:  $V_{CE-Fault(T_{(TH)})} = 9\text{ V} - n \times VF$  (where  $n$  is the number of DESAT diodes).

When using two diodes instead of one, diodes with half the required maximum reverse-voltage rating can be selected.

#### 10.2.2.9 Determining the Maximum Available, Dynamic Output Power, $P_{OD\text{-max}}$

The ISO5852S-Q1 maximum-allowed total power consumption of  $P_D = 251$  mW consists of the total input power,  $P_{ID}$ , the total output power,  $P_{OD}$ , and the output power under load,  $P_{OL}$ :

$$P_D = P_{ID} + P_{OD} + P_{OI} \quad (1)$$

With:

$$P_{ID} = V_{CC1-\max} \times I_{CC1-\max} = 5.5 \text{ V} \times 4.5 \text{ mA} = 24.75 \text{ mW} \quad (2)$$

and:

$$P_{OD} = (V_{CC2} - V_{EE2}) \times I_{CC2-\max} = (15 \text{ V} - [-8 \text{ V}]) \times 6 \text{ mA} = 138 \text{ mW} \quad (3)$$

then:

$$P_{OL} = P_D - P_{ID} - P_{OD} = 251 \text{ mW} - 24.75 \text{ mW} - 138 \text{ mW} = 88.25 \text{ mW} \quad (4)$$

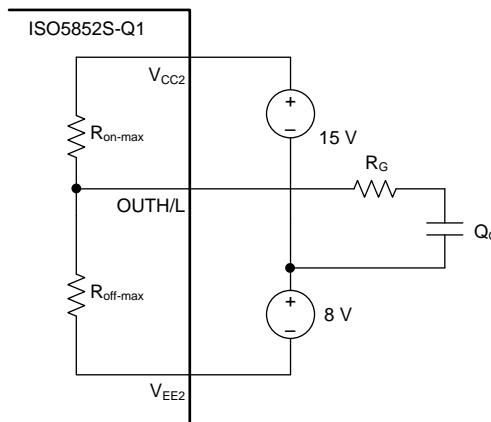
In comparison to  $P_{OL}$ , the actual dynamic output power under worst case condition,  $P_{OL-WC}$ , depends on a variety of parameters:

$$P_{OL-WC} = 0.5 \times f_{INP} \times Q_G \times (V_{CC2} - V_{EE2}) \times \left( \frac{r_{on-\max}}{r_{on-\max} + R_G} + \frac{r_{off-\max}}{r_{off-\max} + R_G} \right)$$

where

- $f_{INP}$  = signal frequency at the control input IN+
- $Q_G$  = power device gate charge
- $V_{CC2}$  = positive output supply with respect to GND2
- $V_{EE2}$  = negative output supply with respect to GND2
- $r_{on-\max}$  = worst case output resistance in the on-state: 4  $\Omega$
- $r_{off-\max}$  = worst case output resistance in the off-state: 2.5  $\Omega$
- $R_G$  = gate resistor

When  $R_G$  is determined, [Equation 5](#) is to be used to verify whether  $P_{OL-WC} < P_{OL}$ . [Figure 56](#) shows a simplified output stage model for calculating  $P_{OL-WC}$ .



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**Figure 56. Simplified Output Model for Calculating  $P_{OL-WC}$**

#### 10.2.2.10 Example

This example considers an IGBT drive with the following parameters:

- $I_{ON-PK} = 2 \text{ A}$
- $Q_G = 650 \text{ nC}$
- $f_{INP} = 20 \text{ kHz}$
- $V_{CC2} = 15 \text{ V}$
- $V_{EE2} = -8 \text{ V}$

Applying the value of the gate resistor  $R_G = 10 \Omega$ .

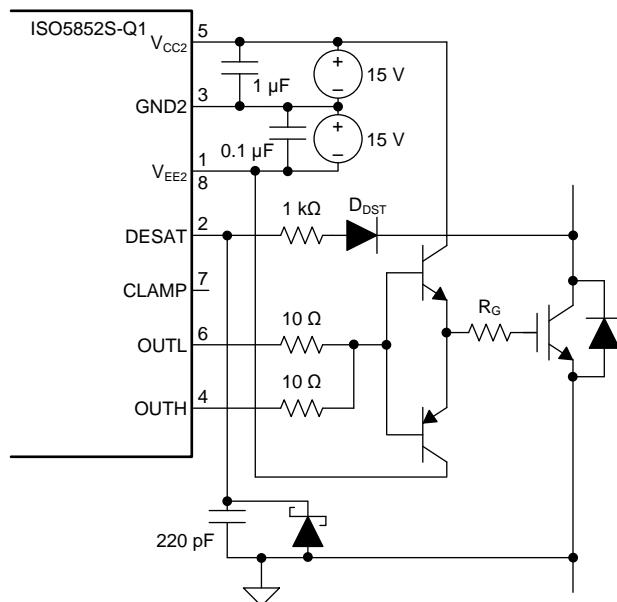
Then, calculating the worst-case output-power consumption as a function of  $R_G$ , using [Equation 5](#)  $r_{on-\max}$  = worst case output resistance in the on-state: 4  $\Omega$ ,  $r_{off-\max}$  = worst case output resistance in the off-state: 2.5  $\Omega$ ,  $R_G$  = gate resistor yields

$$P_{OL-WC} = 0.5 \times 20 \text{ kHz} \times 650 \text{ nC} \times (15 \text{ V} - (-8 \text{ V})) \times \left( \frac{4 \Omega}{4 \Omega + 10 \Omega} + \frac{2.5 \Omega}{2.5 \Omega + 10 \Omega} \right) = 72.61 \text{ mW} \quad (6)$$

Because  $P_{OL-WC} = 72.61$  mW is less than the calculated maximum of  $P_{OL} = 88.25$  mW, the resistor value of  $R_G = 10 \Omega$  is suitable for this application.

### 10.2.2.11 Higher Output Current Using an External Current Buffer

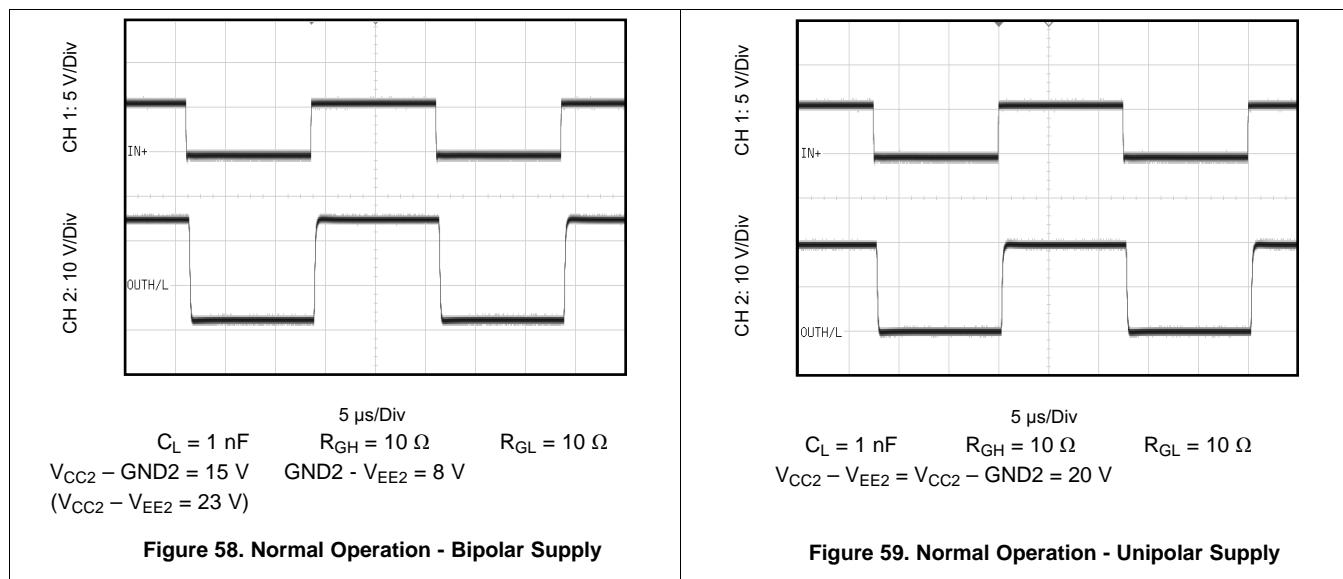
To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in Figure 57) can be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8 A, the D44VH10/ D45VH10 pair for up to 15 A maximum.



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Figure 57. Current Buffer for Increased Drive Current

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

To help ensure reliable operation at all data rates and supply voltages, a  $0.1\text{-}\mu\text{F}$  bypass capacitor is recommended at the  $V_{CC1}$  input supply pin and a  $1\text{-}\mu\text{F}$  bypass capacitor is recommended at the  $V_{CC2}$  output supply pin. The capacitors should be placed as close to the supply pins as possible. The recommended placement of the capacitors is 2 mm (maximum) from the input and output power supply pins ( $V_{CC1}$  and  $V_{CC2}$ ).

## 12 Layout

### 12.1 Layout Guidelines

minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 60](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

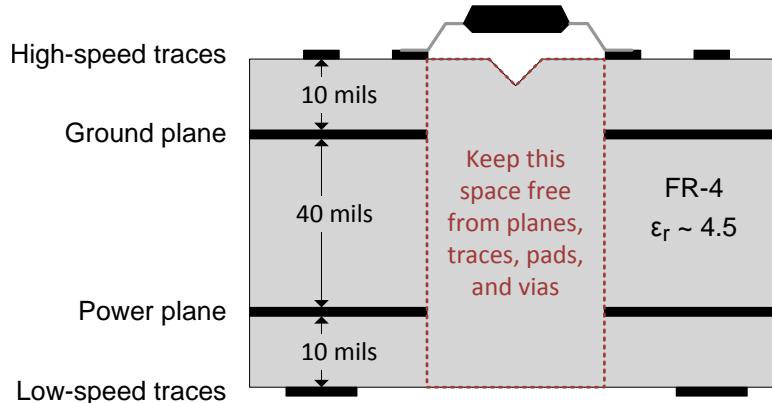
- Routing the high-current or sensitive traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the gate driver and the microcontroller and power transistors. Gate driver control input, Gate driver output OUTH/L and DESAT should be routed in the top layer.
- Placing a solid ground plane next to the sensitive signal layer provides an excellent low-inductance path for the return current flow. On the driver side, use GND2 as the ground plane.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately  $100\text{ pF/inch}^2$ . On the gate-driver  $V_{EE2}$  and  $V_{CC2}$  can be used as power planes. They can share the same layer on the PCB as long as they are not connected together.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

For more detailed layout recommendations, including placement of capacitors, impact of vias, reference planes, routing, and other details, refer to the [Digital Isolator Design Guide](#) (SLLA284).

### 12.2 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

### 12.3 Layout Example



**Figure 60. Recommended Layer Stack**

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation see the following:

- *Digital Isolator Design Guide* (SLLA284)
- *ISO5852S Evaluation Module (EVM) User's Guide* (SLLU207)
- *Isolation Glossary* (SLLA353)

### 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.3 Community Resources

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.4 Trademarks

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### 13.5 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

 ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

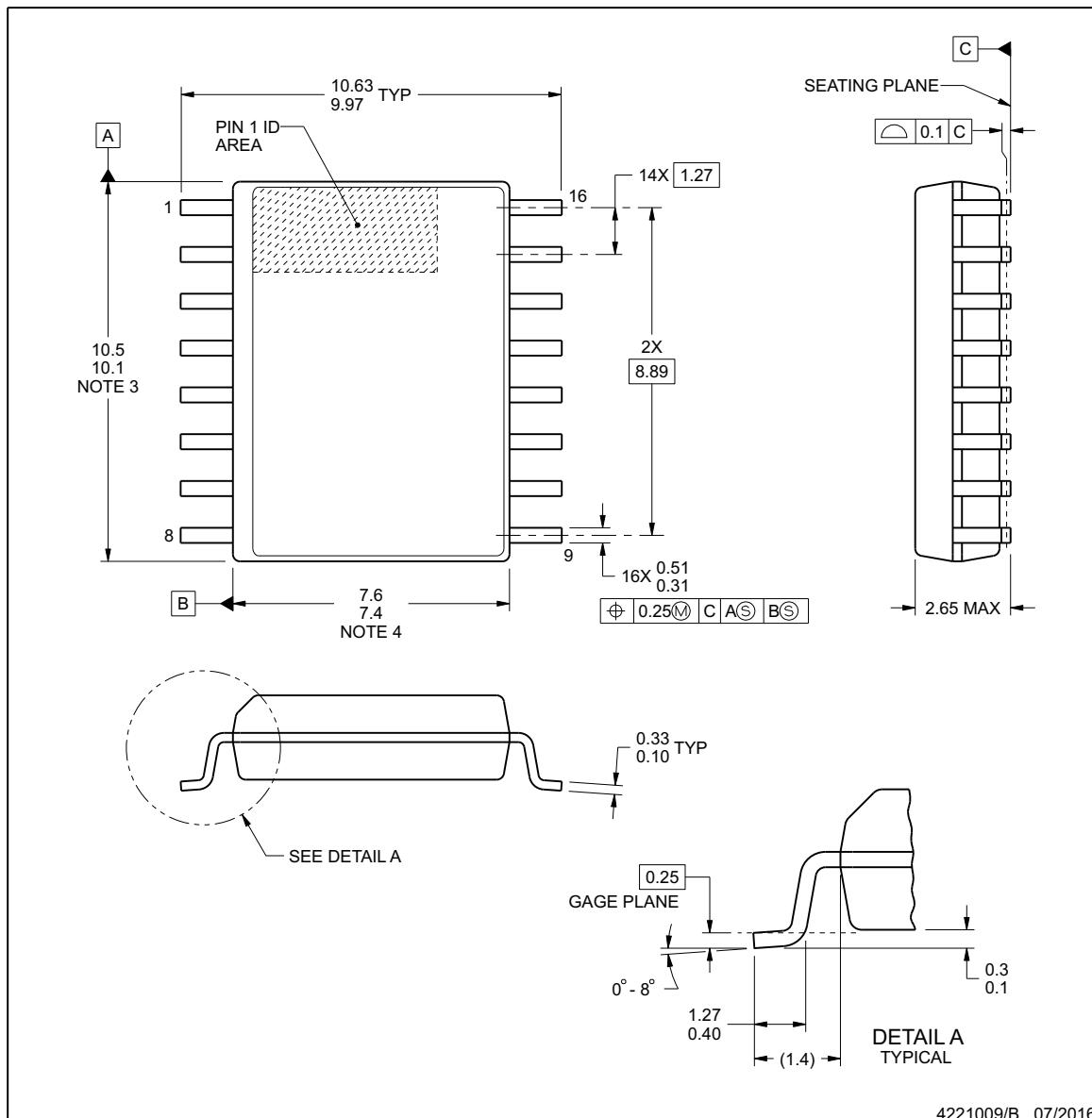
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



## NOTES:

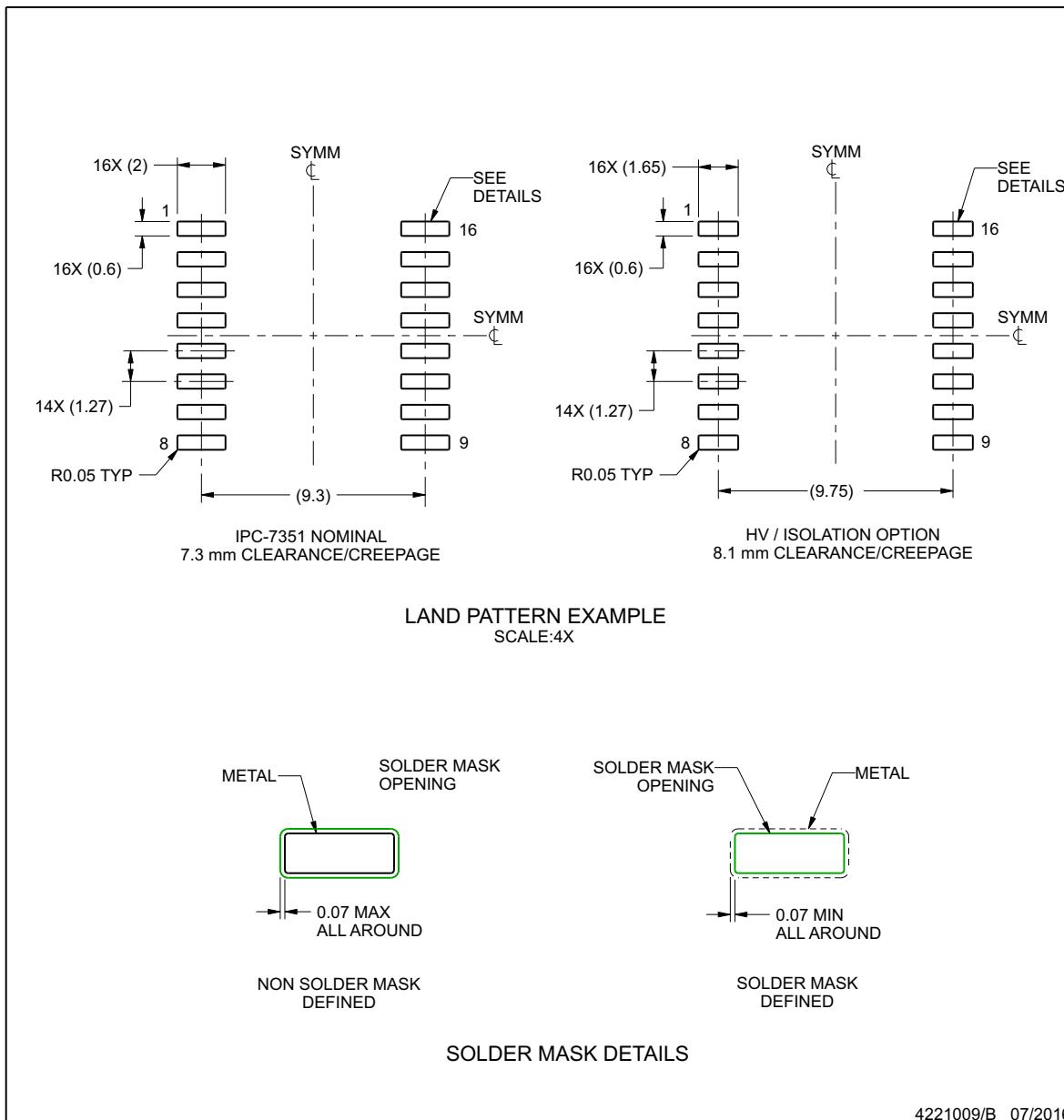
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

## EXAMPLE BOARD LAYOUT

### DW0016B

### SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

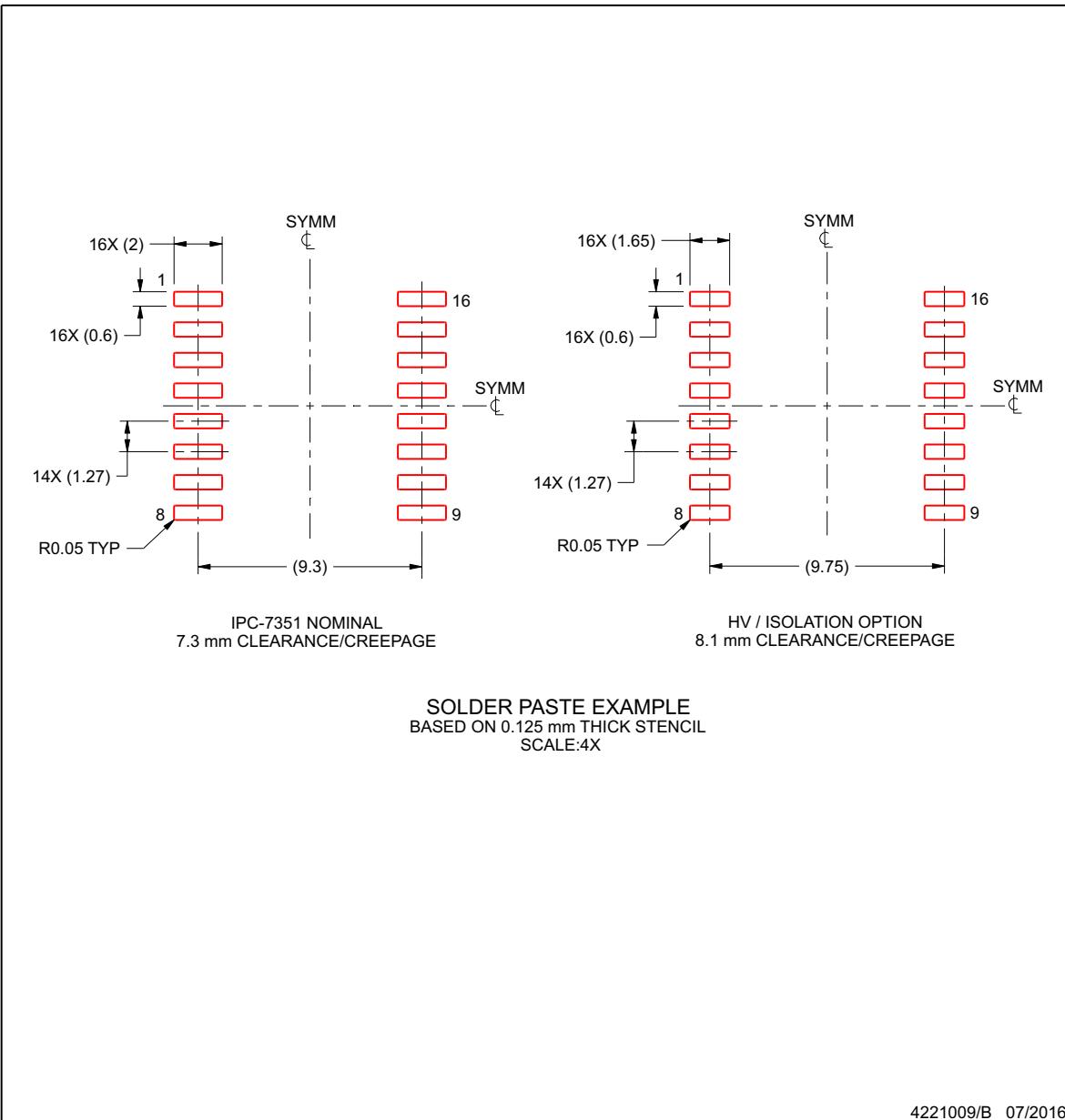
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**DW0016B**

### **SOIC - 2.65 mm max height**

SOIC



#### NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO5852SQDWQ1	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	-40 to 125	ISO5852SQ
ISO5852SQDWQRQ1	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5852SQ
ISO5852SQDWQRQ1.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5852SQ

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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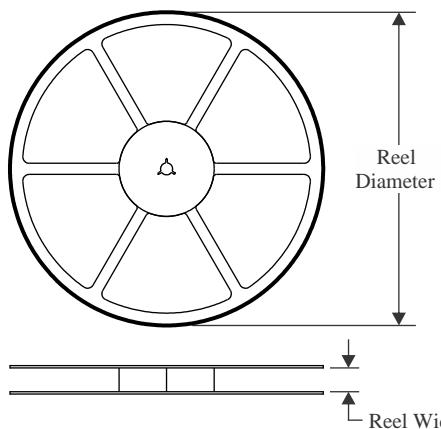
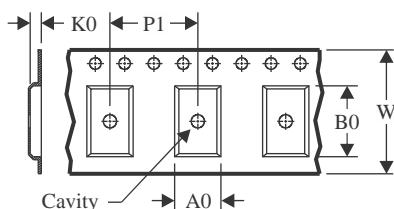
- Catalog : [ISO5852S](#)

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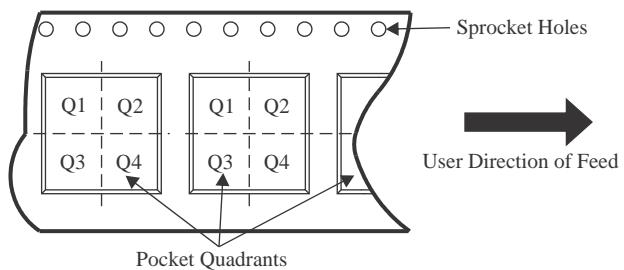
- Enhanced Product : [ISO5852S-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

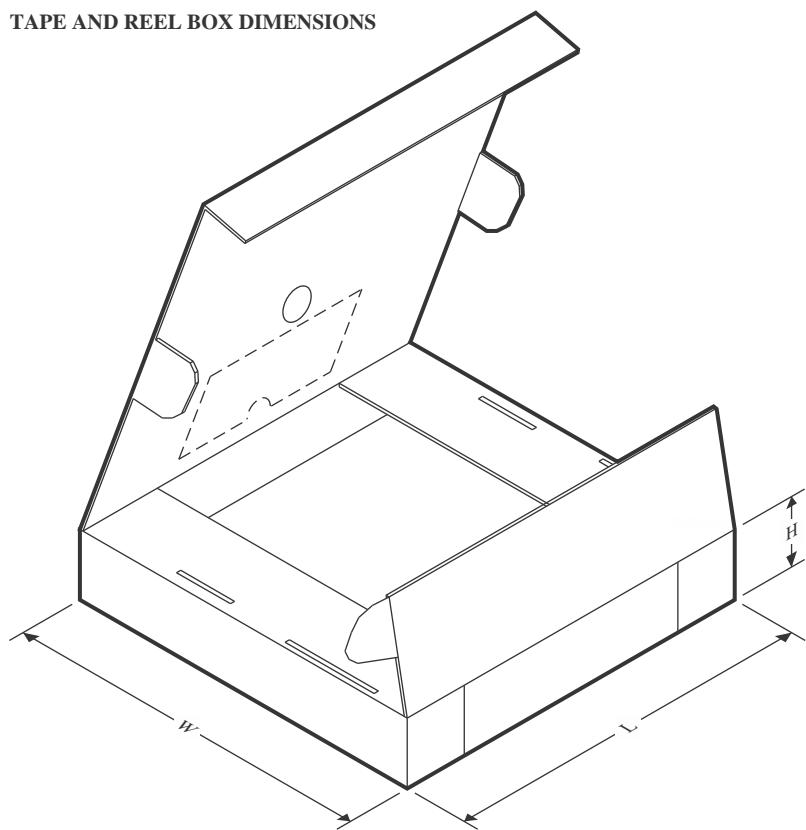
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO5852SQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO5852SQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0

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